

N-Channel Power MOSFET

900V, 4A, 4.0Ω

FEATURES

- Low $R_{DS(ON)}$ 4Ω (Max.)
- Low gate charge typical @ 25nC (Typ.)
- Improve dV/dt capability

APPLICATION

- High efficiency switch mode power Supply
- Lighting

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	900	V
$R_{DS(on)}$ (max)	4	Ω
Q_g	25	nC



Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Drain-Source Voltage	V_{DS}	900		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$	4	4*
		$T_C = 100^\circ\text{C}$	2.2	2.2*
Pulsed Drain Current ^(Note 2)	I_{DM}	16	16 *	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	123	38.7	W
Single Pulsed Avalanche Energy ^(Note 3)	E_{AS}	474		mJ
Single Pulsed Avalanche Current ^(Note 3)	I_{AS}	4		A
Repetitive Avalanche Energy ^(Note 2)	E_{AR}	12.3		mJ
Peak Diode Recovery ^(Note 7)	dV/dt	4.5		V
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.01	3.23	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62.5		°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	900	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2	--	4	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 900V, V_{GS} = 0V$	I_{DSS}	--	--	10	μA
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 2.0A$	$R_{DS(on)}$	--	3.2	4.0	Ω
Forward Transconductance	$V_{DS} = 30V, I_D = 2.0A$	g_{fs}	--	6	--	S
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 720V, I_D = 4.0A,$ $V_{GS} = 10V$	Q_g	--	25	--	nC
Gate-Source Charge		Q_{gs}	--	4.8	--	
Gate-Drain Charge		Q_{gd}	--	10.2	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	955	--	pF
Output Capacitance		C_{oss}	--	80	--	
Gate Resistance	$F = 1MHz, \text{open drain}$	R_g	--	--	4	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 450V,$ $R_{GEN} = 25\Omega,$ $I_D = 4.0A, V_{GS} = 10V,$	$t_{d(on)}$	--	49	--	ns
Turn-On Rise Time		t_r	--	38	--	
Turn-Off Delay Time		$t_{d(off)}$	--	146	--	
Turn-Off Fall Time		t_f	--	50	--	
Source-Drain Diode (Note 4)						
Forward On Voltage	$I_S = 4.0A, V_{GS} = 0V$	V_{SD}	--	--	1.5	V
Reverse Recovery Time	$V_{GS} = 0V, I_S = 4A$	t_{rr}	--	487	--	ns
Reverse Recovery Charge		$di_f/dt = 100A/\mu s$	Q_{rr}	--	2.8	--

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. $L = 56mH, I_{AS} = 4.0A, V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}.$
4. Pulse test: $PW \leq 300\mu s, \text{duty cycle} \leq 2\%.$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.
7. $I_{SD} \leq 4A, di/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}, \text{Starting } T_J = 25^\circ\text{C}.$

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM4N90CZ C0G	TO-220	50pcs / Tube
TSM4N90CI C0G	ITO-220	50pcs / Tube

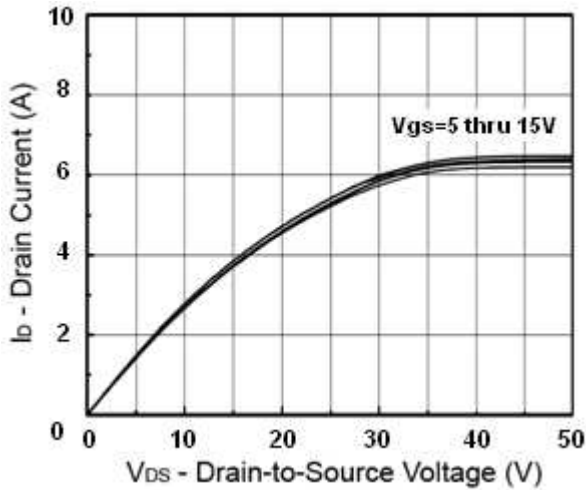
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

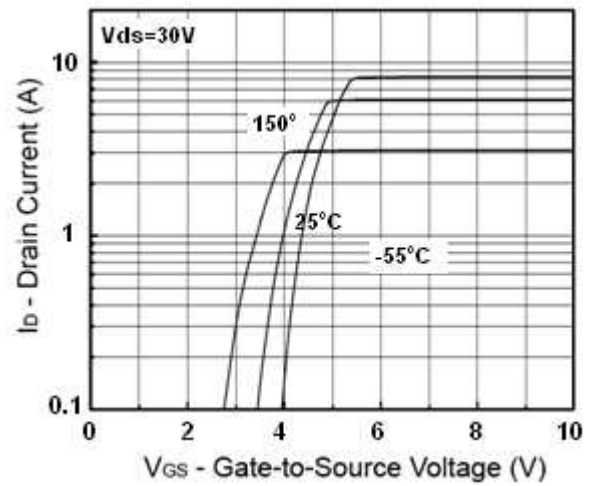
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

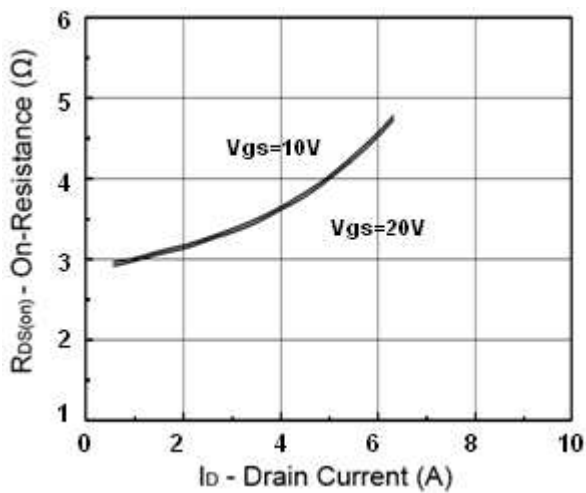
Output Characteristics



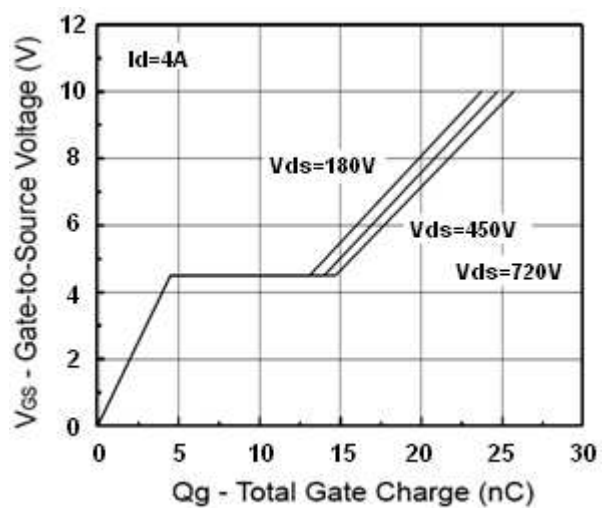
Transfer Characteristics



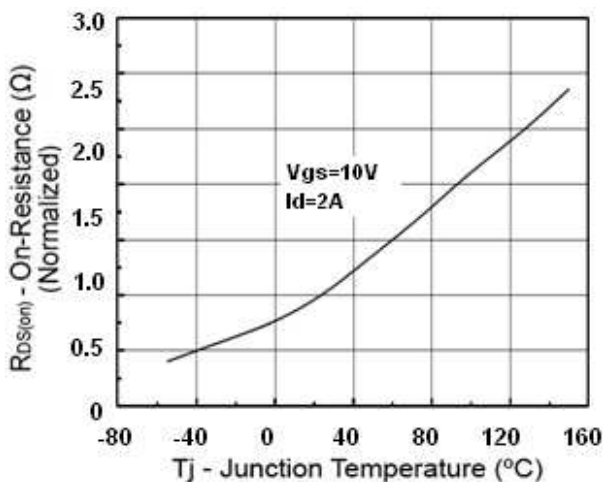
On-Resistance vs. Drain Current



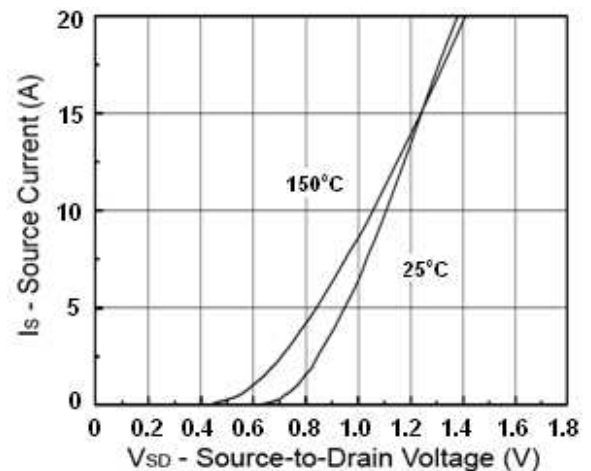
Gate Charge



On-Resistance vs. Junction Temperature



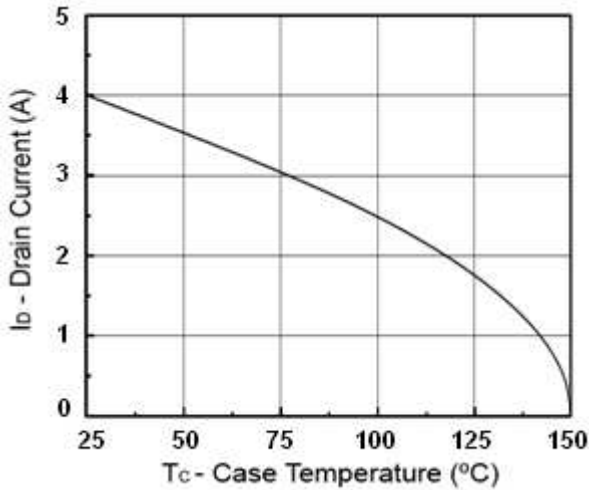
Source-Drain Diode Forward Voltage



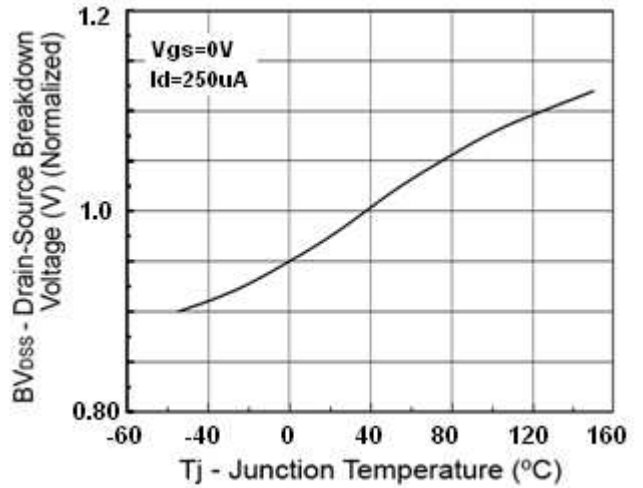
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

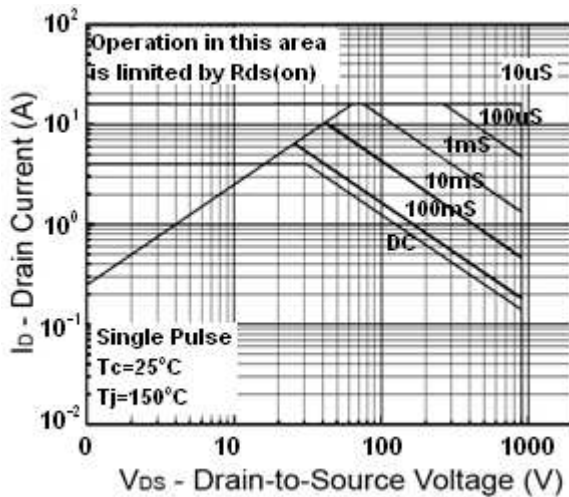
Drain Current vs. Case Temperature



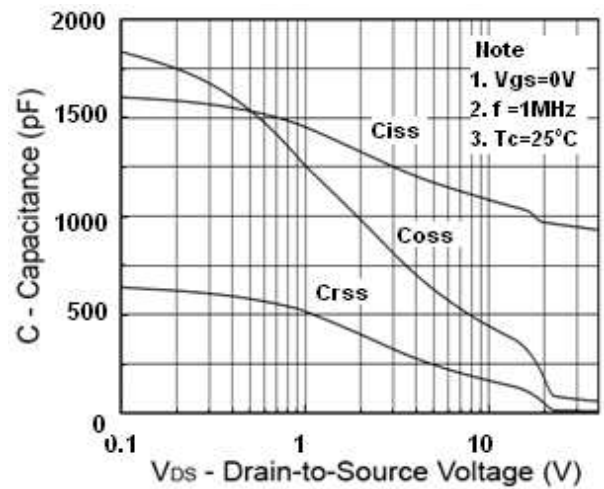
BV_{DSS} vs. Junction Temperature



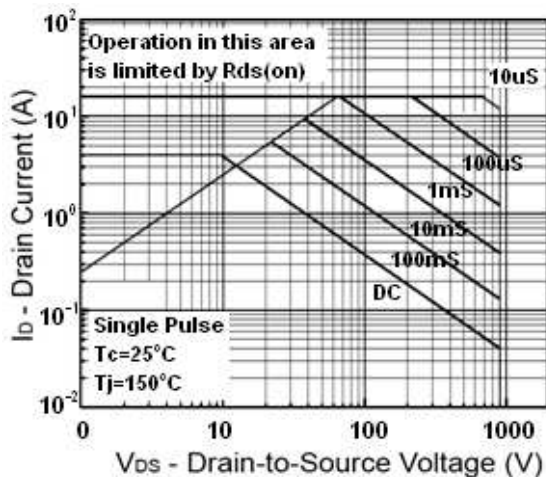
Maximum Safe Operating Area



Capacitance vs. Drain-Source Voltage



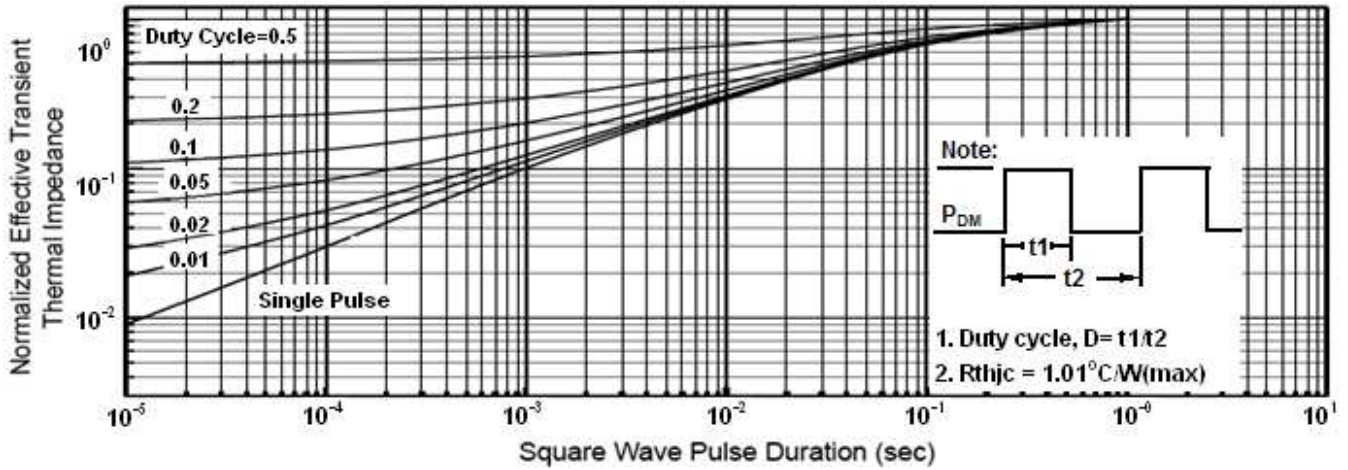
Maximum Safe Operating Area (ITO-220)



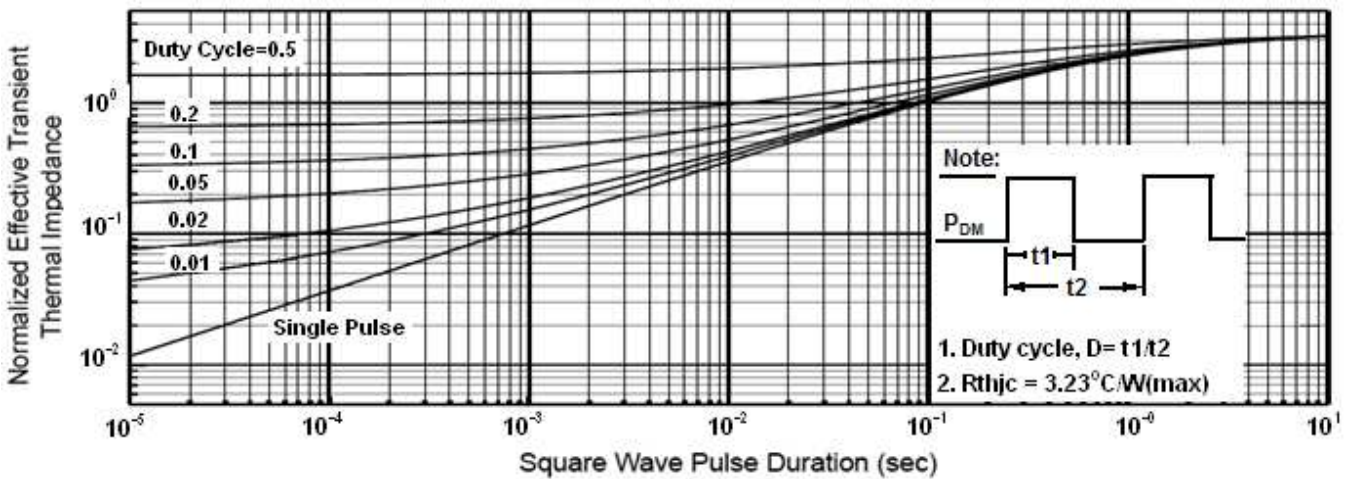
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

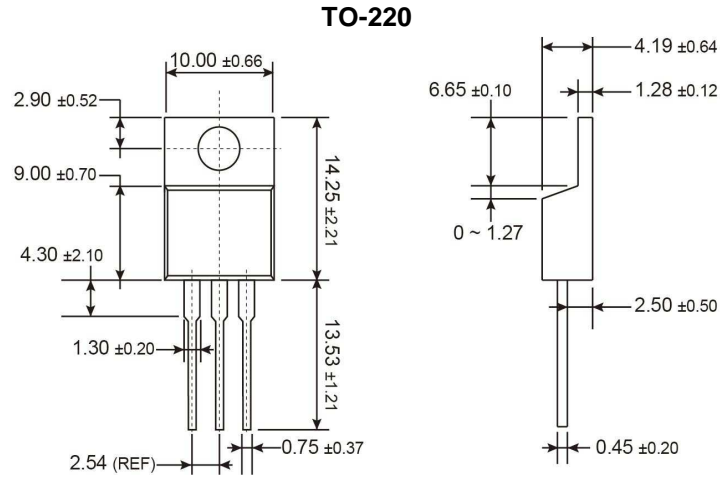
Normalized Thermal Transient Impedance, Junction-to-Ambient (TO-220)



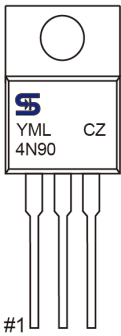
Normalized Thermal Transient Impedance, Junction-to-Ambient (ITO-220)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

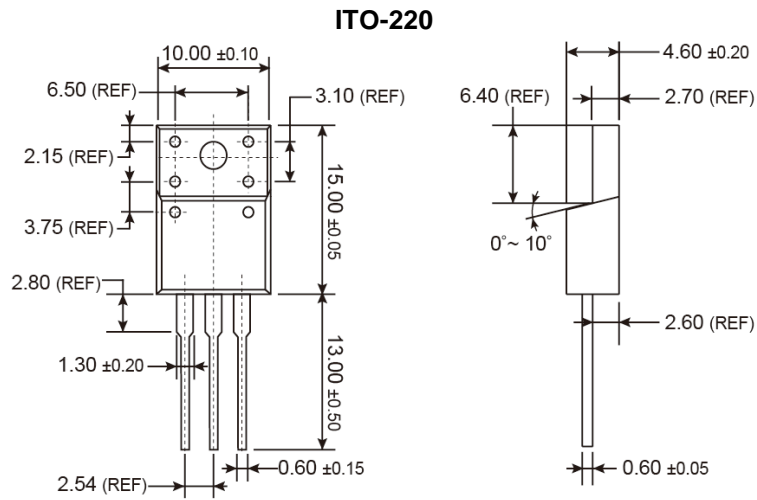


MARKING DIAGRAM

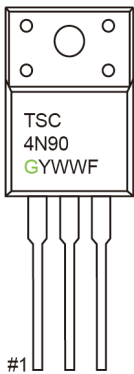


- Y** = Year Code
- M** = Month Code for Halogen Free Product
 - O** =Jan **P** =Feb **Q** =Mar **R** =Apr
 - S** =May **T** =Jun **U** =Jul **V** =Aug
 - W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

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