

QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1255

16-BIT, 250KSPS ADC

LTC1605CG/LTC1606CG

DESCRIPTION

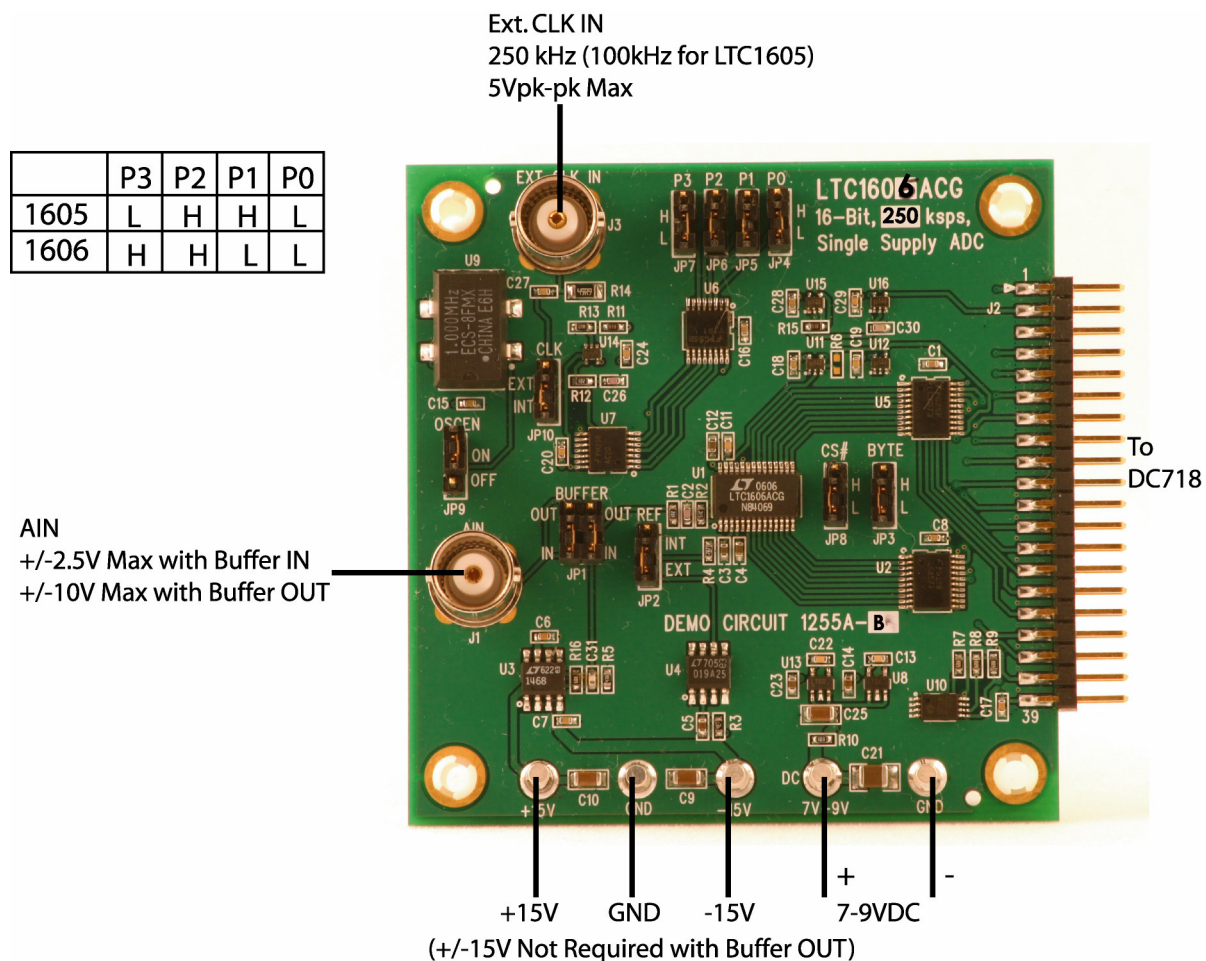
The LTC1606 is a 250Ksps ADC that draws only 75mW from a single +5V Supply, while the LTC1605 is a 100Ksps ADC that draws only 55mW from a single +5V supply. DC1255 can use either part. The following text refers to the LTC1606 but it also applies to the LTC1605 with appropriate sampling frequency considerations.

Demonstration circuit 1255 provides the user a means of evaluating the performance of the LTC1605/LTC1606 and is intended to demonstrate recommended grounding, part placement, routing and bypassing.

Design files for this circuit board are available. Call the LTC factory.

LTC is a trademark of Linear Technology Corporation

Figure1. Connection Diagram



DC718B QUICK START PROCEDURE

Connect DC1255A to a DC718B USB High Speed Data Collection Board using connector J2. Connect DC718B to a host PC with a standard USB A/B cable. Apply 7V-9V DC to the 7V-9V and GND terminals. Apply +15V and -15V to the indicated terminals, if the internal buffer is to be used (default). Apply a low jitter signal source to J1. As a clock source, either the onboard clock or a low jitter 250kHz 10dBm sine wave or square wave to connector J3 can be used. Note that J3 has a 50 Ω termination resistor to ground. Run the QuickEval-II software (Pscope.exe version K51 or later) supplied with DC718B or download it from www.linear.com.

DC1255 SETUP

DC Power

DC1255 requires 7-9VDC at approximately 24mA and +/- 15V to power amplifier U3. If you do not use U3 (see jumper JP1) you do not have to provide +/-15V. The 7-9VDC supply powers the ADC through a LT1761-5 regulator which provides protection against accidental reverse bias. See Figure 1 for connection details.

Clock Source

JP10 (CLK) determines whether DC1255 is internally (default) or externally clocked. The internal clock consists of an ECS 1MHz clock oscillator, which is divided by a 74VHC161 counter. This oscillator can be turned off by setting JP9 (OSCEN) to the OFF position. Jumpers (JP4-JP7) set the internal clock divider ratio for the appropriate ADC (LTC1605 or LTC1606). See the table in Figure 1 for jumper settings.

For an external clock, you must provide a low jitter 10dBm sine or square wave to J3. Note that J3 has a 50 Ω termination resistor to ground. Driving this input with logic will be difficult. Slow rising edges may compromise SNR of the converter in the presence of high-amplitude higher frequency input signals. The demo board incorporates an edge detector circuit in

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The Pscope software should recognize DC1255A and configure itself automatically.

Click the Collect button (See Figure 2) to begin acquiring data. Depending on which board was previously used by Pscope, it may be necessary to press Collect a second time. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

the form of an inverter (U14) followed by a 200nsec delay, feeding, along with the original clock source, a two input NAND gate (U7B). This will generate an approximate 200nsec active low pulse at the ADC if the clock high time is greater than 200nsec. A 50% duty cycle clock at 250kHz is typically used to test these demo boards. Shorter duty cycle pulses (active High at J3) can be used to a minimum of 40nsec.

Data Output

Parallel data output from this board (0V-3.3V), if not connected to DC718, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired.

BYTE and CS# Jumpers

The demo board is typically shipped with BYTE (**JP3**) and CS# (**JP8**) tied to ground. If you intend to operate this device in a fashion that involves these lines, you can use the jumpers as a means of introducing these signals from an external source.

Reference

JP2 allows you to select an on chip reference or an external LT1019A-2.5 (default) as the reference. The

typical drift specifications of the external reference are similar to the on chip reference, but the LT1019-2.5 has guaranteed maximums.

Analog Input

The demo board is shipped with **JP1** in the “IN” position, in which case, the input amplifier is in the signal path. With **JP1** in the “IN” position, U3 (LT1468) provides a gain of 9dB. This will allow a signal generator, with a 2.5V RMS output level to drive the converter to full scale. This amplifier does not compromise the SNR or distortion performance of the converter. The input noise density of the LT1468 itself is 5nV/√Hz.

In the circuit as configured, the feedback network impedance and the amplifier’s input noise current contribute noise power; to produce an input referred noise density of 7.44nV/√Hz. With a gain of 2.82, this produces 17uV RMS of noise in the 675kHz bandwidth imposed by the converter. This is a signal to noise ratio of 112dB at full scale. This is of course not verifiable at the output of the ADC.

With JP1 in the “OUT” position, the input impedance at J1 is 10KΩ. With JP1 in the “IN” position, the input impedance is very high.

If J1 is driven by a generator intended to drive a 50Ω impedance, you may want to use a 50Ω through-terminator. If a higher impedance source is to be evaluated, you will see better results with the amplifier in the signal path.

If you want to evaluate the amplifier in unity gain, remove R5, or solder a low value resistor in parallel with R16. If you want to evaluate the amplifier with higher gain, you may reduce the value of R5. If you use very high quality resistors, you should be able to increase the gain to 50 before the noise floor of the converter rises discernibly. A voltage gain of 10 should result in the typical SNR of 90dB dropping to 89.9dB. A voltage gain of 50 should give approx 88.7dB, and a gain of 100 would give approximately 86dB SNR. THD will increase but with a gain of 50, the THD of the LT1468 is still typically in the range of -90dB.

If the amplifier is configured for high gain, ground potential differences between the various instruments

on your bench top may be found to develop a differential component at the input to the demo board. Transformer isolation may be required to produce good results with a gain of 50.

Data Collection

The system used for data collection may have a negative effect on how well the demo board performs, if it produces significant ground current through the demo board.

This demo board is tested in house by duplicating the FFT plot shown in the lower left of page 6 of the LTC1606 data sheet. This involves using a low jitter, 250kHz clock source for the encode clock, along with a low noise, low distortion sinusoidal generator at a frequency in the neighborhood of 1KHz. The amplifier is “IN” for in house test, and the input signal level is approx -1dBfs. The FFT shown in the data sheet is a 4096-point FFT, with the input frequency at precisely 1037.5976Hz. This frequency is “coherent” (produces an integral number of cycles of the fundamental within the window) for a 250kHz clock frequency, and a prime number of cycles (17 cycles). A prime number of integral cycles exercises the greatest number of possible input codes. Other clock rates require different input frequencies for coherent sampling. To calculate the input frequency f_i , for a given sampling frequency f_s , number of samples n and prime integer m , use the following formula.

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that

$$f_i = \frac{m}{n} * f_s$$

is common is feeding the converter with a frequency, that is a sub-multiple of the sample rate, and which will only exercise a small subset of the possible output codes.

Also, note that DC1255 does not have an anti-aliasing filter. Following jumper JP1, is an 800kHz first order low pass filter (R1 and C2).

This does not appreciably change the -3dB point of the converter, which is typically 675kHz. Hence, R1 and C2 do not constitute an anti-aliasing filter. If you

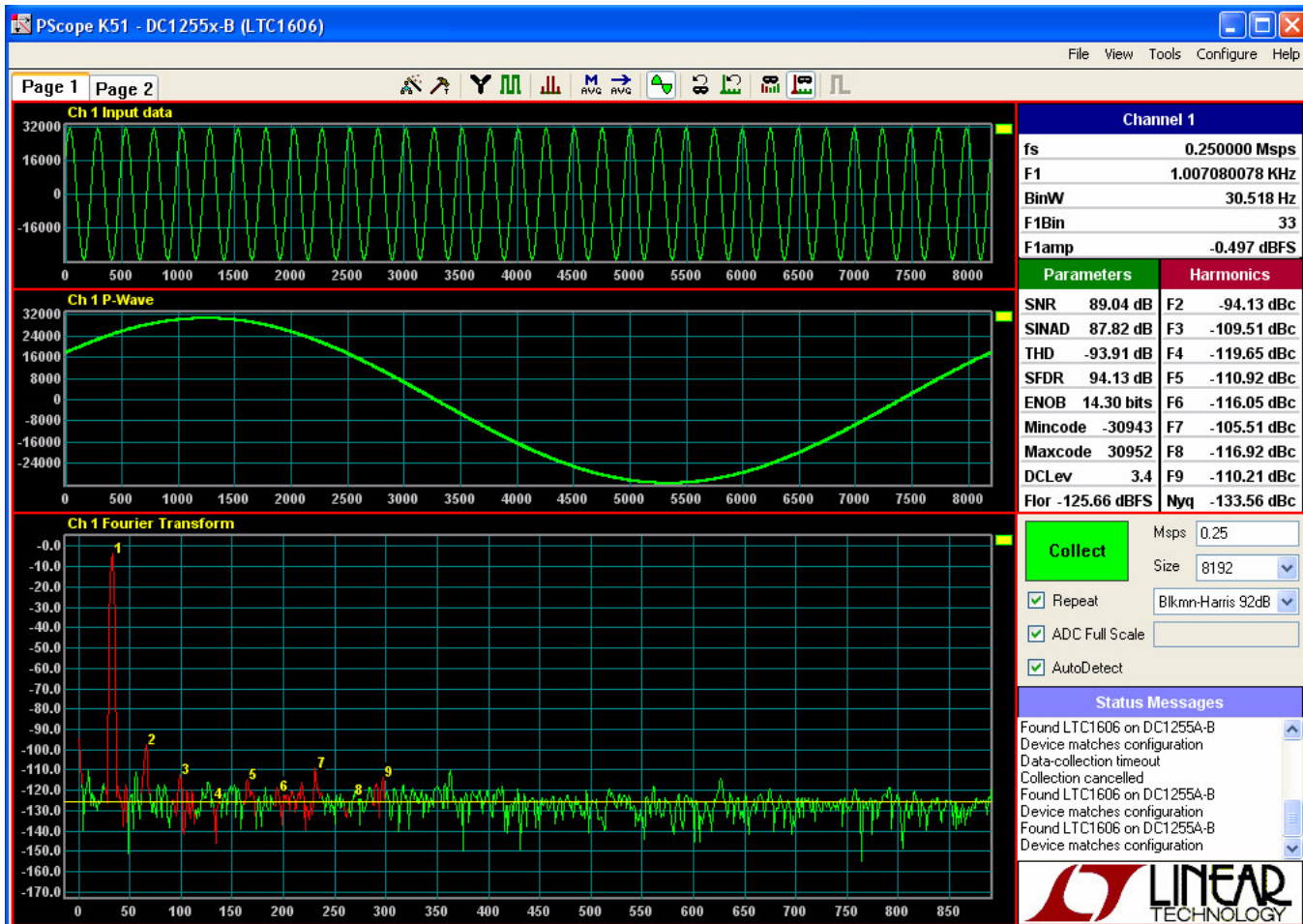
require an anti-aliasing filter in your evaluation, it should generally be placed prior to the LT1468 or any external amplifier in the signal path. If you have frequency components that are above Nyquist ($1/2 f_s$), and up to and beyond 675KHz they will fold back into the DC-125KHz base band, and become indistinguishable from signals in this band.

If you do not have a signal generator capable of ppm levels of frequency accuracy, you can use an FFT with windowing to reduce the “leakage” or spreading of the fundamental, to get a close approximation of the performance parameters. If an amplifier or clock

source with poor phase noise is used, the windowing will not improve the SNR.

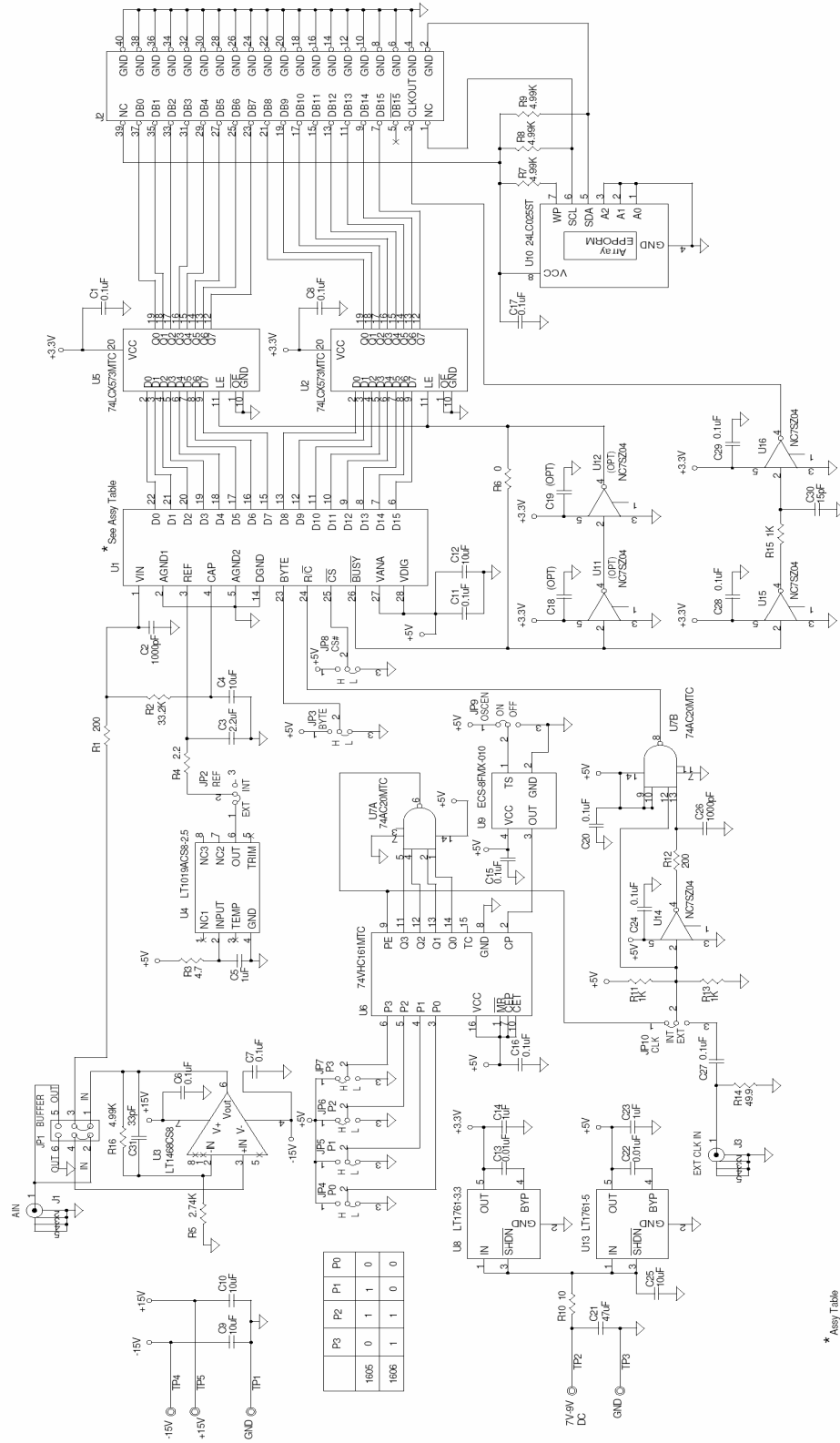
The signal source typically used for in house testing is a B&K 1051. The internal clock source is adequate for most applications. As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC should be used as a guideline for placement, and routing of the various components associated with the ADC. Note should also be taken of the ground plane used in the layout of this board.

Figure 2. DC1255 FastDAACS Screenshot



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16-BIT, 250KSPS ADC



* Assy Table

| Assy Type | U1 | CONVERSION RATE |
|-----------|------------|-----------------|
| A | LTC1605ACG | 100kps |
| B | LTC1608ACG | 250kps |

CUSTOMER NOTICE
 LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER SPECIFICATIONS. HOWEVER, THE USER MUST VERIFY THE OPERATION OF THE ACTUAL APPLICATION, COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT. LINEAR TECHNOLOGY ACCEPTS NO LIABILITY FOR ANY DAMAGE TO PROPERTY OR PERSONS ARISING FROM THE USE OF THIS CIRCUIT. THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

CONTRACT NO. _____
APPROVALS _____
 DRAWN: HELEN
 CHECKED: _____
 APPROVED: _____
 ENGINEER: GUY H.
 DESIGNER: _____

DATE 8/28/07
TITLE LTC1605ACG/LTC1608ACG 16-Bit, 250kps, Single Supply ADC
REV A
DESIGN CODE DMCND
CASE CODE DC1255A-A-B
SCALE _____
FILE NAME _____
SHEET 1 OF 1

QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1255

16-BIT, 250KSPS ADC

| Item | Qty | Reference | Part Description | Manufacturer / Part # |
|--|-----|---|------------------------------------|-----------------------------------|
| REQUIRED CIRCUIT COMPONENTS: | | | | |
| 1 | 13 | C1, C11, C6, C8, C15-C17 C20, C24, C27-C29 | CAP., X7R, 0.1uF, 25V, 10%, 0603 | AVX, 06033C104KAT2A |
| 2 | 3 | C9, C10, C25 | CAP., X5R, 10uF, 25V, 10%, 1206 | Taiyo Yuden, TMK316BJ106KL-T |
| 3 | 2 | C4, C12 | CAP., X5R, 10uF, 6.3V, 10%, 0603 | Murata, GRM188R60J106ME47D |
| 4 | 1 | C3 | CAP., X5R, 2.2uF, 16V, 10%, 0603 | Taiyo Yuden, EMK107BJ225KA-T |
| 5 | 3 | C5, C14, C23 | CAP., X7R, 1uF, 16V, 10%, 0603 | Taiyo Yuden, EMK107BJ105KA-TR |
| 6 | 2 | C13, C22 | CAP., X7R, 0.01uF, 50V, 10%, 0603 | AVX, 06035C103KAT |
| 7 | 1 | C21 | CAP., X5R, 47uF, 16V, 20%, 1210 | Taiyo Yuden, EMK325BJ476MMI-T |
| 8 | 2 | C2, C26 | CAP, NPO, 1000pF, 50V, 10%, 0603 | AVX, 06035A102KAT |
| 9 | 1 | C30 | CAP., X7R, 15pF, 50V, 10%, 0603 | AVX, 06035A150KAT |
| 10 | 1 | C31 | CAP., X7R, 33pF, 50V, 10%, 0603 | AVX, 06035A330KAT |
| 11 | 2 | R1, R12 | RES., CHIP, 200, 1/10W, 5%, 0603 | YAGEO, RC0603JR-07200RL |
| 12 | 1 | R2 | RES., CHIP, 33.2K, 1/10W, 1%, 0603 | YAGEO, RC0603FR-0733K2L |
| 13 | 1 | R3 | RES., CHIP, 4.7, 1/10W, 1%, 0603 | YAGEO, RT0603FR-074R7L |
| 14 | 1 | R4 | RES., CHIP, 2.2, 1/10W, 1%, 0603 | YAGEO, RC0603FR-072R2L |
| 15 | 1 | R5 | RES., CHIP, 2.74K, 1/10W, 1%, 0603 | YAGEO, RT0603FR-072K74L |
| 16 | 1 | R6 | RES., CHIP, 0, 1/10W, 0603 | YAGEO, RT0603FR-070RL |
| 17 | 4 | R7, R8, R9, R16 | RES., CHIP, 4.99K, 1/10W, 1%, 0603 | YAGEO, RT0603FR-074K99L |
| 18 | 1 | R10 | RES., CHIP, 10, 1/10W, 5%, 0603 | YAGEO, RC0603JR-0710RL |
| 19 | 4 | R11, R13, R15 | RES., CHIP, 1K, 1/10W, 1%, 0603 | YAGEO, RT0603FR-071KL |
| 20 | 1 | R14 | RES., CHIP, 49.9, 1/4W, 1%, 1206 | YAGEO, RT1206FR-0749R9L |
| 21 | 2 | U2, U5 | IC, 74LCX573MTC, TSSOP-20PIN | FAIRCHILD, 74LCX573MTCX |
| 22 | 1 | U3 | IC, LT1468CS8, S8 | LINEAR TECH., LT1468CS8#PBF |
| 23 | 1 | U4 | IC, LT1019ACCS8.2.5, S8 | LINEAR TECH., LT1019ACCS8.2.5#PBF |
| 24 | 1 | U6 | IC, 74VHC161MTC, TSSOP | FAIRCHILD, 74VHC161MTCX |
| 25 | 1 | U7 | IC, 74AC20MTC, TSSOP | FAIRCHILD, 74AC20MTCX |
| 26 | 1 | U8 | IC, LT1761ES5-3.3, SOT-23 | LINEAR TECH., LT1761ES5-3.3#PBF |
| 27 | 1 | U9 | IC, 1.000MHZ ECS-8FMX-010 | ECS INC, ECS-8FMX-010-TR |
| 28 | 1 | U10 | IC, 24LC025ST, TSSOP | MICROCHIP 24LC025-I/ST |
| 29 | 3 | U14, U15, U16 | IC, NC7SZ04P5X, SC71 | FAIRCHILD, NC7SZ04P5X |
| 30 | 1 | U13 | IC, LT1761ES5-5, SOT-23 | LINEAR TECH., LT1761ES5-5#PBF |
| 31 | 1 | U1 | IC, LTC1605ACG#PBF, SSOP | LINEAR TECH., LTC1605ACG#PBF |
| ADDITIONAL DEMO BOARD CIRCUIT COMPONENTS: | | | | |
| 1 | 0 | C18, C19(OPT) | CAP., X7R, 0.1uF, 25V, 10%, 0603 | AVX, 06033C104KAT2A |
| 2 | 0 | U11, U12(OPT) | IC, NC7SZ04P5X, SC70 | FAIRCHILD, NC7SZ04P5X |
| HARDWARE-FOR DEMO BOARD ONLY: | | | | |
| 1 | 1 | JP1 | 0.1" DOUBLE ROW HEADER 2X3 | SAMTEC, TSW-103-07-L-D |
| 2 | 9 | JP2 - JP10 | 0.1" SINGLE ROW HEADER, 3 PIN | SAMTEC, TSW-103-07-L-S |
| 3 | 10 | JP1 - JP10 | SHUNT, .1" BLK | SAMTEC SNT-100-BK-G |
| 4 | 5 | TP1-TP5 | TESTPOINT, TURRET, .095" | MILL-MAX, 2501-2-00-90-00-00 |
| 5 | 2 | J1, J3 | CONN, BNC, 5 PINS | CONNEX, 112404 |
| 6 | 1 | J2 | CONN, HDR, 1 X, 1 CNTRS, 40PIN | SAMTEC, TSW-120-07-L-D |
| 7 | 4 | STAND OFF | STAND-OFF, NYLON 0.375" tall | KEYSTONE, 8832 (SNAP ON) |

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16-BIT, 250KSPS ADC

| Item Qty | Reference | Part Description | Manufacturer / Part # |
|--|-----------|---|-------------------------------|
| REQUIRED CIRCUIT COMPONENTS: | | | |
| 1 | 13 | C1,C11,C6-C8,C15-C17 C20,C24,C27-C29 | AVX, 06033C104KAT2A |
| 2 | 3 | CAP., X5R, 10uF, 25V, 10%, 0603 | Taiyo Yuden, TMK316BJ106KL-T |
| 3 | 2 | CAP., X5R, 10uF, 6.3V, 10%, 0603 | Murata, GRM188R60J106ME47D |
| 4 | 1 | CAP., X5R, 2.2uF, 16V, 10%, 0603 | Taiyo Yuden, EMK107BJ225KA-T |
| 5 | 3 | CAP., X7R, 1uF, 16V, 10%, 0603 | Taiyo Yuden, EMK107BJ105KA-TR |
| 6 | 2 | CAP., X7R, 0.01uF, 50V, 10%, 0603 | AVX, 06035C103KAT |
| 7 | 1 | CAP., X5R, 47uF, 16V, 20%, 1210 | Taiyo Yuden, EMK325BJ476MM-T |
| 8 | 2 | CAP., NPO, 1000pF, 50V, 10%, 0603 | AVX, 06035A102KAT |
| 9 | 1 | CAP., X7R, 15pF, 50V, 10%, 0603 | AVX, 06035A150KAT |
| 10 | 1 | CAP., X7R, 33pF, 50V, 10%, 0603 | AVX, 06035A330KAT |
| 11 | 2 | RES., CHIP, 200, 1/10W, 5%, 0603 | YAGEO, RC0603JR-07200RL |
| 12 | 1 | RES., CHIP, 33.2K, 1/10W, 1%, 0603 | YAGEO, RC0603FR-0733K2L |
| 13 | 1 | RES., CHIP, 4.7, 1/10W, 1%, 0603 | YAGEO, RT0603FR-074R7L |
| 14 | 1 | RES., CHIP, 2.2, 1/10W, 1%, 0603 | YAGEO, RC0603FR-072R2L |
| 15 | 1 | RES., CHIP, 2.74K, 1/10W, 1%, 0603 | YAGEO, RT0603FR-072K74L |
| 16 | 1 | RES., CHIP, 0, 1/10W, 0603 | YAGEO, RT0603FR-070RL |
| 17 | 4 | RES., CHIP, 4.99K, 1/10W, 1%, 0603 | YAGEO, RT0603FR-074K99L |
| 18 | 1 | RES., CHIP, 10, 1/10W, 5%, 0603 | YAGEO, RC0603JR-0710RL |
| 19 | 4 | RES., CHIP, 1K, 1/10W, 1%, 0603 | YAGEO, RT0603FR-071KL |
| 20 | 1 | RES., CHIP, 49.9, 1/4W, 1%, 1206 | YAGEO, RT1206FR-0749R9L |
| 21 | 2 | U2,U5 | IC, 74LCX573MTC, TSSOP-20PIN |
| 22 | 1 | U3 | IC, LT1468CS8, S8 |
| 23 | 1 | U4 | IC, LT1019AC8S8-2.5, S8 |
| 24 | 1 | U6 | IC, 74VHC161MTC, TSSOP |
| 25 | 1 | U7 | IC, 74AC20MTC, TSSOP |
| 26 | 1 | U8 | IC, LT1761ES5-3.3, SOT-23 |
| 27 | 1 | U9 | IC, 1.000MHZ ECS-8FMX-010 |
| 28 | 1 | U10 | IC, 24LC025ST, TSSOP |
| 29 | 3 | U14,U15,U16 | IC, NC7SZ04P5X, SC71 |
| 30 | 1 | U13 | IC, LT1761ES5-5, SOT-23 |
| 31 | 1 | U1 | IC, LTC1606ACG#PBF, SSOP |
| ADDITIONAL DEMO BOARD CIRCUIT COMPONENTS: | | | |
| 1 | 0 | C18,C19(OPT) | AVX, 06033C104KAT2A |
| 2 | 0 | U11,U12(OPT) | FAIRCHILD, NC7SZ04P5X |
| HARDWARE-FOR DEMO BOARD ONLY: | | | |
| 1 | 1 | JP1 | SAMTEC, TSW-103-07-L-D |
| 2 | 9 | JP2 - JP10 | SAMTEC, TSW-103-07-L-S |
| 3 | 10 | JP1 - JP10 | SAMTEC, SNT-100-BK-G |
| 4 | 5 | TP1-TP5 | MILL-MAX, 2501-2-00-80-00-00 |
| 5 | 2 | J1,J3 | CONNEX, 112404 |
| 6 | 1 | J2 | SAMTEC, TSW-120-07-L-D |
| 7 | 4 | STAND OFF | KEYSTONE, 8832 (SNAP ON) |

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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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Email: org@lifeelectronics.ru