

# 74LVT241

## 3.3 V octal buffer/line driver; 3-state

Rev. 4 — 27 March 2019

Product data sheet

## 1. General description

The 74LVT241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables ( $\overline{1OE}$ ,  $2OE$ ), each controlling four of the 3-state outputs.

## 2. Features

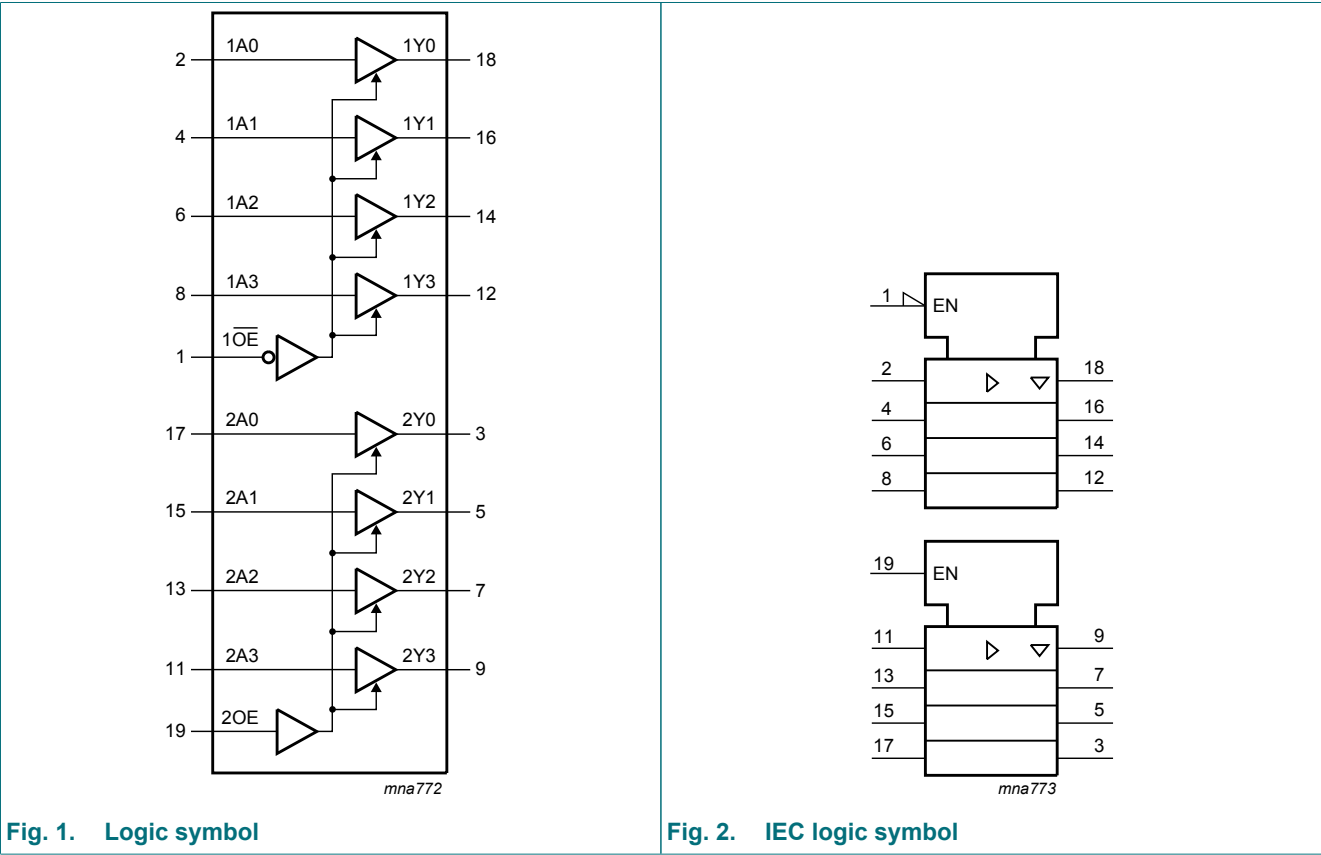
- 3-state buffers
- Octal bus interface
- Input and output interface capability to systems at 5 V supply
- TTL input and output switching levels
- Output capability: +64 mA/-32 mA
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Bus-hold data inputs eliminate the need for external pull-up resistors for unused inputs
- Live insertion/extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus

## 3. Ordering information

Table 1. Ordering information

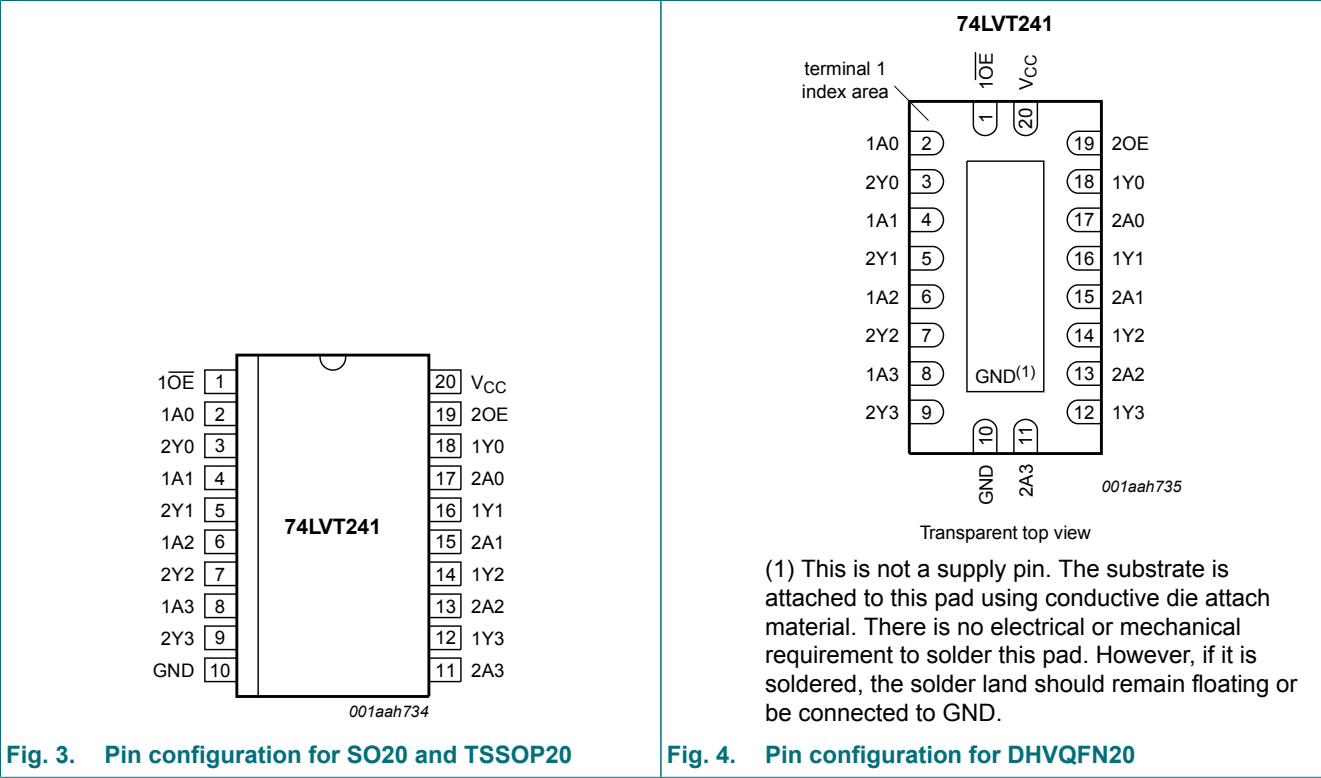
| Type number | Package           |          |                                                                                                                                |          |
|-------------|-------------------|----------|--------------------------------------------------------------------------------------------------------------------------------|----------|
|             | Temperature range | Name     | Description                                                                                                                    | Version  |
| 74LVT241D   | -40 °C to +85 °C  | SO20     | plastic small outline package; 20 leads; body width 7.5 mm                                                                     | SOT163-1 |
| 74LVT241PW  | -40 °C to +85 °C  | TSSOP20  | plastic thin shrink small outline package; 20 leads; body width 4.4 mm                                                         | SOT360-1 |
| 74LVT241BQ  | -40 °C to +85 °C  | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm | SOT764-1 |

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol     | Pin            | Description                       |
|------------|----------------|-----------------------------------|
| 1OE        | 1              | output enable input (active LOW)  |
| 1A0 to 1A3 | 2, 4, 6, 8     | data input                        |
| 2A0 to 2A3 | 17, 15, 13, 11 | data input                        |
| GND        | 10             | ground (0 V)                      |
| 1Y0 to 1Y3 | 18, 16, 14, 12 | data output                       |
| 2Y0 to 2Y3 | 3, 5, 7, 9     | data output                       |
| 2OE        | 19             | output enable input (active HIGH) |
| VCC        | 20             | supply voltage                    |

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = High impedance "OFF" state.*

| Inputs |     |     |     | Outputs |     |
|--------|-----|-----|-----|---------|-----|
| 1OE    | 2OE | 1An | 2An | 1Yn     | 2Yn |
| L      | H   | L   | L   | L       | L   |
| L      | H   | H   | H   | H       | H   |
| H      | L   | X   | X   | Z       | Z   |

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol           | Parameter               | Conditions                          | Min      | Max  | Unit |
|------------------|-------------------------|-------------------------------------|----------|------|------|
| V <sub>CC</sub>  | supply voltage          |                                     | -0.5     | +4.6 | V    |
| V <sub>I</sub>   | input voltage           |                                     | [1] -0.5 | +7.0 | V    |
| V <sub>O</sub>   | output voltage          | output in OFF or HIGH state         | [1] -0.5 | +7.0 | V    |
| I <sub>IK</sub>  | input clamping current  | V <sub>I</sub> < 0 V                | -50      | -    | mA   |
| I <sub>OK</sub>  | output clamping current | V <sub>O</sub> < 0 V                | -50      | -    | mA   |
| I <sub>O</sub>   | output current          | output in LOW state                 | -        | 128  | mA   |
|                  |                         | output in HIGH state                | -64      | -    | mA   |
| T <sub>stg</sub> | storage temperature     |                                     | -65      | +150 | °C   |
| T <sub>j</sub>   | junction temperature    |                                     | [2] -    | +150 | °C   |
| P <sub>tot</sub> | total power dissipation | T <sub>amb</sub> = -40 °C to +85 °C | [3] -    | 500  | mW   |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[3] For SO20 package: above 70 °C derate linearly with 8 mW/K.  
 For TSSOP20 package: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN20 package: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol           | Parameter                           | Conditions                                        | Min | Max | Unit |
|------------------|-------------------------------------|---------------------------------------------------|-----|-----|------|
| V <sub>CC</sub>  | supply voltage                      |                                                   | 2.7 | 3.6 | V    |
| V <sub>I</sub>   | input voltage                       |                                                   | 0   | 5.5 | V    |
| I <sub>OH</sub>  | HIGH-level output current           |                                                   | -32 | -   | mA   |
| I <sub>OL</sub>  | LOW-level output current            |                                                   | -   | 32  | mA   |
|                  |                                     | current duty cycle ≤ 50 %; f <sub>i</sub> ≥ 1 kHz | -   | 64  | mA   |
| T <sub>amb</sub> | ambient temperature                 | in free air                                       | -40 | +85 | °C   |
| Δt/ΔV            | input transition rise and fall rate | output enabled                                    | 0   | 10  | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V);  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

| Symbol          | Parameter                          | Conditions                                                                                                                                           | Min            | Typ[1]         | Max       | Unit          |
|-----------------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------------|-----------|---------------|
| $V_{IK}$        | input clamping voltage             | $V_{CC} = 2.7\text{ V}$ ; $I_{IK} = -18\text{ mA}$                                                                                                   | -1.2           | -0.9           | -         | V             |
| $V_{IH}$        | HIGH-level input voltage           |                                                                                                                                                      | 2.0            | -              | -         | V             |
| $V_{IL}$        | LOW-level input voltage            |                                                                                                                                                      | -              | -              | 0.8       | V             |
| $V_{OH}$        | HIGH-level output voltage          | $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$                                                                       | $V_{CC} - 0.2$ | $V_{CC} - 0.1$ | -         | V             |
|                 |                                    | $V_{CC} = 2.7\text{ V}$ ; $I_{OH} = -8\text{ mA}$                                                                                                    | 2.4            | 2.5            | -         | V             |
|                 |                                    | $V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -32\text{ mA}$                                                                                                   | 2.0            | 2.2            | -         | V             |
| $V_{OL}$        | LOW-level output voltage           | $V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 100\text{ }\mu\text{A}$                                                                                          |                | 0.1            | 0.2       | V             |
|                 |                                    | $V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 24\text{ mA}$                                                                                                    | -              | 0.3            | 0.5       | V             |
|                 |                                    | $V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 16\text{ mA}$                                                                                                    | -              | 0.25           | 0.4       | V             |
|                 |                                    | $V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 32\text{ mA}$                                                                                                    | -              | 0.3            | 0.5       | V             |
|                 |                                    | $V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 64\text{ mA}$                                                                                                    | -              | 0.4            | 0.55      | V             |
| $I_I$           | input leakage current              | control and data pins                                                                                                                                |                |                |           |               |
|                 |                                    | $V_{CC} = 0\text{ V}$ or $3.6\text{ V}$ ; $V_I = 5.5\text{ V}$                                                                                       | -              | 1              | 10        | $\mu\text{A}$ |
|                 |                                    | control pins                                                                                                                                         |                |                |           |               |
|                 |                                    | $V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND                                                                                                      | -              | 0.1            | $\pm 1$   | $\mu\text{A}$ |
|                 |                                    | data pins [2]                                                                                                                                        |                |                |           |               |
|                 |                                    | $V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$                                                                                                             | -              | 0.1            | 1         | $\mu\text{A}$ |
|                 |                                    | $V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$                                                                                                         | -5             | -1             | -         | $\mu\text{A}$ |
| $I_{OFF}$       | power-off leakage current          | $V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V}$ to $4.5\text{ V}$                                                                                | -              | 1              | $\pm 100$ | $\mu\text{A}$ |
| $I_{BHL}$       | bus hold LOW current               | $V_{CC} = 3.0\text{ V}$ ; $V_I = 0.8\text{ V}$                                                                                                       | 75             | 150            | -         | $\mu\text{A}$ |
| $I_{BHH}$       | bus hold HIGH current              | $V_{CC} = 3.0\text{ V}$ ; $V_I = 2.0\text{ V}$                                                                                                       | -              | -150           | -75       | $\mu\text{A}$ |
| $I_{BHLO}$      | bus hold LOW overdrive current     | $V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$ to $3.6\text{ V}$ [3]                                                                                   | 500            | -              | -         | $\mu\text{A}$ |
| $I_{BHHO}$      | bus hold HIGH overdrive current    | $V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$ to $3.6\text{ V}$ [3]                                                                                   | -              | -              | -500      | $\mu\text{A}$ |
| $I_{LO}$        | output leakage current             | $V_O = 5.5\text{ V}$ ; $V_{CC} = 3.0\text{ V}$ ; output HIGH                                                                                         | -              | 60             | 125       | $\mu\text{A}$ |
| $I_{O(pu/pd)}$  | power-up/power-down output current | $V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V}$ to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $1\text{OE}$ , $2\text{OE} = \text{don't care}$ [4] | -              | $\pm 1$        | $\pm 100$ | $\mu\text{A}$ |
| $I_{OZ}$        | OFF-state output current           | $V_{CC} = 3.6\text{ V}$ ; $V_O = 3.0\text{ V}$                                                                                                       | -              | 1              | 5         | $\mu\text{A}$ |
|                 |                                    | $V_{CC} = 3.6\text{ V}$ ; $V_O = 0.5\text{ V}$                                                                                                       | -5             | -1             | -         | $\mu\text{A}$ |
| $I_{CC}$        | supply current                     | $V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$                                                                                  |                |                |           |               |
|                 |                                    | outputs HIGH                                                                                                                                         | -              | 0.12           | 0.19      | mA            |
|                 |                                    | outputs LOW                                                                                                                                          | -              | 3              | 12        | mA            |
|                 |                                    | outputs disabled [5]                                                                                                                                 | -              | 0.12           | 0.19      | mA            |
| $\Delta I_{CC}$ | additional supply current          | per input pin; $V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$ ; one input = $V_{CC} - 0.6\text{ V}$ other inputs at $V_{CC}$ or GND [6]                   | -              | 0.1            | 0.25      | mA            |
| $C_I$           | input capacitance                  | $1\text{OE}$ and $2\text{OE}$ inputs; outputs disabled; $V_I = 0\text{ V}$ or $3.0\text{ V}$                                                         | -              | 4              | -         | pF            |

| Symbol    | Parameter                | Conditions                                                                               | Min | Typ[1] | Max | Unit |
|-----------|--------------------------|------------------------------------------------------------------------------------------|-----|--------|-----|------|
| $C_{I/O}$ | input/output capacitance | at input/output data pins, outputs disabled;<br>$V_{I/O} = 0\text{ V}$ or $3.0\text{ V}$ | -   | 8      | -   | pF   |

[1] All typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] Unused pins at  $V_{CC}$  or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any  $V_{CC}$  between  $0\text{ V}$  and  $1.2\text{ V}$  with a transition time of up to  $10\text{ ms}$ .

From  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  a transition time of  $100\text{ ms}$  is permitted. This parameter is valid for  $T_{amb} = +25\text{ }^{\circ}\text{C}$  only.

[5]  $I_{CC}$  with the outputs disabled is measured with outputs pulled to  $V_{CC}$  or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground =  $0\text{ V}$ ). For test circuit see Fig. 8;  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

| Symbol    | Parameter                           | Conditions                               | Min | Typ[1] | Max | Unit |
|-----------|-------------------------------------|------------------------------------------|-----|--------|-----|------|
| $t_{PLH}$ | LOW to HIGH propagation delay       | 1An to 1Yn, 2An to 2Yn; see Fig. 5       |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 4.0 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 2.8    | 3.8 | ns   |
| $t_{PHL}$ | HIGH to LOW propagation delay       | 1An to 1Yn, 2An to 2Yn; see Fig. 5       |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 4.0 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 2.8    | 3.8 | ns   |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | $1\overline{OE}$ to 1Yn; see Fig. 6      |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 5.0 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 3.2    | 4.4 | ns   |
|           |                                     | 2OE to 2Yn; see Fig. 7                   |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 5.6 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 3.8    | 5.1 | ns   |
| $t_{PZL}$ | OFF-state to LOW propagation delay  | $1\overline{OE}$ to 1Yn; see Fig. 6      |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 4.9 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 3.1    | 4.3 | ns   |
|           |                                     | 2OE to 2Yn; see Fig. 7                   |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 5.4 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 3.8    | 5.0 | ns   |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | $1\overline{OE}$ to 1Yn; see Fig. 6      |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 5.4 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 2.0 | 3.6    | 5.2 | ns   |
|           |                                     | 2OE to 2Yn; see Fig. 7                   |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 5.0 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 3.1    | 4.5 | ns   |
| $t_{PLZ}$ | LOW to OFF-state propagation delay  | $1\overline{OE}$ to 1Yn; see Fig. 6      |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 4.3 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.6 | 2.9    | 4.2 | ns   |
|           |                                     | 2OE to 2Yn; see Fig. 7                   |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                  | -   | -      | 4.3 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 2.8    | 4.0 | ns   |

[1] Typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$  and  $V_{CC} = 3.3\text{ V}$ .

10.1. Waveforms and test circuit

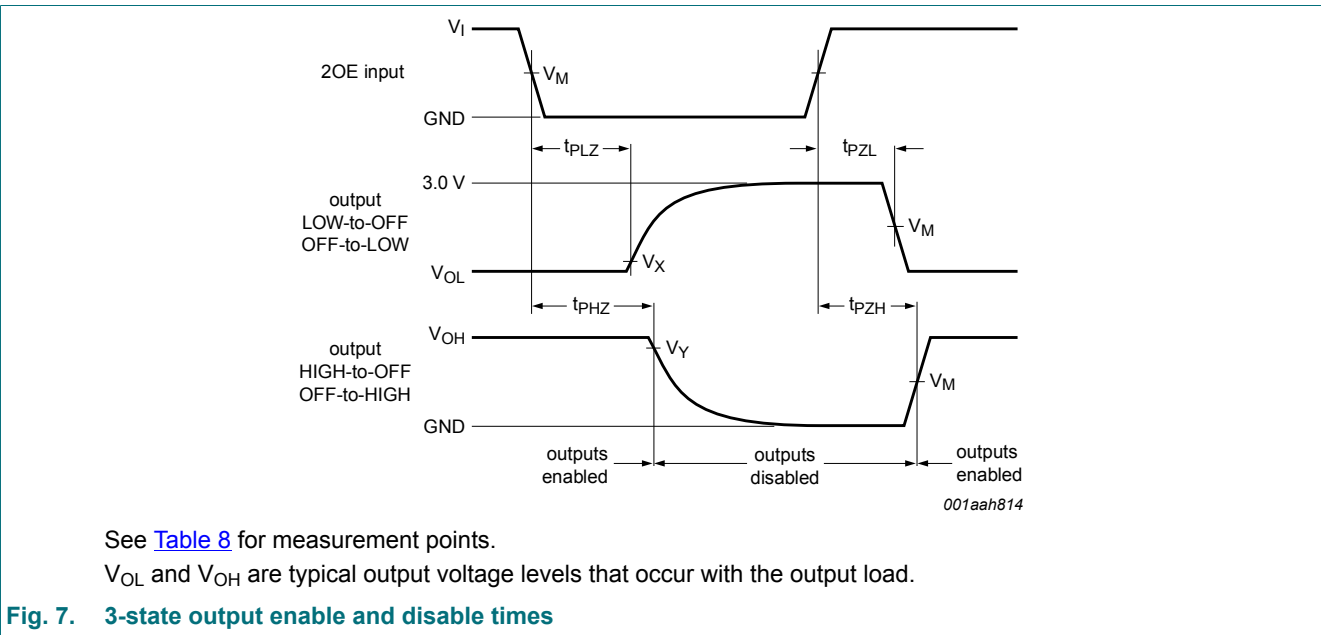
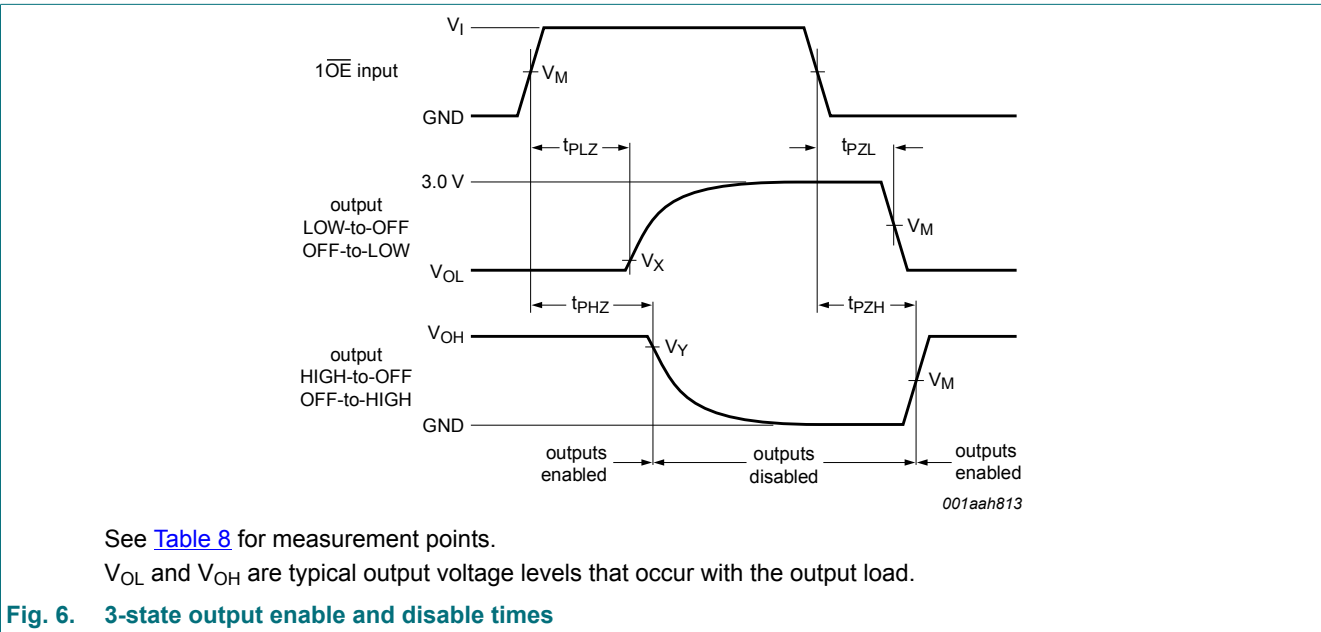
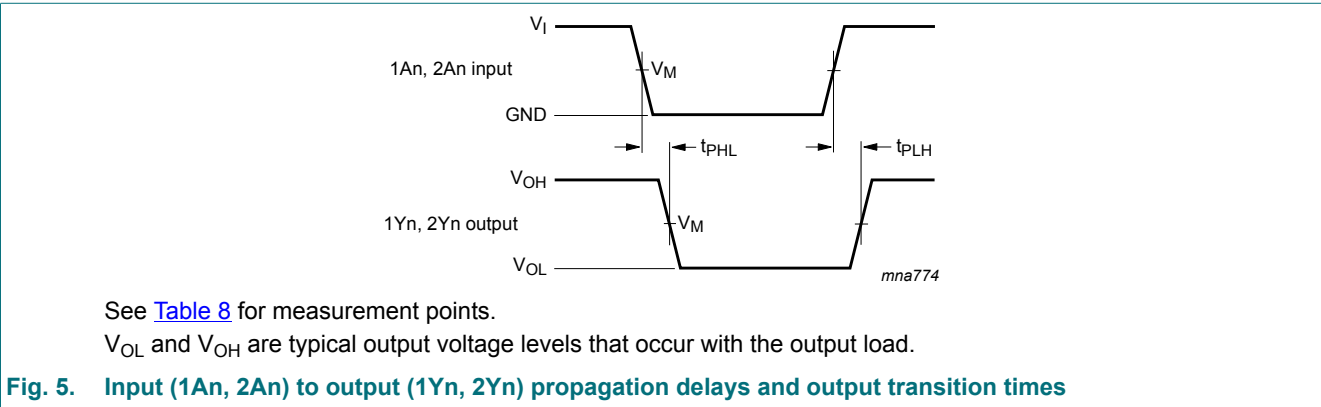
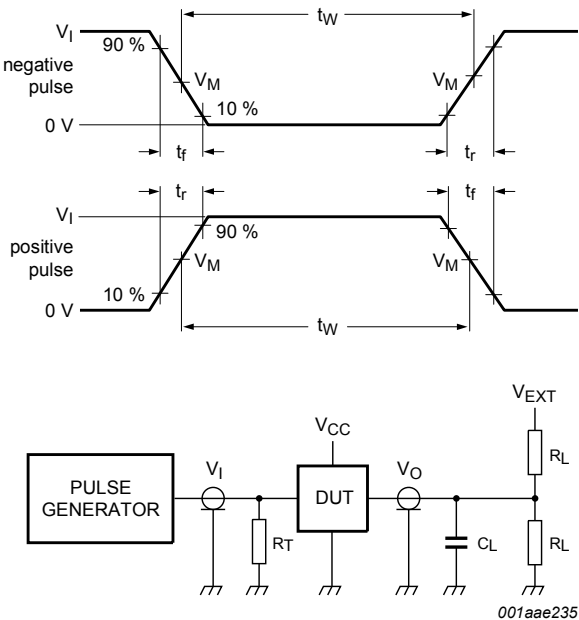


Table 8. Measurement points

| V <sub>CC</sub> | Input          | Output                  |                         |                |
|-----------------|----------------|-------------------------|-------------------------|----------------|
|                 | V <sub>M</sub> | V <sub>X</sub>          | V <sub>Y</sub>          | V <sub>M</sub> |
| 2.7 V to 3.6 V  | 1.5 V          | V <sub>OL</sub> + 0.3 V | V <sub>OH</sub> - 0.3 V | 1.5 V          |



Test data is given in [Table 9](#).  
Definitions test circuit:  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.  
 $V_{EXT}$  = External voltage for measuring switching times.

Fig. 8. Test circuit for switching times

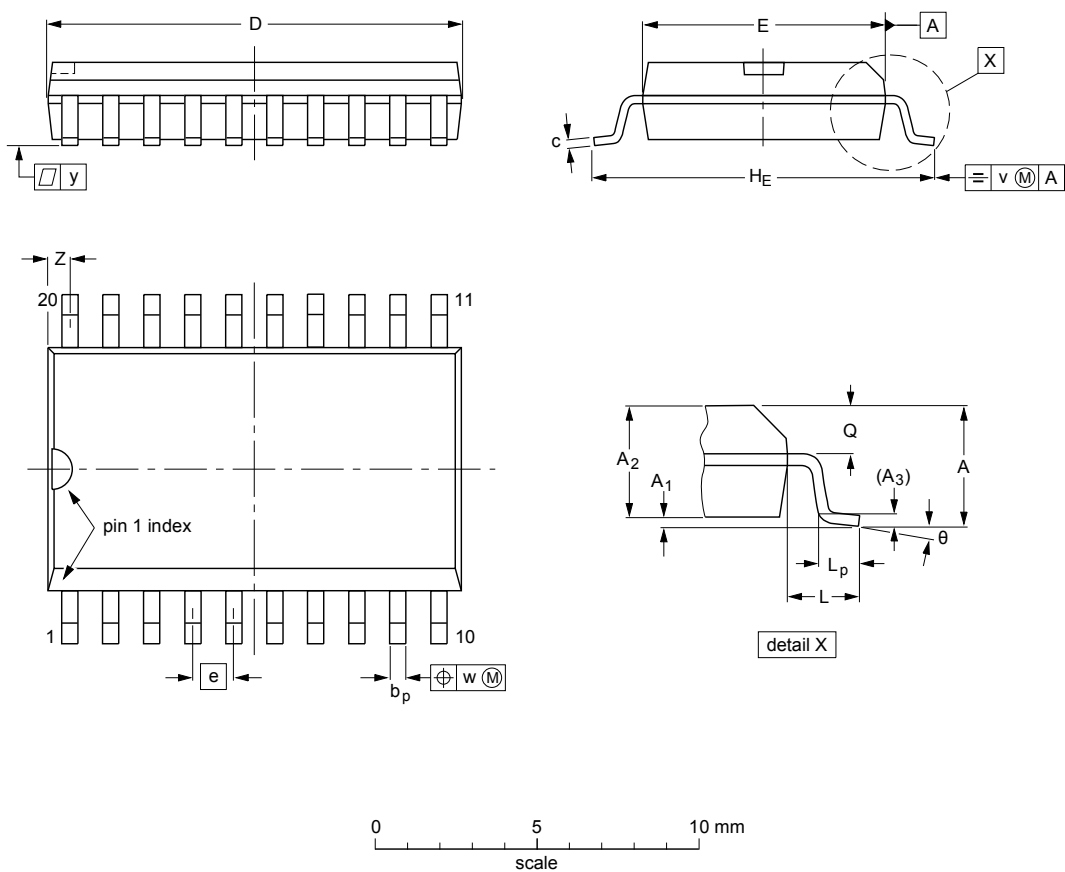
Table 9. Test data

| Input          |                |                |                                 | Load           |                | V <sub>EXT</sub>                    |                                     |                                     |
|----------------|----------------|----------------|---------------------------------|----------------|----------------|-------------------------------------|-------------------------------------|-------------------------------------|
| V <sub>I</sub> | f <sub>i</sub> | t <sub>W</sub> | t <sub>r</sub> , t <sub>f</sub> | R <sub>L</sub> | C <sub>L</sub> | t <sub>PHZ</sub> , t <sub>PZH</sub> | t <sub>PLZ</sub> , t <sub>PZL</sub> | t <sub>PLH</sub> , t <sub>PHL</sub> |
| 2.7 V          | ≤ 10 MHz       | 500 ns         | ≤ 2.5 ns                        | 500 Ω          | 50 pF          | GND                                 | 6 V                                 | open                                |

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A<br>max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|-----------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65      | 0.3<br>0.1     | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 13.0<br>12.6     | 7.6<br>7.4       | 1.27 | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.1       | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49     | 0.30<br>0.29     | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

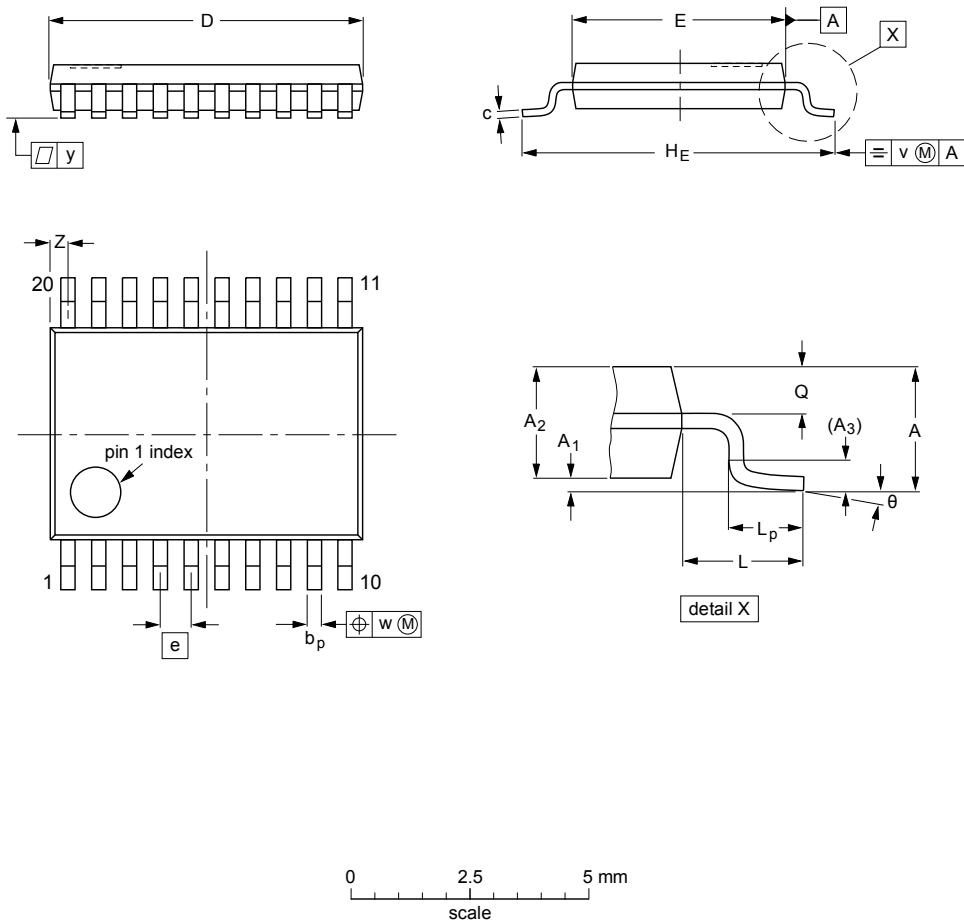
Note  
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE<br>VERSION | REFERENCES |        |       |  | EUROPEAN<br>PROJECTION | ISSUE DATE            |
|--------------------|------------|--------|-------|--|------------------------|-----------------------|
|                    | IEC        | JEDEC  | JEITA |  |                        |                       |
| SOT163-1           | 075E04     | MS-013 |       |  |                        | -99-12-27<br>03-02-19 |

Fig. 9. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A <sub>max.</sub> | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e    | H <sub>E</sub> | L | L <sub>p</sub> | Q          | v   | w    | y   | Z <sup>(1)</sup> | θ        |
|------|-------------------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|---|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 1.1               | 0.15<br>0.05   | 0.95<br>0.80   | 0.25           | 0.30<br>0.19   | 0.2<br>0.1 | 6.6<br>6.4       | 4.5<br>4.3       | 0.65 | 6.6<br>6.2     | 1 | 0.75<br>0.50   | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2       | 8°<br>0° |

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE<br>VERSION | REFERENCES |        |       |  | EUROPEAN<br>PROJECTION                                                                | ISSUE DATE                      |
|--------------------|------------|--------|-------|--|---------------------------------------------------------------------------------------|---------------------------------|
|                    | IEC        | JEDEC  | JEITA |  |                                                                                       |                                 |
| SOT360-1           |            | MO-153 |       |  |  | <del>99-12-27</del><br>03-02-19 |

Fig. 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

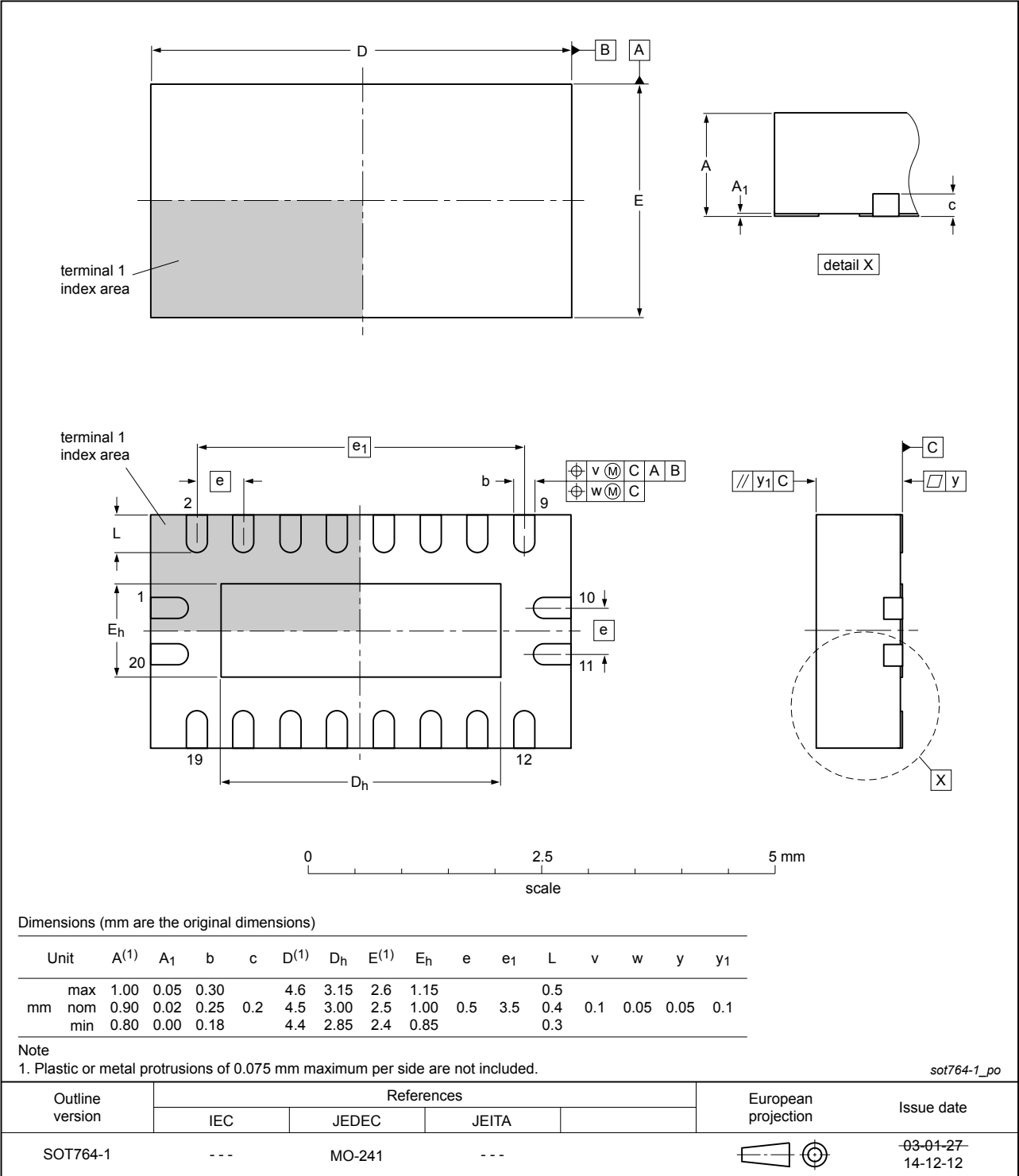


Fig. 11. Package outline SOT764-1 (DHVQFN20)

## 12. Abbreviations

Table 10. Abbreviations

| Acronym | Description                                     |
|---------|-------------------------------------------------|
| BiCMOS  | Bipolar Complementary Metal Oxide Semiconductor |
| CDM     | Charged Device Model                            |
| DUT     | Device Under Test                               |
| ESD     | ElectroStatic Discharge                         |
| HBM     | Human Body Model                                |
| TTL     | Transistor-Transistor Logic                     |

## 13. Revision history

Table 11. Revision history

| Document ID    | Release date                                                                                                                                                                                                                                                                                                                                                                    | Data sheet status     | Change notice | Supersedes    |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------|---------------|
| 74LVT241 v. 3  | 20190327                                                                                                                                                                                                                                                                                                                                                                        | Product data sheet    |               | 74LVT241 v. 3 |
| Modifications: | <ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li><a href="#">Fig. 11</a>: package outline drawing SOT764-1 (DHVQFN20) updated.</li><li>Type number 74LVT241DB (SOT339-1) removed.</li></ul> |                       |               |               |
| 74LVT241 v. 3  | 20080507                                                                                                                                                                                                                                                                                                                                                                        | Product data sheet    | ECN07_046     | 74LVT241 v. 2 |
| Modifications: | <ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>DHVQFN20 package added <a href="#">Section 3</a> and <a href="#">Section 11</a>.</li></ul>                                   |                       |               |               |
| 74LVT241 v. 2  | 19980219                                                                                                                                                                                                                                                                                                                                                                        | Product specification | -             | 74LVT241 v. 1 |
| 74LVT241 v. 1  | 19960529                                                                                                                                                                                                                                                                                                                                                                        | Product specification | -             | -             |

## 14. Legal information

### Data sheet status

| Document status<br>[1][2]      | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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