74LVCU04A

Hex unbuffered inverter

Rev. 8 — 18 December 2015 | Product data sheet

1. General description

The 74LVCU04A is a general purpose hex unbuffered inverter. Each of the six inverters is a single stage with unbuffered outputs.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVCU04AD	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVCU04ADB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVCU04APW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVCU04ABQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

nexperia

4. Functional diagram

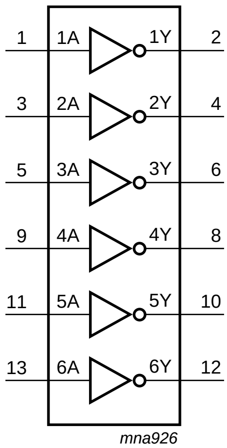


Fig 1. Logic symbol

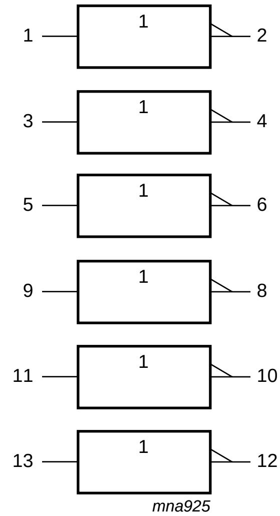


Fig 2. IEC logic symbol

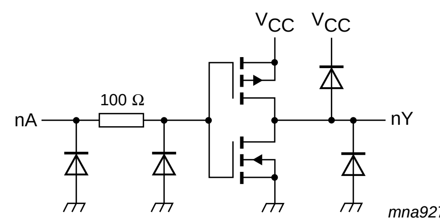


Fig 3. Schematic diagram for one inverter

5. Pinning information

5.1 Pinning

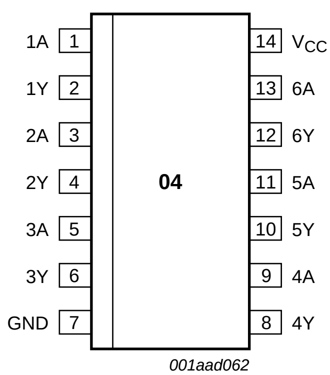
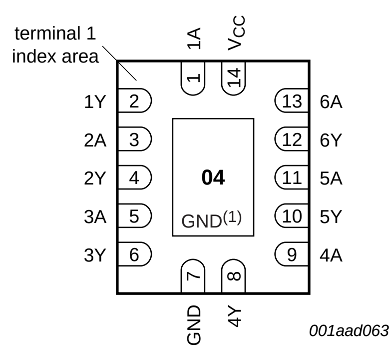


Fig 4. Pin configuration for SO14 and (T)SSOP14



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration for DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input nA	Output nY
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	–50	-	mA
V_I	input voltage	[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	[2]	–0.5	V_{CC} + 0.5	V
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		–100	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{OL(max)}$ = 0.5 V; I_O = –100 μA						
		V_{CC} = 1.2 V	1.08	-	-	1.12	-	V
		V_{CC} = 1.65 V to 1.95 V	1.3	-	-	1.5	-	V
		V_{CC} = 2.3 V to 2.7 V	1.8	-	-	2.0	-	V
		V_{CC} = 3.0 V	2.0	-	-	2.4	-	V
		V_{CC} = 3.6 V	2.4	-	-	2.8	-	V
V_{IL}	LOW-level input voltage	$V_{OH(min)}$ = V_{CC} – 0.5 V; I_O = –100 μA						
		V_{CC} = 1.2 V	-	-	0.12	-	0.1	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.6	-	0.4	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.6	-	0.5	V
		V_{CC} = 3.0 V	-	-	1.0	-	0.6	V
		V_{CC} = 3.6 V	-	-	1.2	-	0.7	V
V_{OH}	HIGH-level output voltage	V_I = GND						
		V_{CC} = 3.0 V; I_O = –100 μA	V_{CC} – 0.2	-	-	V_{CC} – 0.3	-	V
		V_{CC} = 1.65 V; I_O = –4 mA	1.2	-	-	1.05	-	V
		V_{CC} = 2.3 V; I_O = –8 mA	1.8	-	-	1.65	-	V
		V_{CC} = 2.7 V; I_O = –12 mA	2.2	-	-	2.05	-	V
		V_{CC} = 3.0 V; I_O = –18 mA	2.4	-	-	2.25	-	V
		V_{CC} = 3.0 V; I_O = –24 mA	2.2	-	-	2.0	-	V

Table 6. Static characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{CC}$						
		V_{CC} = 3.0 V; I_O = 100 μA	-	-	0.20	-	0.60	V
		V_{CC} = 1.65 V; I_O = 4 mA	-	-	0.45	-	0.65	V
		V_{CC} = 2.3 V; I_O = 8 mA	-	-	0.60	-	0.80	V
		V_{CC} = 2.7 V; I_O = 12 mA	-	-	0.40	-	0.30	V
		V_{CC} = 3.0 V; I_O = 24 mA	-	-	0.55	-	0.80	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I_{CC}	supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V; I_O = 0 A	-	5	500	-	5000	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.5	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 6	[2]						
		V_{CC} = 1.2 V		-	6.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		0.3	3.7	7.8	0.3	9.0	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	2.2	4.4	0.5	5.2	ns
		V_{CC} = 2.7 V		0.5	2.0	4.5	0.5	6.0	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	2.0	4.0	0.5	5.0	ns
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per inverter; V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	2.3	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	5.5	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	8.4	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

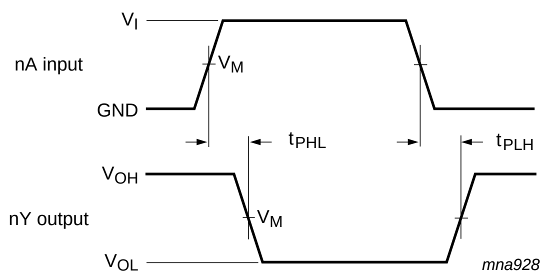
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

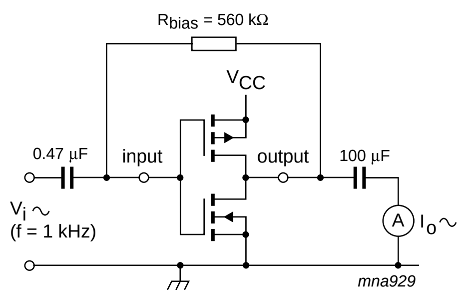
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. Waveforms



V_M = 1.5 V at $V_{CC} \geq 2.7$ V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V;
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

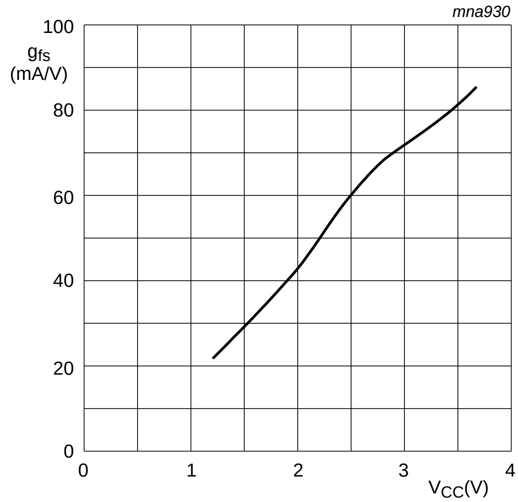
Fig 6. Input (nA) to output (nY) propagation delays



$$g_{fs} = \frac{dI_O}{dV_I}; \ at\ constant\ V_O$$

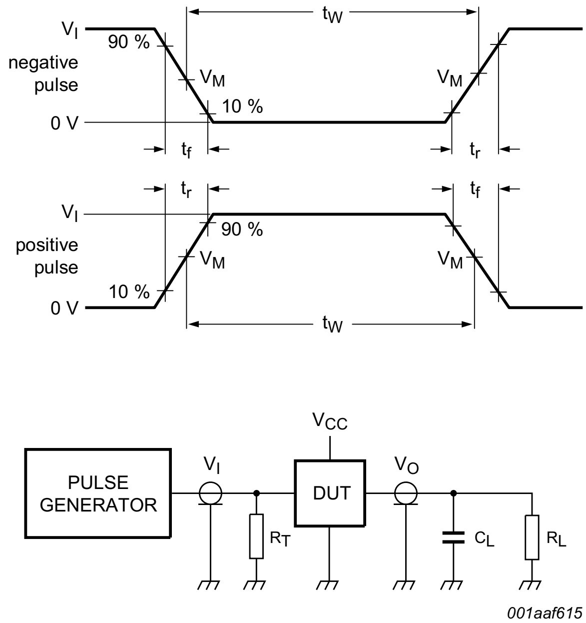
f_i = 1 kHz at V_O is constant

Fig 7. Test setup for measuring forward transconductance



T_{amb} = 25 °C

Fig 8. Typical forward transconductance as a function of supply voltage



Test data is given in Table 8.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 9. Test circuit for measuring switching times

Table 8. Test data

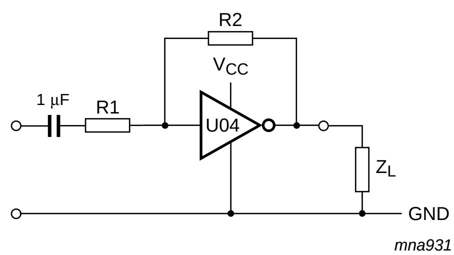
Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

12. Application information

12.1 Application diagrams

Some applications for the 74LVCU04A are:

- Linear amplifier: see Figure 10
- Crystal oscillator designs; see Figure 11
- Astable multivibrator; see Figure 12



$V_{o(p-p)} = V_{CC} - 1.5$ V centered at $0.5V_{CC}$.

$$A_u = -\frac{G_{OL}}{1 + \frac{R1}{R2}(1 + G_{OL})}$$

G_{OL} = loop gain.

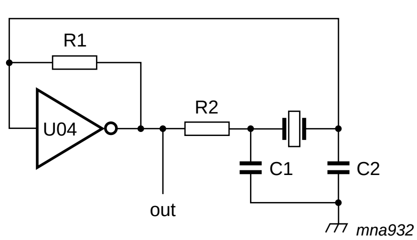
A_u = voltage amplification.

R1 ≥ 3 kΩ, R2 ≤ 1 MΩ

Z_L > 10 kΩ; A_{OL} = 20 (typ.)

Typical unity gain bandwidth product is 5 MHz.

Fig 10. 74LVCU04A used as linear amplifier



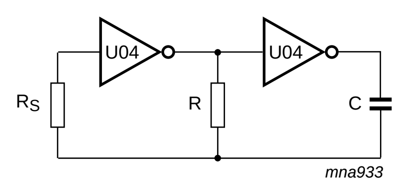
C_1 = 47 pF (typical)

C_2 = 22 pF (typical)

R_1 = 1 to 10 MΩ (typical)

R_2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at V_{CC} = 3 V and f = 1 MHz)

Fig 11. 74LVCU04A used as crystal oscillator



$$f = \frac{1}{T} \approx \frac{1}{2.2RC}$$

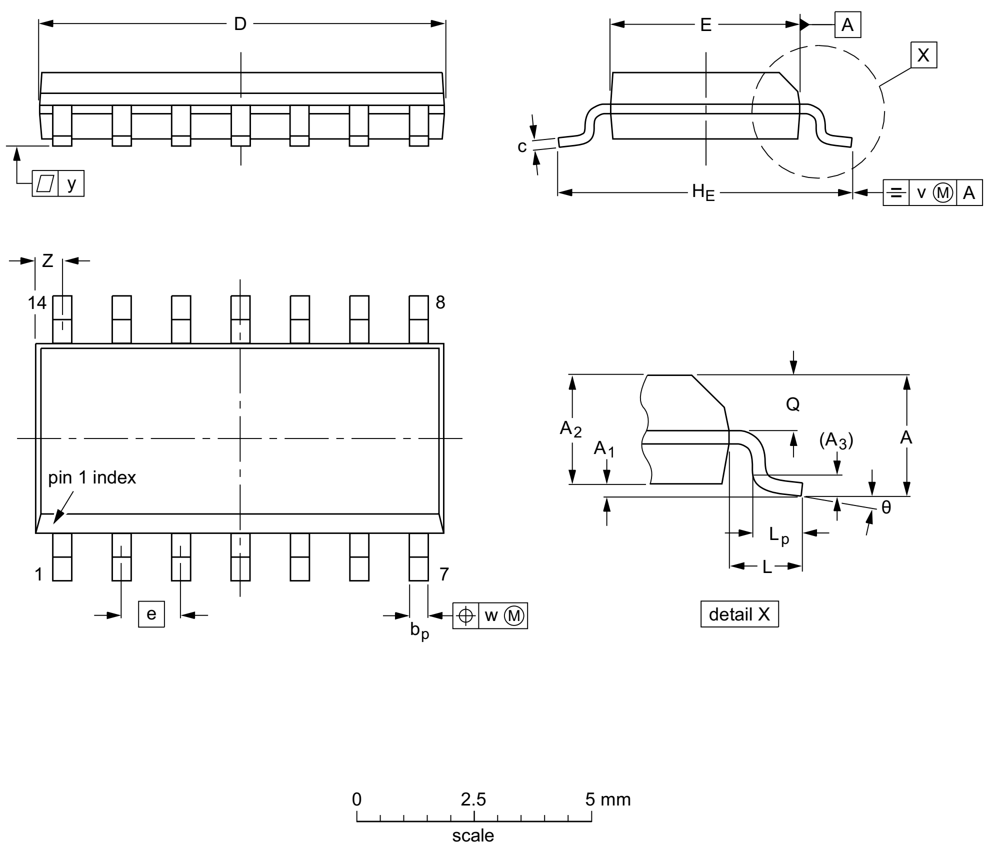
$R_S \approx 2R$.

The average I_{CC} is approximately 3.5 + 0.05f (MHz) × C (pF) [mA] at V_{CC} = 3.0 V.

Fig 12. 74LVCU04A used as astable multivibrator

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

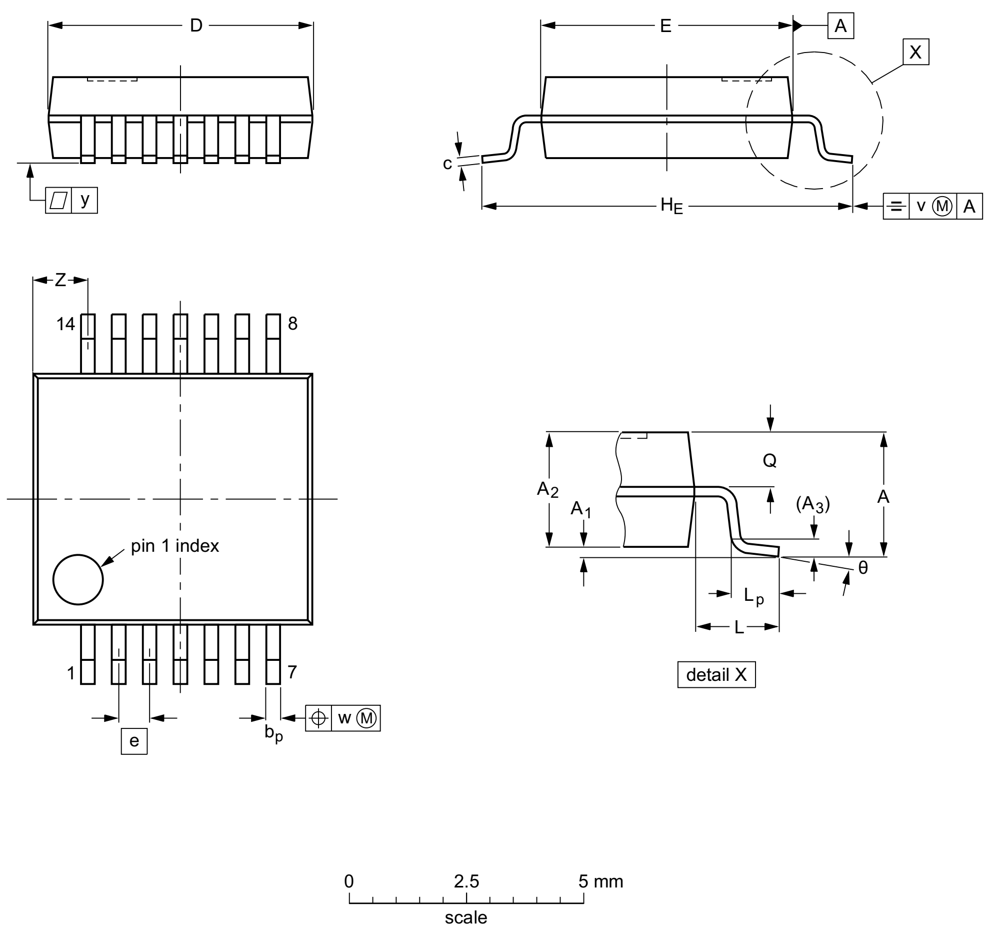
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

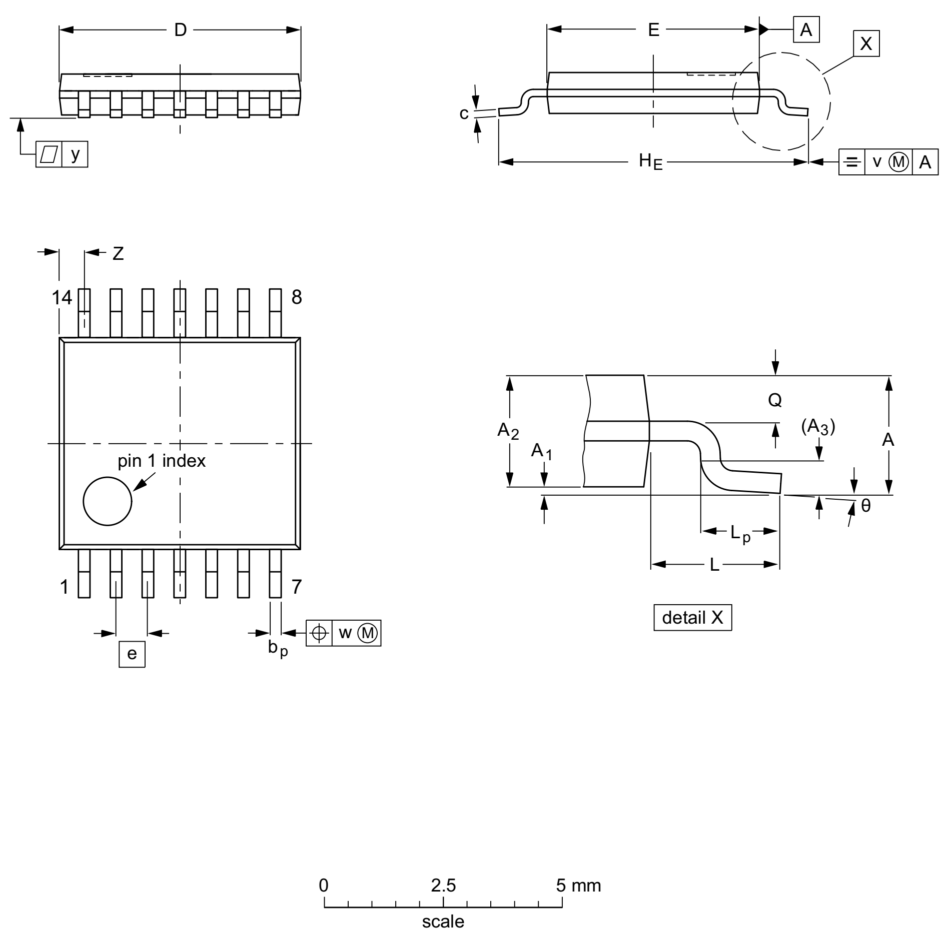
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

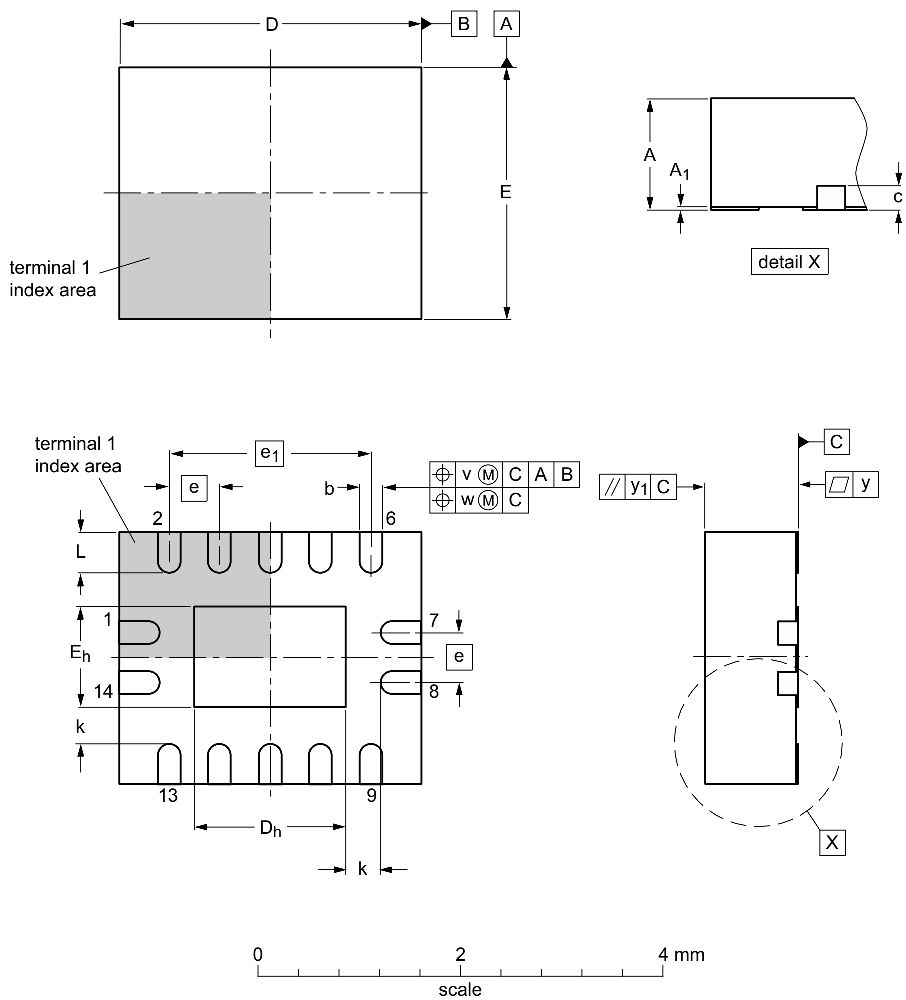
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 15. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

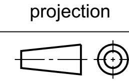
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig 16. Package outline SOT762-1 (DHVQFN14)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCU04A v.8	20151218	Product data sheet	-	74LVCU04A v.7
Modifications:	• Descriptive title updated. Added “unbuffered” (errata).			
74LVCU04A v.7	20111117	Product data sheet	-	74LVCU04A v.6
Modifications:	• Legal pages updated. • Table 6, bodyrow ΔI_{CC}: condition V_{CC} changed.			
74LVCU04A v.6	20110809	Product data sheet	-	74LVCU04A v.5
74LVCU04A v.5	20040312	Product specification	-	74LVCU04A v.4
74LVCU04A v.4	20030901	Product specification	-	74LVCU04A v.3
74LVCU04A v.3	19980729	Product specification	-	74LVCU04A v.2
74LVCU04A v.2	19980729	Product specification	-	74LVCU04A v.1
74LVCU04A v.1	19980729	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

16.2 Definitions

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17. Contact information

For more information, please visit: **http://www.nexperia.com**

For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

18. Contents

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

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