LVDT Signal Conditioner

AD598

FEATURES

Single Chip Solution, Contains Internal Oscillator and Voltage Reference
No Adjustments Required
Insensitive to Transducer Null Voltage
Insensitive to Primary to Secondary Phase Shifts
DC Output Proportional to Position
20 Hz to 20 kHz Frequency Range
Single or Dual Supply Operation
Unipolar or Bipolar Output
Will Operate a Remote LVDT at Up to 300 Feet
Position Output Can Drive Up to 1000 Feet of Cable
Will Also Interface to an RVDT
Outstanding Performance
- **Linearity: 0.05% of FS max**
- **Output Voltage: ±11 V min**
- **Gain Drift: 50 ppm/°C of FS max**
- **Offset Drift: 50 ppm/°C of FS max**

PRODUCT DESCRIPTION

The AD598 is a complete, monolithic Linear Variable Differential Transformer (LVDT) signal conditioning subsystem. It is used in conjunction with LVDTs to convert transducer mechanical position to a unipolar or bipolar dc voltage with a high degree of accuracy and repeatability. All circuit functions are included on the chip. With the addition of a few external passive components to set frequency and gain, the AD598 converts the raw LVDT secondary output to a scaled dc signal. The device can also be used with RVDT transducers.

The AD598 contains a low distortion sine wave oscillator to drive the LVDT primary. The LVDT secondary output consists of two sine waves that drive the AD598 directly. The AD598 operates upon the two signals, dividing their difference by their sum, producing a scaled unipolar or bipolar dc output.

The AD598 uses a unique ratiometric architecture (patent pending) to eliminate several of the disadvantages associated with traditional approaches to LVDT interfacing. The benefits of this new circuit are: no adjustments are necessary, transformer null voltage and primary to secondary phase shift does not affect system accuracy, temperature stability is improved, and transducer interchangeability is improved.

The AD598 is available in two performance grades:

Grade	Temperature Range	Package
AD598JR	0°C to +70°C	20-Pin Small Outline (SOIC)
AD598AD	–40°C to +85°C	20-Pin Ceramic DIP

It is also available processed to MIL-STD-883B, for the military range of –55°C to +125°C.

REV. A

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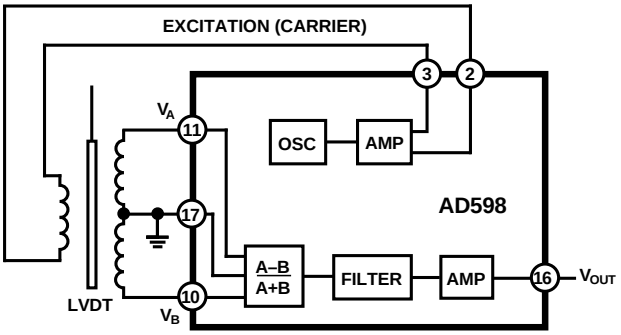
FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD598 offers a monolithic solution to LVDT and RVDT signal conditioning problems; few extra passive components are required to complete the conversion from mechanical position to dc voltage and no adjustments are required.
2. The AD598 can be used with many different types of LVDTs because the circuit accommodates a wide range of input and output voltages and frequencies; the AD598 can drive an LVDT primary with up to 24 V rms and accept secondary input levels as low as 100 mV rms.
3. The 20 Hz to 20 kHz LVDT excitation frequency is determined by a single external capacitor. The AD598 input signal need not be synchronous with the LVDT primary drive. This means that an external primary excitation, such as the 400 Hz power mains in aircraft, can be used.
4. The AD598 uses a ratiometric decoding scheme such that primary to secondary phase shifts and transducer null voltage have absolutely no effect on overall circuit performance.
5. Multiple LVDTs can be driven by a single AD598, either in series or parallel as long as power dissipation limits are not exceeded. The excitation output is thermally protected.
6. The AD598 may be used in telemetry applications or in hostile environments where the interface electronics may be remote from the LVDT. The AD598 can drive an LVDT at the end of 300 feet of cable, since the circuit is not affected by phase shifts or absolute signal magnitudes. The position output can drive as much as 1000 feet of cable.
7. The AD598 may be used as a loop integrator in the design of simple electromechanical servo loops.

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AD598–SPECIFICATIONS (typical @ +25°C and ±15 V dc, C1 = 0.015 μF, R2 = 80 kΩ, R_L = 2 kΩ, unless otherwise noted. See Figure 7.)

Parameter	AD598J Min	AD598J Typ	AD598J Max	AD598A Min	AD598A Typ	AD598A Max	Unit
TRANSFER FUNCTION[1]	$V_{OUT} = \frac{V_A - V_B}{V_A + V_B} \times 500\ \mu A \times R2$						V
OVERALL ERROR[2]							
T_{MIN} to T_{MAX}		0.6	2.35		0.6	1.65	% of FS
SIGNAL OUTPUT CHARACTERISTICS							
Output Voltage Range (T_{MIN} to T_{MAX})	**±11**			**±11**			V
Output Current (T_{MIN} to T_{MAX})	8			6			mA
Short Circuit Current		20			20		mA
Nonlinearity[3] (T_{MIN} to T_{MAX})		75	**±500**		75	**±500**	ppm of FS
Gain Error[4]		0.4	**±1**		0.4	**±1**	% of FS
Gain Drift		20	**±100**		20	**±50**	ppm/°C of FS
Offset[5]		0.3	**±1**		0.3	**±1**	% of FS
Offset Drift		7	**±200**		7	**±50**	ppm/°C of FS
Excitation Voltage Rejection[6]		100			100		ppm/dB
Power Supply Rejection (±12 V to ±18 V)							
PSRR Gain (T_{MIN} to T_{MAX})	**300**	100		**400**	100		ppm/V
PSRR Offset (T_{MIN} to T_{MAX})	**100**	15		**200**	15		ppm/V
Common-Mode Rejection (±3 V)							
CMRR Gain (T_{MIN} to T_{MAX})	**100**	25		**200**	25		ppm/V
CMRR Offset (T_{MIN} to T_{MAX})	**100**	6		**200**	6		ppm/V
Output Ripple[7]		4			4		mV rms
EXCITATION OUTPUT CHARACTERISTICS (@ 2.5 kHz)							
Excitation Voltage Range	2.1		24	2.1		24	V rms
Excitation Voltage							
(R1 = Open)[8]	**1.2**		**2.1**	**1.2**		**2.1**	V rms
(R1 = 12.7 kΩ)[8]	**2.6**		**4.1**	**2.6**		**4.1**	V rms
(R1 = 487 Ω)[8]	**14**		**20**	**14**		**20**	V rms
Excitation Voltage TC[9]		600			600		ppm/°C
Output Current	**30**			**30**			mA rms
T_{MIN} to T_{MAX}	12			12			mA rms
Short Circuit Current		60			60		mA
DC Offset Voltage (Differential, R1 = 12.7 kΩ)							
T_{MIN} to T_{MAX}		30	**±100**		30	**±100**	mV
Frequency	20		20k	20		20k	Hz
Frequency TC, (R1 = 12.7 kΩ)		200			200		ppm/°C
Total Harmonic Distortion		–50			–50		dB
SIGNAL INPUT CHARACTERISTICS							
Signal Voltage	0.1		3.5	0.1		3.5	V rms
Input Impedance		200			200		kΩ
Input Bias Current (AIN and BIN)		1	**5**		1	**5**	μA
Signal Reference Bias Current		2	**10**		2	**10**	μA
Excitation Frequency	0		20	0		20	kHz
POWER SUPPLY REQUIREMENTS							
Operating Range	13		36	13		36	V
Dual Supply Operation (±10 V Output)	±13			±13			V
Single Supply Operation							
0 to +10 V Output	17.5			17.5			V
0 to –10 V Output	17.5			17.5			V
Current (No Load at Signal and Excitation Outputs)		12	**15**		12	**15**	mA
T_{MIN} to T_{MAX}			**16**			**18**	mA
TEMPERATURE RANGE							
JR (SOIC)	0		+70				°C
AD (DIP)				–40		+85	°C
PACKAGE OPTION							
SOIC (R-20)	AD598JR						
Side Brazed DIP (D-20)				AD598AD			

NOTES

[1]V_A and V_B represent the Mean Average Deviation (MAD) of the detected sine waves. Note that for this Transfer Function to linearly represent positive displacement, the sum of V_A and V_B of the LVDT must remain constant with stroke length. See "Theory of Operation." Also see Figures 7 and 12 for R2.

[2]From T_{MIN}, to T_{MAX}, the overall error due to the AD598 alone is determined by combining gain error, gain drift and offset drift. For example the worst case overall error for the AD598AD from T_{MIN} to T_{MAX} is calculated as follows: overall error = gain error at +25°C (±1% full scale) + gain drift from –40°C to +25°C (50 ppm/°C of FS × +65°C) + offset drift from –40°C to +25°C (50 ppm/°C of FS × +65°C) = ±1.65% of full scale. Note that 1000 ppm of full scale equals 0.1% of full scale. Full scale is defined as the voltage difference between the maximum positive and maximum negative output.

[3]Nonlinearity of the AD598 only, in units of ppm of full scale. Nonlinearity is defined as the maximum measured deviation of the AD598 output voltage from a straight line. The straight line is determined by connecting the maximum produced full-scale negative voltage with the maximum produced full-scale positive voltage.

[4]See Transfer Function.

[5]This offset refers to the $(V_A–V_B)/(V_A+V_B)$ input spanning a full-scale range of ±1. [For $(V_A–V_B)/(V_A+V_B)$ to equal +1, V_B must equal zero volts; and correspondingly for $(V_A–V_B)/(V_A+V_B)$ to equal –1, V_A must equal zero volts. Note that offset errors do not allow accurate use of zero magnitude inputs, practical inputs are limited to 100 mV rms.] The ±1 span is a convenient reference point to define offset referred to input. For example, with this input span a value of R2 = 20 kΩ would give V_{OUT} span a value of ±10 volts. Caution, most LVDTs will typically exercise less of the $((V_A–V_B))/((V_A+V_B))$ input span and thus require a larger value of R2 to produce the ±10 V output span. In this case the offset is correspondingly magnified when referred to the output voltage. For example, a Schaevitz E100 LVDT requires 80.2 kΩ for R2 to produce a ±10.69 V output and $(V_A–V_B)/(V_A+V_B)$ equals 0.27. This ratio may be determined from the graph shown in Figure 18, $(V_A–V_B)/(V_A+V_B)$ = (1.71 V rms – 0.99 V rms)/(1.71 V rms + 0.99 V rms). The maximum offset value referred to the ±10.69 V output may be determined by multiplying the maximum value shown in the data sheet (±1% of FS by 1/0.27 which equals ±3.7% maximum. Similarly, to determine the maximum values of offset drift, offset CMRR and offset PSRR when referred to the ±10.69 V output, these data sheet values should also be multiplied by (1/0.27). For this example for the AD598AD the maximum values of offset drift, PSRR offset and CMRR offset would be: 185 ppm/°C of FS; 741 ppm/V and 741 ppm/V respectively when referred to the ±10.69 V output.

[6]For example, if the excitation to the primary changes by 1 dB, the gain of the system will change by typically 100 ppm.

[7]Output ripple is a function of the AD598 bandwidth determined by C2, C3 and C4. See Figures 16 and 17.

[8]R1 is shown in Figures 7 and 12.

[9]Excitation voltage drift is not an important specification because of the ratiometric operation of the AD598.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tested are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

THERMAL CHARACTERISTICS

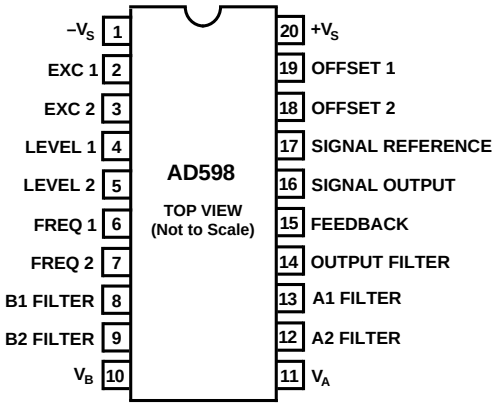
	θ_{JC}	θ_{JA}
SOIC Package	22°C/W	80°C/W
Side Brazed Package	25°C/W	85°C/W

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $–V_S$ . . . . . +36 V
Storage Temperature Range
R Package . . . . . –65°C to +150°C
D Package . . . . . –65°C to +150°C
Operating Temperature Range
AD598JR . . . . . 0°C to +70°C
AD598AD . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
Power Dissipation Up to +65°C . . . . . 1.2 W
Derates Above +65°C . . . . . 12 mW/°C

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD598JR	0°C to +70°C	SOIC	R-20
AD598AD	–40°C to +85C	Ceramic DIP	D-20



AD598–Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted)

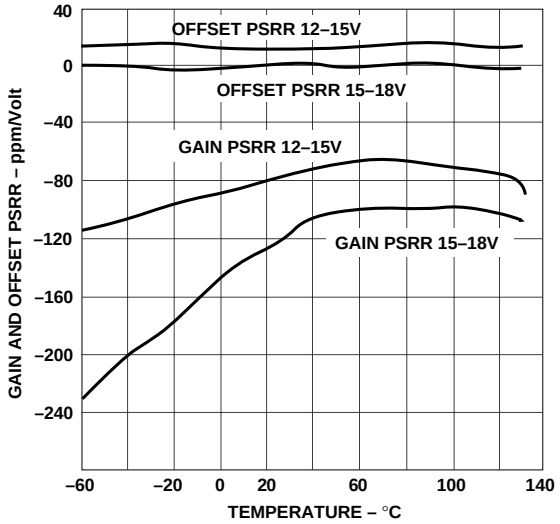


Figure 1. Gain and Offset PSRR vs. Temperature

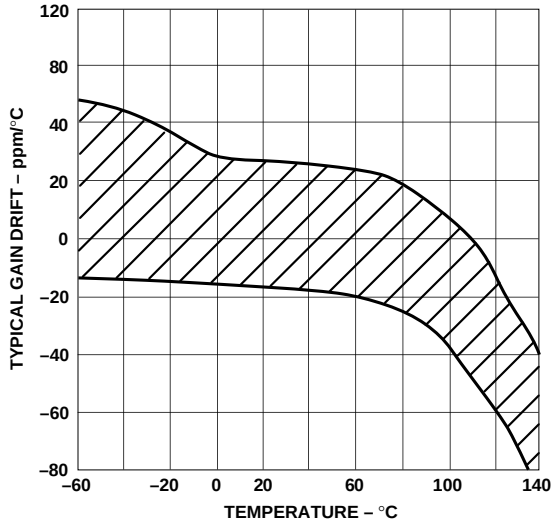


Figure 2. Typical Gain Drift vs. Temperature

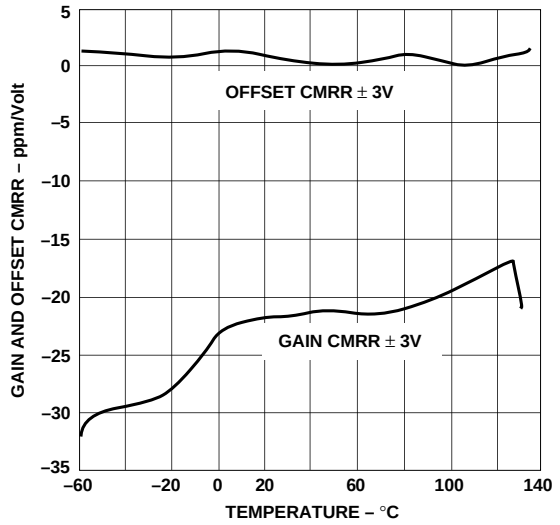


Figure 3. Gain and Offset CMRR vs. Temperature

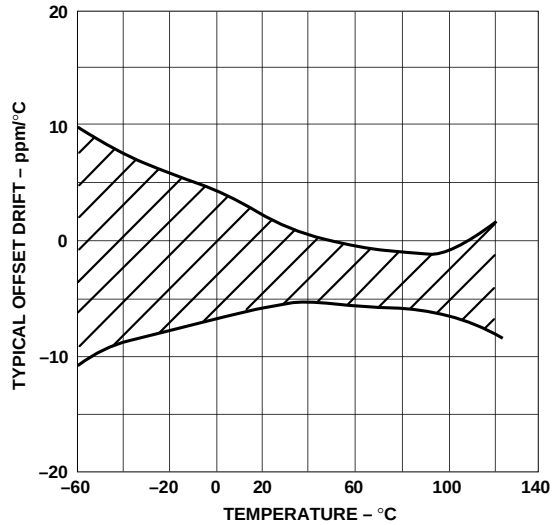


Figure 4. Typical Offset Drift vs. Temperature

THEORY OF OPERATION

A block diagram of the AD598 along with an LVDT (Linear Variable Differential Transformer) connected to its input is shown in Figure 5. The LVDT is an electromechanical transducer whose input is the mechanical displacement of a core and whose output is a pair of ac voltages proportional to core position. The transducer consists of a primary winding energized by an external sine wave reference source, two secondary windings connected in series, and the moveable core to couple flux between the primary and secondary windings.

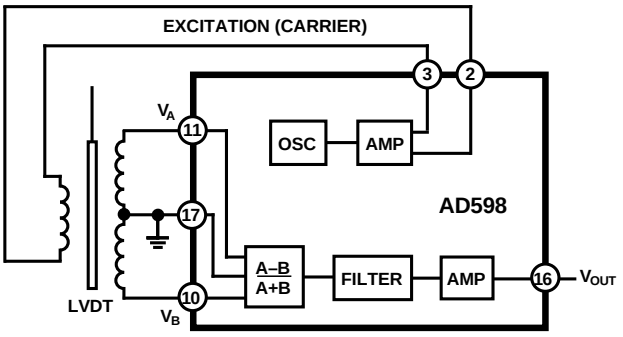


Figure 5. AD598 Functional Block Diagram

The AD598 energizes the LVDT primary, senses the LVDT secondary output voltages and produces a dc output voltage proportional to core position. The AD598 consists of a sine wave oscillator and power amplifier to drive the primary, a decoder which determines the ratio of the difference between the LVDT secondary voltages divided by their sum, a filter and an output amplifier.

The oscillator comprises a multivibrator which produces a triwave output. The triwave drives a sine shaper, which produces a low distortion sine wave whose frequency is determined by a single capacitor. Output frequency can range from 20 Hz to 20 kHz and amplitude from 2 V rms to 24 V rms. Total harmonic distortion is typically –50 dB.

The output from the LVDT secondaries consists of a pair of sine waves whose amplitude difference, (V_A–V_B), is proportional to core position. Previous LVDT conditioners synchronously detect this amplitude difference and convert its absolute value to

a voltage proportional to position. This technique uses the primary excitation voltage as a phase reference to determine the polarity of the output voltage. There are a number of problems associated with this technique such as (1) producing a constant amplitude, constant frequency excitation signal, (2) compensating for LVDT primary to secondary phase shifts, and (3) compensating for these shifts as a function of temperature and frequency.

The AD598 eliminates all of these problems. The AD598 does not require a constant amplitude because it works on the ratio of the difference and sum of the LVDT output signals. A constant frequency signal is not necessary because the inputs are rectified and only the sine wave carrier magnitude is processed. There is no sensitivity to phase shift between the primary excitation and the LVDT outputs because synchronous detection is not employed. The ratiometric principle upon which the AD598 operates requires that the sum of the LVDT secondary voltages remains constant with LVDT stroke length. Although LVDT manufacturers generally do not specify the relationship between V_A+V_B and stroke length, it is recognized that some LVDTs do not meet this requirement. In these cases a nonlinearity will result. However, the majority of available LVDTs do in fact meet these requirements.

The AD598 utilizes a special decoder circuit. Referring to the block diagram and Figure 6 below, an implicit analog computing loop is employed. After rectification, the A and B signals are multiplied by complementary duty cycle signals, d and (I–d) respectively. The difference of these processed signals is integrated and sampled by a comparator. It is the output of this comparator that defines the original duty cycle, d, which is fed back to the multipliers.

As shown in Figure 6, the input to the integrator is [(A+B)d]B. Since the integrator input is forced to 0, the duty cycle d = B/(A+B).

The output comparator which produces d = B/(A+B) also controls an output amplifier driven by a reference current. Duty cycle signals d and (1–d) perform separate modulations on the reference current as shown in Figure 6, which are summed. The summed current, which is the output current, is $I_{REF} \times (1–2d)$.

Since d = B/(A+B), by substitution the output current equals $I_{REF} \times (A–B)/(A+B)$. This output current is then filtered and converted to a voltage since it is forced to flow through the scaling resistor R2 such that:

$$V_{OUT} = I_{REF} \times (A-B)/(A+B) \times R2$$

CONNECTING THE AD598

The AD598 can easily be connected for dual or single supply operation as shown in Figures 7 and 12. The following general design procedures demonstrate how external component values are selected and can be used for any LVDT which meets AD598 input/output criteria.

Parameters which are set with external passive components include: excitation frequency and amplitude, AD598 system bandwidth, and the scale factor (V/inch). Additionally, there are optional features, offset null adjustment, filtering, and signal integration which can be used by adding external components.

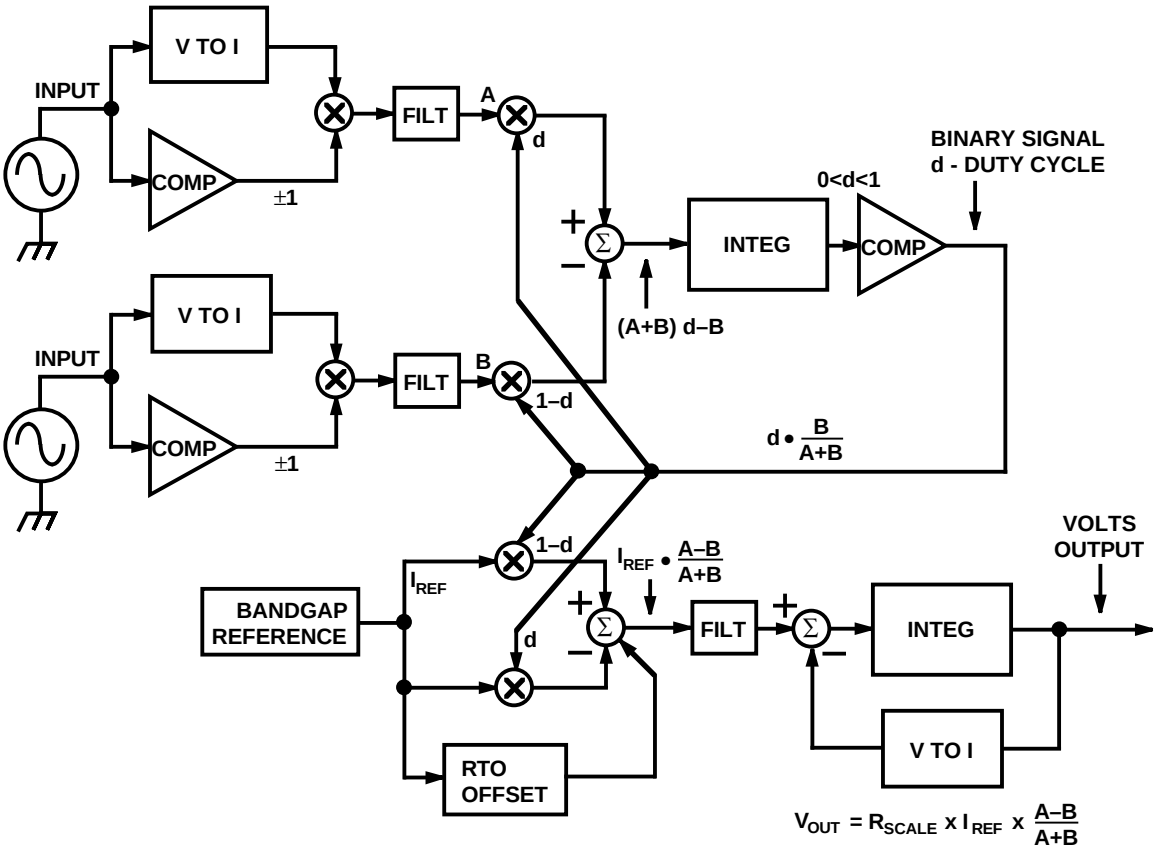


Figure 6. Block Diagram of Decoder

DESIGN PROCEDURE

DUAL SUPPLY OPERATION

Figure 7 shows the connection method with dual ±15 volt power supplies and a Schaevitz E100 LVDT. This design procedure can be used to select component values for other LVDTs as well. The procedure is outlined in Steps 1 through 10 as follows:

1. Determine the mechanical bandwidth required for LVDT position measurement subsystem, $f_{SUBSYSTEM}$. For this example, assume $f_{SUBSYSTEM}$ = 250 Hz.
2. Select minimum LVDT excitation frequency, approximately $10 \times f_{SUBSYSTEM}$. Therefore, let excitation frequency = 2.5 kHz.
3. Select a suitable LVDT that will operate with an excitation frequency of 2.5 kHz. The Schaevitz E100, for instance, will operate over a range of 50 Hz to 10 kHz and is an eligible candidate for this example.
4. Determine the sum of LVDT secondary voltages V_A and V_B. Energize the LVDT at its typical drive level V_{PRI} as shown in the manufacturer's data sheet (3 V rms for the E100). Set the core displacement to its center position where $V_A = V_B$. Measure these values and compute their sum V_A+V_B. For the E100, V_A+V_B = 2.70 V rms. This calculation will be used later in determining AD598 output voltage.
5. Determine optimum LVDT excitation voltage, V_{EXC}. With the LVDT energized at its typical drive level V_{PRI}, set the core displacement to its mechanical full-scale position and measure the output V_{SEC} of whichever secondary produces the largest signal. Compute LVDT voltage transformation ratio, VTR.

$$VTR = V_{PRI}/V_{SEC}$$

For the E100, V_{SEC} = 1.71 V rms for V_{PRI} = 3 V rms. VTR = 1.75.

The AD598 signal input, V_{SEC}, should be in the range of 1 V rms to 3.5 V rms for maximum AD598 linearity and minimum noise susceptibility. Select V_{SEC} = 3 V rms. Therefore, LVDT excitation voltage V_{EXC} should be:

$$V_{EXC} = V_{SEC} \times VTR = 3 \times 1.75 = 5.25\ V\ rms$$

Check the power supply voltages by verifying that the peak values of V_A and V_B are at least 2.5 volts less than the voltages at $+V_S$ and $-V_S$.

6. Referring to Figure 7, for V_S = ±15 V, select the value of the amplitude determining component R1 as shown by the curve in Figure 8.
7. Select excitation frequency determining component C1.

$$C1 = 35\ \mu F\ Hz/f_{EXCITATION}$$

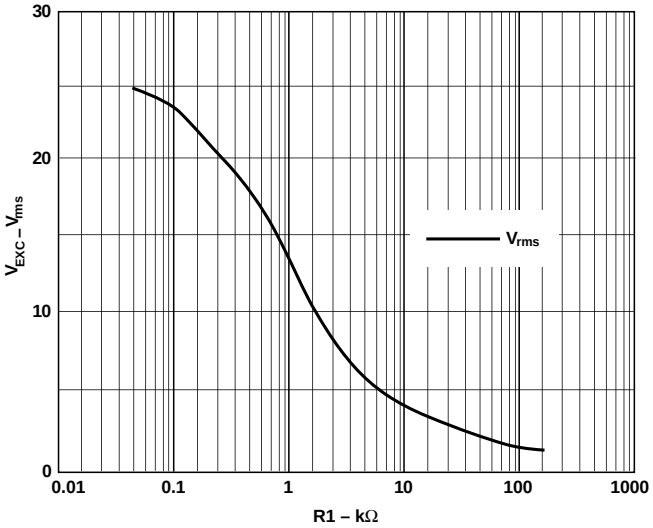


Figure 8. Excitation Voltage V_{EXC} vs. R1

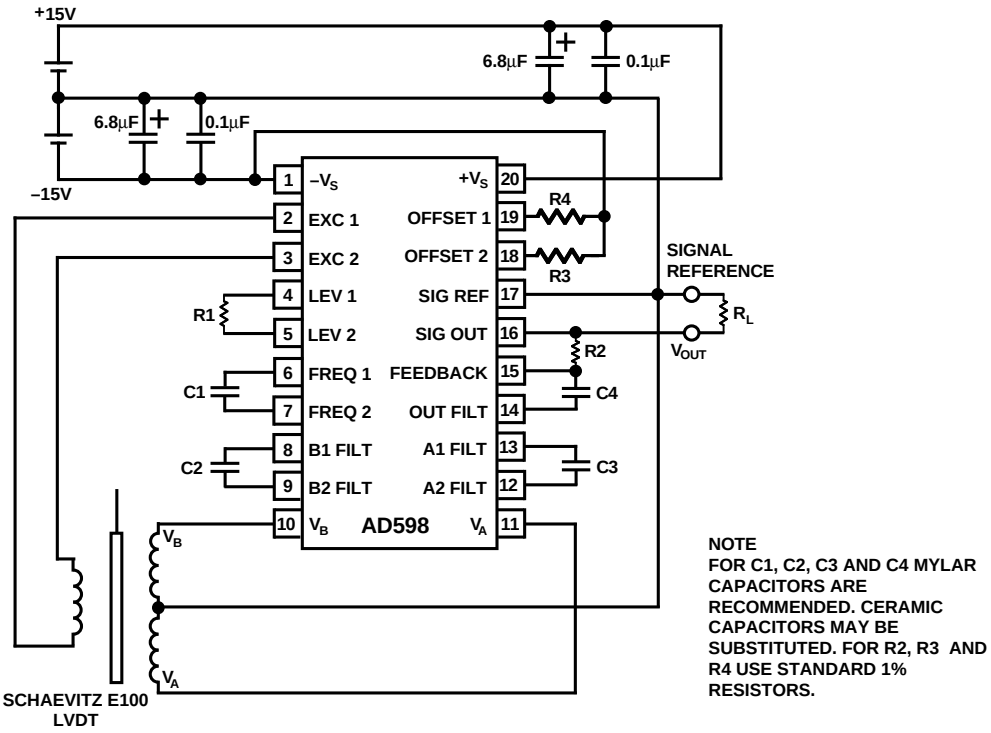


Figure 7. Interconnection Diagram for Dual Supply Operation

8. C2, C3 and C4 are a function of the desired bandwidth of the AD598 position measurement subsystem. They should be nominally equal values.

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/f_{SUBSYSTEM}\ (Hz)$$

If the desired system bandwidth is 250 Hz, then

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/250\ Hz = 0.4\ \mu F$$

See Figures 13, 14 and 15 for more information about AD598 bandwidth and phase characterization.

9. In order to Compute R2, which sets the AD598 gain or full-scale output range, several pieces of information are needed:

a. LVDT sensitivity, S

b. Full-scale core displacement, d

c. Ratio of manufacturer recommended primary drive level, V_{PRI} to (V_A + V_B) computed in Step 4.

LVDT sensitivity is listed in the LVDT manufacturer's catalog and has units of millivolts output per volts input per inch displacement. The E100 has a sensitivity of 2.4 mV/V/mil. In the event that LVDT sensitivity is not given by the manufacturer, it can be computed. See section on Determining LVDT Sensitivity.

For a full-scale displacement of d inches, voltage out of the AD598 is computed as

$$V_{OUT} = S \times \left[\frac{V_{PRI}}{(V_A + V_B)}\right] \times 500\ \mu A \times R2 \times d.$$

V_{OUT} is measured with respect to the signal reference, Pin 17 shown in Figure 7.

Solving for R2,

$$R2 = \frac{V_{OUT} \times (V_A + V_B)}{S \times V_{PRI} \times 500\ \mu A \times d} \qquad (1)$$

Note that V_{PRI} is the same signal level used in Step 4 to determine (V_A + V_B).

For V_{OUT} = 20 V full-scale range (±10 V) and d = 0.2 inch full-scale displacement (±0.1 inch),

$$R2 = \frac{20\,V \times 2.70\,V}{2.4 \times 3 \times 500\ \mu A \times 0.2} = 75.3\ k\Omega$$

V_{OUT} as a function of displacement for the above example is shown in Figure 9.

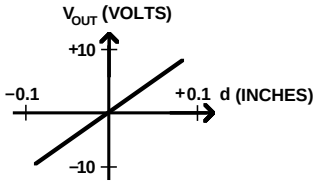


Figure 9. V_{OUT} (±10 V Full Scale) vs. Core Displacement (±0.1 Inch)

10. Selections of R3 and R4 permit a positive or negative output voltage offset adjustment.

$$V_{OS} = 1.2\,V \times R2 \times \left(\frac{1}{R3 + 5\ k\Omega^{\star}} - \frac{1}{R4 + 5\ k\Omega^{\star}}\right) \qquad (2)$$

*These values have a ±20% tolerance.

For no offset adjustment R3 and R4 should be open circuit.

To design a circuit producing a 0 V to +10 V output for a displacement of ±0.1 inch, set V_{OUT} to +10 V, d = 0.2 inch and solve Equation (1) for R2.

$$R2 = 37.6\ k\Omega$$

This will produce a response shown in Figure 10.

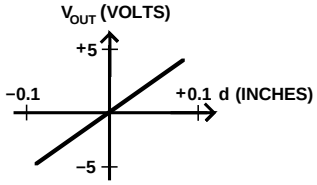


Figure 10. V_{OUT} (±5 V Full Scale) vs. Core Displacement (±0.1 Inch)

In Equation (2) set V_{OS} = 5 V and solve for R3 and R4. Since a positive offset is desired, let R4 be open circuit.

Rearranging Equation (2) and solving for R3

$$R3 = \frac{1.2 \times R2}{V_{OS}} - 5\ k\Omega = 4.02\ k\Omega$$

Figure 11 shows the desired response.

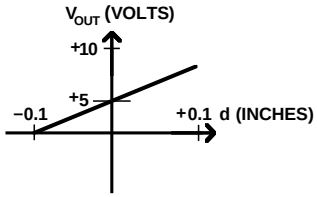


Figure 11. V_{OUT} (0 V–10 V Full Scale) vs. Displacement (±0.1 Inch)

DESIGN PROCEDURE
SINGLE SUPPLY OPERATION

Figure 12 shows the single supply connection method.

For single supply operation, repeat Steps 1 through 10 of the design procedure for dual supply operation, then complete the additional Steps 11 through 14 below. R5, R6 and C5 are additional component values to be determined. V_{OUT} is measured with respect to SIGNAL REFERENCE.

11. Compute a maximum value of R5 and R6 based upon the relationship

$$R5 + R6 \le V_{PS}/100\ \mu A$$

12. The voltage drop across R5 must be greater than

$$2 + 10\ k\Omega^{\star}\left(\frac{1.2\,V}{R4 + 5\ k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2}\right) Volts$$

Therefore

$$R5 \ge \frac{2 + 10\ k\Omega^{\star}\left(\frac{1.2\,V}{R4 + 5\,k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2}\right)}{100\ \mu A}\ Ohms$$

*These values have ±20% tolerance.

Based upon the constraints of R5 + R6 (Step 11) and R5 (Step 12), select an interim value of R6.

13. Load current through R_L returns to the junction of R5 and R6, and flows back to V_{PS}. Under maximum load conditions, make sure the voltage drop across R5 is met as defined in Step 12.

    As a final check on the power supply voltages, verify that the peak values of V_A and V_B are at least 2.5 volts less than the voltages at $+V_S$ and $-V_S$.

14. C5 is a bypass capacitor in the range of 0.1 µF to 1 µF.

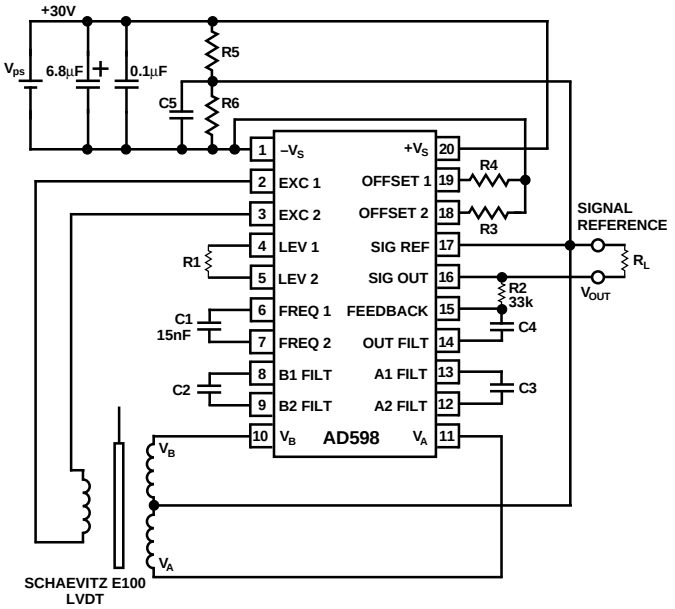


Figure 12. Interconnection Diagram for Single Supply Operation

Gain Phase Characteristics

To use an LVDT in a closed loop mechanical servo application, it is necessary to know the dynamic characteristics of the transducer and interface elements. The transducer itself is very quick to respond once the core is moved. The dynamics arise primarily from the interface electronics. Figures 13, 14 and 15 show the frequency response of the AD598 LVDT Signal Conditioner. Note that Figures 14 and 15 are basically the same; the difference is frequency range covered. Figure 14 shows a wider range of mechanical input frequencies at the expense of accuracy. Figure 15 shows a more limited frequency range with enhanced accuracy. The figures are transfer functions with the input to be considered as a sinusoidally varying mechanical position and the output as the voltage from the AD598; the units of the transfer function are volts per inch. The value of C2, C3 and C4, from Figure 7, are all equal and designated as a parameter in the figures. The response is approximately that of two real poles. However, there is appreciable excess phase at higher frequencies. An additional pole of filtering can be introduced with a shunt capacitor across R2, (see Figure 7); this will also increase phase lag.

When selecting values of C2, C3 and C4 to set the bandwidth of the system, a trade-off is involved. There is ripple on the "dc" position output voltage, and the magnitude is determined by the filter capacitors. Generally, smaller capacitors will give higher system bandwidth and larger ripple. Figures 16 and 17 show the magnitude of ripple as a function of C2, C3 and C4, again all equal in value. Note also a shunt capacitor across R2 shown as a parameter (see Figure 7). The value of R2 used was 81 kΩ with a Schaevitz E100 LVDT.

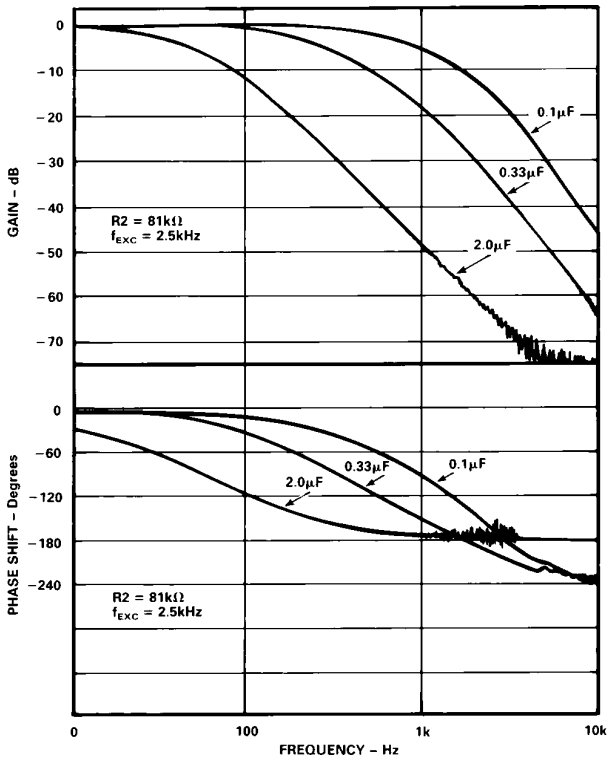


Figure 13. Gain and Phase Characteristics vs. Frequency (0 kHz–10 kHz)

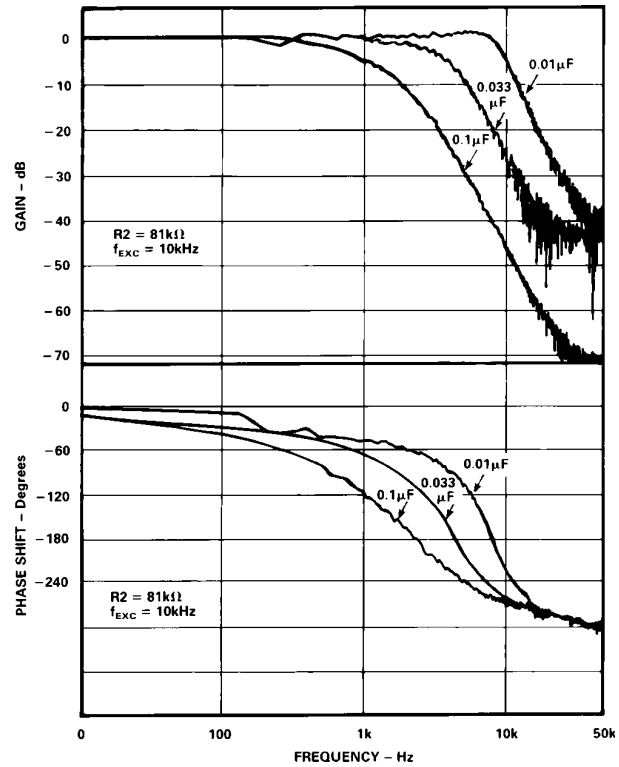


Figure 14. Gain and Phase Characteristics vs. Frequency (0 kHz–50 kHz)

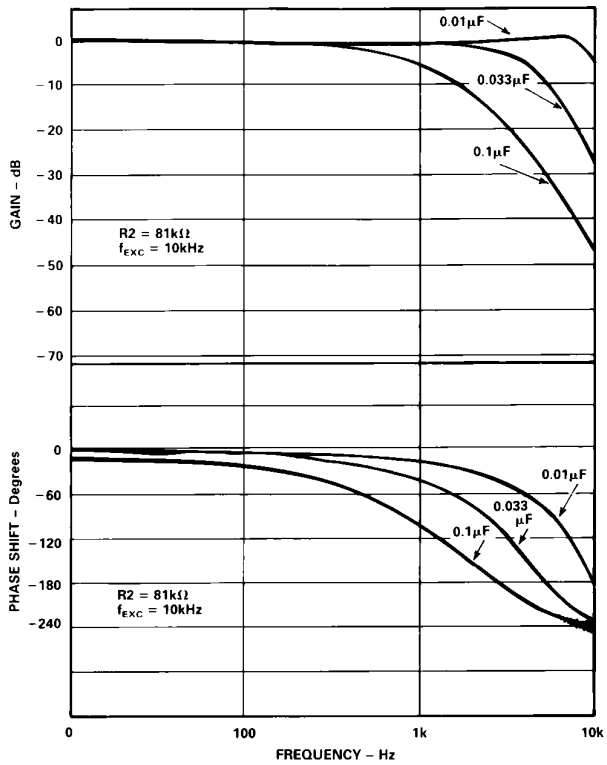


Figure 15. Gain and Phase Characteristics vs. Frequency (0 kHz–10 kHz)

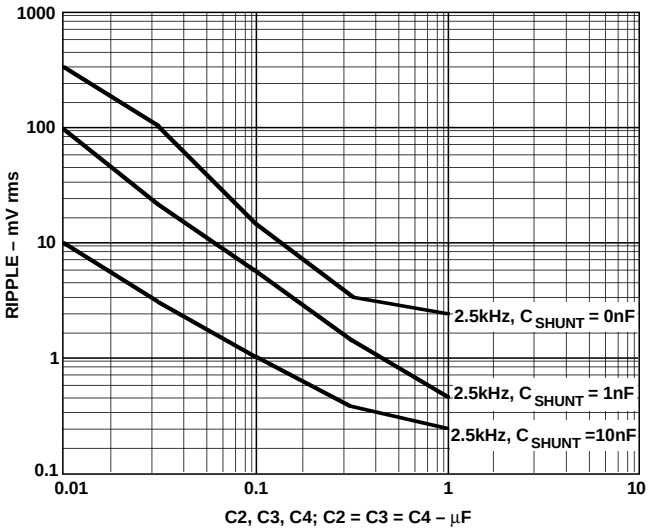


Figure 16. Output Voltage Ripple vs. Filter Capacitance

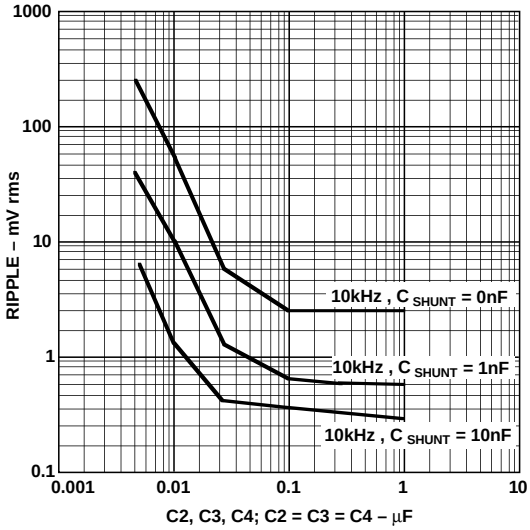


Figure 17. Output Voltage Ripple vs. Filter Capacitance

Determining LVDT Sensitivity

LVDT sensitivity can be determined by measuring the LVDT secondary voltages as a function of primary drive and core position, and performing a simple computation.

Energize the LVDT at its recommended primary drive level, V_{PRI} (3 V rms for the E100). Set the core to midpoint where $V_A = V_B$. Set the core displacement to its mechanical full-scale position and measure secondary voltages V_A and V_B.

$$Sensitivity = \frac{V_A(at\ Full\ Scale) - V_B\ (at\ Full\ Scale)}{V_{PRI} \times d}$$

From Figure 18,

$$Sensitivity = \frac{1.71 - 0.99}{3 \times 100\ mils} = 2.4\ mV/V/mil$$

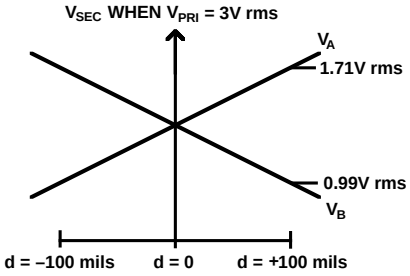


Figure 18. LVDT Secondary Voltage vs. Core Displacement

Thermal Shutdown and Loading Considerations

The AD598 is protected by a thermal overload circuit. If the die temperature reaches 165°C, the sine wave excitation amplitude gradually reduces, thereby lowering the internal power dissipation and temperature.

Due to the ratiometric operation of the decoder circuit, only small errors result from the reduction of the excitation amplitude. Under these conditions the signal-processing section of the AD598 continues to meet its output specifications.

The thermal load depends upon the voltage and current delivered to the load as well as the power supply potentials. An LVDT Primary will present an inductive load to the sine wave excitation. The phase angle between the excitation voltage and current must also be considered, further complicating thermal calculations.

PROVING RING-WEIGH SCALE

Figure 20 shows an elastic member (steel proving ring) combined with an LVDT to provide a means of measuring very small loads. Figure 19 shows the electrical circuit details.

The advantage of using a Proving Ring in combination with an LVDT is that no friction is involved between the core and the coils of the LVDT. This means that weights can be measured without confusion from frictional forces. This is especially important for very low full-scale weight applications.

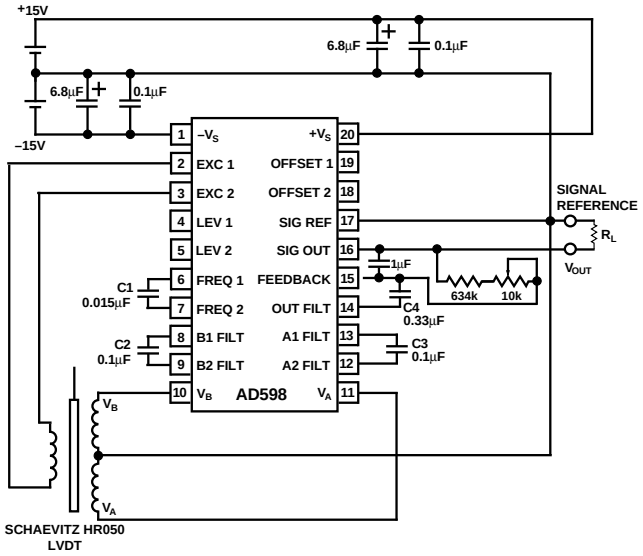


Figure 19. Proving Ring-Weigh Scale Circuit

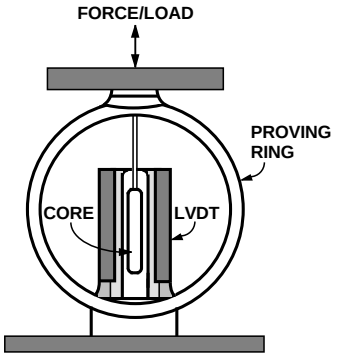


Figure 20. Proving Ring-Weigh Scale Cross Section

Although it is recognized that this type of measurement system may best be applied to weigh very small weights, this circuit was designed to give a full-scale output of 10 V for a 500 lb weight, using a Morehouse Instruments model 5BT Proving Ring. The LVDT is a Schaevitz type HR050 (±50 mil full scale). Although this LVDT provides ±50 mil full scale, the value of R2 was calculated for d = ±30 mil and V_{OUT} equal to 10 V as in Step 9 of the design procedures.

The 1 μF capacitor provides extra filtering, which reduces noise induced by mechanical vibrations. The other circuit values were calculated in the usual manner using the design procedures.

This weigh-scale can be designed to measure tare weight simply by putting in an offset voltage by selecting either R3 or R4 (as shown in Figures 7 and 12). Tare weight is the weight of a container that is deducted from the gross weight to obtain the net weight.

The value of R3 or R4 can be calculated using one of two separate methods. First, a potentiometer may be connected between Pins 18 and 19 of the AD598, with the wiper connected to $-V_{SUPPLY}$. This gives a small offset of either polarity; and the value can be calculated using Step 10 of the design procedures. For a large offset in one direction, replace either R3 or R4 with a potentiometer with its wiper connected to $-V_{SUPPLY}$.

The resolution of this weigh-scale was checked by placing a 100 gram weight on the scale and observing the AD598 output signal deflection on an oscilloscope. The deflection was 4.8 mV.

The smallest signal deflection which could be measured on the oscilloscope was 450 μV which corresponds to a 10 gram weight. This 450 μV signal corresponds to an LVDT displacement of 1.32 microinches which is equivalent to one tenth of the wave length of blue light.

The Proving Ring used in this circuit has a temperature coefficient of 250 ppm/°C due to Young's Modulus of steel. By putting a resistor with a temperature coefficient in place of R2 it is possible to temperature compensate the weigh-scale. Since the steel of the Proving Ring gets softer at higher temperatures, the deflection for a given force is larger, so a resistor with a negative temperature coefficient is required.

SYNCHRONOUS OPERATION OF MULTIPLE LVDTS

In many applications, such as multiple gaging measurement, a large number of LVDTs are used in close physical proximity. If these LVDTs are operated at similar carrier frequencies, stray magnetic coupling could cause beat notes to be generated. The resulting beat notes would interfere with the accuracy of measurements made under these conditions. To avoid this situation all the LVDTs are operated synchronously.

The circuit shown in Figure 21 has one master oscillator and any number of slaves. The master AD598 oscillator has its frequency and amplitude programmed in the usual manner via R1 and C2 using Steps 6 and 7 in the design procedures. The slave AD598s all have Pins 6 and 7 connected together to disable their internal oscillators. Pins 4 and 5 of each slave are connected to Pins 2 and 3 of the master via 15 kΩ resistors, thus setting the amplitudes of the slaves equal to the amplitude of the master. If a different amplitude is required the 15 kΩ resistor values should be changed. Note that the amplitude scales linearly with the resistor value. The 15 kΩ value was selected because it matches the nominal value of resistors internal to the circuit. Tolerances of 20% between the slave amplitudes arise due to differing internal resistors values, but this does not affect the operation of the circuit.

Note that each LVDT primary is driven from its own power amplifier and thus the thermal load is shared between the AD598s. There is virtually no limit on the number of slaves in this circuit, since each slave presents a 30 kΩ load to the master AD598 power amplifier. For a very large number of slaves (say 100 or more) one may need to consider the maximum output current drawn from the master AD598 power amplifier.

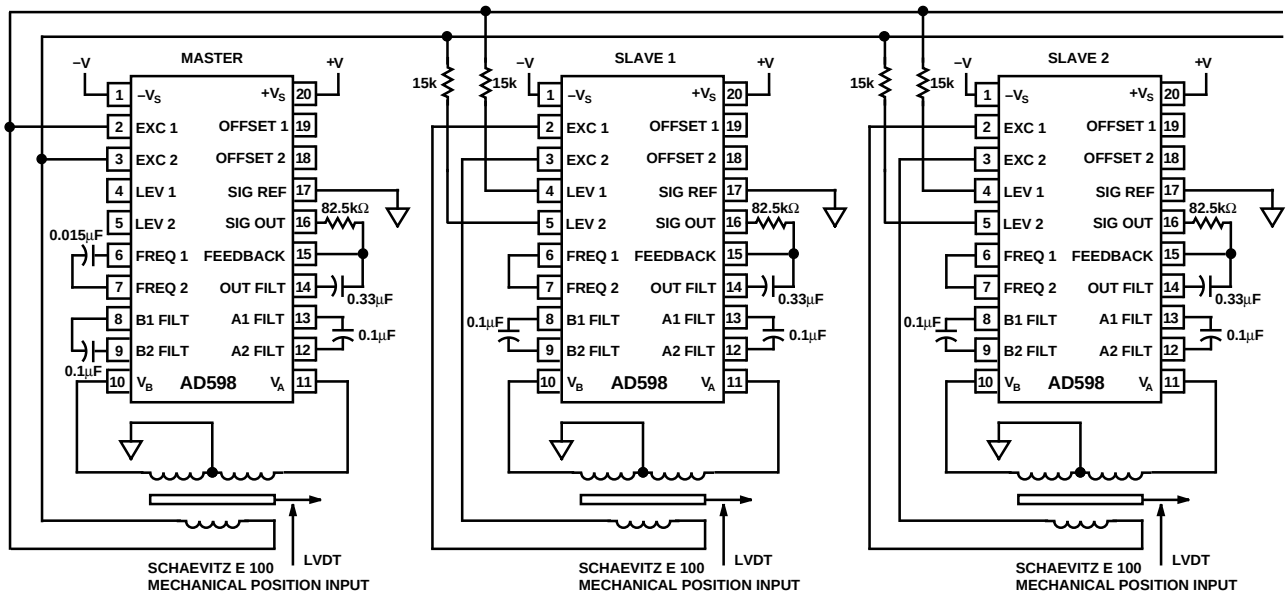


Figure 21. Multiple LVDTs—Synchronous Operation

HIGH RESOLUTION POSITION-TO-FREQUENCY CIRCUIT

In the circuit shown in Figure 22, the AD598 is combined with an AD652 voltage-to-frequency (V/F) converter to produce an effective, simple data converter which can make high resolution measurements.

This circuit transfers the signal from the LVDT to the V/F converter in the form of a current, thus eliminating the errors normally caused by the offset voltage of the V/F converter. The V/F converter offset voltage is normally the largest source of error in such circuits. The analog input signal to the AD652 is converted to digital frequency output pulses which can be counted by simple digital means.

This circuit is particularly useful if there is a large degree of mechanical vibration (hum) on the position to be measured. The hum may be completely rejected by counting the digital frequency pulses over a gate time (fixed period) equal to a multiple of the hum period. For the effects of the hum to be completely rejected, the hum must be a periodic signal.

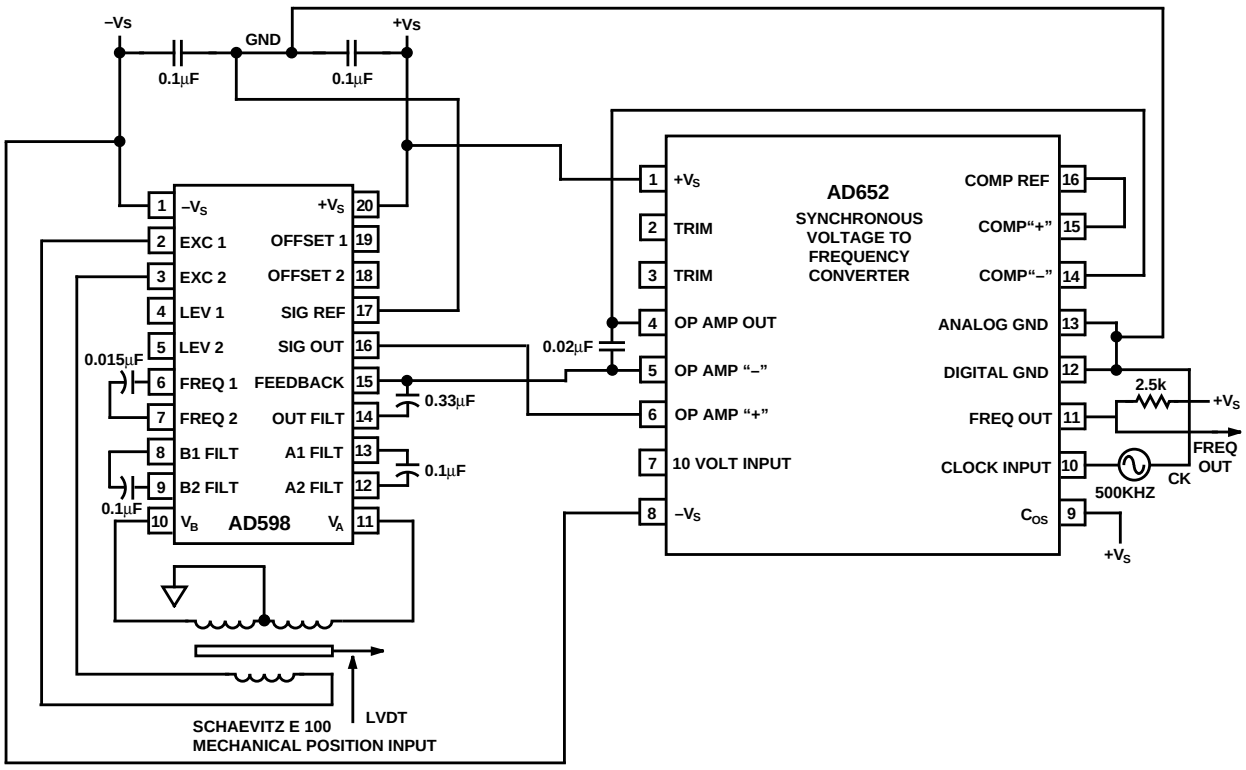


Figure 22. High Resolution Position-to-Frequency Converter

The V/F converter is currently set up for unipolar operation. The AD652 data sheet explains how to set up for bipolar operation. Note that when the LVDT core is centered, the output frequency is zero. When the LVDT core is positioned off center, and to one side, the frequency increases to a full-scale value. To introduce bipolar operation to this circuit, an offset must be introduced at the LVDT as shown in Step 10 of the design procedures.

LOW COST SET-POINT CONTROLLER

A low cost set-point controller can be implemented with the circuit shown in Figure 23. Such a circuit could possibly be used in automobile fuel control systems. The potentiometer, P1, is attached to the gas pedal, and the LVDT is attached to the butterfly valve of the fuel injection system or carburetor. The position of the butterfly valve is electronically controlled by the position of the gas pedal, without mechanical linkage.

This circuit is a simple two IC closed loop servo-controller. It is simple because the LVDT circuit is functioning as the loop integrator. By putting a capacitor in the feedback path (normally occupied by R2), the output signal from the AD598 corresponds to the time integral of the position being measured by the LVDT. The LVDT position signal is summed with the offset signal introduced by the potentiometer, P1. Since this sum is integrated, it must be forced to zero. Thus the LVDT position is forced to follow the value of the input potentiometer, P1. The output signal from the AD598 drives the LM675 power amplifier, which in turn drives the solenoid.

This circuit has dual advantages of being both low cost and high accuracy. The high accuracy results from avoiding the offset errors normally associated with converting the LVDT signal to a voltage and then subsequently integrating that voltage.

MECHANICAL FOLLOWER SERVO-LOOP

Figure 24 shows how two Schaevitz E100 LVDTs may be combined with two AD598s in a mechanical follower servo-loop configuration. One of the LVDTs provides the mechanical input position signal, while the other LVDT mimics the motion.

The signal from the input position circuit is fed to the output as a current so that voltage offset errors are avoided. This current signal is summed with the signal from the output position LVDT; this summed signal is integrated such that the output position is now equal to the input position. This circuit is an efficient means of implementing a mechanical servo-loop since only three ICs are required.

This circuit is similar to the previous circuit (Figure 23) with one exception: the previous circuit uses a potentiometer instead of an LVDT to provide the input position signal. Replacing the potentiometer with an LVDT offers two advantages. First, the increased reliability and robustness of the LVDT can be exploited in applications where the position input sensor is located in a hostile environment. Second, the mechanical motions of the input and output LVDTs are guaranteed to be identical to within the matching of their individual scale factors. These particular advantages make this circuit ideal for application as a hydraulic actuator controller.

DIFFERENTIAL GAGING

LVDTs are commonly used in gaging systems. Two LVDTs can be used to measure the thickness or taper of an object. To measure thickness, the LVDTs are placed on either side of the object to be measured. The LVDTs are positioned such that there is a known maximum distance between them in the fully retracted position.

This circuit is both simple and inexpensive. It has the advantage that two LVDTs may be driven from one AD598, but the disadvantage is that the scale factor of each LVDT may not match exactly. This causes the workpiece thickness measurement to vary depending upon its absolute position in the differential gage head.

This circuit was designed to produce a ±10 V signal output swing, composed of the sum of the two independent ±5 V swings from each LVDT. The output voltage swing is set with an 80.9 kΩ resistor. The output voltage V_{OUT} for this circuit is given by:

$$V_{OUT} = \left[\frac{(V_A - V_B)}{(V_A + V_B)} + \frac{(V_C - V_D)}{(V_C + V_D)}\right] \times 500\ \mu A \times R2.$$

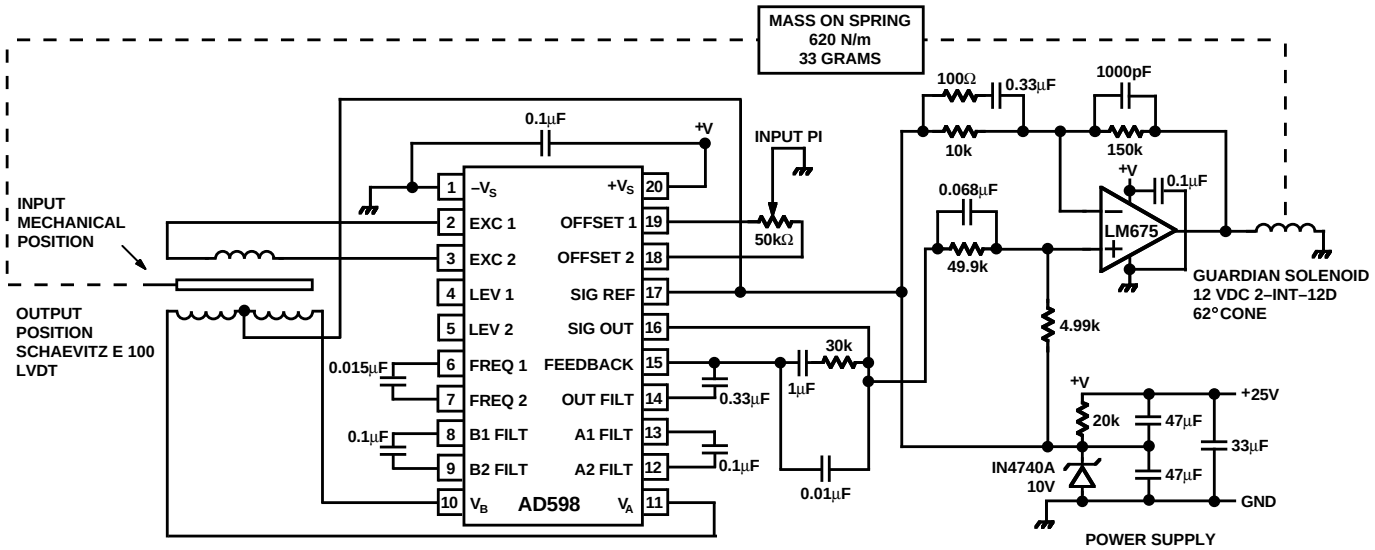


Figure 23. Low Cost Set-Point Controller

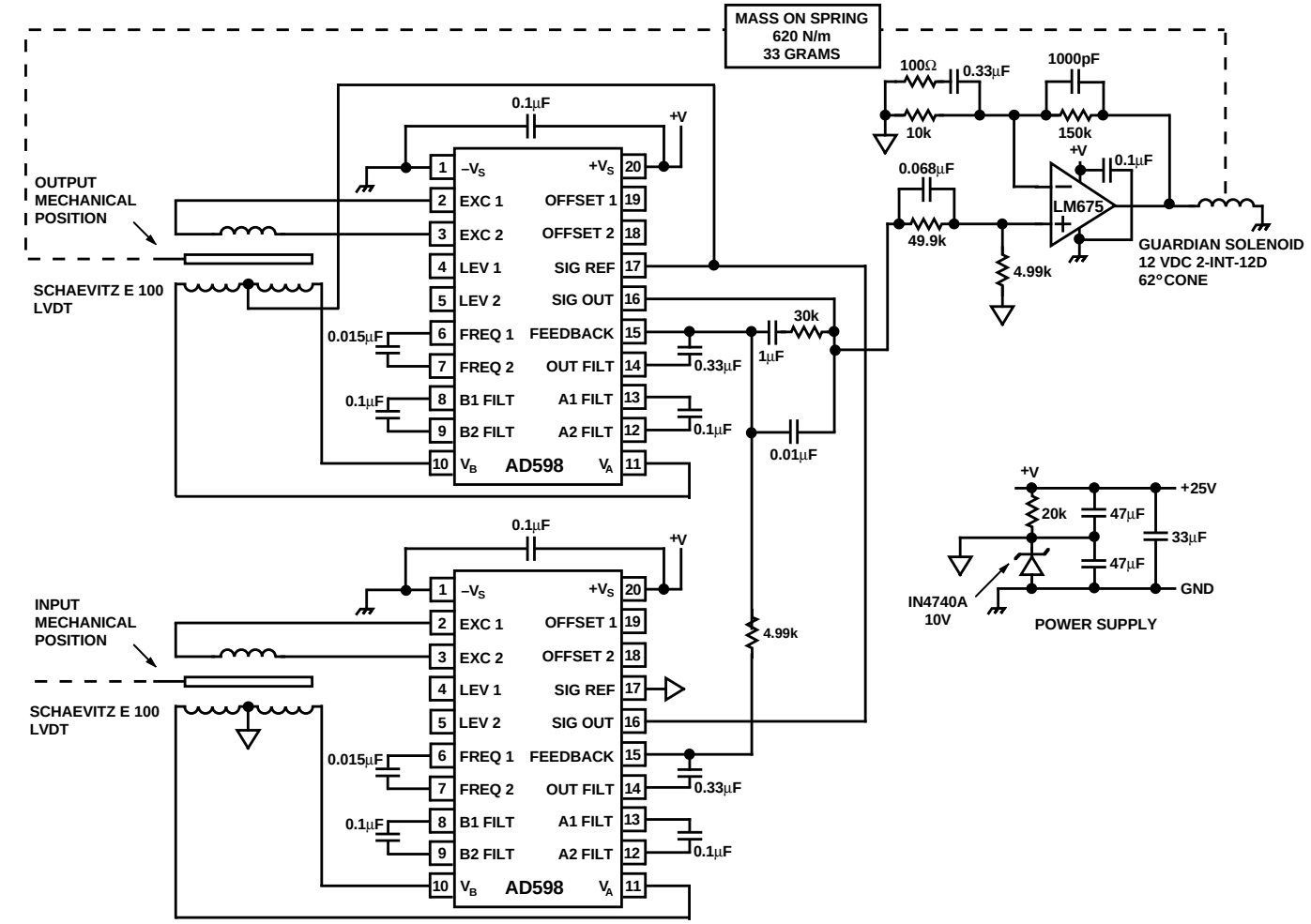


Figure 24. Mechanical Follower Servo-Loop

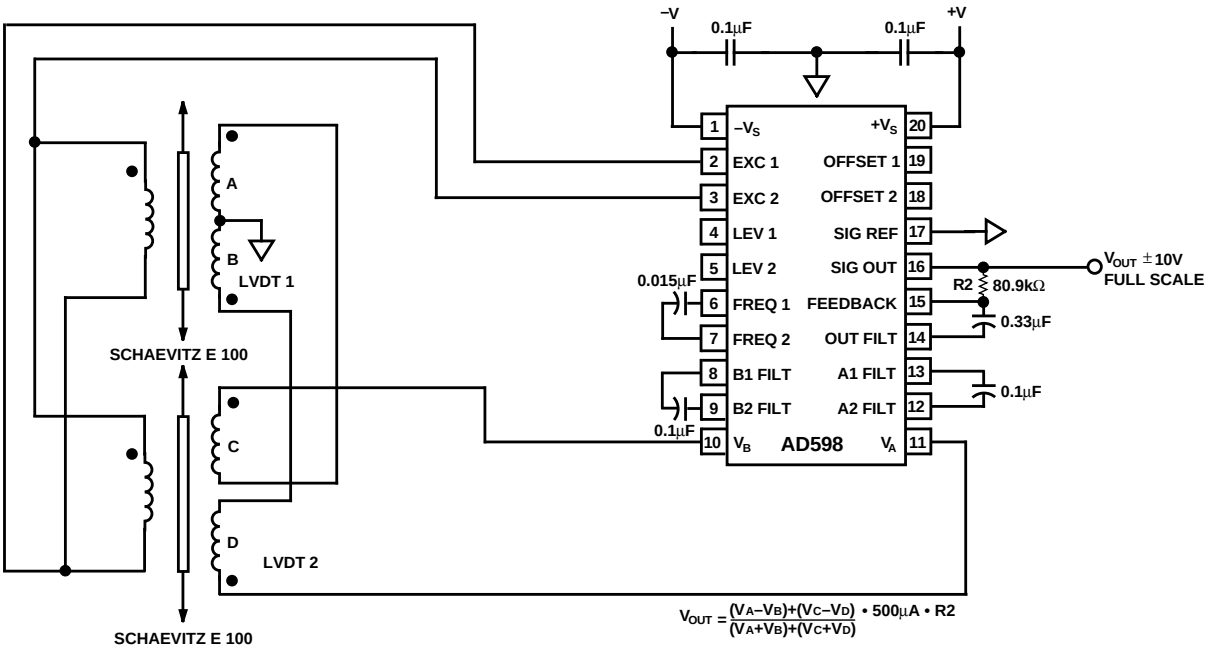


Figure 25. Differential Gaging

PRECISION DIFFERENTIAL GAGING

The circuit shown in Figure 26 is functionally similar to the differential gaging circuit shown in Figure 25. In contrast to Figure 25, it provides a means of independently adjusting the scale factor of each LVDT so that both scale factors may be matched.

The two LVDTs are driven in a master-slave arrangement where the output signal from the slave LVDT is summed with the output signal from the master LVDT. The scale factor of the slave LVDT only is adjusted with R1 and R2. The summed scale factor of the master LVDT and the slave LVDT is adjusted with R3.

R1 and R2 are chosen to be 80.9 kΩ resistors to give a ±10 V full-scale output signal for a single Schaevitz E100 LVDT. R3 is chosen to be 40.2 kΩ to give a ±10 V output signal when the two E100 LVDT output signals are summed. The output voltage for this circuit is given by:

$$V_{OUT} = \left[\frac{(V_A - V_B)}{(V_A + V_B)} + \frac{(V_C - V_D)}{(V_C + V_D)} \times \frac{R2}{R1}\right] \times 500\ \mu A \times R3.$$

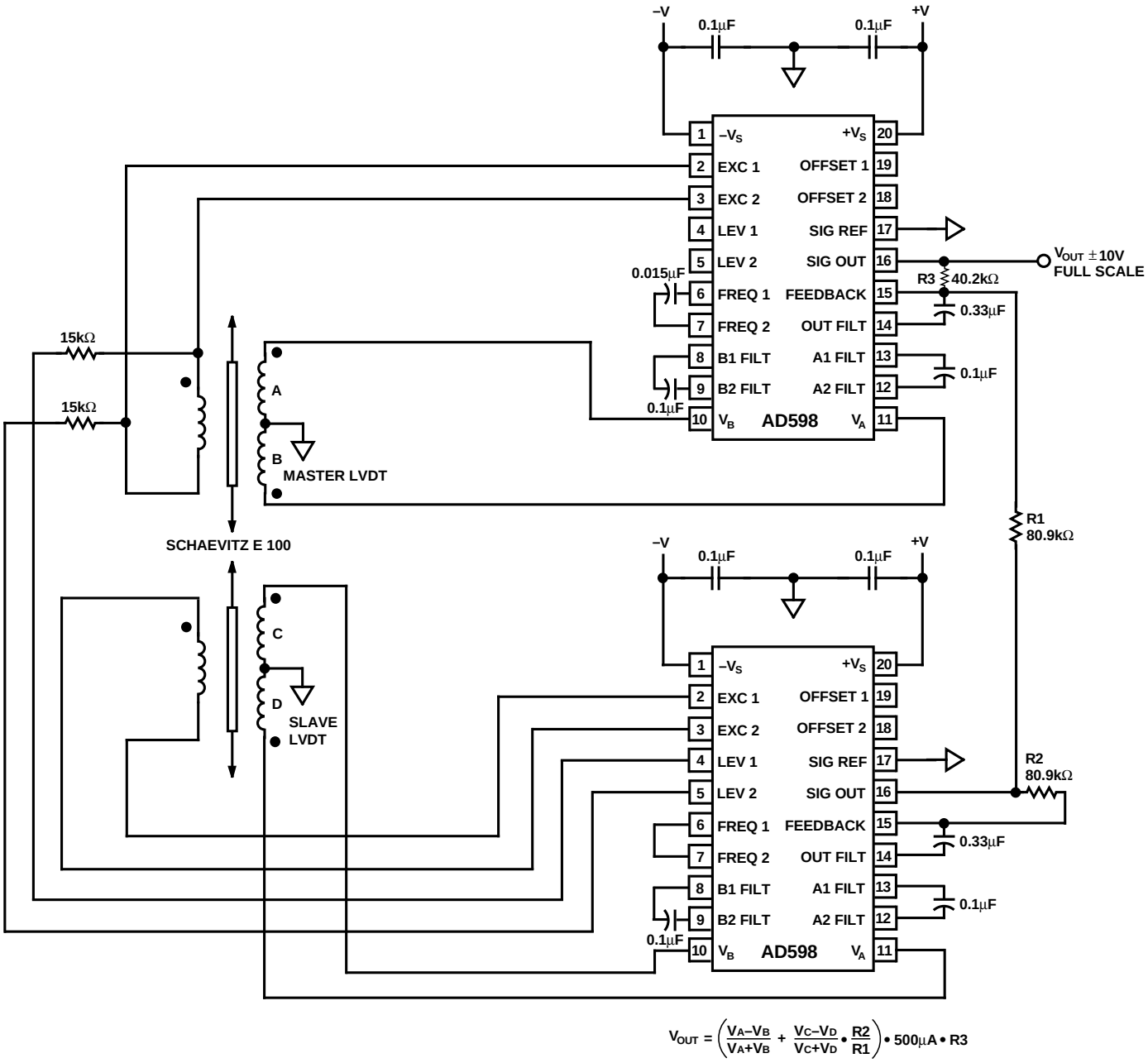


Figure 26. Precision Differential Gaging

OPERATION WITH A HALF-BRIDGE TRANSDUCER

Although the AD598 is not intended for use with a half-bridge type transducer, it may be made to function with degraded performance.

A half-bridge type transducer is a popular transducer. It works in a similar manner to the LVDT in that two coils are wound around a moveable core and the inductance of each coil is a function of core position.

In the circuit shown in Figure 27 the V_A and V_B input voltages are developed as two resistive-inductor dividers. If the inductors are equal (i.e., the core is centered), the V_A and V_B input voltages to the AD598 are equal and the output voltage V_{OUT} is zero. When the core is positioned off center, the inductors are unequal and an output voltage V_{OUT} is developed.

The linearity of this circuit is dependent upon the value of the resistors in the resistive-inductor dividers. The optimum value may be transducer dependent and therefore must be selected by trial and error. The 300 Ω resistors in this circuit optimize the nonlinearity of the transfer function to within several tenths of 1%. This circuit uses a Sangamo AGH1 half-bridge transducer. The 1 μF capacitor blocks the dc offset of the excitation output signal. The 4 nF capacitor sets the transducer excitation frequency to 10 kHz as recommended by the manufacturer.

ALTERNATE HALF-BRIDGE TRANSDUCER CIRCUIT

This circuit suffers from similar accuracy problems to those mentioned in the previous circuit description. In this circuit the V_A input signal to the AD598 really and truly is a linear function of core position, and the input signal V_B, is one half of the excitation voltage level. However, a nonlinearity is introduced by the A–B/A+B transfer function.

The 500 Ω resistors in this circuit are chosen to minimize errors caused by dc bias currents from the V_A and V_B inputs. Note that in the previous circuit these bias currents see very low resistance paths to ground through the coils.

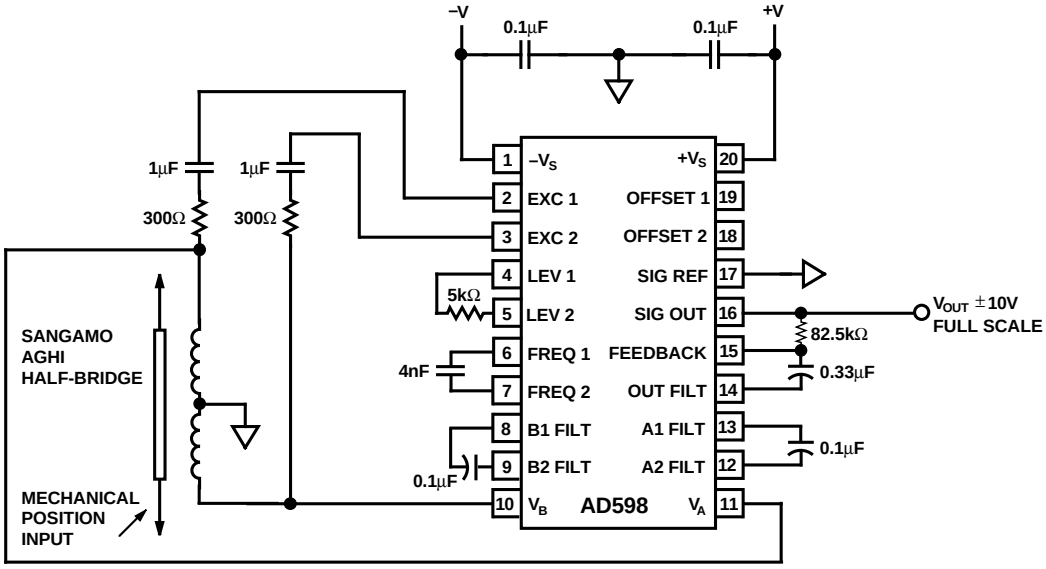


Figure 27. Half-Bridge Operation

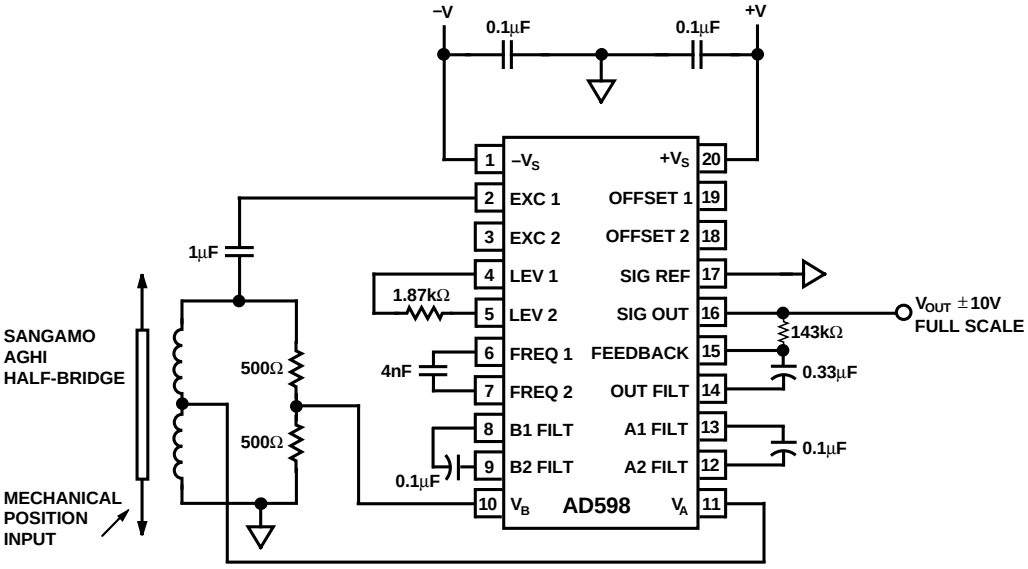
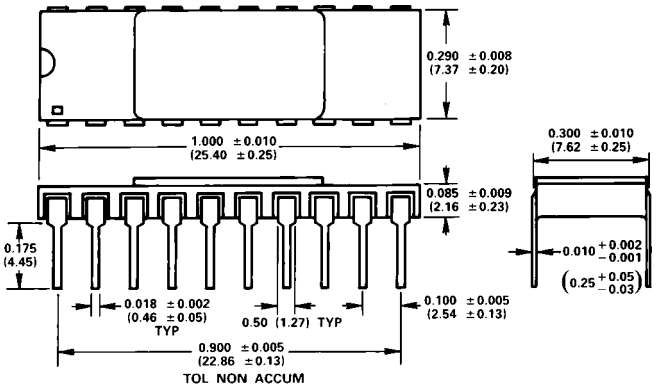


Figure 28. Alternate Half-Bridge Circuit

OUTLINE DIMENSIONS

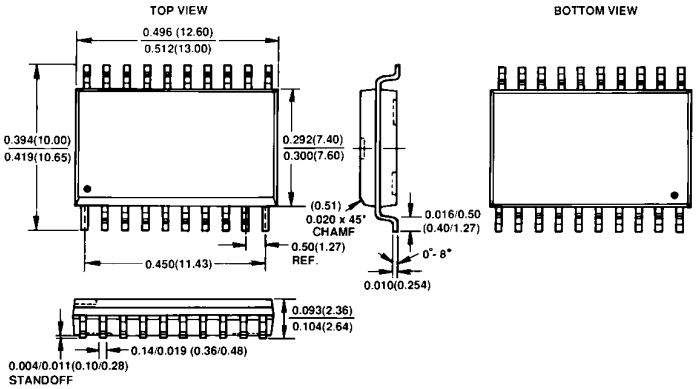
Dimensions shown in inches and (mm).

20-Pin Sized Brazed Ceramic DIP



NOTES:
1. LEAD NUMBER 1 IDENTIFIED BY DOT OR NOTCH.
2. LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

20-Lead Wide Body Plastic SOIC (R) Package



NOTES
1. DIMENSIONS SHOWN IN INCHES AND (MM).
2. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATIONS MS-013-AA.
3. DIMENSIONS SHOWN AS (-- / --) ARE MIN. / MAX.

C1330–10–10/89

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- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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