

**DATA SHEET**

# SE5003L1-R: High-Power (+19 dBm) 802.11ac WLAN Power Amplifier with Integrated Power Detector

## Applications

- IEEE802.11ac WLAN enabled:
  - Access points
  - Media gateways
  - Set-top boxes
  - LCD TVs
- Other broadband triple-play multimedia applications

## Features

- Linear output power of +19 dBm for IEEE 802.11ac 256-QAM, EVM < 1.8% @ 5.0 V
- High gain of 32 dB @ 5.0 V
- 3.3 to 5 V operation
- Power shutdown mode
- Superior gain flatness
- Fully matched at RF input/output ports
- Load insensitive power detector
- Small footprint QFN (20-pin, 4 x 4 mm) SMT package (MSL3, 260 °C per JEDEC J-STD-020)

**NEW**



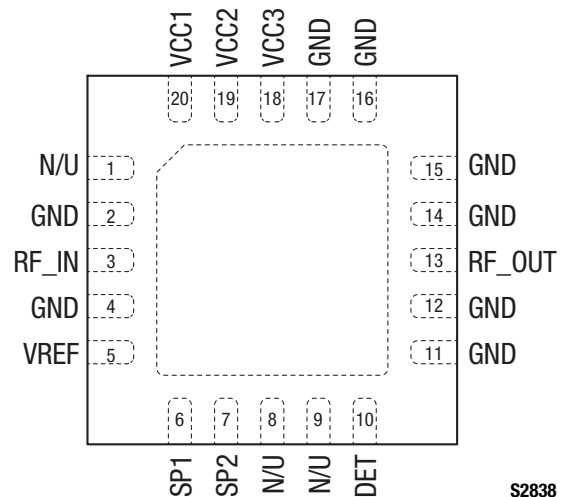
Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

## Description

Skyworks SE5003L1-R is a 5-GHz Microwave Monolithic Integrated Circuit (MMIC) Power Amplifier (PA) with superior output power, linearity, and efficiency. These features make the SE5003L1-R ideal for Wireless Local Area Network (WLAN IEEE 802.11ac) applications.

The device is fabricated using Indium Gallium Phosphide (InGaP) Heterojunction Bipolar Transistor (HBT) technology. The device is internally matched and mounted in a 20-pin, 4 x 4 mm Quad Flat No-Lead (QFN) Surface-Mounted Technology (SMT) package, which allows for a highly manufacturable low-cost solution.

The device package and pinout for the 20-pin QFN are shown in Figure 1. A block diagram of the SE5003L1-R is shown in Figure 2.



**Figure 1. SE5003L1-R Pinout – 20-Pin QFN (Top View)**

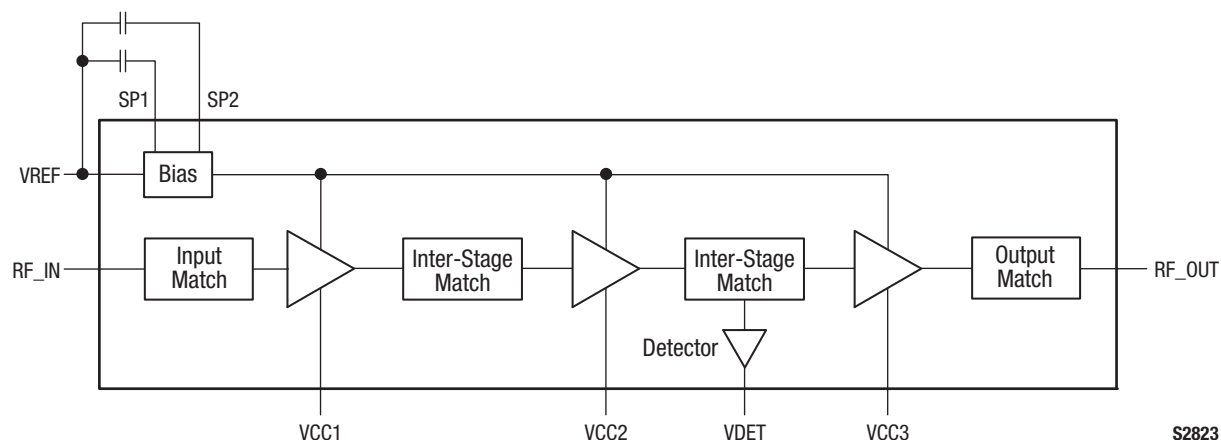


Figure 2. SE5003L1-R Block Diagram

## Technical Description

The SE5003L1-R PA contains all of the needed RF matching and DC biasing circuits. The device also provides an output power detector voltage.

The SE5003L1-R is a three-stage, HBT InGaP device optimized for high linearity and power efficiency. These features make the device suitable for wideband digital applications, where PA linearity and power consumption are of critical importance (e.g., WiFi systems or WLANs).

The device has been characterized with the highest specified data rates for IEEE802.11ac (256 QAM). Under these stringent test conditions, the device exhibits excellent spectral purity and power efficiency.

## Electrical and Mechanical Specifications

Signal pin assignments and functional pin descriptions are described in Table 1. The absolute maximum ratings of the SE5003L1-R are provided in Table 2. Recommended operating conditions are specified in Table 3. Electrical specifications are provided in Tables 4 through 8.

Typical performance characteristics of the SE5003L1-R are illustrated in Figures 3 through 8.

Table 1. SE5003L1-R Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	N/U	Not used; open circuit.	11	GND	Ground
2	GND	Ground	12	GND	Ground
3	RF_IN	RF input	13	RF_OUT	Power amplifier RF output
4	GND	Ground	14	GND	Ground
5	VREF	Reference voltage	15	GND	Ground
6	SP1	Port for optional capacitor to improve dynamic EVM	16	GND	Ground
7	SP2	Port for optional capacitor to improve dynamic EVM	17	GND	Ground
8	N/U	Not used; open circuit.	18	VCC3	Third stage supply voltage
9	N/U	Not used; open circuit.	19	VCC2	Second stage supply voltage
10	DET	Analog power detector output	20	VCC1	First stage supply voltage

**Table 2. SE5003L1-R Absolute Maximum Ratings (Note 1)**

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	VCC1, VCC2	−0.3	VCC3	V
	VCC3	−0.3	+6.0	V
Reference voltage	VREF	−0.3	+3.6	V
RF input power	P <sub>IN</sub>		+6	dBm
Operating temperature	T <sub>OP</sub>	−40	+85	°C
Storage temperature	T <sub>ST</sub>	−40	+150	°C
Junction temperature	T <sub>J</sub>		+160	°C
Thermal resistance	Θ <sub>JC</sub>		43	°C/W
Electrostatic Discharge Human Body Model (HBM), Class 1A	ESD		250	V

**Note 1:** Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

**CAUTION:** Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

**Table 3. SE5003L1-R Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	VCC1, VCC2	3.0	VCC3	VCC3	V
	VCC3	3.0	5.0	5.5	V
Reference voltage	VREF	2.8		2.9	V
Case operating temperature	T <sub>OP</sub>	−40	+25	+85	°C

**Table 4. SE5003L1-R Electrical Specifications: DC Characteristics (Note 1)**

(VCC1 = VCC2 = VCC3 = 5.0 V, VREF = 2.85 V, T<sub>OP</sub> = +25 °C as Measured on the Evaluation Board, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply current	I <sub>CC</sub>	P <sub>OUT</sub> = +19 dBm, 5.0 V		205	240	mA
		P <sub>OUT</sub> = +23 dBm, 54 Mbps, 5.0 V		300	340	mA
		P <sub>OUT</sub> = +19 dBm, 3.3 V		200	230	mA
		P <sub>OUT</sub> = +21 dBm, 3.3 V		230	265	mA
		VREF = 0 V, No RF		0.5	10	μA
Quiescent Current	I <sub>Q</sub>	No RF		120		mA
Reference voltage enabled	VREF_H		2.80	2.85	2.90	V
Reference voltage disabled	VREF_L		0		0.5	V
Reference voltage current	IREF	VREF voltage set to 2.85 V		10		mA

**Note 1:** Performance is guaranteed only under the conditions listed in this Table.

**Table 5. SE5003L1-R Electrical Specifications: General, 5.0 V Operation (Note 1)**  
(VCC1 = VCC2 = VCC3 = 5.0 V, VREF = 2.85 V, TOP = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f		5.15		5.90	GHz
Output power	POUT	802.11ac, MCS9, 1.8% DEVM, HT80	+17	+18		dBm
		802.11ac, MCS9, 1.8% DEVM, HT40	+18	+19		dBm
		802.11n, MCS7, 3% DEVM, HT40	+22	+23		dBm
		802.11n, MCS0, HT40, mask compliant	+24			dBm
1 dB output compression point	OP1dB	PIN = CW	+28	+32		dBm
Small signal gain	IS21I		28	32	35	dB
Input return loss	IS11I				-11	dB
Gain variation over band	$\Delta S_{21}$			$\pm 1.5$		dB
2 <sup>nd</sup> and 3 <sup>rd</sup> harmonics	2fo, 3fo	POUT = +23 dBm		-45		dBm/MHz
Rise and fall time	tr, tf			0.5		$\mu$ s
Stability		POUT = +23 dBm, Vcc = 5 V, 54 Mbps, 64 QAM, VSWR = 6:1, all phases	All non-harmonically related outputs < -50 dBc/100 kHz			
Ruggedness		PIN = -10 dBm, CW, VSWR = 6:1, all phases	No damage			

**Note 1:** Performance is guaranteed only under the conditions listed in this Table.**Table 6. SE5003L1-R Electrical Specifications: General, 3.3 V Operation (1 of 2) (Note 1)**  
(VCC1 = VCC2 = VCC3 = 3.3 V, VREF = 2.85 V, TOP = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f		5.15		5.90	GHz
Output power	POUT	802.11ac, MCS9, 1.8% DEVM, HT80	+17	+18		dBm
		802.11ac, MCS9, 1.8% DEVM, HT40	+18	+19		dBm
		802.11n, MCS7, 3% DEVM, HT40	+20	+21		dBm
		802.11n, MCS0, HT40, mask compliant	+22			dBm
1 dB output compression point	OP1dB	PIN = CW	+24	+28		dBm
Small signal gain	IS21I		27	31	34	dB
Input return loss	IS11I				-11	dB
Gain variation over band	$\Delta S_{21}$			$\pm 1.5$		dB
2 <sup>nd</sup> and 3 <sup>rd</sup> harmonics	2fo, 3fo	POUT = +23 dBm		-45	-42	dBm/MHz
Rise and fall time	tr, tf			0.5		$\mu$ s

**Table 6. SE5003L1-R Electrical Specifications: General, 3.3 V Operation (2 of 2) (Note 1)**  
**(VCC1 = VCC2 = VCC3 = 3.3 V, VREF = 2.85 V, TOP = +25 °C, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Stability		POUT = +23 dBm, VCC = 5 V, 54 Mbps, 64 QAM, VSWR = 6:1, all phases	All non-harmonically related outputs < -50 dBc/100 kHz			
Ruggedness		PIN = -10 dBm, CW, VSWR = 6:1, all phases	No damage			

**Note 1:** Performance is guaranteed only under the conditions listed in this Table.

**Table 7. SE5003L1-R Electrical Specifications: Power Detector Characteristics for 5.0 V Operation (Note 1)**  
**(VCC = 5.0 V, VREF = 2.85 V, TOP = +25 °C, f = 5.4 GHz, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Output power detector range	PDR		0		OP1dB	dBm
Detector voltage	VDET	POUT = +23 dBm		1.00		V
		POUT = No RF		0.35		V
Detector accuracy	ERRDET	$\Delta P_{OUT}$ @ constant VDET:				
		5.15 GHz to 5.70 GHz	-0.5		+0.5	dB
		5.70 GHz to 5.85 GHz	-0.5		+0.5	dB
		VSWR = 3:1 -1.5 to +1.5 dB	-1.5		+1.5	dB
Output impedance	PDZOUT			700		$\Omega$
DC load impedance	PDZLOAD			26.5		k $\Omega$

**Note 1:** Performance is guaranteed only under the conditions listed in this Table.

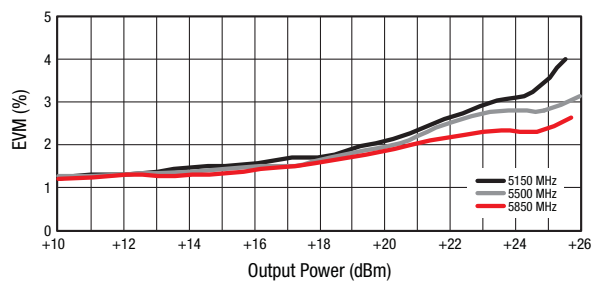
**Table 8. SE5003L1-R Electrical Specifications: Power Detector Characteristics for 3.3 V Operation (Note 1)**  
**(VCC = 3.3 V, VREF = 2.85 V, TOP = +25 °C, f = 5.4 GHz, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Output power detector range	PDR		0		OP1dB	dBm
Detector voltage	VDET	POUT = +22 dBm		0.85		V
		POUT = No RF		0.35		V
Detector accuracy	ERRDET	$\Delta P_{OUT}$ @ constant VDET:				
		5.15 GHz to 5.70 GHz	-0.5		+0.5	dB
		5.70 GHz to 5.85 GHz	-0.5		+0.5	dB
		VSWR = 3:1 -1.5 to +1.5 dB	-1.5		+1.5	dB
Output impedance	PDZOUT			700		$\Omega$
DC load impedance	PDZLOAD			26.5		k $\Omega$

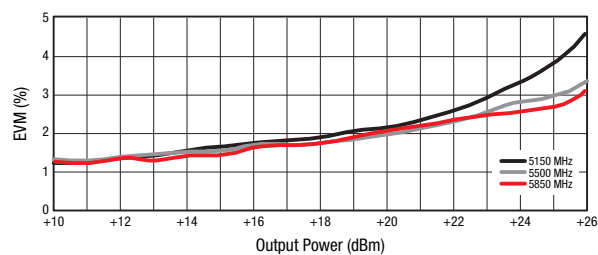
**Note 1:** Performance is guaranteed only under the conditions listed in this Table.

## Typical Performance Characteristics

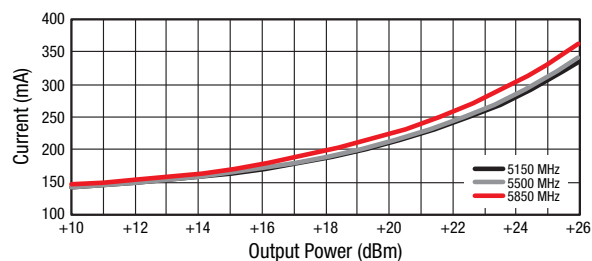
(VCC1 = VCC2 = VCC3 = 5.0 V, T<sub>OP</sub> = +25 °C, Unless Otherwise Noted)



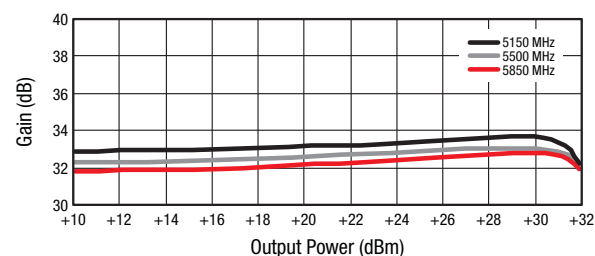
**Figure 3. EVM vs Output Power  
(802.11ac, MCS9, HT80)**



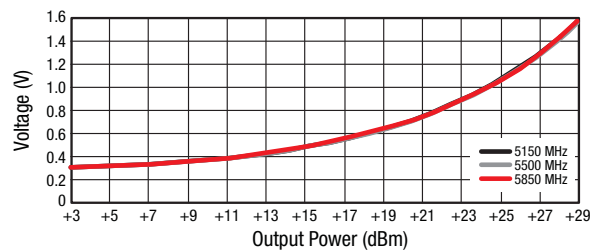
**Figure 4. EVM vs Output Power  
(802.11ac, MCS9, HT40)**



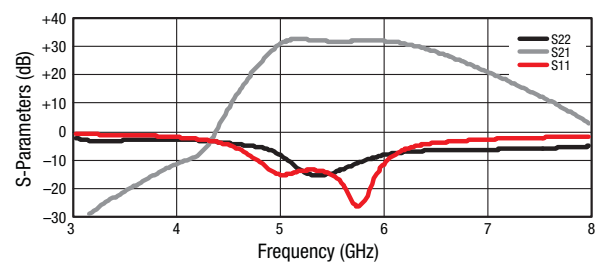
**Figure 5. Operating Current vs Output Power  
(OFDM, 256 QAM, HT40, 100% Duty Cycle)**



**Figure 6. Gain vs Output Power**



**Figure 7. Detector Voltage vs Output Power**



**Figure 8. Small Signal Parameters vs Frequency**

## Evaluation Board Description

The SE5003L1-R Evaluation Board is used to test the performance of the SE5003L1-R WLAN PA. A schematic diagram of the SE5003L1-R Evaluation Board is shown in Figure 9. A photograph of the Evaluation Board is shown in Figure 10. Component values for the SE5003L1-R Evaluation Board are listed in Table 9.

## Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SE5003L1-R has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required. For further information, refer to the Skyworks Application Note *PCB Design Guidelines for High Power Dissipation Packages*, document number 201211.
- Bypass capacitors should be used on the DC supply lines. Refer to the schematic drawing in Figure 9 for further details.
- The RF lines should be well separated from each other with solid ground in between traces to maximize input-to-output isolation.

**NOTE:** A poor connection between the slug and ground increases junction temperature ( $T_J$ ), which reduces the lifetime of the device.

## Evaluation Board Setup Procedure

Step 1: Connect system ground to pin 1 of connector J3.

Step 2: Apply 5.0 V to pins 4, 6, and 8 of connector J3.

Step 3: By applying 2.85 V on VREF (pin 2 of the J3 header), the PA is enabled. By placing a ground on VREF, the PA is disabled and placed in a shutdown state, drawing minimal current.

Step 4: The 5 GHz amplifier performance can be monitored by applying an RF signal to connector J2 (RF\_IN). Monitor the output power on the RF\_OUT port connector, J1.

Step 5: Detector performance can be monitored on pin 10 of connector J3.

Care should be taken not to overdrive the amplifier by applying too much RF on the device input. A suitable starting input power setting would be -20 dBm.

## Package Dimensions

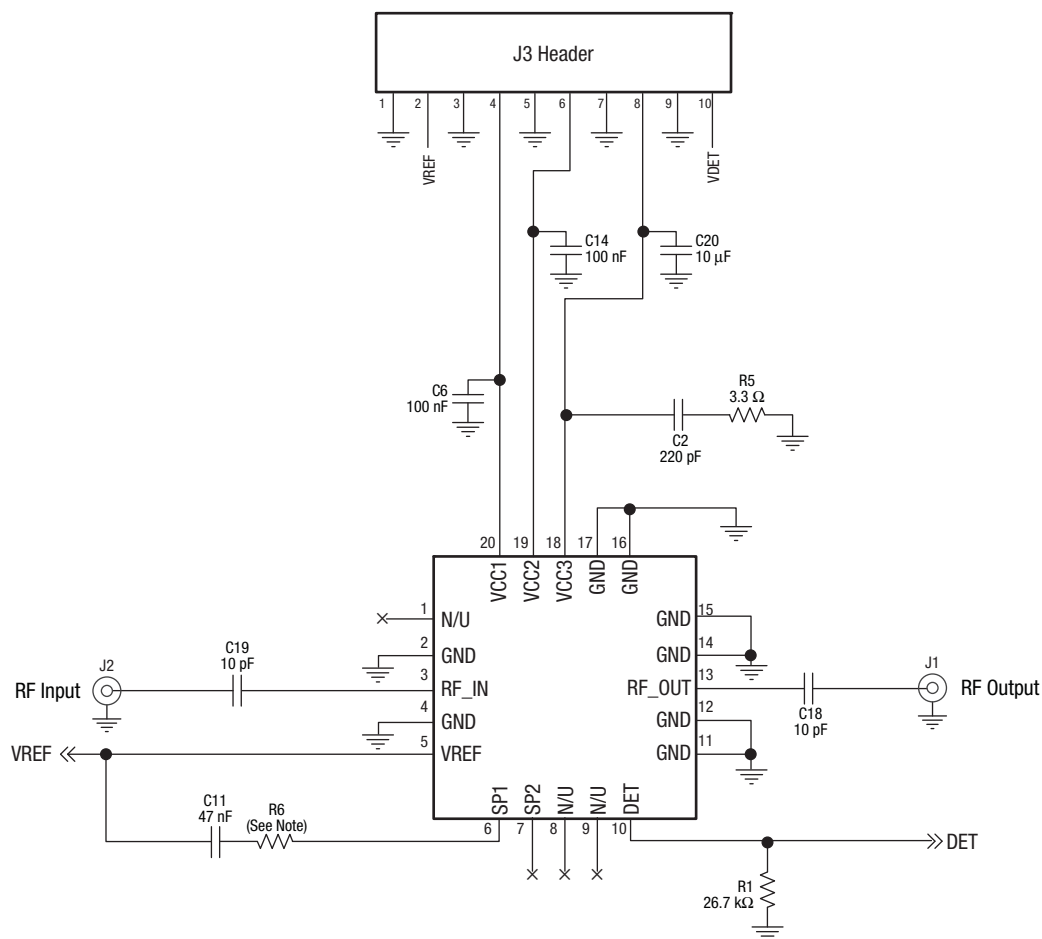
Typical case markings for the SE5003L1-R are shown in Figure 11. The PCB layout footprint for the SE5003L1-R is provided in Figure 12. Package dimensions for the 20-pin QFN are shown in Figure 13, and tape and reel dimensions are provided in Figure 14.

## Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SE5003L1-R is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



*Note: Some component labels may be different than the corresponding component symbol shown here. Component values, however, are accurate as of the date of this Data Sheet.*

*Component R6 = 2.2 kΩ for 3.3 V operation, 510 Ω for 5.0 V operation.*

Y0013

**Figure 9. SE5003L1-R Evaluation Board Schematic**



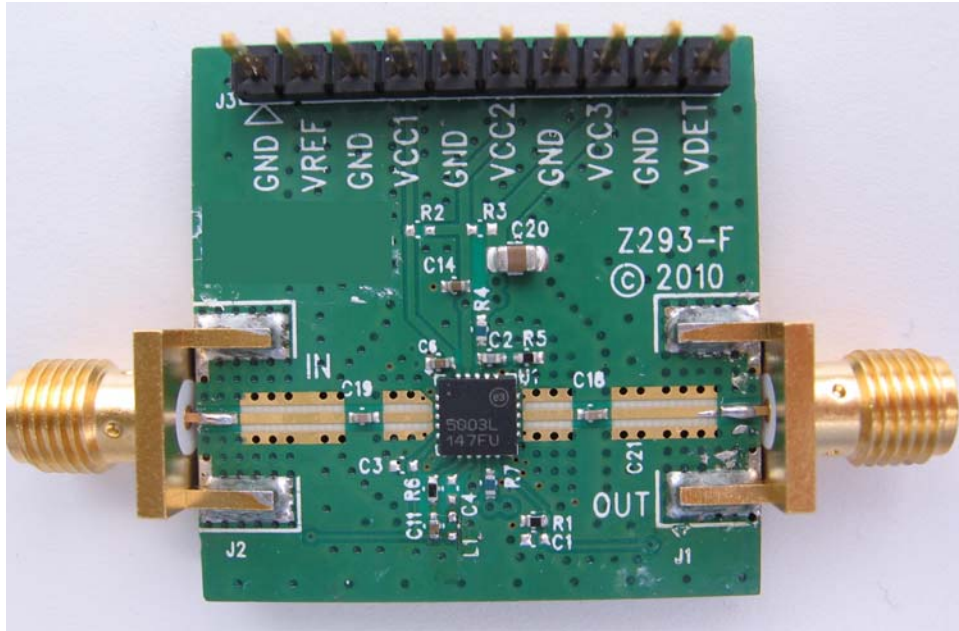


Figure 10. SE5003L1-R Evaluation Board

Table 9. SE5003L1-R Evaluation Board Bill of Materials

Component	Size	Value	Vendor	Part #	Comments
C2	0402	220 pF	Murata	GRM1555C1H221JA01	Multilayer ceramic
C6, C14	0402	100 nF	Murata	GRM155R61A104KA01	Multilayer ceramic
C11	0402	47 nF	Murata	GRM155R71E473KA88	Multilayer ceramic
C18, C19	0402	10 pF	Murata	GRM1555C1H100JZ01	Multilayer ceramic
C20	0805	10 $\mu$ F	Murata	GRM21BR61A106KE19	Ceramic
J1, J2	End launch	SMA	Johnson Components	142-0701-851	SMA end launch straight jack receptacle, tab contact
J3	100 mil	10X1	Samtec	TSW-110-07-G-S	100 mil header
R1	0402	26/7 k $\Omega$	Panasonic	ERJ2RKF2672	Thick film chip resistor
R5	0402	3.3 $\Omega$	Panasonic	ERJ2GEJ3R3	Thick film chip resistor
R6	0402 0402	2.2 k $\Omega$ (3.3 V operation) 510 $\Omega$ (5 V operation)	Panasonic Panasonic	ERJ3GEJ222 ERJ2GEJ621	Thick film chip resistor Thick film chip resistor

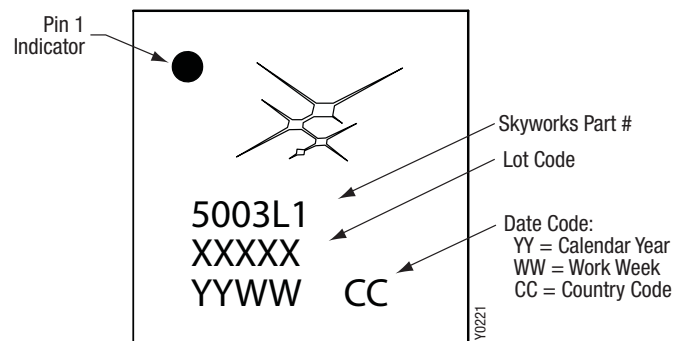
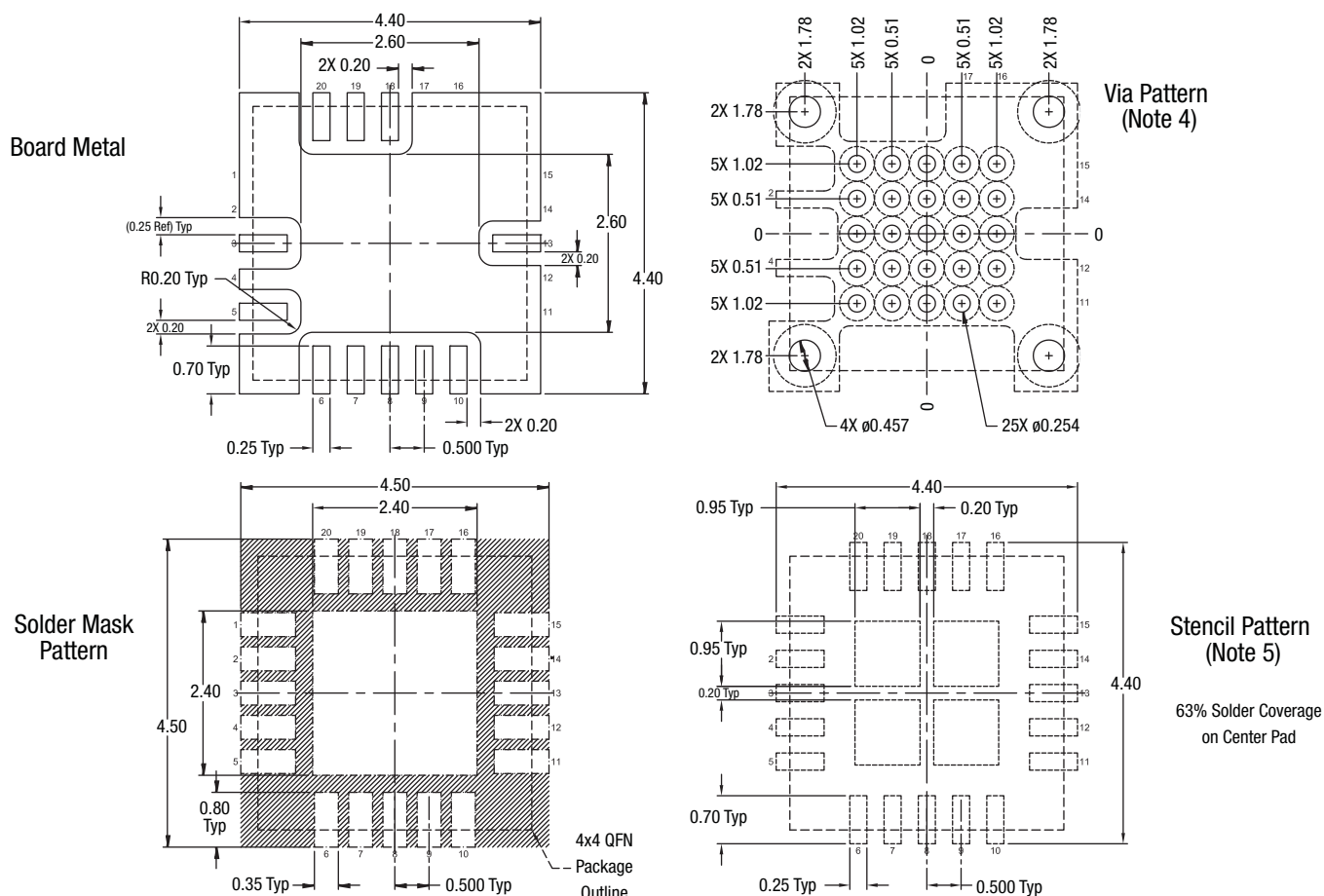


Figure 11. Typical Case Markings (Top View)



**NOTES:**

1. All measurements are in millimeters.
2. Dimensioning and tolerancing according to ASME Y14.5M-1994.
3. Unless specified, dimensions are symmetrical about center lines.
4. Via hole recommendations: 0.025 mm Cu via wall plating (minimum), via holes to be filled with conductive paste and plated over.
5. Stencil recommendations: 0.125 mm stencil thickness, laser cut apertures trapezoidal walls, and rounded corners offer better paste release.

Y0222

**Figure 12. PCB Layout Footprint for the SE5003L1-R**

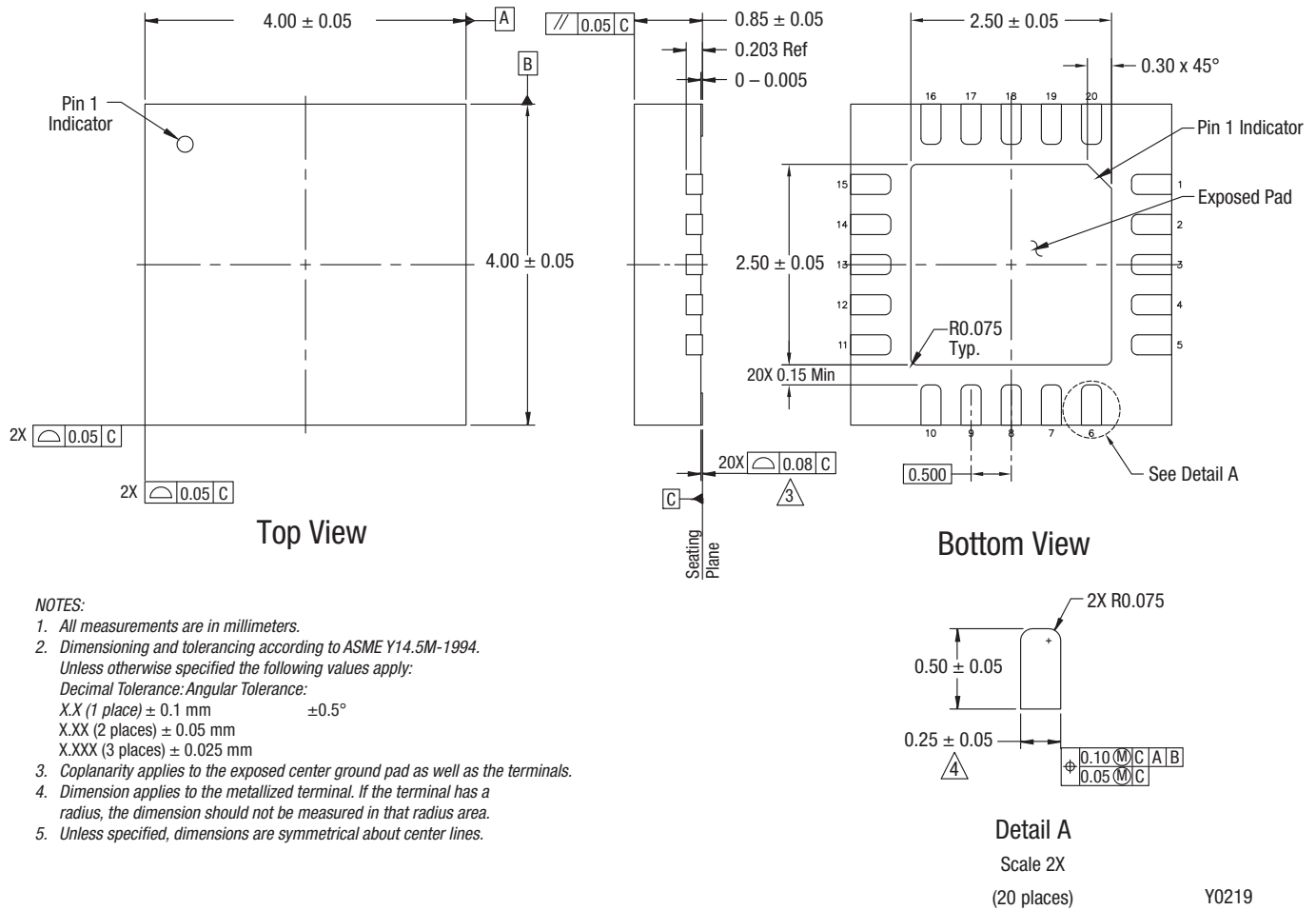
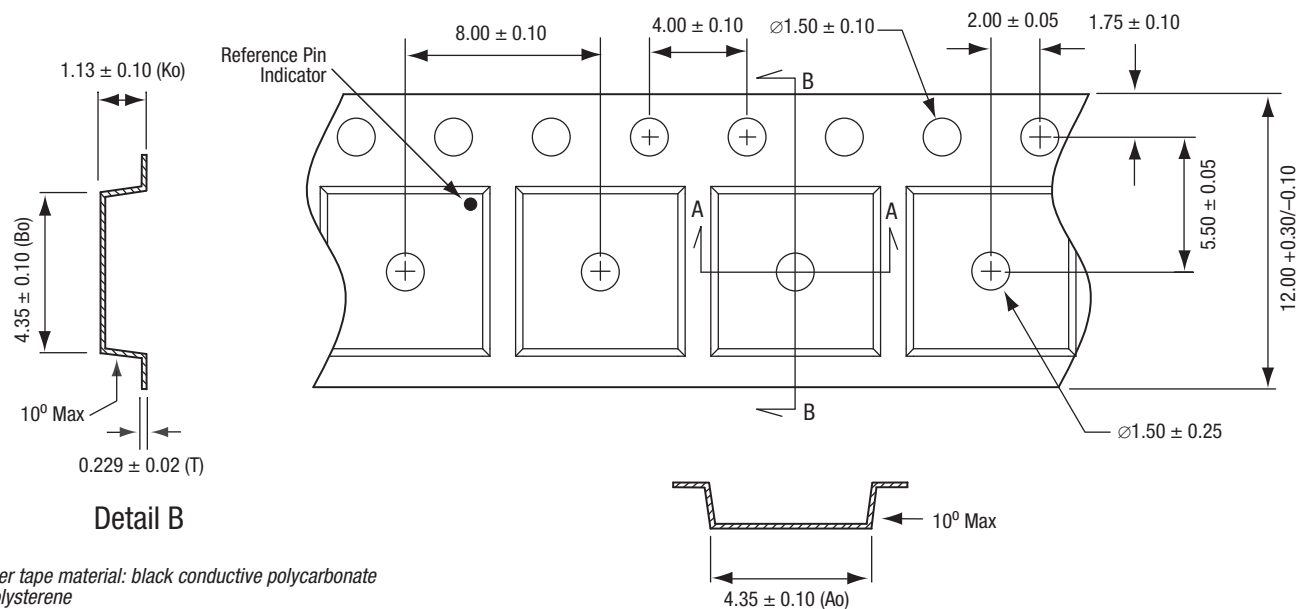


Figure 13. SE5003L1-R 20-Pin QFN Package Dimensions



Detail B

Detail A

Notes:

1. Carrier tape material: black conductive polycarbonate or polystyrene
2. Cover tape material: transparent conductive PSA
3. Cover tape size: 9.3 mm width
4. ESD surface resistivity is  $\leq 1 \times 10^8$  Ohms/square per EIA, JEDEC tape and reel specification.
5. Tolerance: .XX =  $\pm 0.10$
6. All measurements are in millimeters

S2585

Figure 14. SE5003L1-R 20-Pin QFN Tape and Reel Dimensions

## Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SE5003L1-R High-Power WLAN Power Amplifier	SE5003L1-R	SE5003L1-R-EK1

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Тел: +7 (812) 336 43 04 (многоканальный)

Email: [org@lifeelectronics.ru](mailto:org@lifeelectronics.ru)

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