Ordering number : ENA2172

LC89091JA

CMOS IC

Digital Audio Interface Receiver

ON Semiconductor®

http://onsemi.com

1. Overview

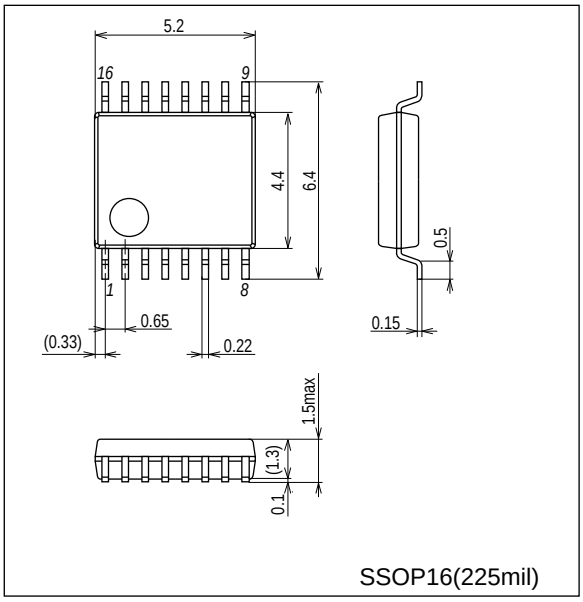
The LC89091JA is a digital audio interface receiver that demodulates signals according to the data transfer format between digital audio devices via IEC60958, IEC61937 and JEITA CPR-1205.
It supports demodulation sampling frequencies of up to 192kHz.
The LC89091JA adjusts to using in various systems including AV receivers, digital TVs and DVD recorders.

2. Features

- S/PDIF demodulation process according to IEC60958, IEC61937 and JEITA CPR-1205
- Outputs master clock: 512fs, 256fs and 128fs (with output frequency automatic adjustment function)
- Audio data output interface: 24-bit I^2S and MSB first left justified
- I^2C microcontroller interface (with address automatic increment function)
- Built-in power-on reset circuit
- Supply voltages: 3.0 to 3.6V
- Package: SSOP16 (lead-free and halogen-free)
- Operation guarantee temperature: -30 to 70°C

3. Package Dimensions

unit : mm (typ)
3178B



SSOP16(225mil)

* I^2C Bus is a trademark of Philips Corporation.

February, 2013

4. Pin Assignment

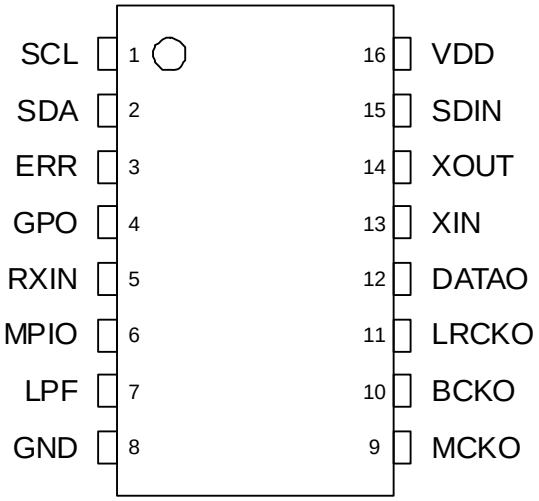


Figure 4.1: LC89091JA Pin Assignment

5. Pin Functions

Table 5.1: Pin Functions

No	Name	I/O	Function
1	SCL	I	Microcontroller interface I^2C: clock input pin
2	SDA	I	Microcontroller interface I^2C: data input pin
		O	Microcontroller interface I^2C: data output pin
3	ERR	O	PLL lock error and data error flag output pin (initial output)
			Output data mute signal output pin
4	GPO	O	Channel status bit-1 (PCM or non-PCM flag) output pin (initial output)
			Input S/PDIF (RXIN or MPIO) through output pin
			General purpose output pin
5	RXIN	I	3.3V tolerance TTL-compatible S/PDIF input pin
6	MPIO	O	Channel status emphasis flag output pin (initial output)
		I	3.3V tolerance TTL-compatible S/PDIF input pin
7	LPF	O	PLL: Loop filter connection output pin
8	GND		Digital GND
9	MCKO	O	Master clock output pin (512fs, 256fs, and 128fs)
10	BCKO	O	Bit clock output pin (64fs)
11	LRCKO	O	LR clock output pin (fs)
12	DATAO	O	Serial audio data output pin (I^2S and left justified)
13	XIN	I	Crystal resonator connection or external clock input pin (24.576MHz)
14	XOUT	O	Crystal resonator connection output pin
15	SDIN	I	Serial audio data input pin
16	VDD		Digital power supply (3.3V)

*Pin.2 and Pin 6 configure an open-drain output.

*Pin.2 needs a pull-up resistor when using microcontroller interface.

*Pin.6 needs a pull-up resistor when set to the output.

6. Block Diagram

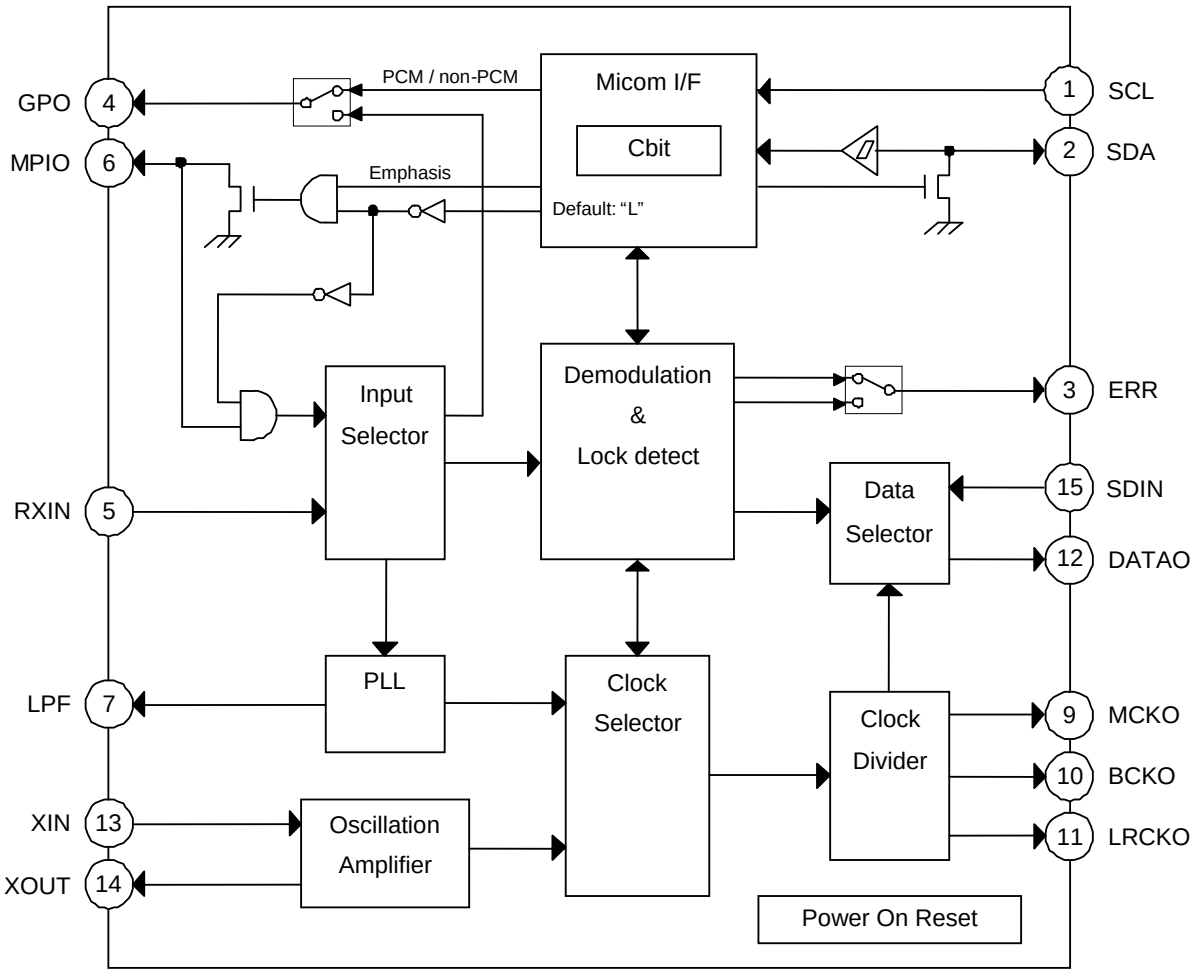


Figure 6.1: LC89091JA Block Diagram

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7.1: Absolute Maximum Ratings at GND=0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	7.1.1	-0.3 to 4.6	V
Input voltage	V_{IN}	7.1.2	-0.3 to V_{DD} max+0.3 (max.4.6Vp-p)	V
Output voltage	V_{OUT}	7.1.3	-0.3 to V_{DD} max+0.3 (max.4.6Vp-p)	V
Storage ambient temperature	Tstg		-55 to 125	°C
Operating ambient temperature	Topr		-30 to 70	°C
Maximum input/output current	I_{IN}, I_{OUT}	7.1.4	±20	mA

7.1.1: V_{DD} pin
7.1.2: SCL, SDA, RXIN, MPIO, XIN and SDIN pins
7.1.3: SDA, ERR, GPO, MPIO, MCKO, BCKO, LRCKO, DATAO and XOUT pins
7.1.4: Per input/output pin

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

7.2 Allowable Operating Range

Table 7.2: Recommended Operating Conditions at GND=0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	7.2.1	3.0	3.3	3.6	V
Input voltage range	V_{IN}	7.2.2	0		3.6	V
Output load capacitance	C_{L1}	7.2.3			20	pF
Output load capacitance	C_{L2}	7.2.4			30	pF
Operating temperature	Vopr		-30	25	70	°C

7.2.1: V_{DD} pin
7.2.2: SCL, SDA, RXIN, MPIO, XIN and SDIN pins
7.2.3: MCKO pin
7.2.4: Output pins expect MCKO pin

7.3 DC Characteristics

Table 7.3: DC Characteristics at Ta=-30 to 70°C, V_{DD}=3.0 to 3.6V, GND=0V

Parameter	Symbol	Conditions	min	max	Unit
Input, High	V_{IH}	7-3-1	0.7 V_{DD}		V
Input, Low	V_{IL}			0.2V_{DD}	V
Input, High	V_{IH}	7.3.2	2.0		V
Input, Low	V_{IL}			0.8	V
Output, High	V_{OH}	7.3.3	V_{DD}-0.8		V
Output, Low	V_{OL}			0.4	V
V_{DD} Supply Current	I_{DD1}	7.3.4		20	mA
V_{DD} Supply Current	I_{DD2}	7.3.5		2	μA

7.3.1: CMOS-compatible: XIN pin (while external clock inputs)
7.3.2: TTL-compatible: SCL, SDA, RXIN, MPIO and SDIN pins
7.3.3: I_{OH}=-4mA, I_{OL}=4mA: ERR, MCKO, BCKO, LRCKO, DATAO and XOUT output pins
I_{OH}=-2mA, I_{OL}=2mA: SDA and MPIO output pins
7.3.4: Input fs: 96kHz, MCKO: 512fs output status
7.3.5: "PDMODE=1"

7.4 AC Characteristics

Table 7.4: AC Characteristics at Ta=-30 to 70°C, V_{DD}=3.0 to 3.6V, GND=0V

Parameter	Symbol	min	typ	max	Unit
VDD rise slope	t_{VDD}	-	-	100	ms
RXIN and MPIO input receive frequency	f_{RFS}	28	-	195	kHz
RXIN and MPIO input duty factor	f_{RXDUY}	40	50	60	%
XIN clock input frequency	f_{XF}	-	24.576	-	MHz
MCKO clock output frequency	f_{MCK}	4	-	50	MHz
MCKO clock output duty factor	$f_{XMCKDUY}$	40	-	60	%
MCKO-BCKO output delay	t_{MBO}	-10	-	10	ns
BCKO-LRCKO output delay	t_{BLO}	-10	-	10	ns
BCKO-DATAO output delay	t_{BDO}	-10	-	10	ns
LRCKO-DATAO output delay	t_{LDO}	-10	-	10	ns

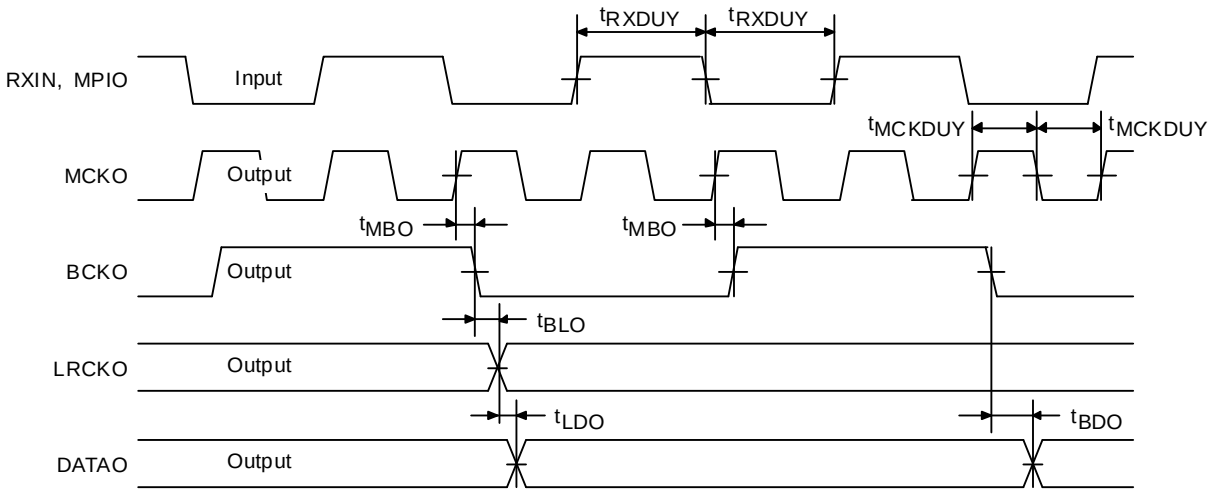


Figure 7.1: AC Characteristics

7.5 I²C Microcontroller Interface AC Characteristics

Table 7.5: AC Characteristics at Ta=-30 to 70°C, V_{DD}=3.0 to 3.6V, GND=0V

Parameter	Symbol	min	max	Unit
RSTB input pulse width (L)	t_{RSTdw}	-	400	kHz
SCL input frequency	f_{SCL}	600	-	ns
SCL input pulse width (L)	t_{SCLdw}	1300	-	ns
SCL input pulse width (H)	t_{SCLuw}	600	-	ns
Start (repeated) setup	t_{CSBuw}	600	-	ns
SDA hold	$t_{SDAhold}$	0	900	ns
SDA setup	$t_{SDAsetup}$	100	-	ns
SCL-SDA rise time	$t_{SCLSDArd}$	20+0.1Cb	300	ns
SCL-SDA fall time	$t_{SCLSDAfd}$	20+0.1Cb	300	ns
Stop setup	$t_{STOPsetup}$	600	-	ns
Bus open	$t_{BUSopen}$	1300	-	ns
Spike pulse width	t_{SPKpw}	0	50	ns

C_b = total capacitance of one bus line in pF.

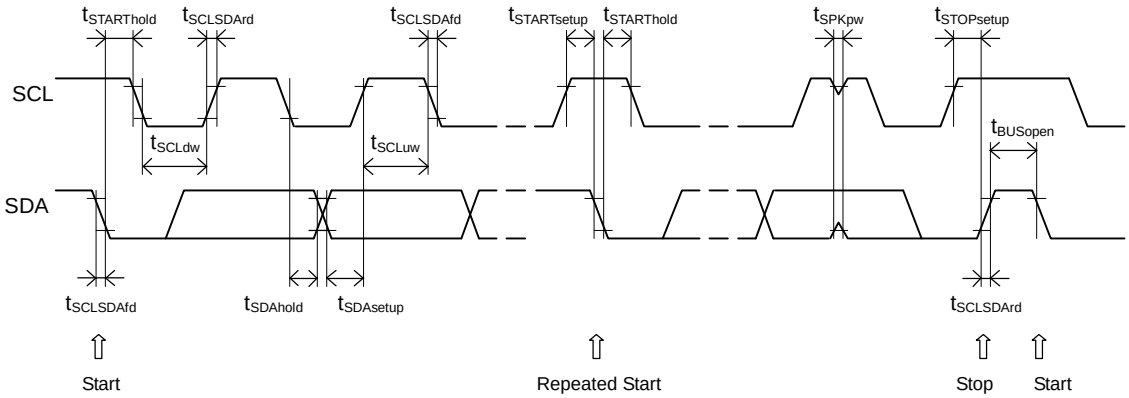


Figure 7.2: I²C Microcontroller Interface AC Characteristics

8. System Settings

8.1 Power-On Reset

- The LC89091JA features a built-in power-on reset circuit, and constantly monitors the power supply status.

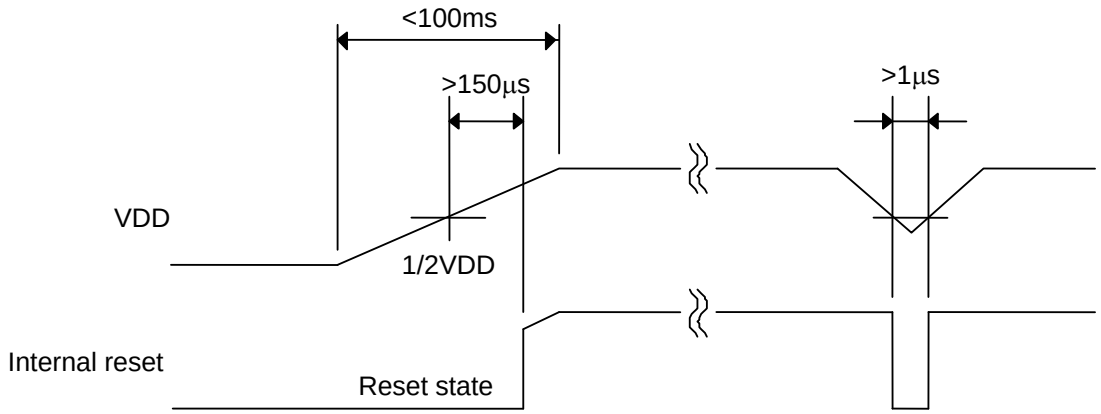


Figure 8.1: Power-On Reset Timing

Table 8.1: Output Port State Immediately after Power-On Reset

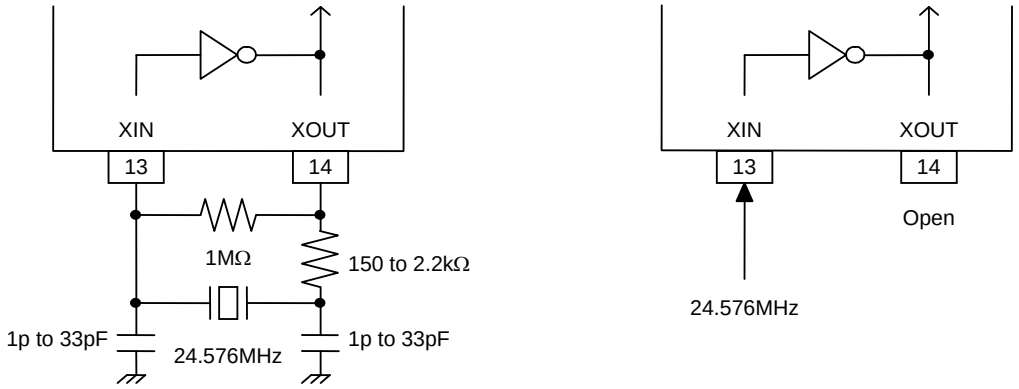
Pin No.	Port Name	Output State	Pin No.	Port Name	Output State
3	ERR	H output	10	BCKO	XIN/4 input clock output (6.144MHz)
4	GPO	L output (Non-PCM flag)	11	LRCKO	XIN/256 input clock output (96kHz)
6	MPIO	Hi-Z output (Emphasis flag)	12	DATAO	SDIN input data output
9	MCKO	XIN input clock output (24.576MHz)	14	XOUT	XIN invert output

8.2 Register Reset and Power-Down Mode

- The SYSRST register resets circuits other than register.
- During reset period, register setting state hold and can also change.
- Although a system is reset by SYSRST register, the oscillation amplifier operates, and the clock is output to MCKO, BCKO and LRCKO pins. But, DATAO pin outputs "L" without relation to the setup.
- The system is set power-down mode by PDMODE register.
- During power-down mode period, register setting state hold and can also change.
- In power-down mode, the circuits expect a power-on reset and a microcontroller interface will be set to stop condition all the circuit operations, and the clock is not output.

8.3 Oscillation Amplifier Pin Settings (XIN, XOUT)

- The LC89091JA has a built-in oscillation amplifier, and connects a quartz resonator, feedback resistor and load capacitance to XIN and XOUT to configure an oscillation circuit. The figure below shows the connection diagram.
- When connecting a quartz resonator, use one with a fundamental wave, and be aware that the load capacitance depends on the quartz resonator characteristics, so thorough investigation should be made.
- If the built-in oscillation amplifier is not used and an oscillation module is used as the clock source instead, connect the output of an external clock supply source to XIN. At this time, it is not necessary to connect a feedback resistor between XIN and XOUT.
- Always supply 24.576MHz clock to XIN.
- XIN clock is output to MCKO, BCKO and LRCKO while PLL is locked.



(a) XIN and XOUT Quartz Resonator Connection Diagram (b) XIN External Clock Input Diagram

Figure 8.2: XIN and XOUT External Circuit Connection Diagram

8.4 Loop Filter Pin Setting (LPF)

- The LC89091JA has a built-in VCO (Voltage Controlled Oscillator) that synchronizes with sampling frequencies from 32kHz to 192kHz and with the data with a transfer rate from 4MHz to 25MHz.
- The PLL is locked at 512fs.
- LPF is a pin for the PLL loop filter. Connect the resistor and capacitors shown in the right figure, as close to the pin as possible.

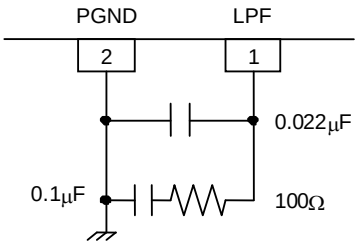


Figure 8.3: LPF External Circuit Connection Diagram

8.5 Clocks

8.5.1 Master Clock

- The clock source is selected between the following two master clocks.
  1) PLL source: 512fs
  2) XIN source: 24.576MHz

8.5.2 PLL Source Master Clock

- The PLL synchronizes with the input S/PDIF and outputs 512fs clock.
- The PLL clock is controlled by PLLACC, PLLDIV[1:0] and PRSEL[1:0] register settings.
- Normally, "PLLACC=0" is set and PLL clock is output for each input sampling frequency band. At this setting, output clock frequency fluctuation by varying the sampling frequency is kept to a narrow band, such as 512fs output when fs=32kHz to 48kHz, 256fs output when fs=64kHz to 96kHz, and 128fs output when fs=128kHz to 192kHz.
- When "PLLACC=0" is set, the PLL clock is set with the PLLDIV[1:0] register
- When "PLLACC=0" is set, during the PLL is locked, switching is not performed even when the PLLDIV[1:0] register setting is changed. These registers switching are executed when the PLL is in unlocked status. This setting becomes valid after the PLL is locked again.
- To set an output clock that does not depend on the S/PDIF input sampling frequency, "PLLACC=1" is set. At this setting, the clock frequency is always multiplied by a constant and output, such as output at 256fs for all sampling frequencies from 32kHz to 192kHz.
- When "PLLACC=1" is set, the PLL clock is set with the PRSEL[1:0] register.
- When "PLLACC=1" is set, PRSEL[1:0] register can be changed even PLL lock state.
- The change to "PLLACC=1" from "PLLACC=0" is possible even PLL lock state. But, the setting change to "PLLACC=0" from "PLLACC=1" becomes valid after the PLL is locked again.
- The PLL output clock setting flow is shown below.

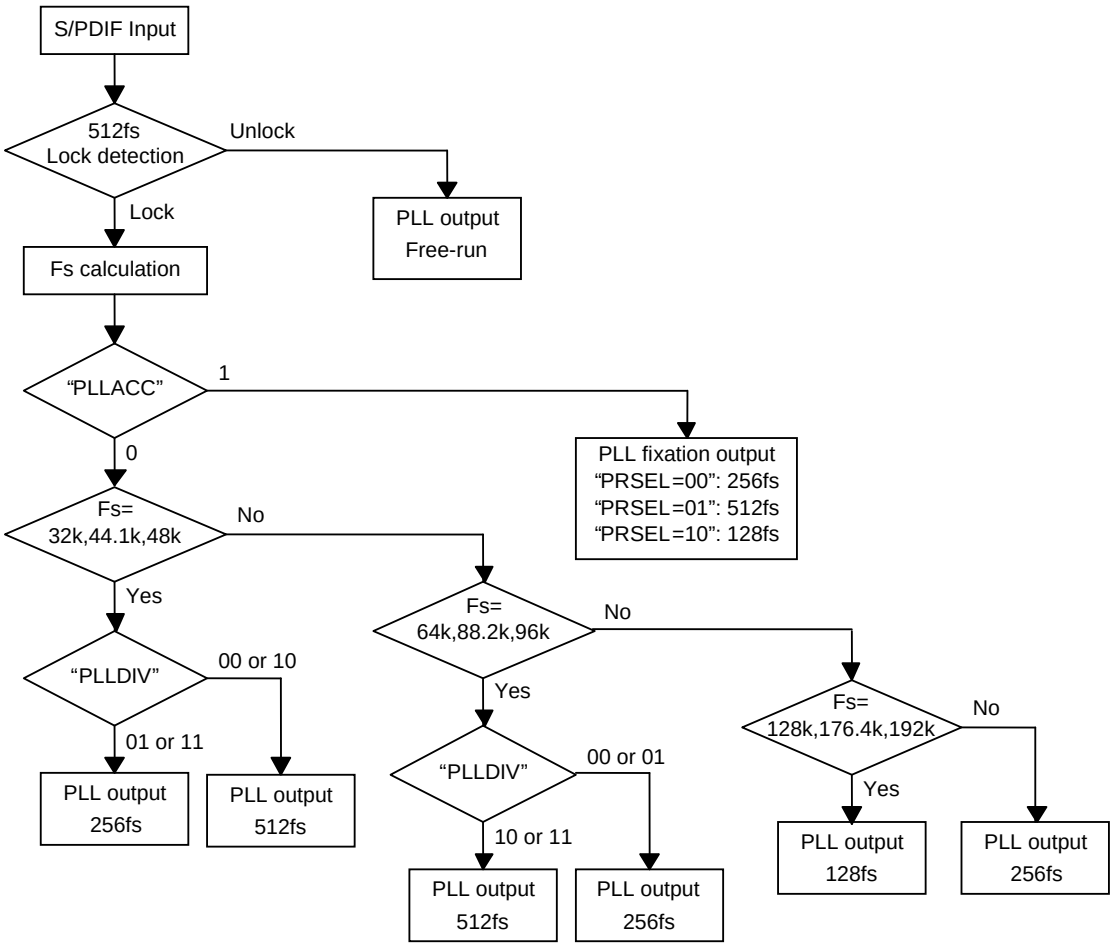


Figure 8.4: PLL Output Clock Flow Diagram

- The PLL clock output frequencies are shown below.
- When "PLLACC=1" and "PRSEL[1:0]=01" (512fs) are set, 128kHz, 176.4kHz and 192kHz S/PDIF reception results in a PLL output frequency that exceeds 50MHz, so direct output to MCKO is not guaranteed.

Table 8.2: PLL Clock Output Frequencies (Bold settings are initial values.)

S/PDIF fs (kHz)	PLL clock output frequencies (MHz)						
	"PLLACC=0" (Fixed multiple outputs for each input fs band)				"PLLACC=1" (Fixed multiple outputs of input fs)		
	"PLLDIV=00"	"PLLDIV=01"	"PLLDIV=10"	"PLLDIV=11"	"PRSEL=00" (256fs)	"PRSEL=01" (512fs)	"PRSEL=10" (128fs)
32	**16.38**	8.19	16.38	8.19	8.19	16.38	4.09
44.1	**22.57**	11.28	22.57	11.28	11.28	22.57	5.64
48	**24.57**	12.28	24.57	12.28	12.28	24.57	6.14
64	**16.38**	16.38	32.76	32.76	16.38	32.76	8.19
88.2	**22.57**	22.57	45.15	45.15	22.57	45.15	11.28
96	**24.57**	24.57	49.15	49.15	24.57	49.15	12.28
128	**16.38**	16.38	16.38	16.38	32.76	65.54 *	16.38
176.4	**22.57**	22.57	22.57	22.57	45.15	90.32 *	22.57
192	**24.57**	24.57	24.57	24.57	49.15	98.30 *	24.57

*: Direct output to the MCKO pin is not guaranteed.

8.5.3 XIN Source Master Clock (XIN, XOUT)

- Supply XIN with clocks all the time to be used in the following applications.
  1) Clock source when the PLL is unlocked
  2) PLL lock-in support
  3) Calculation of the S/PDIF input data sampling frequency
- 24.576MHz clock always has to supply to XIN.
- Normally, the oscillation amplifier automatically stops while the PLL is locked, but operation that always operates regardless of the PLL status can also be set. This is set with the AMPOPR register.
  The AMPOPR register must be set before S/PDIF input, or the setting must be completed while the PLL is unlocked.
- For fixing a system clock to a XIN clock, PLL is changed into an unlocking state. The ADMODE register always sets PLL as an unlocking state.
- The output clock frequency at the time of XIN source is set up with the XOUTCK register.

Table 8.3: List of Output Clock Frequencies

Output Pin Name	When PLL is unlocked, XIN source clock (XIN input clock)	When PLL is locked, PLL source clock (Internal VCO clock)
	24.576 MHz	512fs
Master clock MCKO	24.576 MHz	512fs 256fs 128fs
Bit clock BCKO	6.144 MHz 3.072 MHz	64fs
L/R clock LRCKO	96 kHz 48 kHz	fs

8.5.4 Output clock switching (MCKO, BCKO, LRCKO)

- The clock source of PLL clock or XIN clock is switched automatically according to the PLL locked or unlocked status.
- The output clock switches 2.7ms after the change of PLL status.

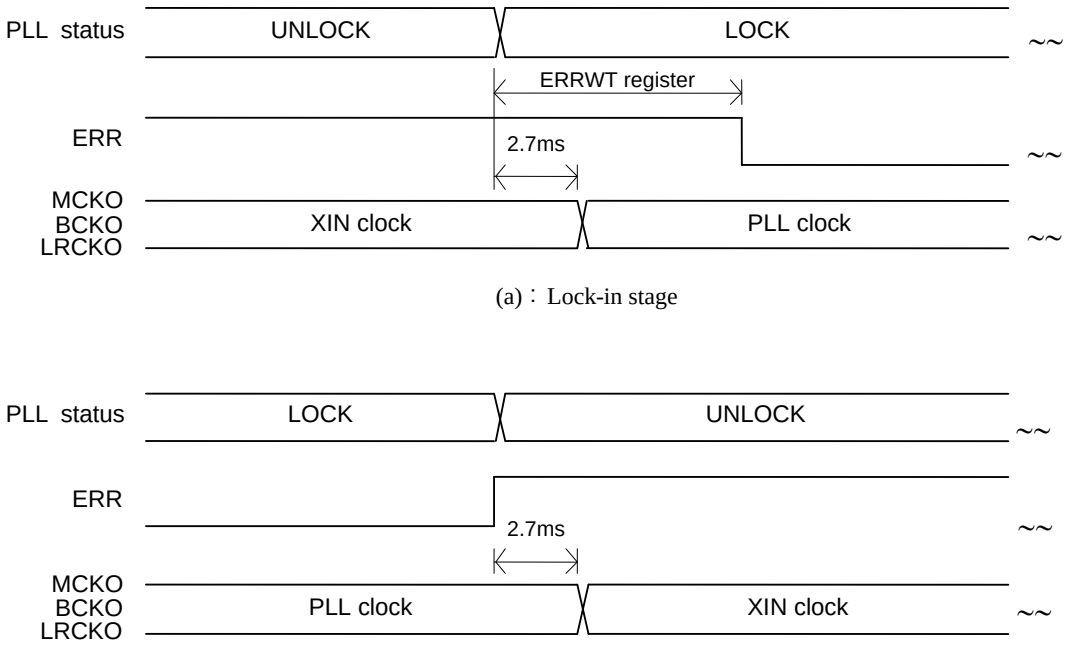


Figure 8.5: Timing Chart of Output Clock Switching

8.5.5 Calculation of digital input data sampling frequency

- The input data sampling frequency is calculated using the XIN clock.
- In the "AMPOPR=0" mode (initial value) where the oscillation amplifier automatically stops according to the lock status of the PLL, the input data sampling frequency is calculated during the ERR error period and completed when the oscillation amplifier stops with holding the value. Therefore, the value remains unchanged until the PLL becomes unlocked.
- If the oscillation amplifier is in a continuous operation mode ("AMPOPR=1"), calculation is repeated constantly. Even if sampling changes within the PLL capture range for input data whose channel status sampling information does not change, the calculation results that follow the input data can be read.
- The calculation results can be readout with the microcontroller interface.

8.6 Data

8.6.1 Reception range of S/PDIF input

- The input data reception range is 32kHz to 192kHz.

8.6.2 S/PDIF Input/Output pins (RXIN, MPIO, GPO)

- Two digital input pins and one through output pin are provided.
- RXIN and MPIO are TTL input level pins with 3.3V-tolerance voltage.
- MPSEL register needs to be set up, using MPIO as S/PDIF input.
- The demodulation data is selected with DINSEL register.
- All the S/PDIF input pins can receive 32kHz to 192kHz data.
- GPO is input selector output pin, and output the S/PDIF through data.
- The demodulated data and the through output data can be selected separately.
- The GPO pin output data is selected with GPOSEL[1:0] and THRSEL register.
- When MPIO is no-load at an output setup, don't choose MPIO by DINSEL or THRSEL register.
- In order to stop demodulation processing and to switch to oscillation amplifier operation, the S/PDIF input to RXIN and MPIO is stopped, or PLL is always set as an unlocking state by ADMODE register.

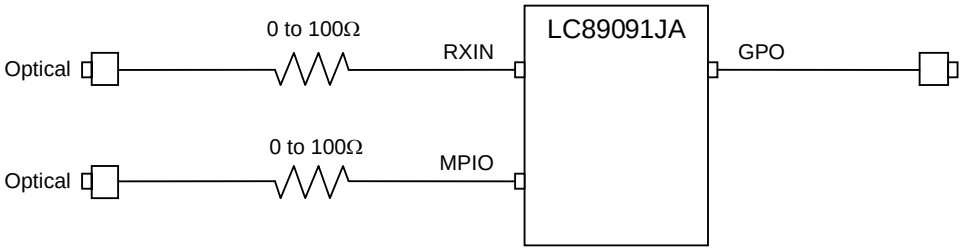
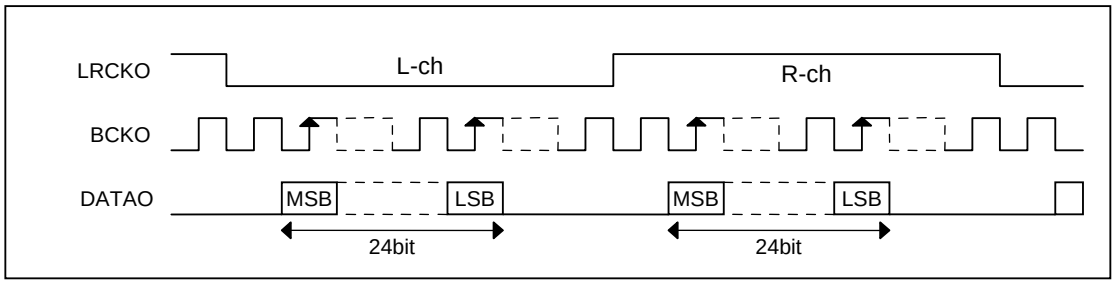


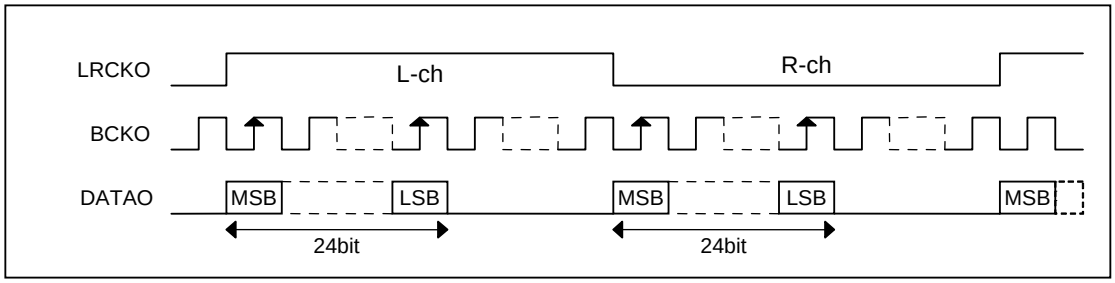
Figure 8.6: S/PDIF Input Circuit Example

8.6.3 Output Data Format (DATAO)

- The DATAO output data format is set with DAFORM register.
- The initial value of the output format is I^2S. The data is output synchronized with BCKIN falling edge.



[DAFORM=0] : I^2S Data Output

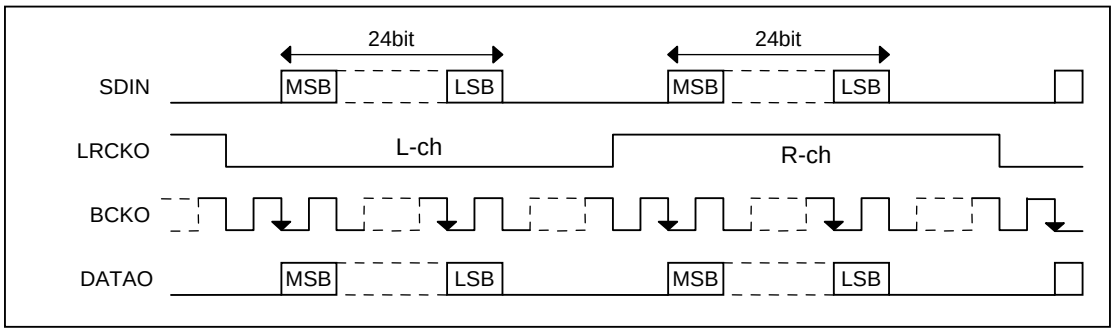


[DAFORM=1] : MSB first Left-Justified Data Output

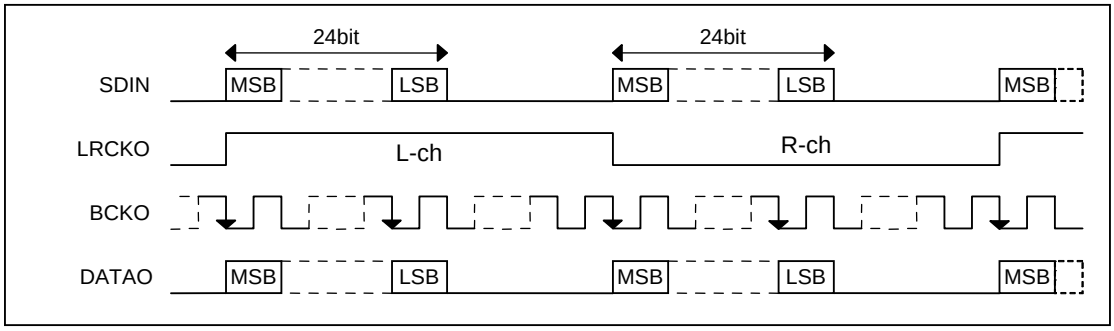
Figure 8.7: DATAO pin Data Output Timing

8.6.4 Serial audio data input format (SDIN)

- The LC89091JA is provided with a serial data input pin of SDIN.
- The format of the serial audio data input to SDIN and the demodulation data output format must be identical.
- The SDIN data to be input must be synchronization with the BCKO and LRCKO clocks.
- The data input from the SDIN pin is through-output to the DATAO pin. Data format conversion cannot be performed.
- Normally, SDIN input data is output to DATAO pin when PLL is unlocked. But, with the ADMODE register setting, the SDIN input data is output to DATAO regardless of the locked/unlocked status of the PLL.
- The SDIN pin must be connected to GND when it is not used.



[DAFORM=0] : I^2S Data Input

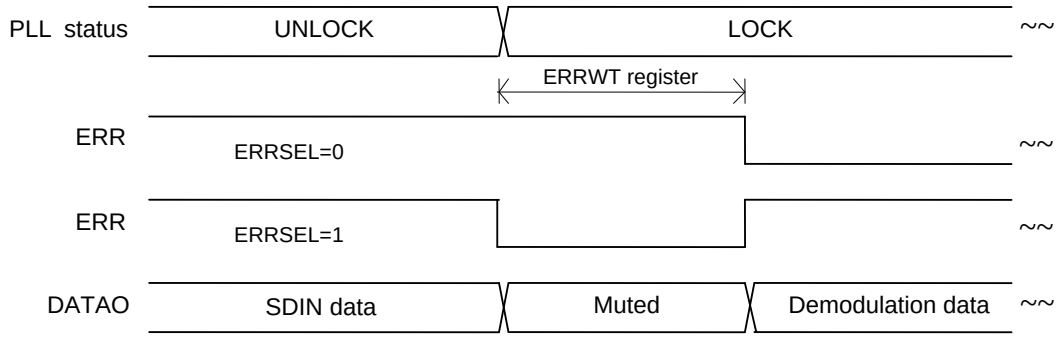


[DAFORM=1] : MSB first Left-Justified Data Input

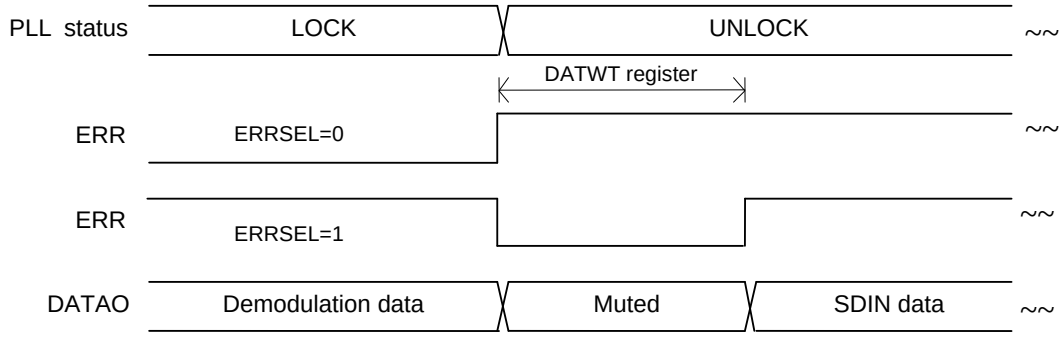
Figure 8.8: SDIN pin Data Input Timing

8.6.5 Output data switching (SDIN, DATAO)

- DATAO outputs demodulation data when the PLL is locked, and outputs SDIN input data when the PLL is unlocked. This output is automatically switched according to the PLL locked/unlocked status.
- When SDIN input data is selected, SDIN input data must synchronize with clock source.
- DATAO output switches via a mute period.
- It adjusts by ERRWT register during the mute period at the time of PLL lock-in process.
- It adjusts by DATWT register during the mute period at the time of PLL unlock process
- With the DATMUT setting, the DATAO output data can be also muted forcibly.
- NPMODE register can be muted the DATAO output data, when non-PCM data is received. Non-PCM data applies to the state of the channel status bit 1.



(a)： Lock-in stage



(b)： Unlock stage

Figure 8.9: Timing Chart of DATAO Output Data Switching

8.7 Error Output Processing (ERR)

- The ERR output can be selected the following outputs by the ERRSEL register.

8.7.1 Lock Error and Data Error Output ("ERRSEL=0")

- The ERR pin outputs an error flag when PLL lock error or data error occurs.
- The ERR is output synchronizing with LRCKO and can be readout with the microcontroller interface.

8.7.1.1 PLL Lock Error

- The PLL gets unlocked for input data that lost bi-phase modulation regularity, or input data for which preambles B, M and W cannot be detected.
- However, even if preambles B, M and W are detected if the timing does not conform to the IEC60958, the PLL get unlocked and processed. For example, period of preamble B is not every192 frames.
- The ERR outputs "H" when the PLL lock error occurs.
- The ERR outputs "L" when the data demodulation returns normal and "H" is held for somewhere between 3m to 36ms.
- This holding time is set with the ERRWT register.

Table 8.4: ERR Release Maintenance Period after a PLL Locks

S/PDIF input sampling frequency (kHz)	ERR release maintenance period after a PLL locks (ms)	
	"ERRWT=0"	"ERRWT=1"
32	18	36
44.1	13	26
48	12	24
88.2	6.5	13
96	6	12
176.4	3.3	6.5
192	3	6

8.7.1.2 Input Data Parity Error

- An odd number of errors among parity bits in input data and input parity errors are detected.
- The ERR outputs "H" when an input parity error occurs.
- When an input parity error occurs, output data is replaced to the data of one frame ago.
  However, when having received non-PCM data, data does not replace. In this case, data including an error is output.

8.7.1.3 Other Errors

- Even if ERR turns to "L", the channel status bits of 24 to 27 (sampling frequency information) are always fetched and the data of the previous block is compared with the current data. Moreover, the input data sampling frequency is calculated from the fs clock extracted from the input data, and the fs calculated value is compared in the same way as described above. If any difference is detected in these data, ERR is instantly made "H" and the same processing as for PLL lock errors is carried out. In this case, the clock source is switched to XIN and processing is restarted at lock status identification processing.
- In order to support sources with a variable fs (for example, a CD player with a variable pitch function), any change in fs made after ERR is reset is not reflected on ERR unless such change exceeds the PLL capture range.

8.7.2 DATAO data Mute Signal Output ("ERRSEL=1")

- This mode outputs the state of the audio data outputted from the DATAO pin. (See “Figure 8.9”)
- A mute processing setup at the time of non-PCM audio data reception ("NPMODE=1")) is also reflected.

Table 8.5: DATAO Output State Signal Output

ERR output	DATAO output conditions
L	Muted
H	Outputted

8.8 General Purpose Output (GPO)

- The GPO output can be selected the following outputs by the GPOSEL[1:0] register.

8.8.1 Channel Status Bit 1 Output ("GPOSEL[1:0]=00")

- The initial mode outputs bit 1 of the channel status that indicates whether the input bi-phase data is PCM audio data. It is immediately output upon detection of ERR even during an error output period.

Table 8.6: Channel Status Bit 1 Output

GPO output	GPO output conditions
L	Audio sample word represents linear PCM samples (Bit1=L)
H	Audio sample word used for other purposes (Bit 1=H)

8.8.2 S/PDIF Through-output ("GPOSEL[1:0]=01")

- The data selected by the S/PDIF input selector (DINSEL register) is output. The output data is selected with the THRSEL register.

Table 8.7: Output of S/PDIF data

GPO output	GPO output conditions
RXIN or MPIO input data	"GPOSEL[1:0]=01"

8.8.3 Microcontroller Register Output ("GPOSEL[1:0]=10 or 11")

- This mode outputs a serial data that is set by the microcontroller interface. It can be used as a control signal of peripheral circuitry.

Table 8.8: Microcontroller Register Output

GPO output	GPO output conditions
L	"GPOSEL[1:0]=10"
H	"GPOSEL[1:0]=11"

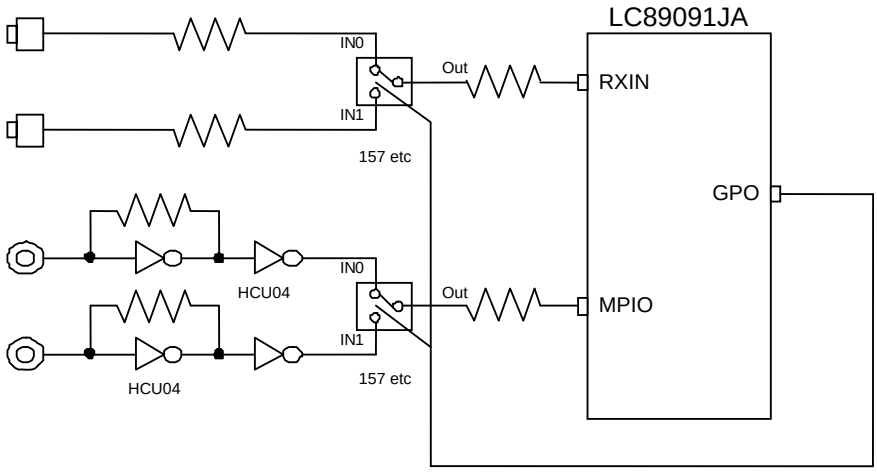


Figure 8.10: GPOSEL [1:0] register Example of Use

8.9 Multi Purpose Input/Output (MPIO)

- MPIO can be selected the following input/output by the MPSEL register.
- MPIO needs a pull-up resistor when set to the output.
- When not using MPIO, it uses no connecting (open state).
  However, don't choose MPIO by DINSEL or THRSEL register.

8.9.1 Pre-emphasis Flag Output ("MPSEL=0")

- The initial mode outputs pre-emphasis of the channel status that indicates whether there is 50/15μs emphasis parameter for consumer.
- MPIO becomes a Hi-Z output when an emphasis signal is not detected. For this reason, it connects with a pull-up resistor. The example of use is shown below

Table 8.9: Pre-emphasis Flag Output

MPIO output	MPIO output conditions
Hi-Z (H**)	No pre-emphasis
L	50/15μs pre-emphasis

**: When MPIO connects with a pull-up resistor

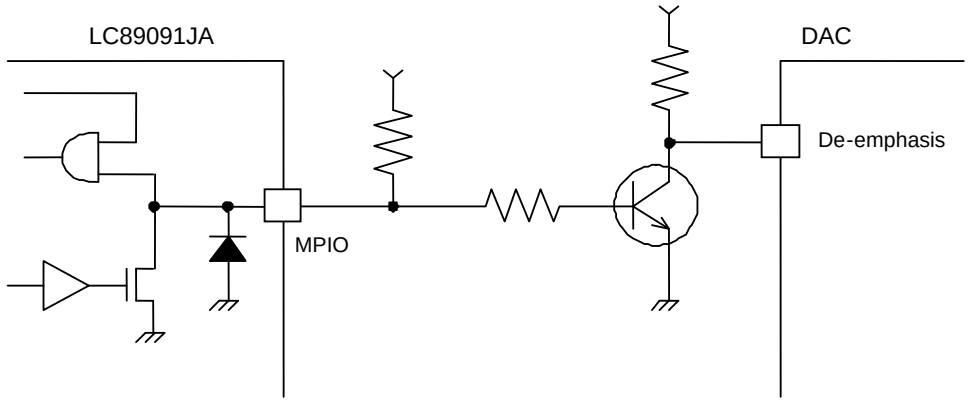


Figure 8.11: MPIO Output Example of Use (Pre-emphasis Output)

8.9.1 S/PDIF data Input ("MPSEL=1")

- MPIO can be used as S/PDIF input terminal by "MPSEL=1".
- MPIO immediately after power-on is set as an output state. For this reason, before input all the S/PDIF signals, MPIO is set as an input state by MPSEL register. If S/PDIF signal input (RXIN input) before MPSEL register setup and pre-emphasis flag is detected, MPIO output will short-circuit with peripheral circuitry. Therefore, before S/PDIF signal input, MPIO setup must be complete.

9. Microcontroller Interface

- The LC89091JA is controlled via I^2C (Fast-mode, 400kHz).

9.1 Terminal Setup (SCL, SDA)

- The pull-up resistor is connected to SCL and SDA pins.
  The resistor should take current and timing into consideration enough.
- If the clock line will not be Hi-Z state, the pull-up resistor of SCL may delete.
- When not using microcontroller, SCL and SDA make GND connection. In this case, initial value of register is set up.

9.2 Data Transfer

- I^2C slave transceiver interface is based on ver2.1 (HS mode un-corresponding).
- At first, input Start condition and Slave-address, an acknowledge generates, WRITE operation and READ operation (input Register-address and Control-data) is executed. After the command execution, input Stop condition.
- SDA line state must be constant while SCL is "H". State change on SDA line is restricted while SCL line is "L". If SDA data changes while SCL line is "H", it will be recognized as Start condition or Stop condition.

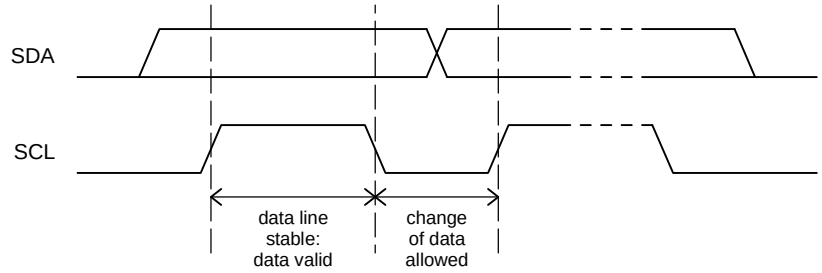


Figure 9.1: Data transfer on I^2C bus

9.3 Start and Stop Condition

- The Start condition is generated by the transition of "H" to "L" on SDA line while SCL line is "H".
- The Stop condition is generated by the transition of "L" to "H" on SDA line while SCL line is "H".

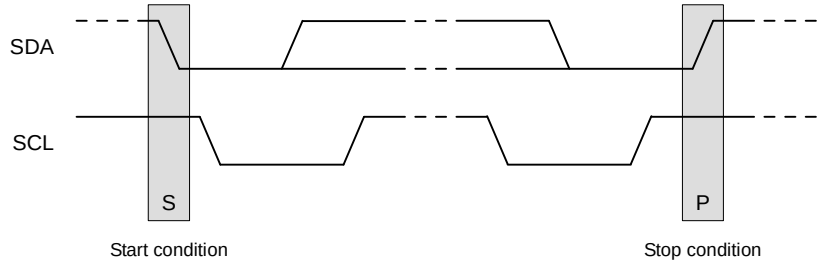


Figure 9.2: Start and Stop Condition

9.4 Acknowledge

- After receiving bits (1 byte) of data, SDA line is released, LC89091JA will stabilize SDA line in "L" state.
  This operation is called "acknowledgement".
- The LC89091JA generates an acknowledgement upon receipt of Start condition and Slave-address.
  Furthermore, for a WRITE instruction, an acknowledgement is generated whenever receipt of each byte is completed.
  For a READ instruction, succeeded by generation of an acknowledgement, the LC89091JA releases the SDA line after outputting data at the designated address, and it monitors the SDA line condition.
  When the microcontroller generates an acknowledgement without sending Stop condition, the LC89091JA outputs data at the next address location. When no acknowledgement is generated, the LC89091JA ends data output (not acknowledged).

9.5 Slave-address

- The Slave-address inputs after the Start condition.
- The Slave-address is configured with the upper 7-bits. Data of the upper 5-bits is Device code that is input "00100". The next 2-bits are Device address that is input "10".
- When the R/W bit is "1", the READ instruction is executed, and when it is "0", the WRITE instruction is executed.

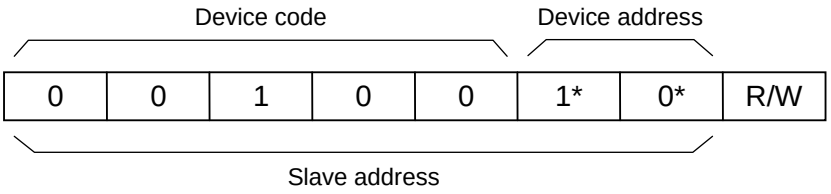


Figure 9.3: Slave-address Configuration

9.6 Register-address

- After transmitting 1 byte of data containing Slave-address, Register-address is set up from next byte.

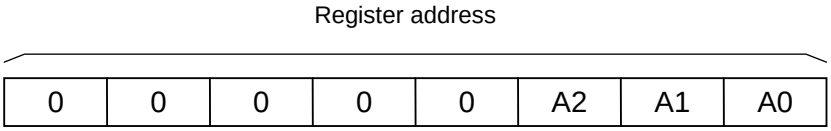


Figure 9.4: Register-address Configuration

9.7 Control Data

- The control data inputs after Register-address transmission.
- The control data (D7 to D0) is configured with MSB first.

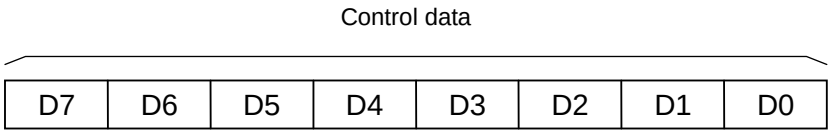


Figure 9.5: Control Data Configuration

9.8 WRITE Operation

- When the R/W bit is "0", the WRITE instruction is executed.
- After Start condition input, Slave-address (R/W=0) and Register-address are input one by one.
- After an acknowledge is generated, the write data is taken in by SCL↑ in front of an acknowledge clock pulse.
- When the Slave-address is differ, an acknowledge is not generated, SDA line will be in an open state. In this case, it has to input from Start conditions (S).

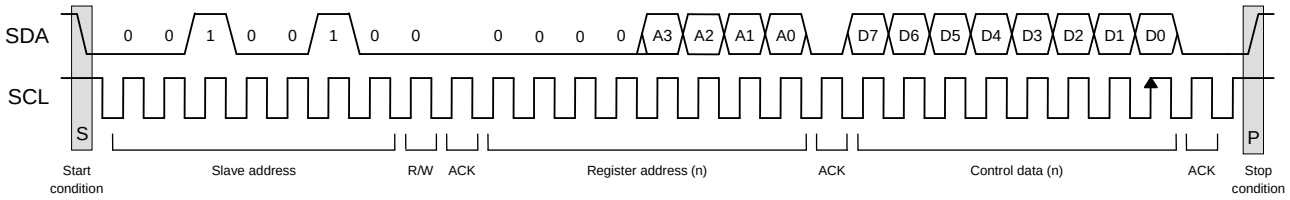


Figure 9.6: I²C Data Write Timing Chart (Byte Write)

- After receipt of 8 bits (1 byte) data, when data (1 byte) transmits further without sending Stop conditions after an acknowledge generation, the Register-address counter is incremented by one and data is stored in the next address.
- If an address value becomes 08h address, address counter will "rolls over" to 00h address and data is stored from 00h and the previous data will be overwritten.

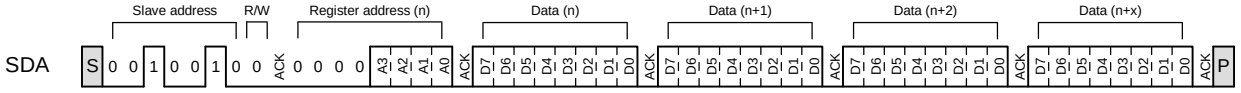


Figure 9.7: I²C Data Write Timing Chart (Page Write)

9.9 READ Operation

- When the R/W bit is "1", the READ instruction is executed.
- After Start condition input, Slave-address (R/W=0) and Register-address are input one by one.
- After an acknowledge is generated, Start condition (Sr) and Slave-address (R/W=1) input again. And, after an acknowledge is generated, the data of the Register-address specified is output.
- If the microcontroller does not generate an acknowledge but generate the Stop condition, the LC89091JA discontinues transmission.

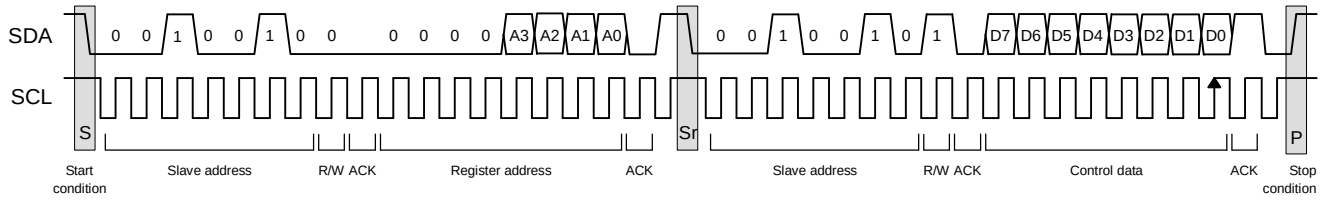


Figure 9.8: I^{2}C Data Read Timing Chart (Random Read)

- If a microcontroller returns an acknowledge after 8 bits (1 byte) data output, the data (1 byte) of the next address will be read continuously.
- If an address value becomes 08h address, the next address will be read from 00h data one by one.
- If a microcontroller does not generate an acknowledge but generate the Stop condition, the LC89091JA discontinues transmission.

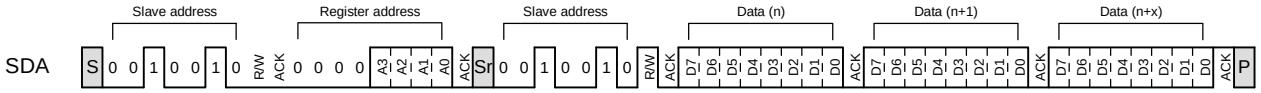


Figure 9.9: I^{2}C Data Read Timing Chart (Sequential Read)

9.10 Registers

9.10.1 Register Map

Table 9.1: Register Map

Setting Item	R/W	Adr	D7	D6	D5	D4	D3	D2	D1	D0
System	R/W	00h	"0"	MPSEL	DATWT	ERRWT	ADMODE	AMPOPR	PDMODE	SYSRST
Clock	R/W	01h	"0"	"0"	XOUTCK	PRSEL1	PRSEL0	PLLDIV1	PLLDIV0	PLLACC
Data	R/W	02h	NPMODE	ERRSEL	GPOSEL1	GPOSEL0	DATMUT	THRSEL	DINSEL	DAFORM
Fs calculation	R	03h	0	0	0	ERRFLG	FSC3	FSC2	FSC1	FSC0
Channel status	R	04h	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
	R	05h	CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8
	R	06h	CS23	CS22	CS21	CS20	CS19	CS18	CS17	CS16
	R	07h	CS31	CS30	CS29	CS28	CS27	CS26	CS25	CS24
	R	08h	CS39	CS38	CS37	CS36	CS35	CS34	CS33	CS32

- "0" is a reserved bit. Always must be set to "0".

9.10.2 Details of Registers

Address: 00h; System Setting

00h	D7	D6	D5	D4	D3	D2	D1	D0
Register name	"0"	MPSEL	DATWT	ERRWT	ADMODE	AMPOPR	PDMODE	SYSRST
Initial value	0	0	0	0	0	0	0	0
Setting	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SYSRST System reset

0: Don’t reset (initial value)

1: Reset all circuits other than registers

PDMODE Power down mode setting

0: Normal operation (initial value)

1: Power down mode (clock operation stop)

AMPOPR Oscillation amplifier operation setting

0: Automatic stopping of oscillation amplifier while PLL is locked (initial value)

1: Permanent continuous operation

ADMODE S/PDIF reception refusal mode setting

0: Normal operation (initial value)

1: Always PLL unlock state

ERRWT ERR wait time setting after PLL is locked

0: Error is canceled after 3 occurrences of preamble B are counted (initial value)

1: Error is canceled after 6 occurrences of preamble B are counted

DATWT DATAO wait time setting after PLL is unlocked

0: Mute is canceled after about 5.4 ms (initial value)

1: Mute is canceled after about 342ms

MPSEL MPIO pin input/output setting

0: Pre-emphasis flag output (initial value)

1: S/PDIF input

Address: 01h; Clock Setting

01h	D7	D6	D5	D4	D3	D2	D1	D0
Register name	"0"	"0"	XOUTCK	PRSEL1	PRSEL0	PLLDIV1	PLLDIV0	PLLACC
Initial value	0	0	0	0	0	0	0	0
Setting	R	R	R/W	R/W	R/W	R/W	R/W	R/W

PLLACC PLL clock lock frequency setting

0: Automatic control (initial value)

1: Manual setting

PLLDIV[1:0] PLL lock time MCKO output setting when PLLACC is set to "0"

00: 512fs output: When receiving 32kHz, 44.1kHz, 48kHz (initial value)
256fs output: When receiving 64kHz, 88.2kHz, 96kHz
128fs output: When receiving 128kHz, 176.4kHz, 192kHz

01: 256fs output: When receiving 32kHz, 44.1kHz, 48kHz
256fs output: When receiving 64kHz, 88.2kHz, 96kHz
128fs output: When receiving 128kHz, 176.4kHz, 192kHz

10: 512fs output: When receiving 32kHz, 44.1kHz, 48kHz
512fs output: When receiving 64kHz, 88.2kHz, 96kHz
128fs output: When receiving 128kHz, 176.4kHz, 192kHz

11: 256fs output: When receiving 32kHz, 44.1kHz, 48kHz
512fs output: When receiving 64kHz, 88.2kHz, 96kHz
128fs output: When receiving 128kHz, 176.4kHz, 192kHz

PRSEL[1:0] PLL lock time MCKO output setting when PLLACC is set to "1"

00: 256fs output (initial value)

01: 512fs output

10: 128fs output

11: Reserved

XOUTCK XIN clock output setting when PLL is unlocked

0: MCKO=24.576MHz, BCKO=6.144MHz, LRCKO=96kHz (initial value)

1: MCKO=24.576MHz, BCKO=3.072MHz, LRCKO=48kHz

Address: 02h; Data setting

02h	D7	D6	D5	D4	D3	D2	D1	D0
Register name	NPMODE	ERRSEL	GPOSEL1	GPOSEL0	DATMUT	THRSEL	DINSEL	DAFORM
Initial value	0	0	0	0	0	0	0	0
Setting	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DAFORM Audio data output format setting

0: I^2S data output (initial value)

1: 24-bit MSB first, left-justified data output

DINSEL Data demodulation input setting

0: RXIN (initial value)

1: MPIO (when "MPSEL=1")

THRSEL GPO output data setting when "GPOSEL[1:0]=01"

0: RXIN (initial value)

1: MPIO (when "MPSEL=1")

DATMUT DATAO pin output setting

0: Output SDIN data while PLL is unlocked (initial value)

1: Mute, "L" output

GPOSEL[1:0] GPO output data setting

00: Channel status bit 1 output (initial value)

01: Input S/PDIF through output

10: "L" output

11: "H" output

ERRSEL ERR pin output setting

0: PLL lock error or transfer data parity error output (initial value)

1: DATAO data mute signal output

NPMODE DATAO pin output setting when S/PDIF non-PCM data is received

0: Output (initial value)

1: Mute, "L" output

- When MPIO is no-load at an output setup, don't choose MPIO by DINSEL or THRSEL register.
- DATAO is muted when non-PCM data is detected at "NPMODE=1". But, due to it is not a data error, ERR output PLL lock state ("L" output).

Address: 03h; Input fs calculation value

03h	D7	D6	D5	D4	D3	D2	D1	D0
Register name	0	0	0	ERRFLG	FSC3	FSC2	FSC1	FSC0
Setting	R	R	R	R	R	R	R	R

FSC[3:0] Input data fs calculation result read

0000: 44.1kHz
0001: Out of range
0010: 48kHz
0011: 32kHz
0100: -
0101: -
0110: -
0111: -
1000: 88.2kHz
1001: -
1010: 96kHz
1011: 64kHz
1100: 176.4kHz
1101: 128kHz
1110: 192kHz
1111: -

ERRFLG ERR pin output read (It can be read when "ERRSEL=1")

0: No transfer error while PLL is locked
1: Transfer error exists or PLL is unlocked

Address: 04h to 08h; Channel status information (read only)

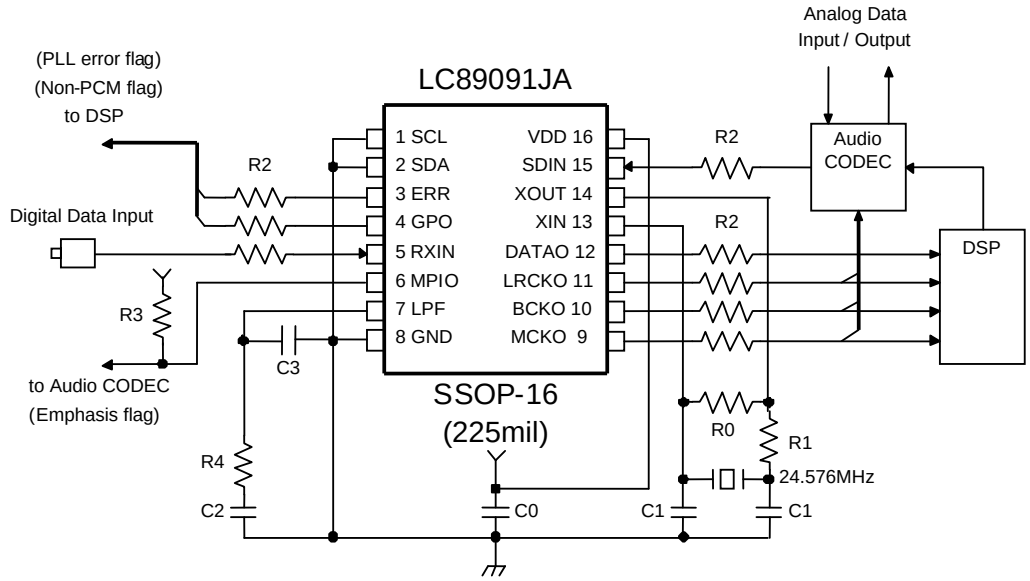
Address	D7	D6	D5	D4	D3	D2	D1	D0
04h	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
05h	CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8
06h	CS23	CS22	CS21	CS20	CS19	CS18	CS17	CS16
07h	CS31	CS30	CS29	CS28	CS27	CS26	CS25	CS24
08h	CS39	CS38	CS37	CS36	CS35	CS34	CS33	CS32

Table 9.2: Channel Status Register Contents

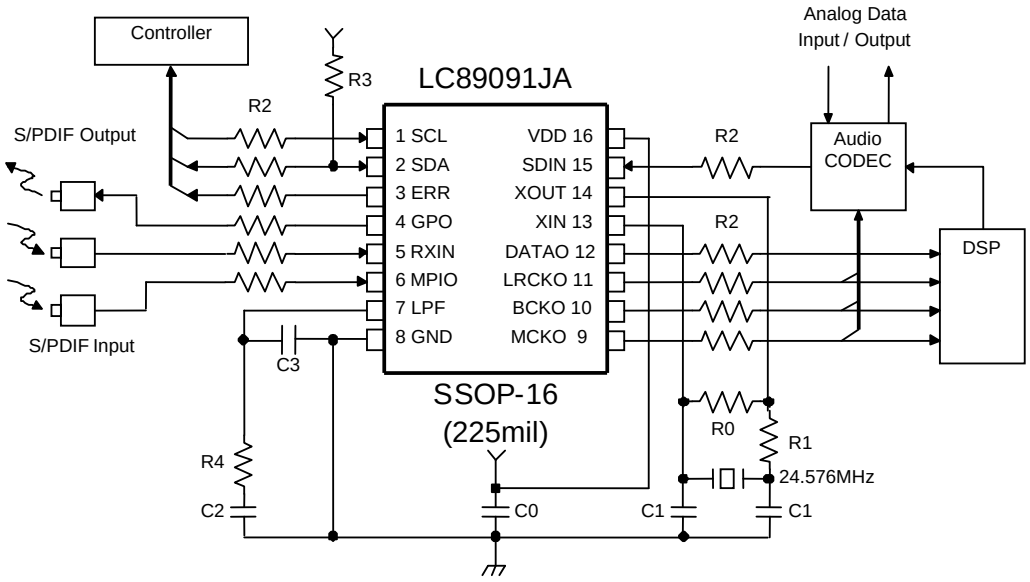
Adr	Reg	CS Bit	Description	Adr	Reg	CS Bit	Description
04h	CS0	bit0	Application	07h	CS24	bit24	Sampling frequency
	CS1	bit1	Control		CS25	bit25	
	CS2	bit2			CS26	bit26	
	CS3	bit3			CS27	bit27	
	CS4	bit4			CS28	bit32	Clock accuracy
	CS5	bit5			CS29	bit33	
	CS6	bit6	Not defined		CS30	bit30	Not defined
	CS7	bit7			CS31	bit31	
05h	CS8	bit8	Category code	08h	CS32	bit32	Bit width
	CS9	bit9			CS33	bit33	
	CS10	bit10			CS34	bit34	
	CS11	bit11			CS35	bit35	
	CS12	bit12			CS36	bit36	Original sampling frequency
	CS13	bit13			CS37	bit37	
	CS14	bit14			CS38	bit38	
	CS15	bit15			CS39	bit39	
06h	CS16	bit16	Source number				
	CS17	bit17					
	CS18	bit18					
	CS19	bit19					
	CS20	bit20	Channel number				
	CS21	bit21					
	CS22	bit22					
	CS23	bit23					

- For details, check the IEC60958 Specifications

10. Application Circuit Example



(1) Example of microcontroller interface is not used



(2) Example of microcontroller interface is used

Element Symbol	Recommended Parameter	Application	Remarks
C0	0.01μF to 0.1μF	Power supply de-coupling	Ceramic capacitor
R0	1MΩ	Oscillation amplifier feedback	
R1	150Ω to 2.2kΩ	Oscillation amplifier current limit	
C1	1pF to 33pF	Quarts resonator load	Ceramic capacitor with NP0 characteristics
R2	0Ω to 100Ω	Damping resistor	
R3	10kΩ to 100kΩ	Pull-up resistor	
R4	100Ω	PLL loop filter	See 8.4
C2	0.1μF	PLL loop filter	See 8.4
C3	0.022μF	PLL loop filter	See 8.4

Figure 10.1: LC89091JA Application Circuit Example

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