# 50 A VRPower® Integrated Power Stage

## DESCRIPTION

The SiC657 is integrated power stage solutions optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's proprietary 5 mm x 5 mm MLP package, SiC657 enables voltage regulator designs to deliver up to 50 A continuous current per phase.

The internal power MOSFETs utilizes Vishay's state-of-the-art Gen IV TrenchFET technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC657 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and zero current detection to improve light load efficiency. The driver is also compatible with a wide range of PWM controllers, supports tri-state PWM, and 5 V PWM logic.

A user selectable diode emulation mode (ZCD_EN#) is included to improve the light load performance. The device also supports PS4 mode to reduce power consumption when system operates in standby state.

## FEATURES

RoHS COMPLIANT HALOGEN FREE

- Thermally enhanced PowerPAK® MLP55-31L package
- Vishay's Gen IV MOSFET technology and a low side MOSFET with integrated Schottky diode
- Delivers in excess of 50 A continuous current, 55 A at 10 ms peak current
- High efficiency performance
- High frequency operation up to 2 MHz
- Power MOSFETs optimized for 19 V input stage
- 5 V PWM logic with tri-state and hold-off
- Supports PS4 mode light load requirement for IMVP8 with low shutdown supply current (5 V, 3 µA)
- Under voltage lockout for $V_{CIN}$
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

## APPLICATIONS

- Multi-phase VRDs for computing, graphics card and memory
- Intel IMVP-8 VRPower delivery
  - $V_{CORE}$, $V_{GRAPHICS}$, $V_{SYSTEM\ AGENT}$ Skylake, Kabylake platforms
  - $V_{CCGI}$ for Apollo Lake platforms
- Up to 24 V rail input DC/DC VR modules

## TYPICAL APPLICATION DIAGRAM

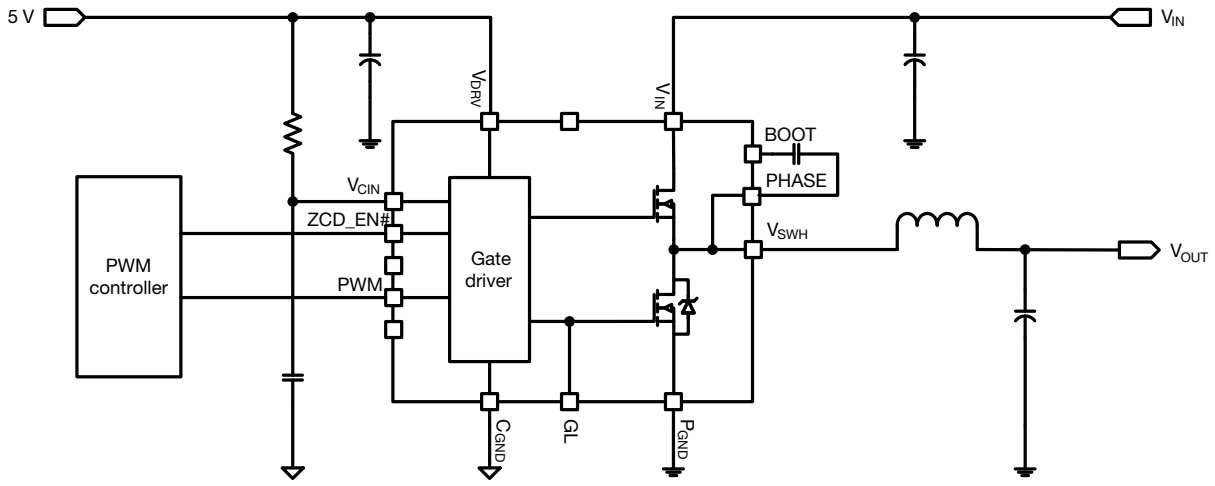



**Fig. 1 - Typical Application Diagram**

## PINOUT CONFIGURATION

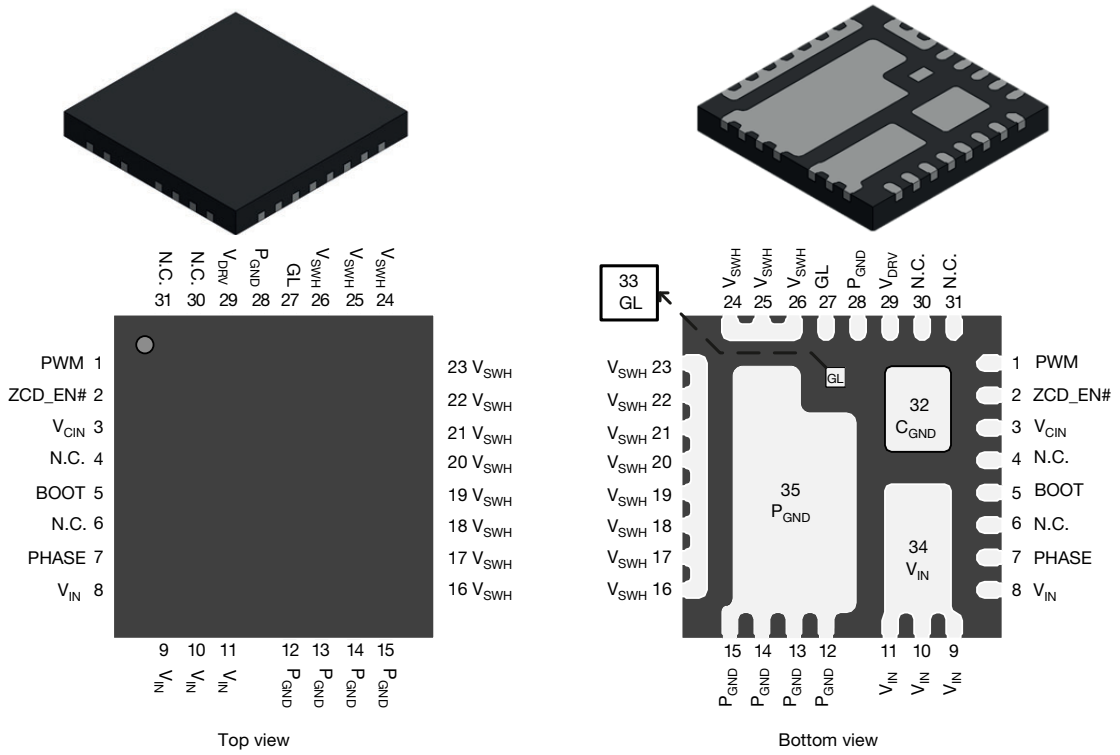
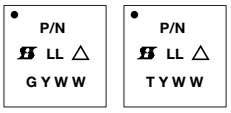
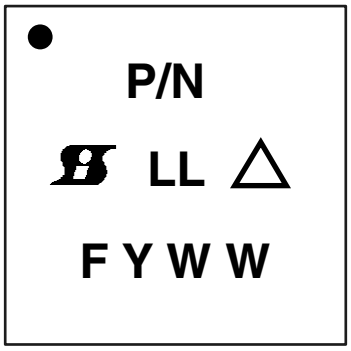



**Fig. 2 - Pin Configuration**

| PIN CONFIGURATION | | |
|---|---|---|
| **PIN NUMBER** | **NAME** | **FUNCTION** |
| 1 | PWM | PWM input logic |
| 2 | ZCD_EN# | The ZCD_EN# pin enables or disables diode emulation. When ZCD_EN# is LOW, diode emulation is allowed. When ZCD_EN# is HIGH, continuous conduction mode is forced.<br>ZCD_EN# can also be put in a high impedance mode by floating the pin. If both ZCD_EN# and PWM are floating, the device shuts down and consumes typically 3 µA (9 µA max.) current |
| 3 | $V_{CIN}$ | Supply voltage for internal logic circuitry |
| 5 | BOOT | High side driver bootstrap voltage |
| 4, 6, 30, 31 | N.C. | Pin 4 can be either left floating or connected to $C_{GND}$. Internally it is either connected to GND or not internally connected depending on manufacturing location.<br>Factory code “G” on line 3, pin 4 = $C_{GND}$<br>Factory code “T” on line 3, pin 4 = not internally connected<br>  |
| 7 | PHASE | Return path of high side gate driver |
| 8 to 11, 34 | $V_{IN}$ | Power stage input voltage. Drain of high side MOSFET |
| 12 to 15, 28, 35 | $P_{GND}$ | Power ground |
| 16 to 26 | $V_{SWH}$ | Phase node of the power stage |
| 27, 33 | GL | Low side MOSFET gate signal |
| 29 | $V_{DRV}$ | Supply voltage for internal gate driver |
| 32 | $C_{GND}$ | Signal ground |

| ORDERING INFORMATION | | | |
|---|---|---|---|
| **PART NUMBER** | **PACKAGE** | **MARKING CODE** | **OPTION** |
| SiC657CD-T1-GE3 | PowerPAK MLP55-31L | SiC657 | 5 V PWM optimized |
| SiC657DB | Reference board | | |

## PART MARKING INFORMATION




| | | |
|---|---|---|
| ● | = | Pin 1 Indicator |
| P/N | = | Part Number Code |
| | = | Siliconix Logo |
| △ | = | ESD Symbol |
| F | = | Assembly Factory Code |
| Y | = | Year Code |
| WW | = | Week Code |
| LL | = | Lot Code |

## ABSOLUTE MAXIMUM RATINGS

| ELECTRICAL PARAMETER | CONDITIONS | LIMIT | UNIT |
|---|---|---|---|
| Input voltage | $V_{IN}$ | -0.3 to +28 | V |
| Control logic supply voltage | $V_{CIN}$ | -0.3 to +7 | |
| Drive supply voltage | $V_{DRV}$ | -0.3 to +7 | |
| Switch node (DC voltage) | $V_{SWH}$ | -0.3 to +28 | |
| Switch node (AC voltage) (1) | | -7 to +35 | |
| BOOT voltage (DC voltage) | $V_{BOOT}$ | 33 | |
| BOOT voltage (AC voltage) (2) | | 40 | |
| BOOT to PHASE (DC voltage) | $V_{BOOT-PHASE}$ | -0.3 to +7 | |
| BOOT to PHASE (AC voltage) (3) | | -0.3 to +8 | |
| All logic inputs and outputs (PWM, ZCD_EN#) | | -0.3 to $V_{CIN}$ +0.3 | |
| Max. operating junction temperature | $T_J$ | 150 | °C |
| Ambient temperature | $T_A$ | -40 to +125 | |
| Storage temperature | $T_{stg}$ | -65 to +150 | |
| Electrostatic discharge protection | Human body model, JESD22-A114 | 2000 | V |
| | Charged device model, JESD22-C101 | 1000 | |

**Notes**

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

(1) The specification values indicated “AC” is $V_{SWH}$ to $P_{GND}$ -8 V (< 20 ns, 10 µJ), min. and 35 V (< 50 ns), max.
(2) The specification value indicates “AC voltage” is $V_{BOOT}$ to $P_{GND}$, 40 V (< 50 ns) max.
(3) The specification value indicates “AC voltage” is $V_{BOOT}$ to $V_{PHASE}$, 8 V (< 50 ns) max.

## RECOMMENDED OPERATING RANGE

| ELECTRICAL PARAMETER | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|
| Input voltage ($V_{IN}$) | 4.5 | - | 24 | V |
| Drive supply voltage ($V_{DRV}$) | 4.5 | 5 | 5.5 | |
| Control logic supply voltage ($V_{CIN}$) | 4.5 | 5 | 5.5 | |
| BOOT to PHASE ($V_{BOOT-PHASE}$, DC voltage) | 4 | 4.5 | 5.5 | |
| Thermal resistance from junction to ambient | - | 10.6 | - | °C/W |
| Thermal resistance from junction to case | - | 1.6 | - | |

## ELECTRICAL SPECIFICATIONS

(ZCD_EN# = 5 V, $V_{IN}$ = 12 V, $V_{DRV}$ and $V_{CIN}$ = 5 V, $T_A$ = 25 °C, unless otherwise stated)

| PARAMETER | SYMBOL | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | |
| **POWER SUPPLY** | | | | | | |
| Control logic supply current | $I_{VCIN}$ | $V_{PWM}$ = FLOAT | - | 80 | - | µA |
| | | $V_{PWM}$ = FLOAT, $V_{ZCD\_EN\#}$ = 0 V | - | 120 | - | |
| | | $f_S$ = 300 kHz, D = 0.1 | - | 300 | - | |
| Drive supply current | $I_{VDRV}$ | $f_S$ = 300 kHz, D = 0.1 | - | 10 | 20 | mA |
| | | $f_S$ = 1 MHz, D = 0.1 | - | 30 | - | |
| PS4 mode supply current | $I_{VCIN}$ + $I_{VDRV}$ | $V_{PWM}$ = $V_{ZCD\_EN\#}$ = FLOAT, $T_A$ = -10 °C to +100 °C | - | 3 | 9 | µA |
| **BOOTSTRAP SUPPLY** | | | | | | |
| Bootstrap diode forward voltage | $V_F$ | $I_F$ = 2 mA | - | - | 0.65 | V |
| **PWM CONTROL INPUT** | | | | | | |
| Rising threshold | $V_{TH\_PWM\_R}$ | | 3.6 | 3.9 | 4.2 | V |
| Falling threshold | $V_{TH\_PWM\_F}$ | | 0.72 | 1 | 1.3 | |
| Tri-state voltage | $V_{TRI}$ | $V_{PWM}$ = FLOAT | - | 2.5 | - | |
| Tri-state rising threshold | $V_{TRI\_TH\_R}$ | | 1.1 | 1.35 | 1.6 | |
| Tri-state falling threshold | $V_{TRI\_TH\_F}$ | | 3.4 | 3.7 | 4 | |
| Tri-state rising threshold hysteresis | $V_{HYS\_TRI\_R}$ | | - | 325 | - | mV |
| Tri-state falling threshold hysteresis | $V_{HYS\_TRI\_F}$ | | - | 250 | - | |
| PWM input current | $I_{PWM}$ | $V_{PWM}$ = 5 V | - | - | 350 | µA |
| | | $V_{PWM}$ = 0 V | - | - | -350 | |
| **ZCD_EN# CONTROL INPUT** | | | | | | |
| Rising threshold | $V_{TH\_ZCD\_EN\#\_R}$ | | 3.3 | 3.6 | 3.9 | V |
| Falling threshold | $V_{TH\_ZCD\_EN\#\_F}$ | | 1.1 | 1.4 | 1.7 | |
| Tri-state voltage | $V_{TRI\_ZCD\_EN\#}$ | $V_{ZCD\_EN\#}$ = FLOAT | - | 2.5 | - | |
| Tri-state rising threshold | $V_{TRI\_ZCD\_EN\#\_R}$ | | 1.5 | 1.8 | 2.1 | |
| Tri-state falling threshold | $V_{TRI\_ZCD\_EN\#\_F}$ | | 2.9 | 3.15 | 3.4 | |
| Tri-state rising threshold hysteresis | $V_{HYS\_TRI\_ZCD\#\_R}$ | | - | 375 | - | mV |
| Tri-state falling threshold hysteresis | $V_{HYS\_TRI\_ZCD\#\_F}$ | | - | 450 | - | |
| ZCD_EN# input current | $I_{ZCD\_EN\#}$ | $V_{ZCD\_EN\#}$ = 5 V | - | - | 100 | µA |
| | | $V_{ZCD\_EN\#}$ = 0 V | - | - | -100 | |
| PS4 exit latency | $t_{PS4EXIT}$ | | - | - | 5 | µs |
| **TIMING SPECIFICATIONS** | | | | | | |
| Tri-state to GH/GL rising propagation delay | $t_{PD\_TRI\_R}$ | No load, see fig. 4 | - | 20 | - | ns |
| Tri-state hold-off time | $t_{TSHO}$ | | - | 150 | - | |
| GH - turn off propagation delay | $t_{PD\_OFF\_GH}$ | | - | 20 | - | |
| GH - turn on propagation delay (dead time rising) | $t_{PD\_ON\_GH}$ | | - | 15 | - | |
| GL - turn off propagation delay | $t_{PD\_OFF\_GL}$ | | - | 20 | - | |
| GL - turn on propagation delay (dead time falling) | $t_{PD\_ON\_GL}$ | | - | 20 | - | |
| PWM minimum on-time | $t_{PWM\_ON\_MIN.}$ | | 30 | - | - | |
| **PROTECTION** | | | | | | |
| Under voltage lockout | $V_{UVLO}$ | $V_{CIN}$ rising, on threshold | - | 3.4 | 3.9 | V |
| | | $V_{CIN}$ falling, off threshold | 2.4 | 2.9 | - | |
| Under voltage lockout hysteresis | $V_{UVLO\_HYST}$ | | - | 500 | - | mV |

**Notes**

(1) Typical limits are established by characterization and are not production tested

(2) Guaranteed by design

## DETAILED OPERATIONAL DESCRIPTION

### PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{PWM\_TH\_R}$ the low side is turned ON and the high side is turned ON. When PWM input is driven below $V_{PWM\_TH\_F}$ the high side is turned OFF and the low side is turned ON. For tri-state logic, the PWM input operates as previously stated for driving the MOSFETs when PWM is logic high and logic low. However, there is an third state that is entered as the PWM output of tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC657 to pull the PWM input into the tri-state region (see definition of PWM logic and tri-state, fig. 4). If the PWM input stays in this region for the tri-state hold-off period, $t_{TSHO}$, both high side and low side MOSFETs are turned OFF. The function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC657 incorporates PWM voltage thresholds that are compatible with 5 V.

### Diode Emulation Mode and PS4 Mode (ZCD_EN#)

The ZCD_EN# pin enables or disables diode emulation mode. When ZCD_EN# is driven below $V_{TH\_ZCD\_EN\#\_F}$, diode emulation is allowed. When ZCD_EN# is driven above $V_{TH\_ZCD\_EN\#\_R}$, continuous conduction mode is forced. Diode emulation mode allows for higher converter efficiency under light load situations. With diode emulation active, the SiC657 will detect the zero current crossing of the output inductor and turn off the low side MOSFET. This ensures that discontinuous conduction mode (DCM) is achieved. Diode emulation is asynchronous to the PWM signal, therefore, the SiC657 will respond to the ZCD_EN# input immediately after it changes state.

The ZCD_EN# pin can be floated resulting in a high impedance state. High impedance on the input of ZCD_EN# combined with a tri-stated PWM output will shut down the SiC657, reducing current consumption to typically 5 µA. This is an important feature in achieving the low standby current requirements required in the PS4 state in ultrabooks and notebooks.

### Voltage Input ($V_{IN}$)

This is the power input to the drain of the high side power MOSFET. This pin is connected to the high power intermediate BUS rail.

### Switch Node ($V_{SWH}$ and PHASE)

The switch node, $V_{SWH}$, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node $V_{SWH}$. This pin is to be used exclusively as the return pin for the BOOT capacitor.

### Ground Connections ($C_{GND}$ and $P_{GND}$)

$P_{GND}$ (power ground) should be externally connected to $C_{GND}$ (control signal ground). The layout of the printed circuit board should be such that the inductance separating $C_{GND}$ and $P_{GND}$ is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V

### Control and Drive Supply Voltage Input ($V_{DRV}$, $V_{CIN}$)

$V_{CIN}$ is the bias supply for the gate drive control IC. $V_{DRV}$ is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

### Bootstrap Circuit (BOOT)

The internal bootstrap diode and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

### Shoot-Through Protection and Adaptive Dead Time

The SiC657 has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high side and low side MOSFETs are not turned ON at the same time. The adaptive dead time control operates as follows. The high side and low side gate voltages are monitored to prevent the one turning ON from tuning ON until the other's gate voltage is sufficiently low (< 1 V). Built in delays also ensure that one power MOS is completely OFF, before the other can be turned ON. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

### Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high side and low side MOSFET gates low until the supply voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC657 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device.

## FUNCTIONAL BLOCK DIAGRAM

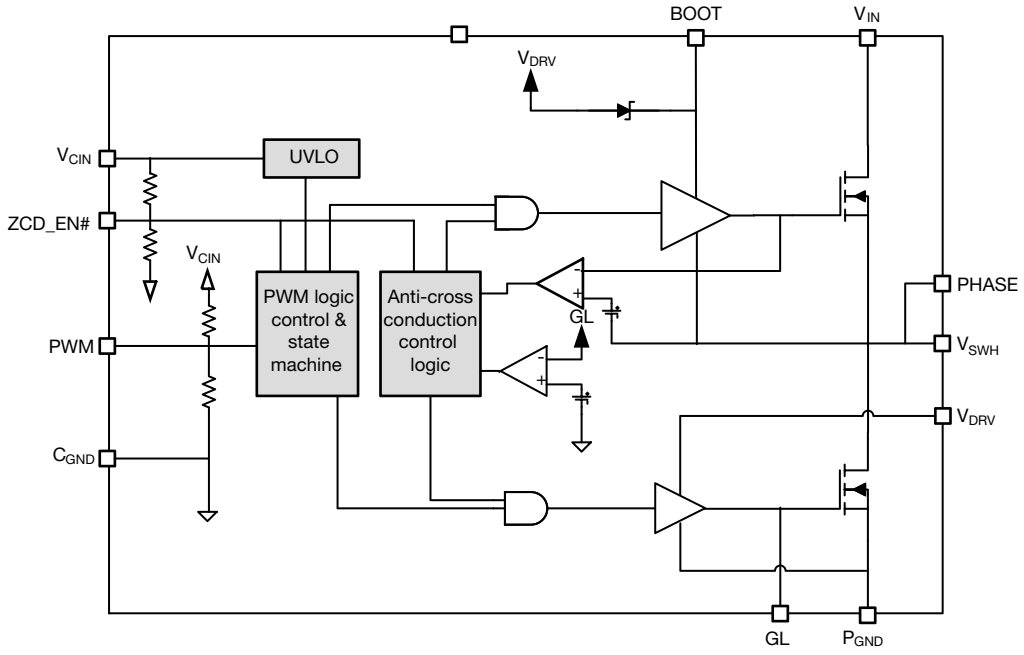



**Fig. 3 - Functional Block Diagram**

| DEVICE TRUTH TABLE | | | |
|---|---|---|---|
| **ZCD_EN#** | **PWM** | **GH** | **GL** |
| Tri-state | X | L | L |
| L | L | L | H, $I_L$ > 0 A<br>L, $I_L$ < 0 A |
| L | H | H | L |
| L | Tri-state | L | L |
| H | L | L | H |
| H | H | H | L |
| H | Tri-state | L | L |

## PWM TIMING DIAGRAM

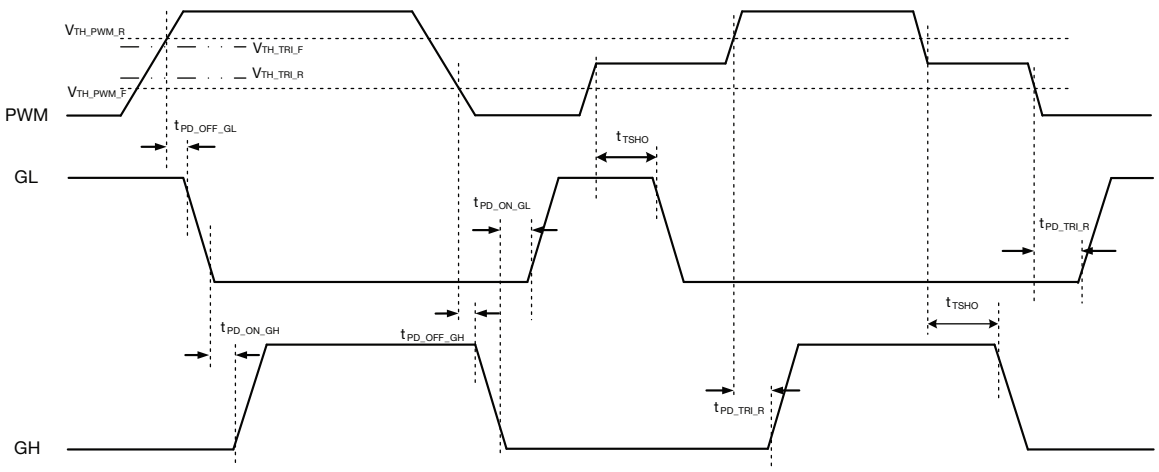



**Fig. 4 - Definition of PWM Logic and Tri-state**

## ZCD_EN# - PS4 EXIT TIMING

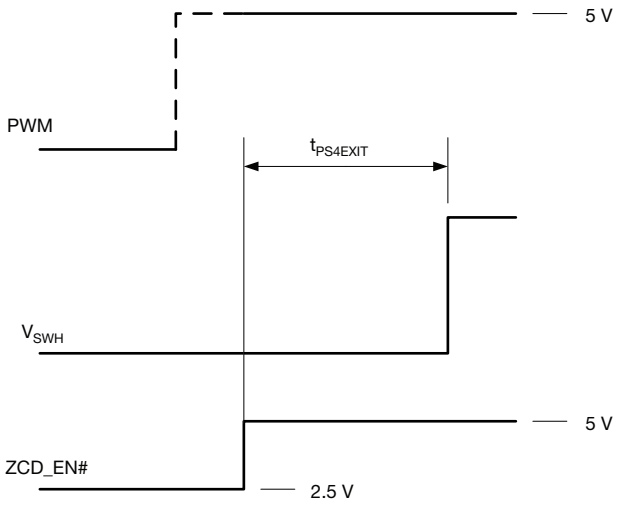



**Fig. 5 - ZCD_EN# - PS4 Exit Timing**

## ELECTRICAL CHARACTERISTICS

Test condition: $V_{IN}$ = 13 V (unless otherwise stated), $V_{DRV}$ = $V_{CIN}$ = 5 V, ZCD_EN# = 5 V, $V_{OUT}$ = 1 V, $L_{OUT}$ = 250 nH (DCR = 0.32 mΩ), $T_A$ = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC657 losses only unless otherwise stated)

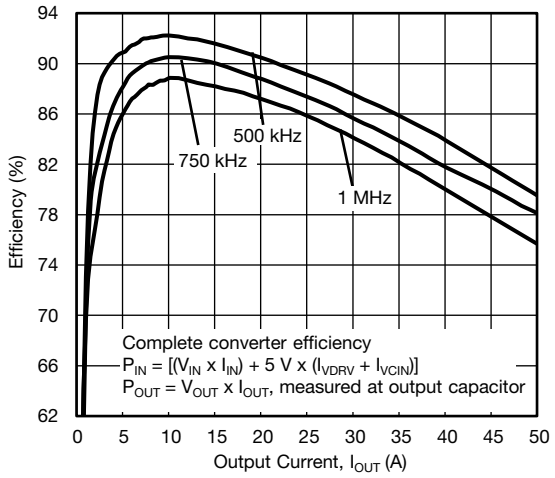



**Fig. 6 - Efficiency vs. Output Current ($V_{IN}$ = 12.6 V)**

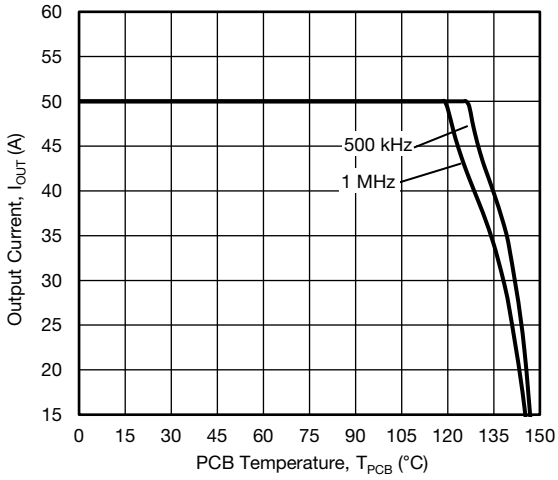



**Fig. 9 - Safe Operating Area ($V_{IN}$ = 12.6 V)**

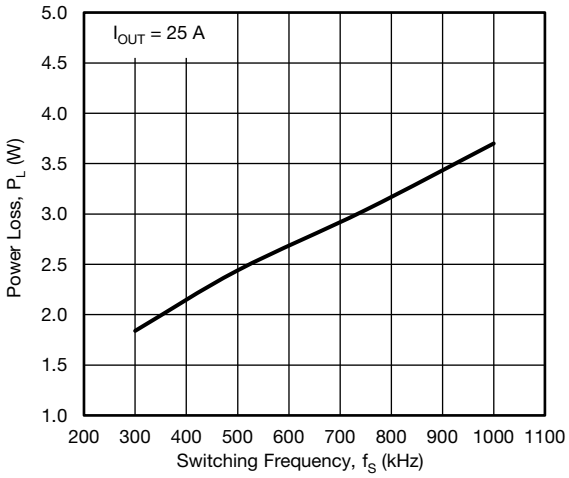



**Fig. 7 - Power Loss vs. Switching Frequency ($V_{IN}$ = 12.6 V)**

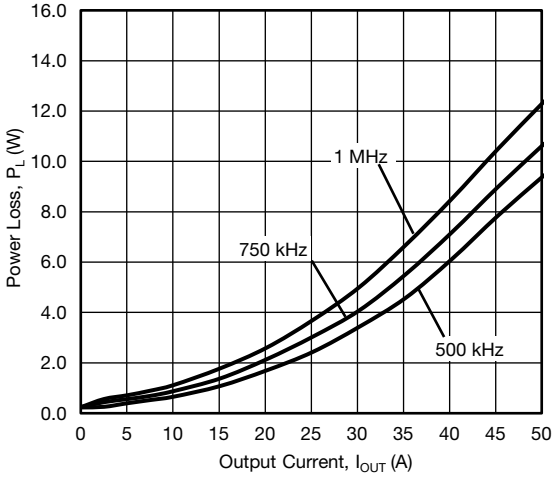



**Fig. 10 - Power Loss vs. Output Current ($V_{IN}$ = 12.6 V)**

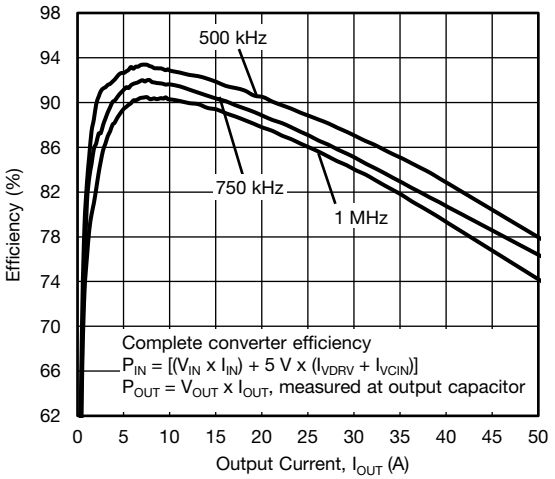



**Fig. 8 - Efficiency vs. Output Current ($V_{IN}$ = 9 V)**

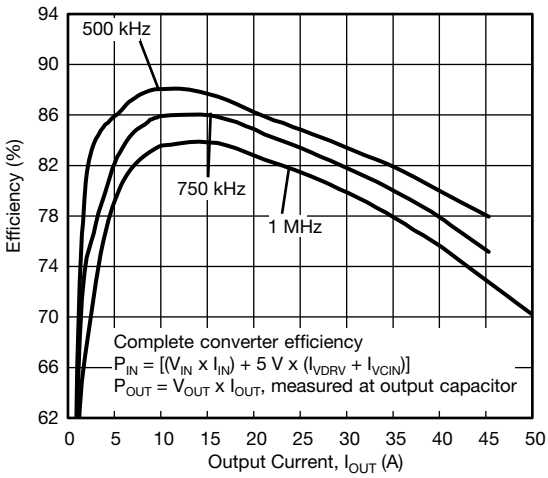



**Fig. 11 - Efficiency vs. Output Current ($V_{IN}$ = 19 V)**

## ELECTRICAL CHARACTERISTICS

Test condition: $V_{IN}$ = 13 V (unless otherwise stated), $V_{DRV}$ = $V_{CIN}$ = 5 V, ZCD_EN# = 5 V, $V_{OUT}$ = 1 V, $L_{OUT}$ = 250 nH (DCR = 0.32 mΩ), $T_A$ = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC657 losses only unless otherwise stated)

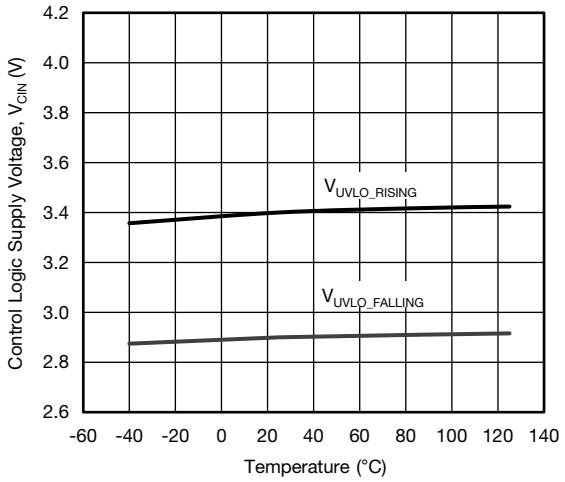



**Fig. 12 - UVLO Threshold vs. Temperature**

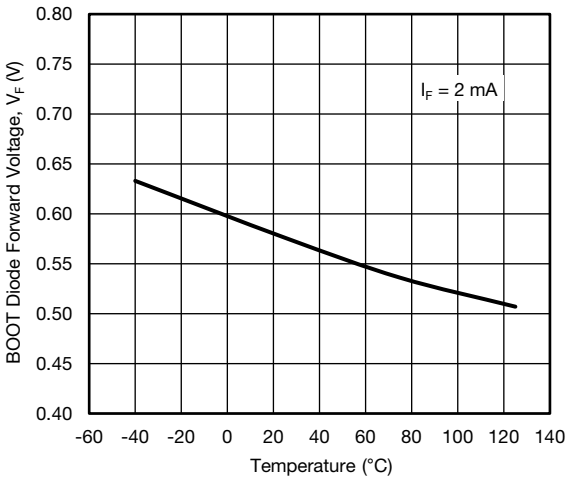



**Fig. 15 - BOOT Diode Forward Voltage vs. Temperature**

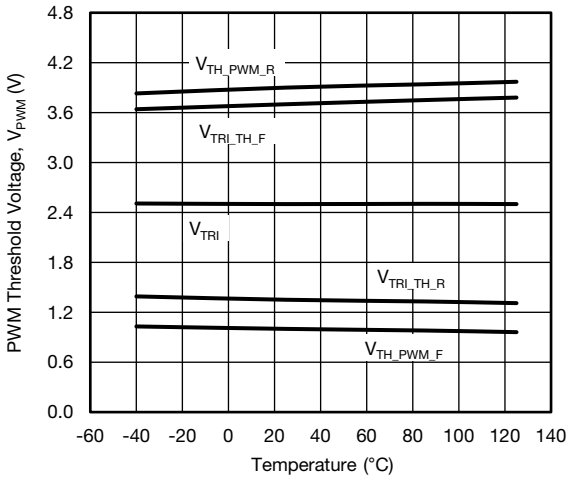



**Fig. 13 - PWM Threshold vs. Temperature**

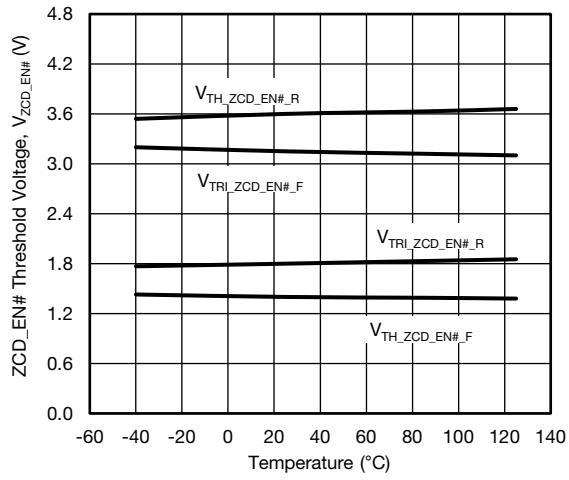



**Fig. 16 - ZCD_EN# Threshold vs. Temperature**

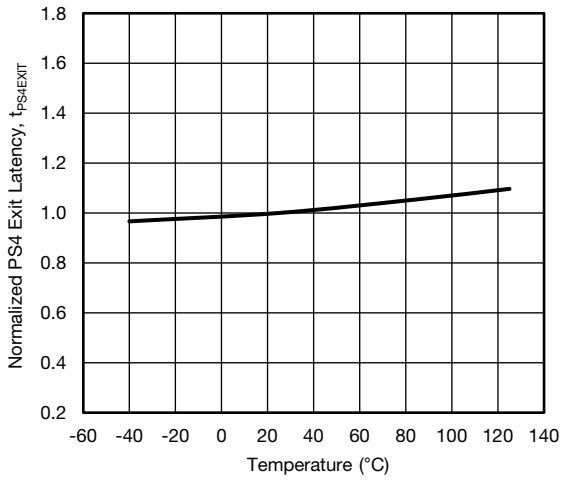



**Fig. 14 - PS4 Exit Latency vs. Temperature**

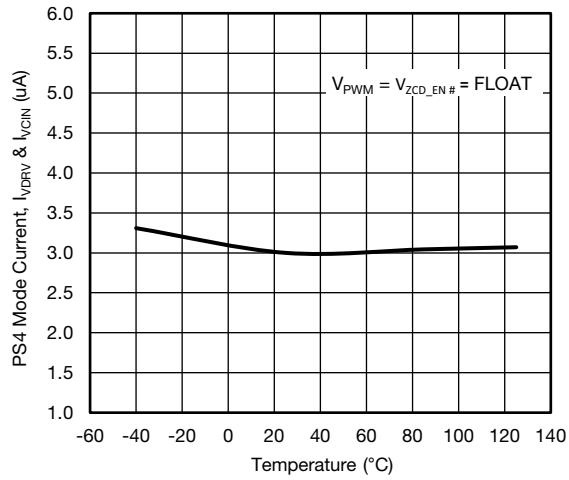
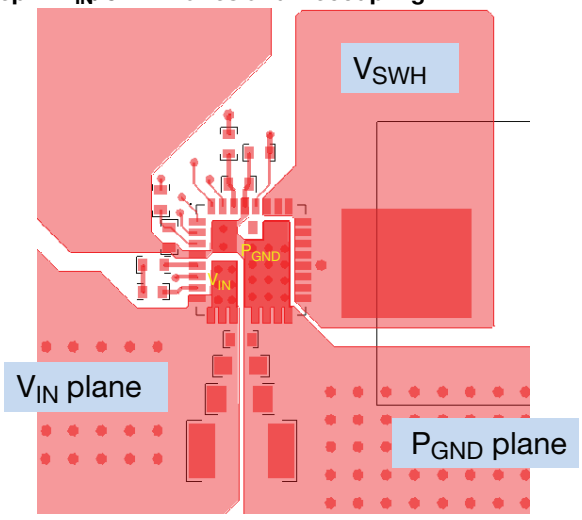



**Fig. 17 - PS4 Mode Current vs. Temperature**

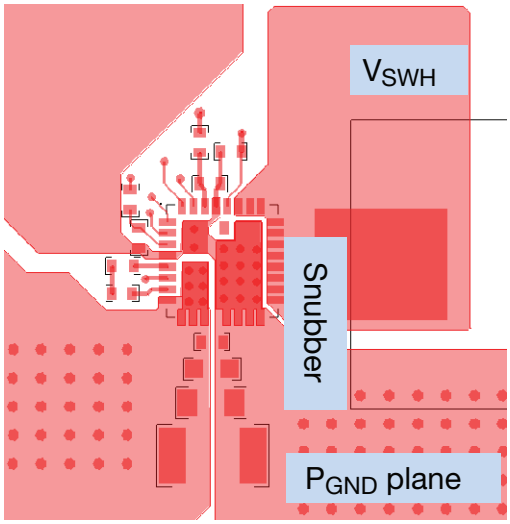
## PCB LAYOUT RECOMMENDATIONS

### Step 1: $V_{IN}$/GND Planes and Decoupling



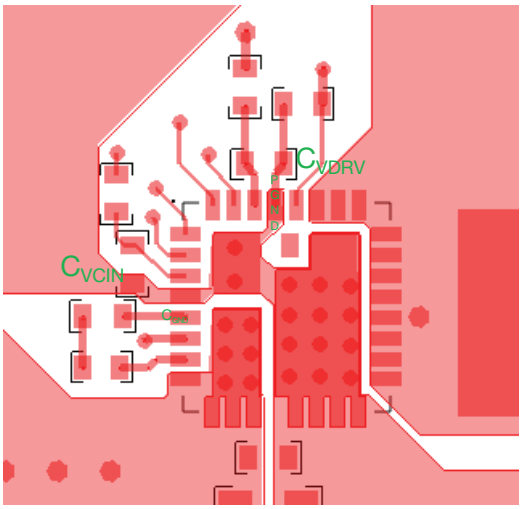

1. Layout $V_{IN}$ and $P_{GND}$ planes as shown above
2. Ceramic capacitors should be placed directly between $V_{IN}$ and $P_{GND}$, and close to the device for best decoupling effect
3. Different values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603 and 0402
4. Smaller capacitance values, closer to device $V_{IN}$ pin(s), - results in better high frequency noise absorbing

### Step 2: $V_{SWH}$ Plane



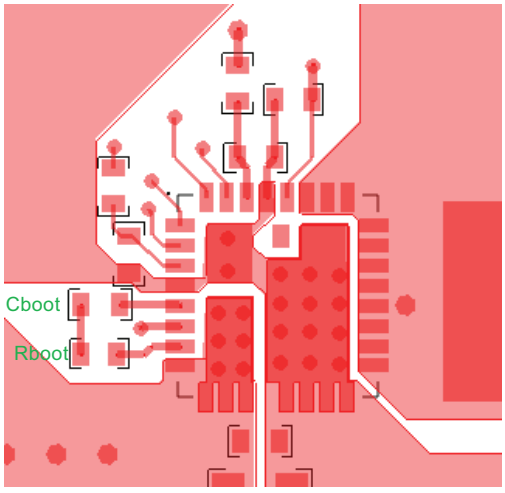

1. Connect output inductor to DrMOS with large plane to lower resistance
2. If a snubber network is required, place the components as shown above, the network can be placed at bottom

### Step 3: $V_{CIN}$/$V_{DRV}$ Input Filter



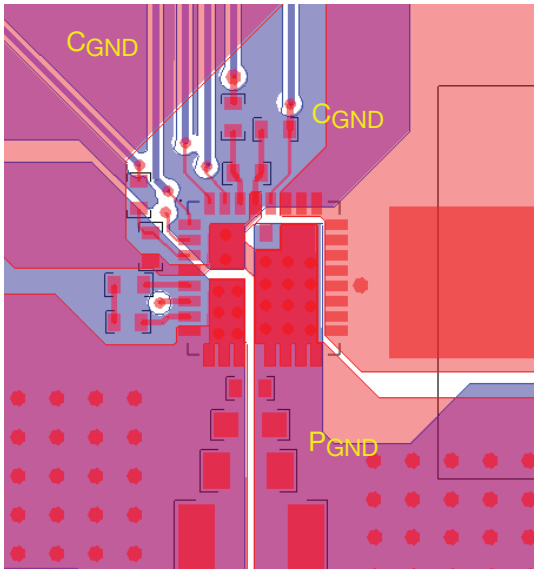

1. The $V_{CIN}$/$V_{DRV}$ input filter ceramic capacitors should be placed close to IC. It is recommended to connect two caps separately
2. $V_{CIN}$ capacitor should be placed between pin 3 ($V_{CIN}$) and pin 4 ($C_{GND}$ of driver IC) to achieve best noise filtering
3. $V_{DRV}$ capacitor should be placed between pin 28 ($P_{GND}$ of driver IC) and pin 29 ($V_{DRV}$) to provide maximum instantaneous driver current for low side MOSFET during switching cycle
4. It is recommended to use a large plane analog ground, $C_{GND}$, plane to reduce parasitic inductance

### Step 4: BOOT Resistor and Capacitor Placement



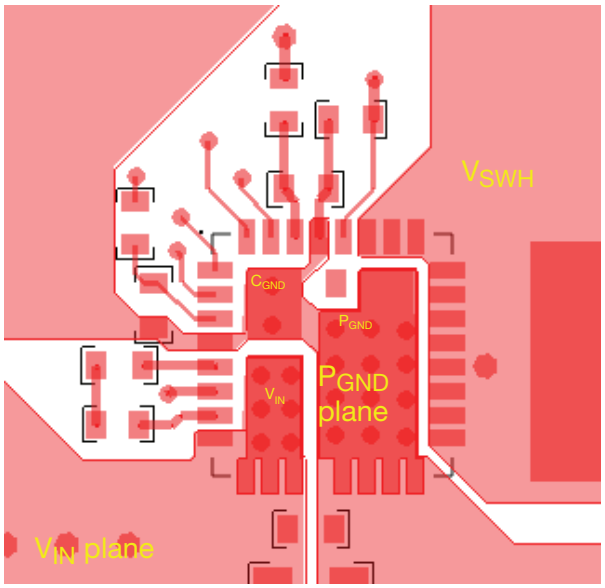

1. The components should be placed close to IC, directly between PHASE (pin 7) and BOOT (pin 5)
2. To reduce parasitic inductance, chip size 0402 can be used

**Step 5: Signal Routing**



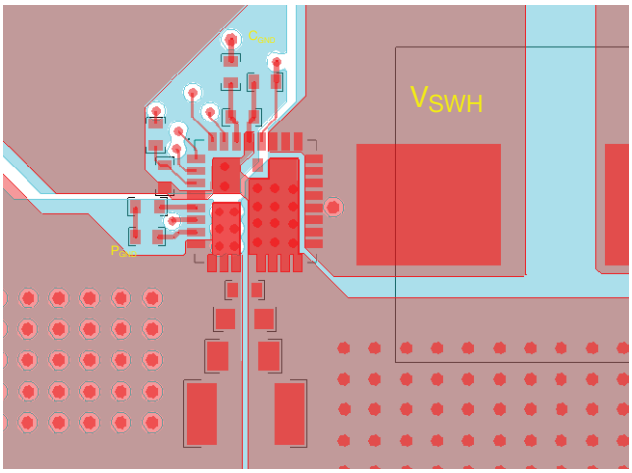

1. Route the PWM / ZCD_EN# signal traces out of the top left corner, next to DrMOS pin 1
2. PWM is an important signal, both signal and return traces should not cross any power nodes on any layer
3. It is best to “shield” traces form power switching nodes, e.g. $V_{SWH}$, to improve signal integrity
4. GL (pin 27) has been connected with GL pad internally and does not need to connect externally

**Step 6: Adding Thermal Relief Vias**




1. Thermal relief vias can be added on the $V_{IN}$ and $P_{GND}$ pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional vias can be added to $V_{IN}$ and $P_{GND}$ planes
3. $V_{SWH}$ pad is a noise source and not recommended to put vias on this plane
4. 8 mil vias for pads and 10 mils vias for planes are the optimal via sizes. Vias on pads may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline

**Step 7: Ground Connection**




1. It is recommended to make a single connection between $C_{GND}$ and $P_{GND}$, this connection can be done on top layer
2. It is recommended to make the entire first inner layer (next to top layer) a ground plane and separate it into $C_{GND}$ and $P_{GND}$ plane
3. These ground planes provide shielding between noise sources on top layer and signal traces on bottom layer

**Multi-Phases VRPower PCB Layout**

The following is an example of 6 phase layout. As can be seen, all the VRPower stages are lined in X-direction compactly with decoupling capacitors next to them. The inductors are placed as close as possible to the SiC657 to minimize the PCB copper loss. Vias are applied on all PADs ($V_{IN}$, $P_{GND}$, $C_{GND}$) of the SiC657 to ensure that both electrical and thermal performance are optimized. Large copper planes are used for all high current loops, such as $V_{IN}$, $V_{SWH}$, $V_{OUT}$ and $P_{GND}$. These copper planes are duplicated in other layers to minimize the inductance and resistance. All the control signals are routed from the SiC657 to a controller placed to the north of the power stage through inner layers to avoid the overlap of high current loops. This achieves a compact design with the output from the inductors feeding a load located to the south of the design as shown in the figure.

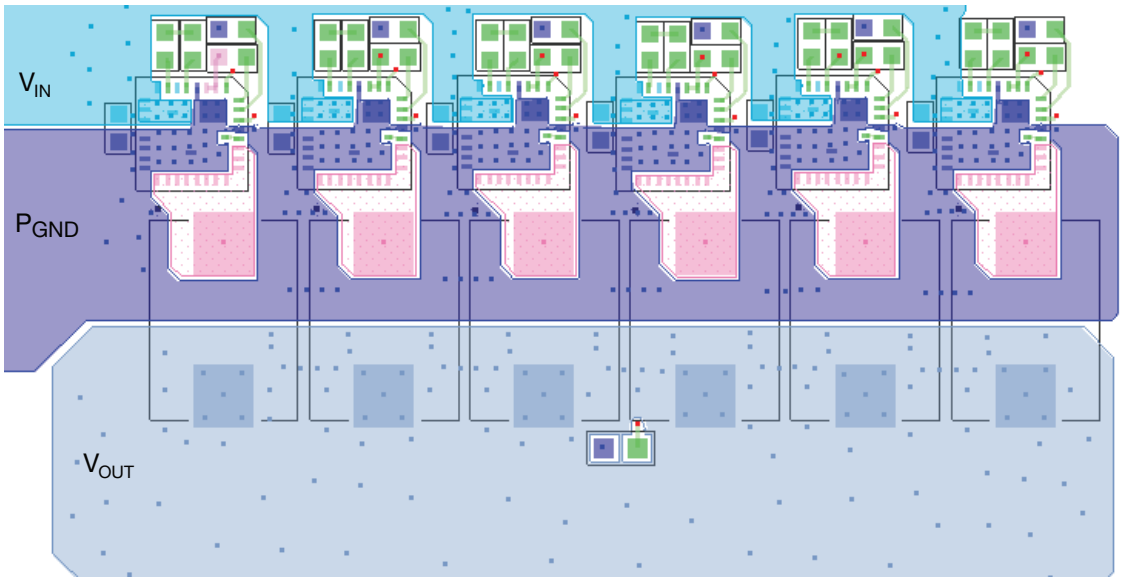



**Fig. 18 - Multi - Phase VRPower Layout Top View**

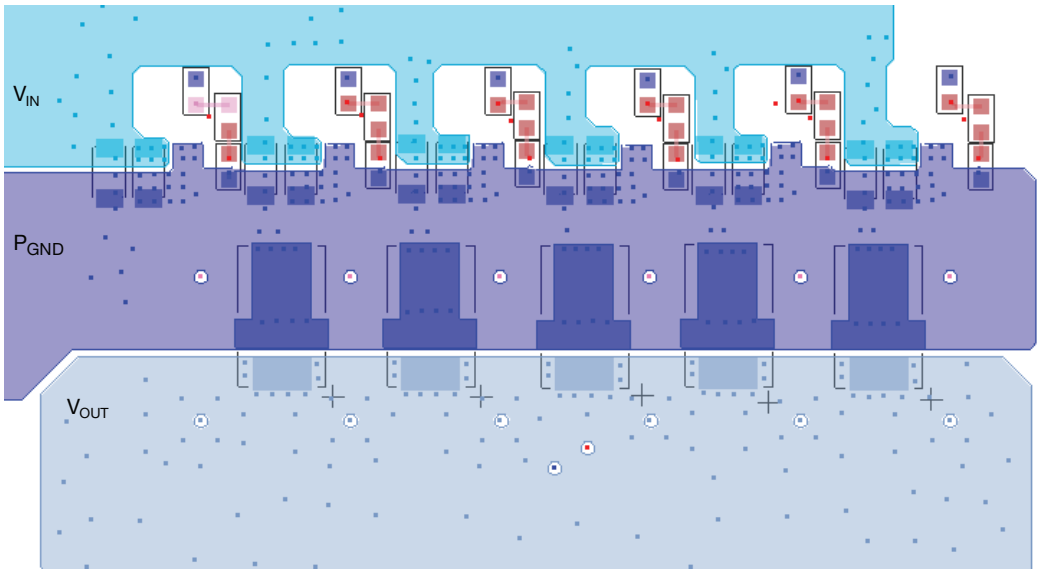



**Fig. 19 - Multi - Phase VRPower Layout Bottom View**

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