Microprocessor Supervisory Circuit

ADM1232A

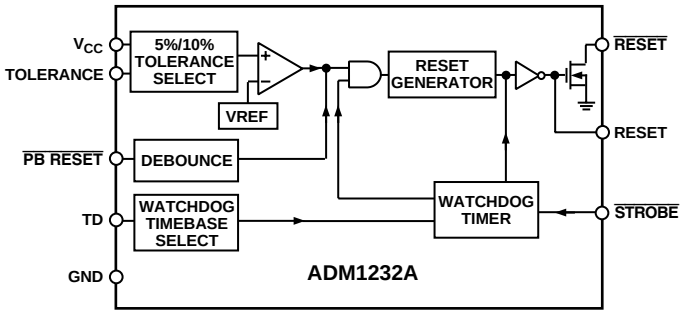
FEATURES

Superior Upgrade for MAX1232 and Dallas DS1232
Low Power Consumption (500 μA max)
Adjustable Precision Voltage Monitor with +4.5 V and +4.75 V Options
Adjustable STROBE Monitor with 150 ms, 600 ms or 1.2 sec Options
No External Components
Fast (20 ns) Strobe Pulsewidth

APPLICATIONS

Microprocessor Systems
Portable Equipment
Computers
Controllers
Intelligent Instruments
Automotive Systems
Protection Against Damage Caused by μP Failure

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM1232A is a superior, pin-compatible upgrade for the MAX1232 and the DS1232LP and DS1232. The ADM1232A can detect strobe pulsewidths as narrow as 20 ns, making it compatible with high speed microprocessors. The Analog Devices ADM1232A is a microprocessor monitoring circuit that can monitor:

1. Microprocessor Supply Voltage.
2. Whether a Microprocessor has locked up.
3. An External Interrupt.

The ADM1232A is available in four different packages:

1. The ADM1232AARM in an 8-lead μSOIC (RM-8).
2. The ADM1232AAN in an 8-lead PDIP (N-8).
3. The ADM1232AARW in a 16-lead wide SOIC (R-16).
4. The ADM1232AARN is an 8-lead narrow SOIC (R-8).

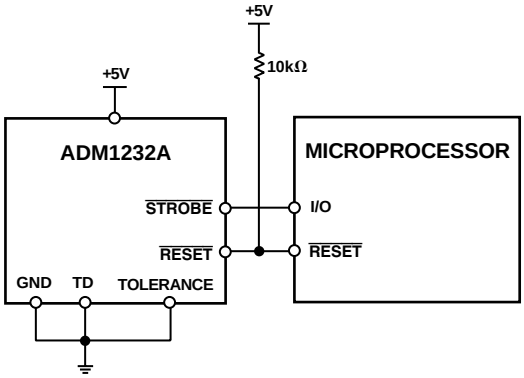


Figure 1. Typical Supply Monitoring Application

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ADM1232A–SPECIFICATIONS (V_{CC} = Full Operating Range, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
TEMPERATURE	–40		+85	°C	$T_A = T_{MIN}$ to T_{MAX}
POWER SUPPLY					
Voltage	4.5	5.0	5.5	V	
Current		20	50	µA	V_{IL}, V_{IH} = CMOS Levels
		200	500	µA	V_{IL}, V_{IH} = TTL Levels
$\overline{\text{STROBE}}$ AND $\overline{\text{PB RESET}}$ INPUTS					
Input High Level	2.0		V_{CC} + 0.3	V	
Input Low Level	–0.3		+0.8	V	
INPUT LEAKAGE CURRENT					
($\overline{\text{STROBE}}$, TOLERANCE)	–1.0		+1.0	µA	
TD		1.6		µA	
OUTPUT CURRENT					
$\overline{\text{RESET}}$	8	10		mA	When V_{CC} Is at 4.5 V–5.5 V
$\overline{\text{RESET}}$, RESET	–8	–12		mA	When V_{CC} Is at 4.5 V–5.5 V
OUTPUT VOLTAGE					
$\overline{\text{RESET}}$/RESET	V_{CC} – 0.5	V_{CC} – 0.1		V	While sourcing less than 500 µA, RESET remains within 0.5 V of V_{CC} on power-down until V_{CC} drops below 2.0 V. While sinking less than 500 µA, $\overline{\text{RESET}}$ remains within 0.5 V of GND on power-down until V_{CC} drops below 2.0 V.
$\overline{\text{RESET}}$/RESET High Level			0.4	V	
$\overline{\text{RESET}}$/RESET Low Level	2.4			V	
1 V OPERATION					
RESET Output Voltage		V_{CC} – 0.1		V	While Sourcing Less than 50 µA
$\overline{\text{RESET}}$ Output Voltage		0.1		V	While Sinking Less than 50 µA
V_{CC} TRIP POINT					
5%	4.5	4.62	4.74	V	TOLERANCE = GND
10%	4.25	4.37	4.49	V	TOLERANCE = V_{CC}
CAPACITANCE					
Input ($\overline{\text{STROBE}}$, TOLERANCE)			5	pF	T_A = +25°C
Output (RESET, $\overline{\text{RESET}}$)			7	pF	T_A = +25°C
$\overline{\text{PB RESET}}$					
Time	20			ms	$\overline{\text{PB RESET}}$ Must Be Held Low for a Minimum
Delay	1	4	20	ms	of 20 ms to Guarantee a Reset
RESET ACTIVE TIME	250	610	1000	ms	
$\overline{\text{STROBE}}$					
Pulsewidth	20			ns	
Timeout Period	62.5	150	250	ms	TD = 0 V
	250	600	1000	ms	TD = Floating
	500	1200	2000	ms	TD = V_{CC}
V_{CC}					
Fall Time	10			µs	Guaranteed by Design
Rise Time	0			µs	Guaranteed by Design
V_{CC} FAIL DETECT TO RESET OUTPUT DELAY					
RESET AND $\overline{\text{RESET}}$ Are Logically Correct			50	µs	After V_{CC} Falls Below the Set Tolerance Voltage (Figure 5)
	250	610	1000	ms	After V_{CC} Rises Above the Set Tolerance Voltage

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{CC} . . . . . +5.5 V
Logic Inputs . . . . . –0.3 V to V_{CC} + 0.3 V
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

N-8
Power Dissipation . . . . . 1000 mW
Derate by 13.5 mW/°C above 25°C
θ_{JA} Thermal Impedance . . . . . 100°C/W

R-16
Power Dissipation . . . . . 900 mW
Derate by 12 mW/°C above 25°C
θ_{JA} Thermal Impedance (Still Air) . . . . . 73°C/W

RM-8
Power Dissipation . . . . . 900 mW
Derate by 12 mW/°C above 25°C
θ_{JA} Thermal Impedance (Still Air) . . . . . 206°C/W

R-8
Power Dissipation . . . . . 900 µW
Derate by 12 mW/°C above 25°C
θ_{JA} Thermal Impedance (Still Air) . . . . . 153°C/W

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Options*
ADM1232AARM	–40°C to +85°C	RM-8
ADM1232AAN	–40°C to +85°C	N-8
ADM1232AARW	–40°C to +85°C	R-16
ADM1232AARN	–40°C to +85°C	R-8

*N = Plastic DIP; R = Small Outline; RM = µSOIC.

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1232A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

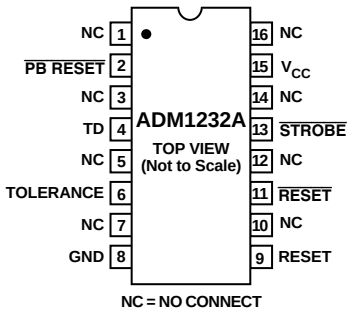


PIN FUNCTION DESCRIPTIONS

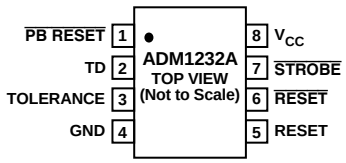
Mnemonic	Function
$\overline{\text{PB RESET}}$	Push Button Reset Input. This debounced input will ignore pulses of less than 1 ms and is guaranteed to respond to pulses greater than 20 ms.
TD	Time Delay Set allows the user to select the maximum amount of time the ADM1232A will allow the $\overline{\text{STROBE}}$ input to remain inactive (i.e., $\overline{\text{STROBE}}$ is not receiving any high-to-low transitions), without forcing the ADM1232A to generate a RESET pulse. (See $\overline{\text{STROBE}}$ specifications, Figure 4 and the note on $\overline{\text{STROBE}}$ timeout selection.)
TOLERANCE	Tolerance Input. This input will determine how much the supply voltage will be allowed to decrease (as a percentage tolerance) before a RESET is asserted. Connect to V_{CC} for 10% and GND for 5%.
GND	0 V ground reference for all signals.
RESET	Active high logic output. Will be asserted when: 1. V_{CC} decreases below the amount specified by the TOLERANCE input or, 2. $\overline{\text{PB RESET}}$ is forced low or, 3. If there are no high-to-low transitions within the limits set by TD at $\overline{\text{STROBE}}$ or, 4. During power-up.
$\overline{\text{RESET}}$	Inverse of RESET, with an open drain output.
$\overline{\text{STROBE}}$	The $\overline{\text{STROBE}}$ input is used to monitor the activity of a microprocessor. If there are no high-to-low transitions within the time specified by TD, a reset will be asserted.
V_{CC}	Power supply input +5 V.

PIN CONFIGURATIONS

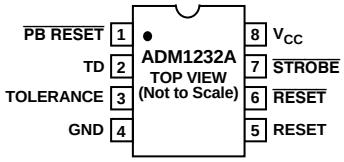
R-16



RM-8



N-8 and R-8



CIRCUIT INFORMATION

PB RESET

The PB RESET input makes it possible to manually reset a system using either a standard push-button switch or a logic low input. An internal debounce circuit provides glitch immunity when used with a switch, reducing the effects of glitches on the line. The debounce circuit is guaranteed to cause the ADM1232A to assert a reset if PB RESET is brought low for more than 20 ms and is guaranteed to ignore low inputs of less than 1 ms.

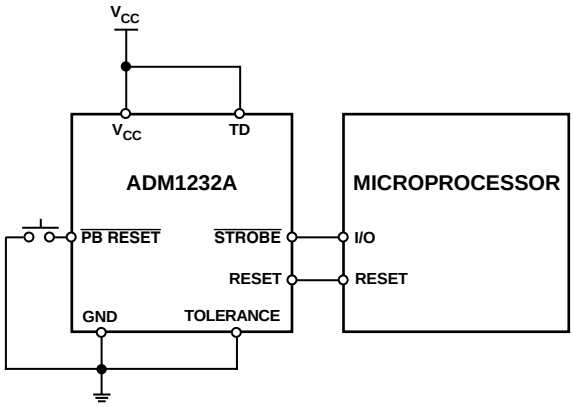


Figure 2. Typical Push Button Reset Application

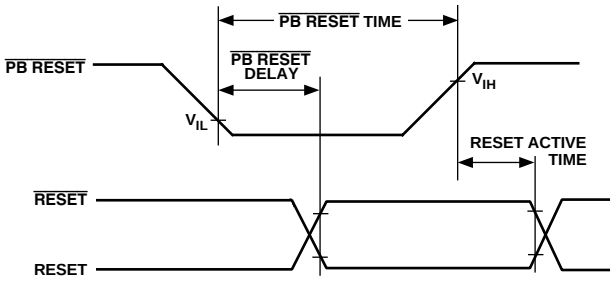


Figure 3. PB RESET

STROBE Timeout Selection

TD or time delay set is used to set the Strobe Timeout Period. The Strobe Timeout Period is defined as being the maximum time between high-to-low transitions (Figure 4) that STROBE will accept before a reset will be asserted. The Strobe timeout settings are listed in Table I.

Table I.

Condition	Min	Typ	Max	Units
TD = 0 V	62.5	150	250	ms
TD = Floating	250	600	1000	ms
TD = V_{CC}	500	1200	2000	ms

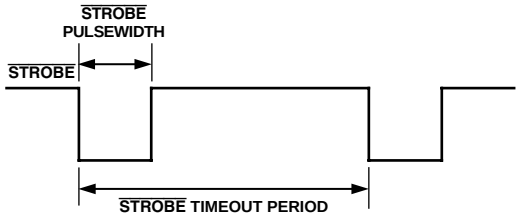


Figure 4. STROBE Parameters

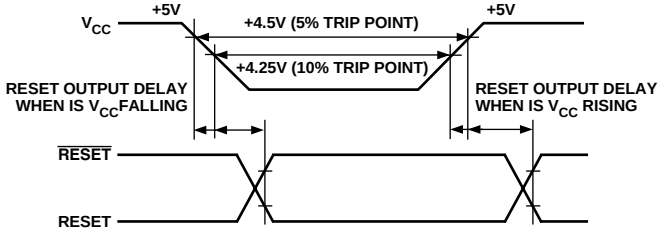


Figure 5. Reset Output Delay

TOLERANCE

The TOLERANCE input is used to determine the level V_{CC} can vary below 5 V without the ADM1232A asserting a reset. Connecting TOLERANCE to ground will select a –5% tolerance level and will cause the ADM1232A to generate a reset if V_{CC} falls below 4.75 V (typical). If TOLERANCE is connected to V_{CC} a –10% tolerance level is selected and will cause the ADM1232A to generate a reset if V_{CC} falls below 4.5 V (typical). Check the parameters for the V_{CC} trip point in the ADM1232A Specifications for more information.

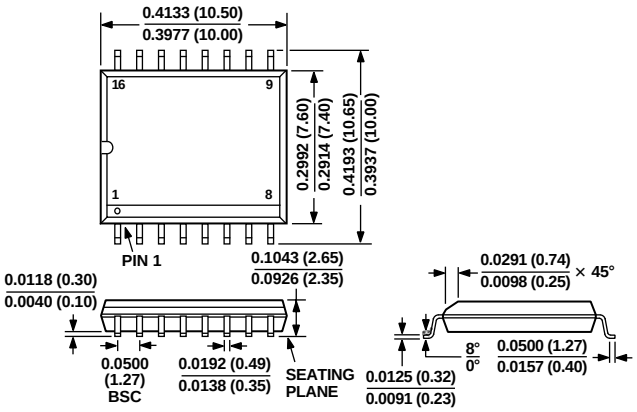
RESET AND RESET OUTPUTS

While RESET is capable of sourcing and sinking current, RESET is an open drain MOSFET which sinks current only. Therefore, it is necessary to pull this output high.

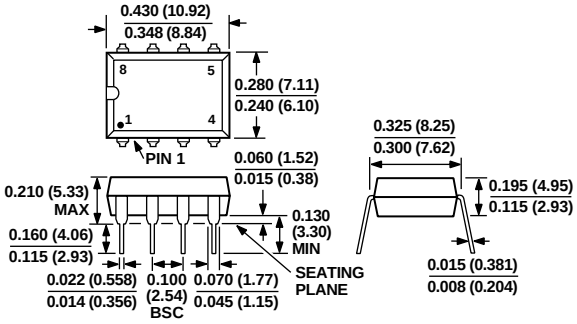
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

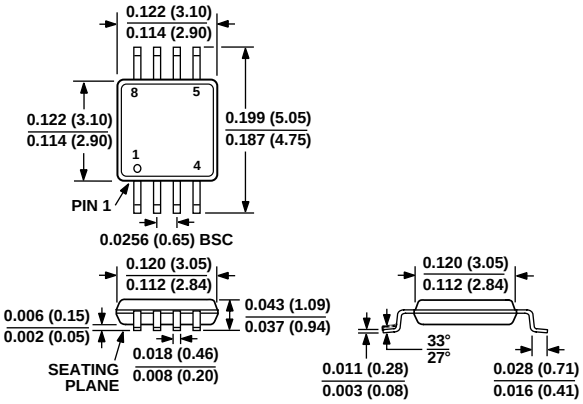
16-Lead Wide SOIC (R-16)



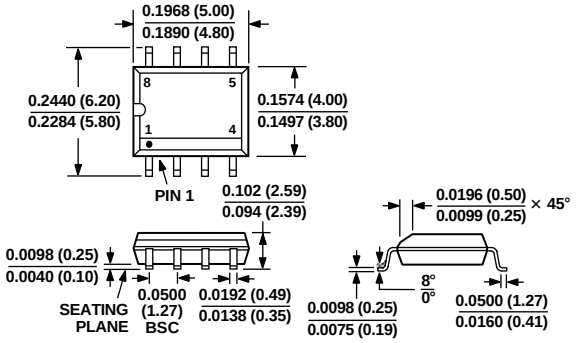
8-Lead PDIP (N-8)



8-Lead μSOIC (RM-8)



8-Lead Narrow SOIC (R-8)



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