

MC74HCU04A

Hex Unbuffered Inverter

High-Performance Silicon-Gate CMOS

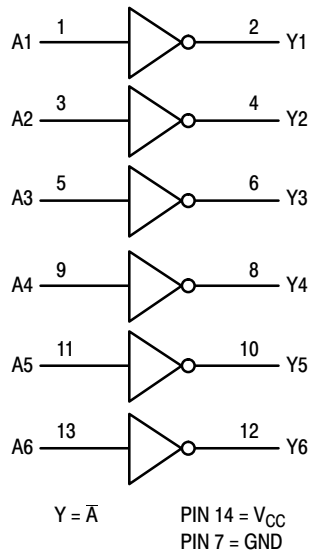
The MC74HCU04A is identical in pinout to the LS04 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single-stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high-input impedance amplifier. For digital applications, the HC04A is recommended.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V; 2.5 to 6.0 V in Oscillator Configurations
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 12 FETs or 3 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

LOGIC DIAGRAM



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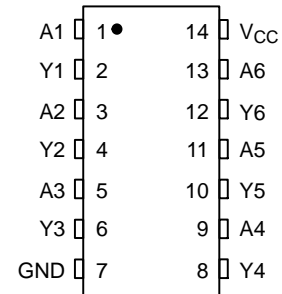


SOIC-14 NB
D SUFFIX
CASE 751A

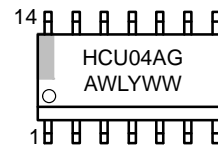


TSSOP-14
DT SUFFIX
CASE 948G

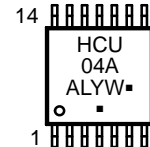
PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC-14 NB



TSSOP-14

- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs A | Outputs Y |
|-------------|--------------|
| L | H |
| H | L |

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MC74HCU04A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|--------------------------------------------------------------------------|------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air SOIC Package† TSSOP Package† | 500 450 | mW |
| T_{stg} | Storage Temperature | -65 to +150 | °C |
| T_L | Lead Temperature, 1 mm from case for 10 Seconds SOIC or TSSOP Package | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|------------------------------------------------------|-----|----------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t_r, t_f | Input Rise and Fall Time (Figure 1) | - | No Limit | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V_{CC} V | Guaranteed Limit | | | Unit |
|----------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------|---------------|------------------|--------|---------|------|
| | | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V_{IH} | Minimum High-Level Input Voltage | | 2.0 | 1.7 | 1.7 | 1.7 | V |
| | | | 3.0 | 2.5 | 2.5 | 2.5 | |
| | | | 4.5 | 3.6 | 3.6 | 3.6 | |
| | | | 6.0 | 4.8 | 4.8 | 4.8 | |
| V_{IL} | Maximum Low-Level Input Voltage | | 2.0 | 0.3 | 0.3 | 0.3 | V |
| | | | 3.0 | 0.5 | 0.5 | 0.5 | |
| | | | 4.5 | 0.8 | 0.8 | 0.8 | |
| | | | 6.0 | 1.1 | 1.1 | 1.1 | |
| V_{OH} | Minimum High-Level Output Voltage | $V_{in} = GND$ $ I_{out} \leq 20 \mu A$ | 2.0 | 1.8 | 1.8 | 1.8 | V |
| | | | 4.5 | 4.0 | 4.0 | 4.0 | |
| | | | 6.0 | 5.5 | 5.5 | 5.5 | |
| | | | | | | | |
| | | $V_{in} = GND$ $ I_{out} \leq 2.4 \text{ mA}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$ | 3.0 | 2.36 | 2.26 | 2.20 | |
| | | | 4.5 | 3.86 | 3.76 | 3.70 | |
| | | | 6.0 | 5.36 | 5.26 | 5.20 | |
| | | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For $V_{CC} = 2.0 \text{ V}$, $V_{out} = 0.2 \text{ V}$ or $V_{CC} - 0.2 \text{ V}$.

MC74HCU04A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) (continued)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
| | | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{CC} I _{out} ≤ 20 μA | 2.0 | 0.2 | 0.2 | 0.2 | V |
| | | | 4.5 | 0.5 | 0.5 | 0.5 | |
| | | | 6.0 | 0.5 | 0.5 | 0.5 | |
| | | V _{in} = V _{CC} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA | 3.0 | 0.32 | 0.32 | 0.32 | |
| | | | 4.5 | 0.32 | 0.37 | 0.40 | |
| | | | 6.0 | 0.32 | 0.37 | 0.40 | |
| | | | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| | | | 6.0 | 1 | 10 | 40 | |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 1 | 10 | 40 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For V_{CC} = 2.0 V, V_{out} = 0.2 V or V_{CC} - 0.2 V.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|----------------------------------------|---------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
| | | | -55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2) | 2.0 | 70 | 90 | 105 | ns |
| | | 3.0 | 40 | 45 | 50 | |
| | | 4.5 | 14 | 18 | 21 | |
| | | 6.0 | 12 | 15 | 18 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 2) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 27 | 32 | 36 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{in} | Maximum Input Capacitance | - | 10 | 10 | 10 | pF |

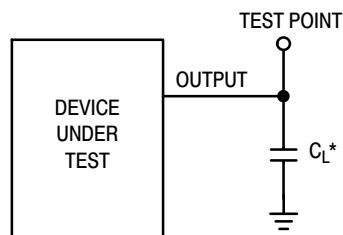
| C _{PD} | Power Dissipation Capacitance (Per Inverter)* | Typical @ 25°C, V _{CC} = 5.0 V | | | pF |
|-----------------|-----------------------------------------------|-----------------------------------------|--|--|----|
| | | 15 | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.



Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

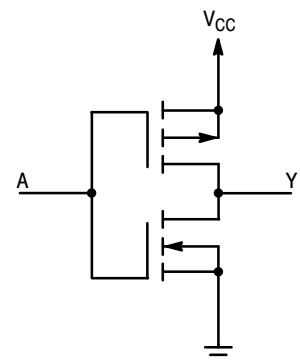


Figure 3. Logic Detail
(1/6 of Device Shown)

MC74HCU04A

TYPICAL APPLICATIONS

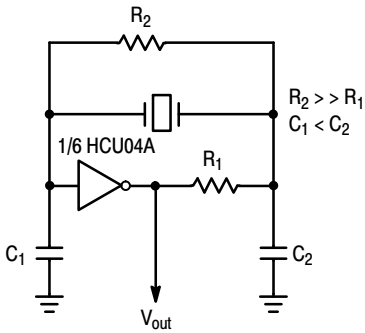


Figure 4. Crystal Oscillator

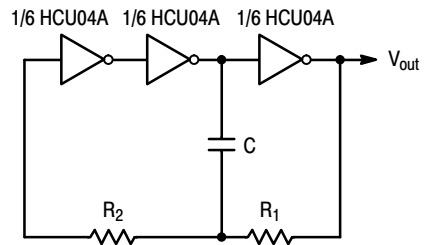


Figure 5. Stable RC Oscillator

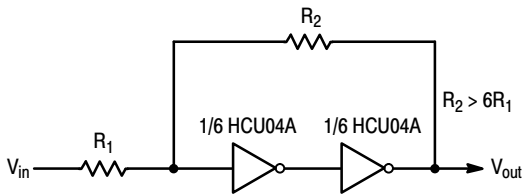


Figure 6. Schmitt Trigger

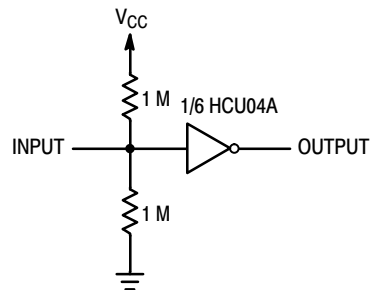


Figure 7. High Input Impedance Single-Stage Amplifier with a 2 to 6 V Supply Range

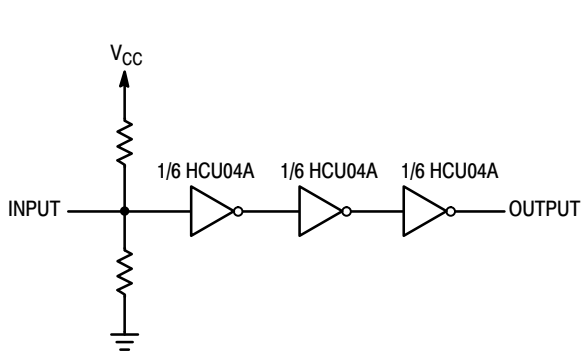
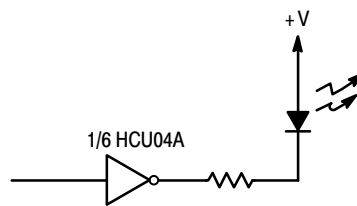


Figure 8. Multi-Stage Amplifier



For reduced power supply current, use high-efficiency LEDs such as the Hewlett-Packard HLMP series or equivalent.

Figure 9. LED Driver

MC74HCU04A

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------------|-------------------------|--------------------|
| MC74HCU04ADG | SOIC-14 NB (Pb-Free) | 55 Units / Rail |
| NLV74HCU04ADG* | SOIC-14 NB (Pb-Free) | 55 Units / Rail |
| MC74HCU04ADR2G | SOIC-14 NB (Pb-Free) | 2500 / Tape & Reel |
| NLV74HCU04ADR2G* | SOIC-14 NB (Pb-Free) | 2500 / Tape & Reel |
| MC74HCU04ADTR2G | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |
| NLV74HCU04ADTR2G* | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |

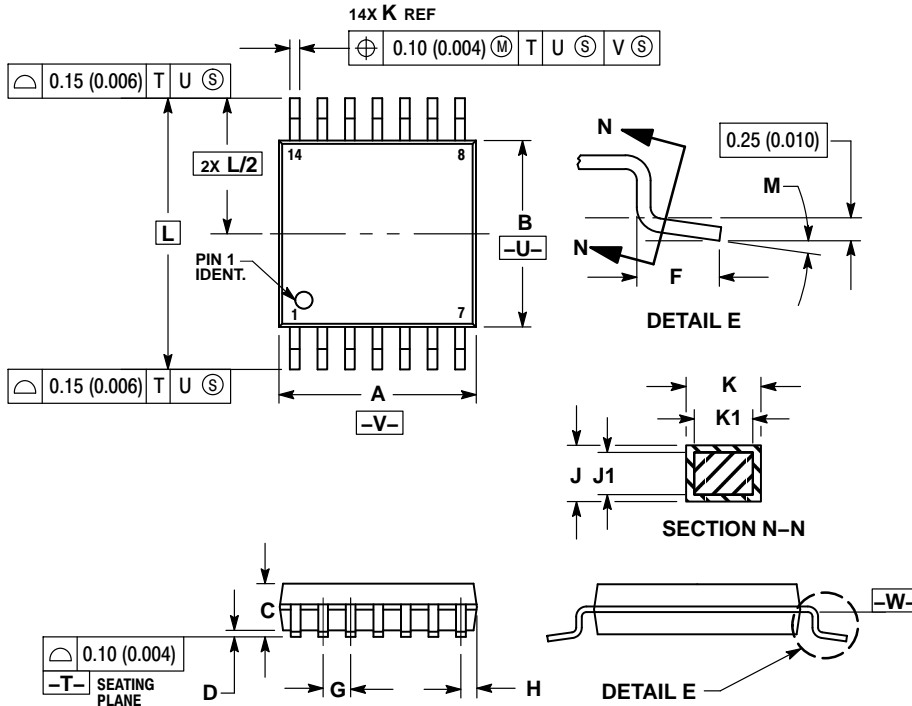
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC74HCU04A

PACKAGE DIMENSIONS

TSSOP-14
CASE 948G
ISSUE B

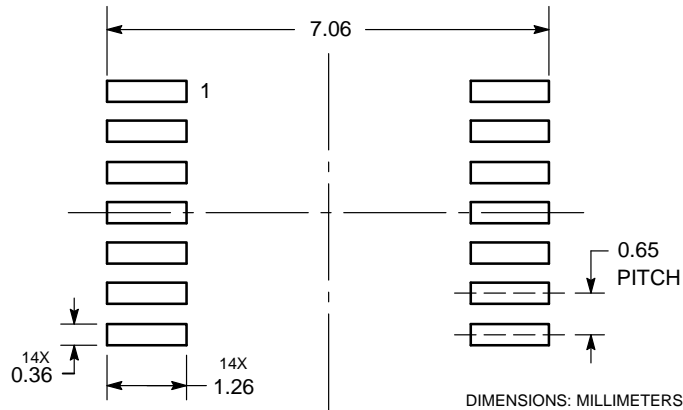


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*

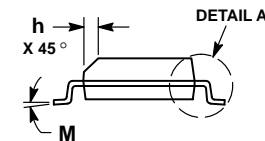
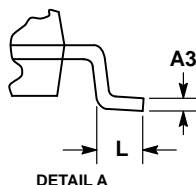
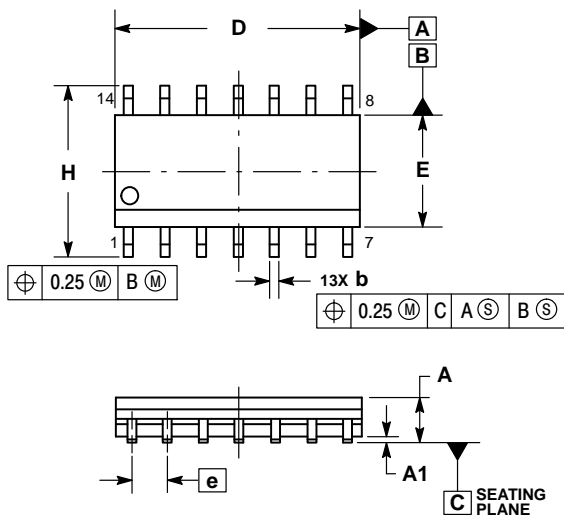


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HCU04A

PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 ISSUE K

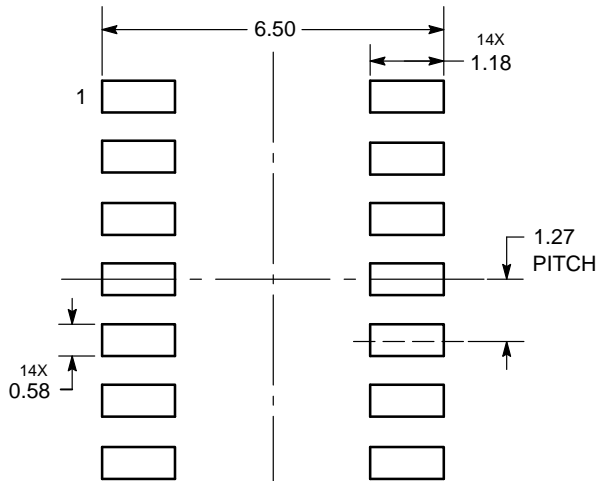


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | | 7° | |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
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- Тестирование поставляемой продукции.
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- Входной контроль качества.
- Наличие сертификата ISO.

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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