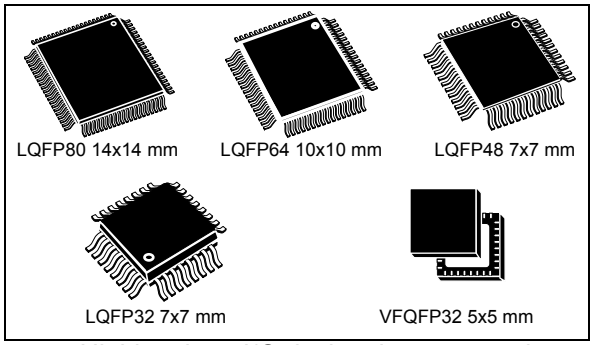
# STM8AF6388

# Automotive 8-bit MCU, with up to 128-Kbyte Flash memory, data EEPROM, 10-bit ADC, timers, LIN, USART, SPI, I2C, 3 to 5.5 V

**Datasheet - production data**

## Features

- AEC-Q10x qualified
- Core
  - Max $f_{CPU}$: 24 MHz
  - Advanced STM8A core with Harvard architecture and 3-stage pipeline
  - Average 1.6 cycles/instruction resulting in 10 MIPS at 16 MHz $f_{CPU}$ for industry standard benchmark
- Memories
  - Program memory: 32 to 128 Kbyte Flash program; data retention 20 years at 55 °C
  - Data memory: up to 2 Kbyte true data EEPROM; endurance 300 kcycle
  - RAM: 6 Kbyte
- Clock management
  - Low-power crystal resonator oscillator with external clock input
  - Internal, user-trimmable 16 MHz RC and low-power 128 kHz RC oscillators
  - Clock security system with clock monitor
- Reset and supply management
  - Wait/auto-wakeup/Halt low-power modes with user definable clock gating
  - Low consumption power-on and power-down reset
- Interrupt management
  - Nested interrupt controller with 32 vectors
  - Up to 37 external interrupts on 5 vectors
- Timers
  - 2 general purpose 16-bit timers with up to 3 CAPCOM channels each (IC, OC, PWM)
  - Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
  - 8-bit AR basic timer with 8-bit prescaler
  - Auto-wakeup timer
  - Window and independent watchdog timers
- I/Os
  - Up to 68 user pins (11 high sink I/Os)




  - Highly robust I/O design, immune against current injection
- Communication interfaces
  - USART with clock output for synchronous operation - LIN master mode
  - LINUART LIN 2.2 compliant, master/slave modes with automatic resynchronization
  - SPI interface up to 10 Mbit/s or $f_{MASTER}/2$
  - $I^2C$ interface up to 400 Kbit/s
- Analog to digital converter (ADC)
  - 10-bit resolution, 2 LSB TUE, 1 LSB linearity and up to 16 multiplexed channels
- Operating temperature up to 150 °C
- Qualification conforms to AEC-Q100 grade 0



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# 1 Introduction

This datasheet refers to the STM8AF6388 products with 32 to 128 Kbytes of program memory.

In the order code, the letter ‘F’ refers to product versions with Flash and data EEPROM and ‘P’ to product versions with FASTROM. The identifiers ‘F’ and ‘P’ do not coexist in a given order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S and STM8A Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

# 2 Description

The STM8AF6388 automotive 8-bit microcontrollers described in this datasheet offer from 32 Kbytes to 128 Kbytes of non volatile memory and integrated true data EEPROM. They are referred to as high density STM8A devices in STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

All devices of the STM8A product line provide the following benefits: reduced system cost, performance and robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, wtachdog, and brown-out reset.

Device performance is ensured by 20 MIPS at 24 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map, and modular peripherals. Full documentation is offered with a wide choice of development tools.

Product longevity is ensured in the STM8A family thanks to their advanced core which is made in a state-of-the art technology for automotive applications with 3.3 V to 5.5 V operating supply.

All STM8A and ST7 microcontrollers are supported by the same tools including STVD/STVP development environment, the STice emulator and a low-cost, third party in-circuit debugging tool.

# 3 Product line-up

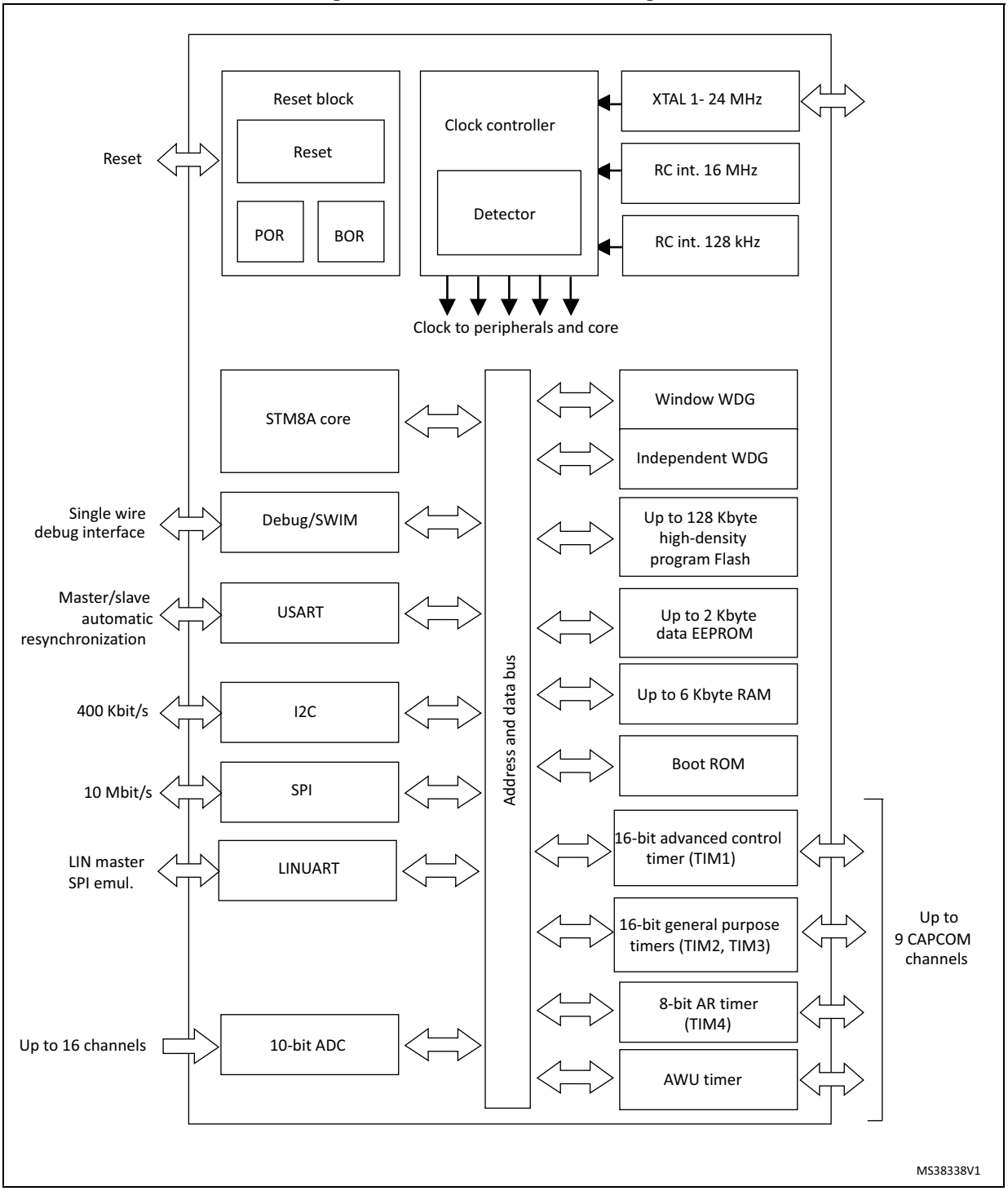
*Table 1* presents the line-up of related products available upon request;

**Table 1. STM8AF6369/8x/Ax product line-up without CAN**

| Order code | Package | High density Flash program memory (bytes) | RAM (bytes) | Data EEPROM (bytes) | 10-bit A/D chan. | Timers (IC/OC/PWM) | Serial interfaces | I/0 wakeup pins |
|---|---|---|---|---|---|---|---|---|
| STM8AF/P63AA | LQFP80 (14x14) | 128 K | 6 K | 2 K | 16 | 1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9) | LIN(UART), SPI, USART, I²C | 68/37 |
| STM8AF/P638A | | 64 K | | | | | | |
| STM8AF/P63A9 | LQFP64 (10x10) | 128 K | | | | | | 52/36 |
| STM8AF/P6389 | | 64 K | | 2 K | | | | |
| STM8AF/P6369 | | 32 K | | 1 K | | | | |
| STM8AF/P63A8 | LQFP48 (7x7) | 128 K | | 2 K | 10 | | | 38/35 |
| STM8AF/P6388 | | 64 K | | | | | | |
| STM8AF/P6386 | LQFP32 (7x7) | | | | 7 | 1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8) | LIN(UART), SPI, I²C | 25/23 |
| STM8AF/P63A6 | VFQFPN32 (5x5) | 128 K | | | | | | |

# 4 Block diagram

**Figure 1. STM8AF6388 block diagram**



1. Legend:
   ADC: Analog-to-digital converter
   BOR: Brownout reset
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent window watchdog
   LINUART: Local interconnect network universal asynchronous receiver transmitter
   POR: Power on reset
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   Window WDG: Window watchdog

# 5 Product overview

This section is intended to describe the family features that are actually implemented in the products covered by this datasheet.

For more detailed information on each feature please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

## 5.1 STM8A central processing unit (CPU)

The 8-bit STM8A core is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

### 5.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16-Mbyte linear memory space
- 16-bit stack pointer with access to a 64 Kbyte stack
- 8-bit condition code register with seven condition flags for the result of the last instruction.

### 5.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

### 5.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

## 5.2 Single wire interface module (SWIM) and debug module (DM)

### 5.2.1 SWIM

The single wire interface module, SWIM, together with an integrated debug module, permits non-intrusive, real-time in-circuit debugging and fast memory programming. The interface can be activated in all device operation modes and can be connected to a running device (hot plugging).The maximum data transmission speed is 145 bytes/ms.

### 5.2.2 Debug module

The non-intrusive debugging module features a performance close to a full-flavored emulator. Besides memory and peripheral operation, CPU operation can also be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints), except the interrupt vector table
- Two advanced breakpoints and 23 predefined breakpoint configurations

## 5.3 Interrupt controller

- Nested interrupts with three software priority levels
- 24 interrupt vectors with hardware priority
- Five vectors for external interrupts (up to 37 depending on the package)
- Trap and reset interrupts

## 5.4 Flash program and data EEPROM

- 32 Kbytes to 128 Kbytes of high density single voltage Flash program memory
- Up to 2 Kbytes true (not emulated) data EEPROM
- Read while write: writing in the data memory is possible while executing code in the Flash program memory.

The whole Flash program memory and data EEPROM are factory programmed with 0x00.

### 5.4.1 Architecture

- The memory is organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes) in parallel
- Writing, erasing, word and block management is handled automatically by the memory interface.

### 5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

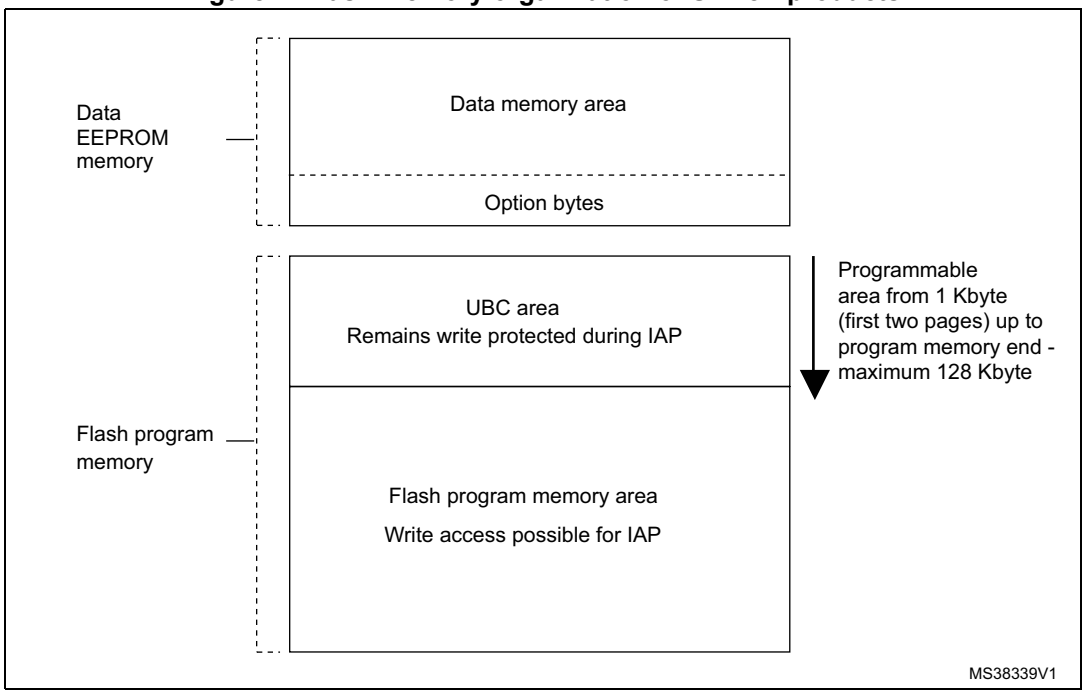
### 5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 128 Kbytes can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 54*).

**Figure 2. Flash memory organization of STM8A products**




### 5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option byte area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user through OPT6/NOPT6 option bytes.

## 5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

### 5.5.1 Features

- **Clock sources**
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
  - 1-24 MHz high-speed external crystal (HSE)
  - Up to 24 MHz high-speed user-external clock (HSE user-ext)
- **Reset**: After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Wakeup**: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- **Clock security system (CSS)**: The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO)**: This feature permits to output a clock signal for use by the application.

### 5.5.2 16 MHz high-speed internal RC oscillator (HSI)

- Default clock after reset 2 MHz (16 MHz/8)
- Fast wakeup time

#### User trimming

The register CLK_HSITRIMR with two trimming bits plus one additional bit for the sign permits frequency tuning by the application program. The adjustment range covers all possible frequency variations versus supply voltage and temperature. This trimming does not change the initial production setting.

### 5.5.3 128 kHz low-speed internal RC oscillator (LSI)

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

### 5.5.4 24 MHz high-speed external crystal oscillator (HSE)

The external high-speed crystal oscillator can be selected to deliver the main clock in normal Run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 24 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

### 5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 24 MHz.

### 5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

**Table 2. Peripheral clock gating bits (CLK_PCKENR1)**

| Control bit | Peripheral |
|---|---|
| PCKEN17 | TIM1 |
| PCKEN16 | TIM3 |
| PCKEN15 | TIM2 |
| PCKEN14 | TIM4 |
| PCKEN13 | LINUART |
| PCKEN12 | USART |
| PCKEN11 | SPI |
| PCKEN10 | $I^2C$ |

Table 3. Peripheral clock gating bits (CLK_PCKENR2)

| Control bit | Peripheral |
|---|---|
| PCKEN27 | - |
| PCKEN26 | Reserved |
| PCKEN25 | Reserved |
| PCKEN24 | Reserved |
| PCKEN23 | ADC |
| PCKEN22 | AWU |
| PCKEN21 | Reserved |
| PCKEN20 | Reserved |

## 5.6 Low-power operating modes

For efficient power management, the application can be put in one of four different low-power modes. Users can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- Wait mode

  In this mode, the CPU is stopped but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.

- Active-halt mode with regulator on

  In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in Active-halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.

- Active-halt mode with regulator off

  This mode is the same as Active-halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.

- Halt mode

  CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

In all modes the CPU and peripherals remain permanently powered on, the system clock is applied only to selected modules. The RAM content is preserved and the brown-out reset circuit remains activated.

## 5.7 Timers

### 5.7.1 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications. The watchdog timer activity is controlled by the application program or option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

#### Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

#### Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

### 5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in Active-halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock.

LSI clock can be internally connected to TIM3 input capture channel 1 for calibration.

### 5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

### 5.7.4 Advanced control and general purpose timers

STM8A devices described in this datasheet, contain up to three 16-bit advanced control and general purpose timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

**Table 4. Advanced control and general purpose timers**

| Timer | Counter width | Counter type | Prescaler factor | Channels | Inverted outputs | Repetition counter | trigger unit | External trigger | Break input |
|---|---|---|---|---|---|---|---|---|---|
| TIM1 | 16-bit | Up/down | 1 to 65536 | 4 | 3 | Yes | Yes | Yes | Yes |
| TIM2 | 16-bit | Up | $2^n$ n = 0 to 15 | 3 | None | No | No | No | No |
| TIM3 | 16-bit | Up | $2^n$ n = 0 to 15 | 2 | None | No | No | No | No |

#### TIM1 - advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and bridge driver.

- 16-bit up, down and up/down AR (auto-reload) counter with 16-bit fractional prescaler.
- Four independent CAPCOM channels configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Trigger module which allows the interaction of TIM1 with other on-chip peripherals. In the present implementation it is possible to trigger the ADC upon a timer event.
- External trigger to change the timer behavior depending on external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Interrupt sources: 4 x input capture/output compare, 1 x overflow/update, 1 x break

#### TIM2, TIM3 - 16-bit general purpose timers

- 16-bit auto-reload up-counter
- 15-bit prescaler adjustable to fixed power of two ratios 1…32768
- Timers with three or two individually configurable CAPCOM channels
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

### 5.7.5 Basic timer

The typical usage of this timer (TIM4) is the generation of a clock tick.

**Table 5. TIM4**

| Timer | Counter width | Counter type | Prescaler factor | Channels | Inverted outputs | Repetition counter | trigger unit | External trigger | Break input |
|---|---|---|---|---|---|---|---|---|---|
| TIM4 | 8-bit | Up | $2^n$ n = 0 to 7 | 0 | None | No | No | No | No |

- 8-bit auto-reload, adjustable prescaler ratio to any power of two from 1 to 128
- Clock source: master clock
- Interrupt source: 1 x overflow/update

## 5.8 Analog to digital converter (ADC)

The STM8A products described in this datasheet contain a 10-bit successive approximation ADC with up to 16 multiplexed input channels, depending on the package.

The ADC name differs between the datasheet and the STM8A/S reference manual (see *Table 6*).

**Table 6. ADC naming**

| Peripheral name in datasheet | Peripheral name in reference manual (RM0016) |
|---|---|
| ADC | ADC2 |

### ADC features

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: $f_{MASTER}$ divided by 2 to 18
- Conversion trigger on timer events, and external events
- Interrupt generation at end of conversion
- Selectable alignment of 10-bit data in 2 x 8 bit result registers
- Shadow registers for data consistency
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{DDA}$
- Schmitt-trigger on analog inputs can be disabled to reduce power consumption

## 5.9 Communication interfaces

The following sections give a brief overview of the communication peripheral. Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see *Table 7*).

**Table 7. Communication peripheral naming correspondence**

| Peripheral name in datasheet | Peripheral name in reference manual (RM0016) |
|---|---|
| USART | UART1 |
| LINUART | UART3 |

### 5.9.1 Universal synchronous/asynchronous receiver transmitter (USART)

The devices covered by this datasheet contain one USART interface. The USART can operate in standard SCI mode (serial communication interface, asynchronous) or in SPI emulation mode. It is equipped with a 16 bit fractional prescaler. It features LIN master support.

Detailed feature list:

- Full duplex, asynchronous communications
- NRZ standard format (mark/space)
- High-precision baud rate generator system
  - Common programmable transmit and receive baud rates up to $f_{MASTER}/16$
- Programmable data word length (8 or 9 bits)
- Configurable stop bits: Support for 1 or 2 stop bits
- LIN master mode:
  - LIN break and delimiter generation
  - LIN break and delimiter detection with separate flag and interrupt source for readback checking.
- Transmitter clock output for synchronous communication
- Separate enable bits for transmitter and receiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - End of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- Six interrupt sources with flags:
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Parity error
  - LIN break and delimiter detection
- Two interrupt vectors:
  - Transmitter interrupt
  - Receiver interrupt
- Reduced power consumption mode
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line

### 5.9.2 Universal asynchronous receiver/transmitter with LIN support (LINUART)

The devices covered by this datasheet contain one LINUART interface. The interface is available on all the supported packages. The LINUART is an asynchronous serial communication interface which supports extensive LIN functions tailored for LIN slave applications. In LIN mode it is compliant to the LIN standards rev 1.2 to rev 2.2.

Detailed feature list:

#### LIN mode

**Master mode**

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

**Slave mode**

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
  - Delimiter too short
  - Synch field error
  - Deviation error (if automatic resynchronization is enabled)
  - Framing error in synch field or identifier field
  - Header time-out

#### UART mode

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- High-precision baud rate generator
  - A common programmable transmit and receive baud rates up to $f_{MASTER}/16$
- Programmable data word length (8 or 9 bits) – 1 or 2 stop bits – parity control
- Separate enable bits for transmitter and receiver
- Error detection flags
- Reduced power consumption mode
- Multi-processor communication - enter mute mode if address match does not occur
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line

### 5.9.3 Serial peripheral interface (SPI)

The devices covered by this datasheet contain one SPI. The SPI is available on all the supported packages.

- Maximum speed: 10 Mbit/s or $f_{MASTER}/2$ for master, 8 Mbit/s or $f_{MASTER}$ /2 for slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave mode/master mode management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - CRC error checking for last received byte

### 5.9.4 Inter integrated circuit ($I^2C$) interface

The devices covered by this datasheet contain one $I^2C$ interface. The interface is available on all the supported packages.

- $I^2C$ master features:
  - Clock generation
  - Start and stop generation
- $I^2C$ slave features:
  - Programmable $I^2C$ address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)
- Status flags:
  - Transmitter/receiver mode flag
  - End-of-byte transmission flag
  - $I^2C$ busy flag
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgement failure after address/data transmission
  - Detection of misplaced start or stop condition
  - Overrun/underrun if clock stretching is disabled

- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

## 5.10 Input/output specifications

The product features four I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain ($I^2C$ interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

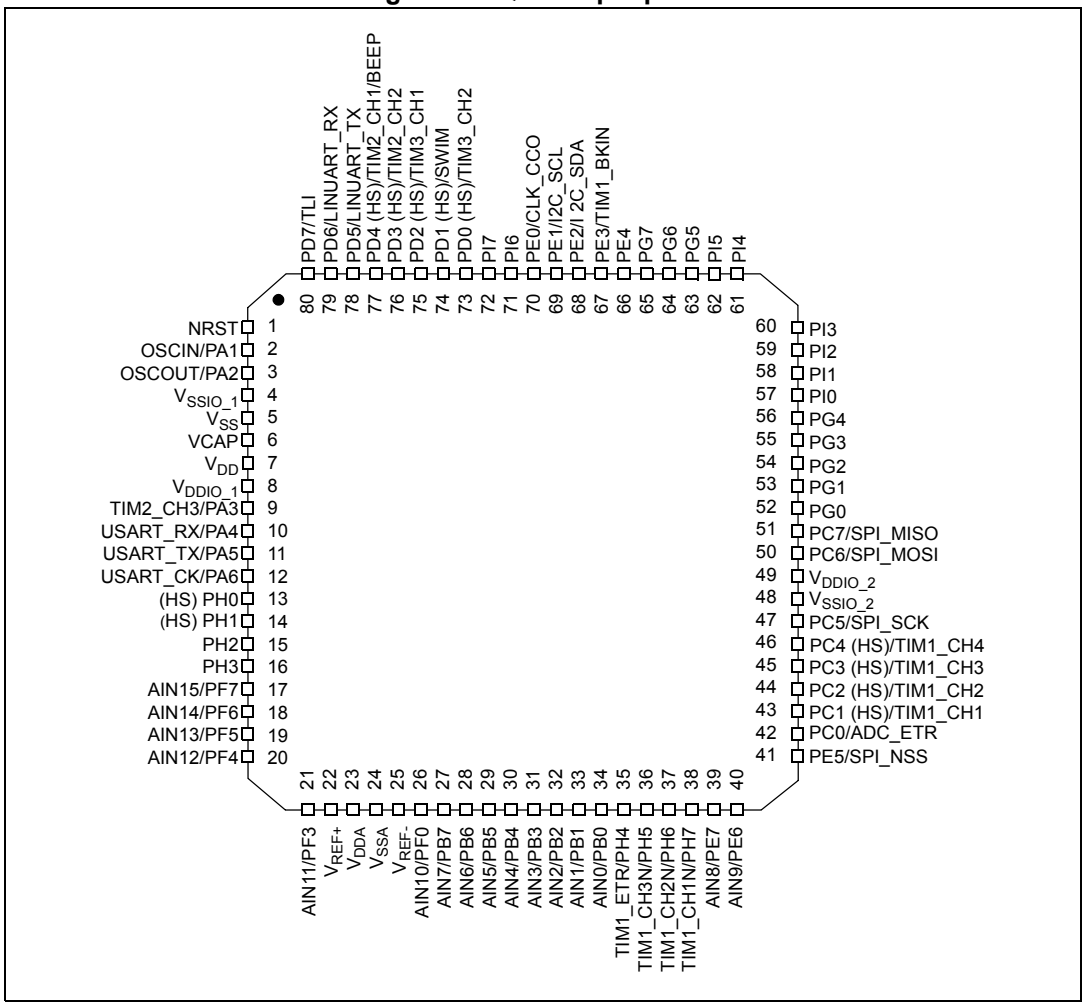
The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

# 6 Pinouts and pin description

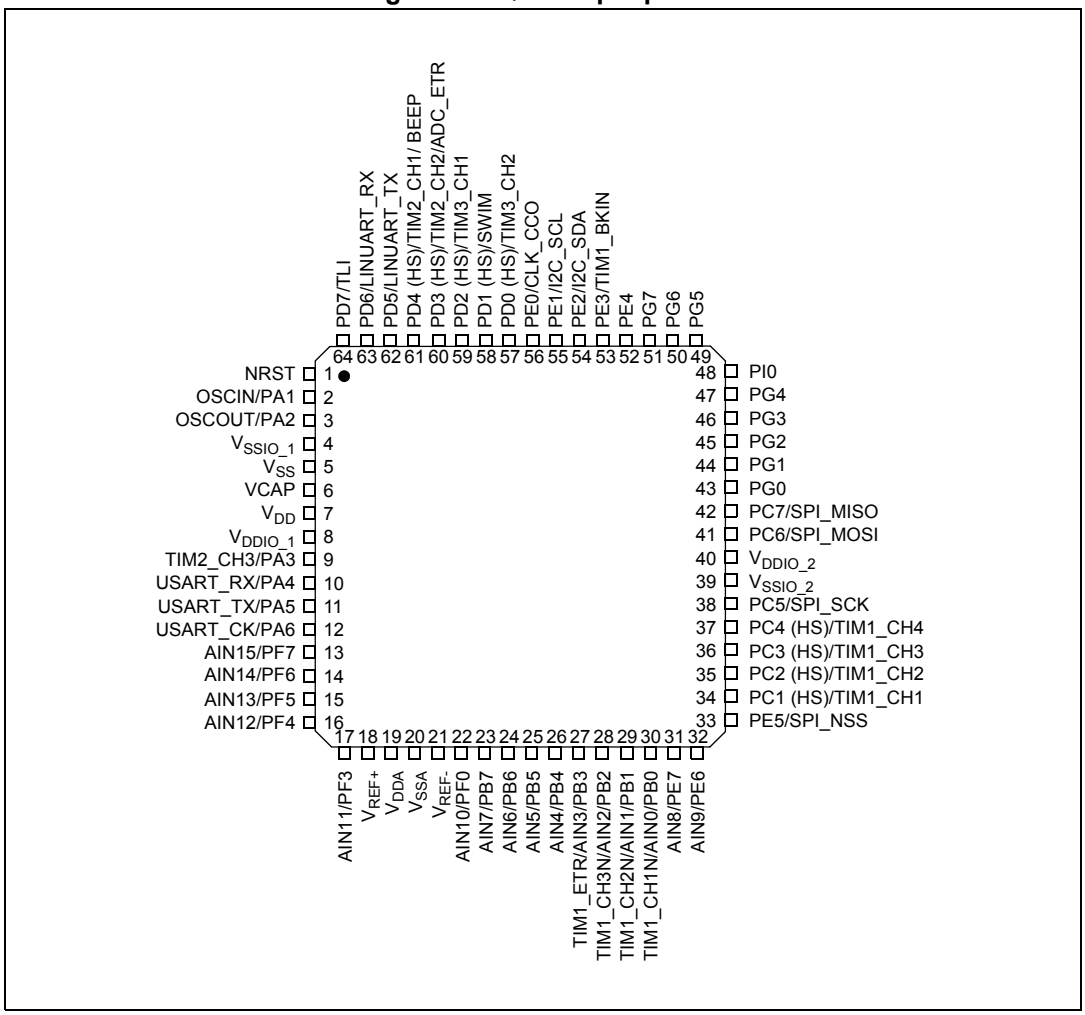
## 6.1 Package pinouts

**Figure 3. LQFP 80-pin pinout**



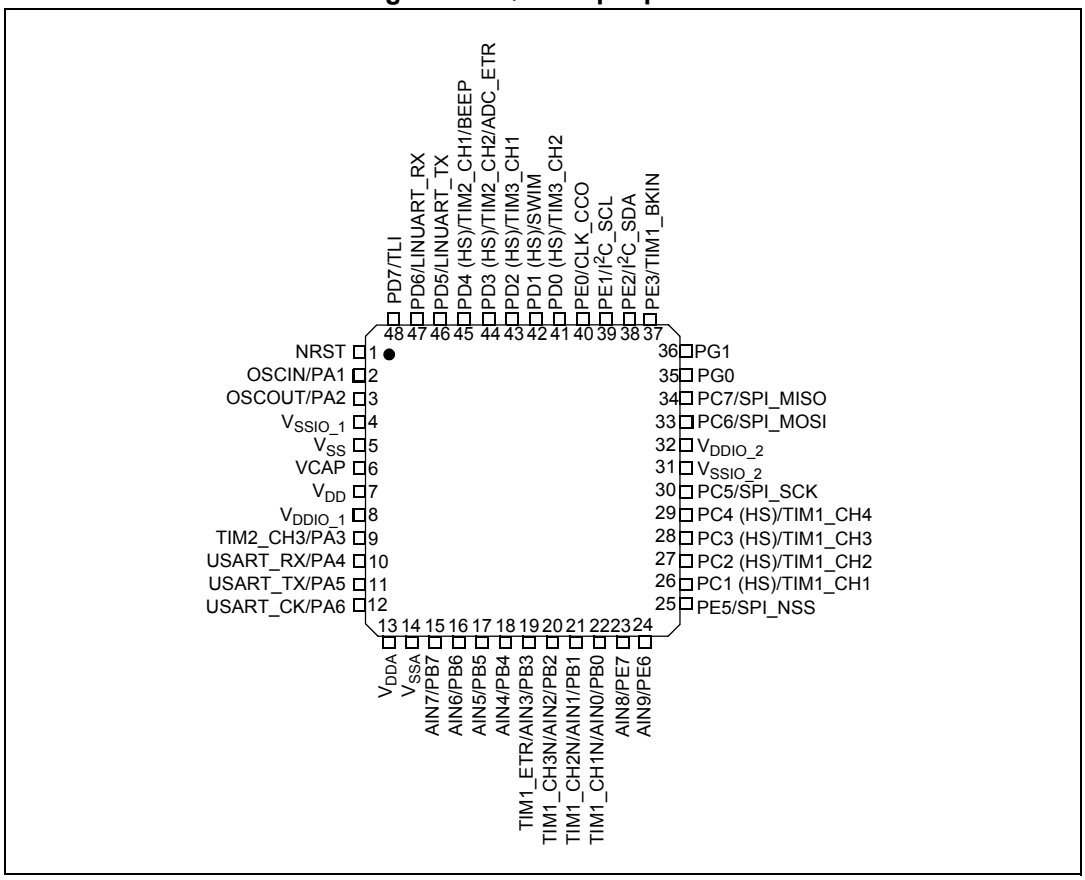

2. (HS) stands for high sink capability.

**Figure 4. LQFP 64-pin pinout**



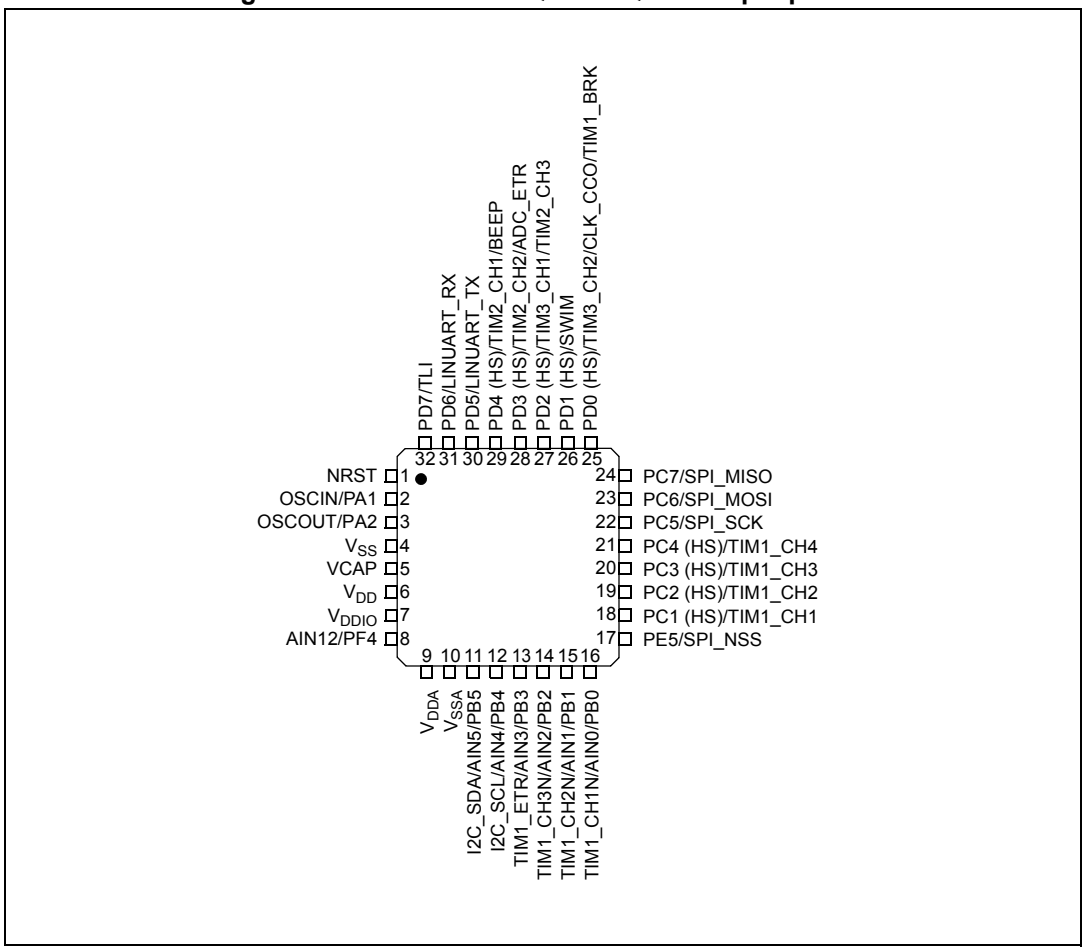

3. HS stands for high sink capability.

**Figure 5. LQFP 48-pin pinout**



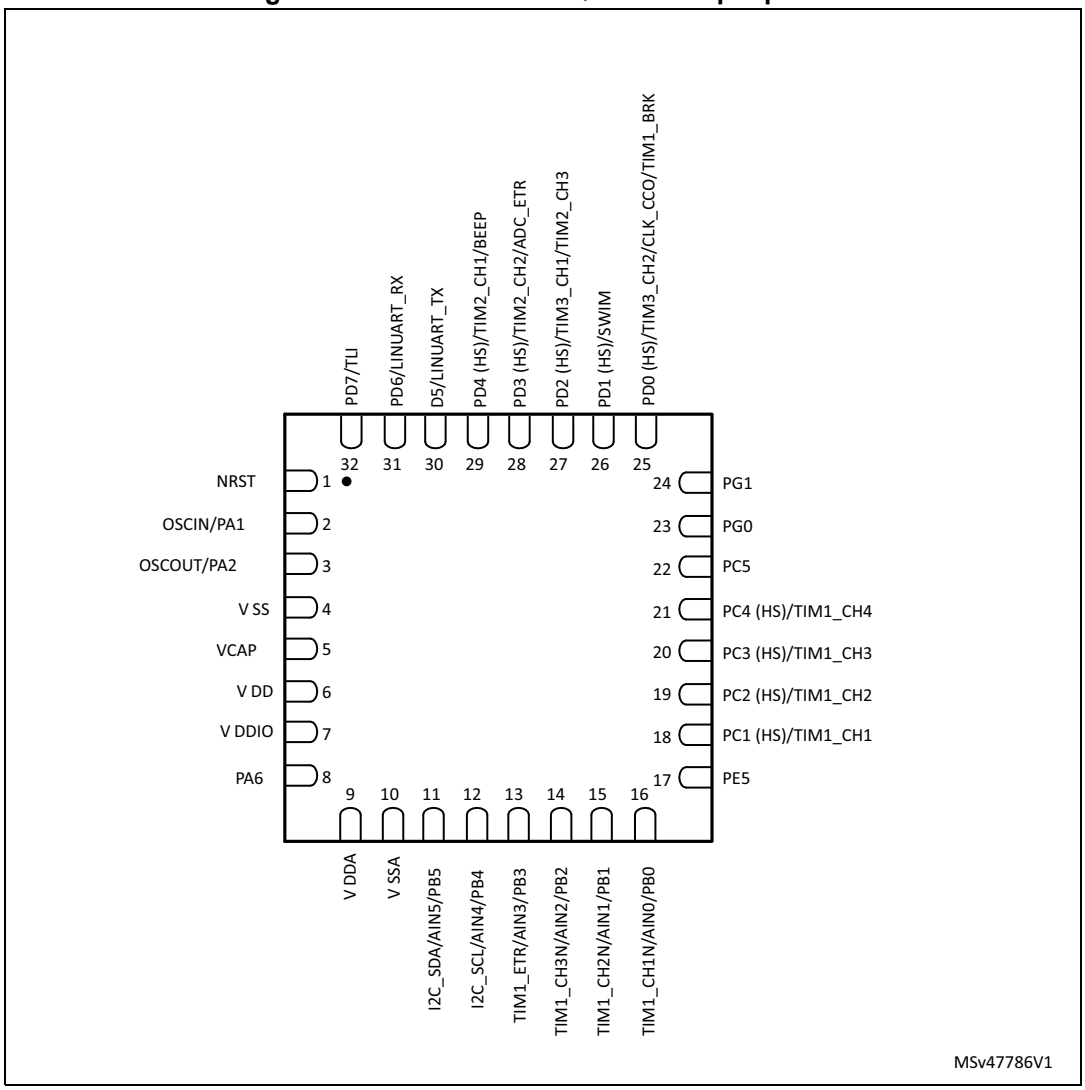

4. HS stands for high sink capability.

**Figure 6. STM8AF62xx LQFP/VFQFPN 32-pin pinout**




1. HS stands for high sink capability.

**Figure 7. STM8AF52x6 VFQFPN32 32-pin pinout**




1. The following I/O ports are not automatically configured by hardware: PA3, PA4, PA5, PA6, PF4, PB6, PB7, PE0, PE1, PE2, PE3, PE6, PE7. As a consequence, they must be put into one of the following configurations by software:
   - configured as input with internal pull-up/down resistor,
   - configured as output push-pull low.
2. HS stands for high sink capability.

**Table 8. Legend/abbreviation for the pin description table**

| | | |
|---|---|---|
| Type | I= input, O = output, S = power supply | |
| Level | Input | CM = CMOS (standard for all I/Os) |
| | Output | HS = high sink (8 mA) |
| Output speed | O1 = Standard (up to 2 MHz)<br>O2 = Fast (up to 10 MHz)<br>O3 = Fast/slow programmability with slow as default state after reset<br>O4 = Fast/slow programmability with fast as default state after reset | |
| Port and control configuration | Input | float = floating, wpu = weak pull-up |
| | Output | T = true open drain, OD = open drain, PP = push pull |
| Reset state | Bold X (pin state after reset release).<br>Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state). | |

**Table 9. STM8AF6388 pin description**

| Pin number | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | LQFP48 | STM8AF62xx LQFP32/VFQFPN32 | | | Floating | Wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 1 | 1 | 1 | 1 | NRST | I/O | - | **X** | - | - | - | - | - | Reset | | - |
| 2 | 2 | 2 | 2 | PA1/OSCIN(1) | I/O | **X** | X | - | - | O1 | X | X | **Port A1** | Resonator/ crystal in | - |
| 3 | 3 | 3 | 3 | PA2/OSCOUT | I/O | **X** | X | X | - | O1 | X | X | **Port A2** | Resonator/ crystal out | - |
| 4 | 4 | 4 | - | $V_{SSIO_1}$ | S | - | - | - | - | - | - | - | I/O ground | | - |
| 5 | 5 | 5 | 4 | $V_{SS}$ | S | - | - | - | - | - | - | - | Digital ground | | - |
| 6 | 6 | 6 | 5 | VCAP | S | - | - | - | - | - | - | - | 1.8 V regulator capacitor | | - |
| 7 | 7 | 7 | 6 | $V_{DD}$ | S | - | - | - | - | - | - | - | Digital power supply | | - |
| 8 | 8 | 8 | 7 | $V_{DDIO_1}$ | S | - | - | - | - | - | - | - | I/O power supply | | - |
| 9 | 9 | 9 | - | PA3/TIM2_CH3 | I/O | **X** | X | X | - | O1 | X | X | **Port A3** | Timer 2 - channel 3 | TIM3_CH1 [AFR1] |
| 10 | 10 | 10 | - | PA4/USART_RX | I/O | **X** | X | X | - | O3 | X | X | **Port A4** | USART receive | - |
| 11 | 11 | 11 | - | PA5/USART_TX | I/O | **X** | X | X | - | O3 | X | X | **Port A5** | USART transmit | - |
| 12 | 12 | 12 | - | PA6/USART_CK | I/O | **X** | X | X | - | O3 | X | X | **Port A6** | USART synchro nous clock | - |
| 13 | - | - | - | PH0 | I/O | X | X | - | HS | O3 | X | X | **Port H0** | - | - |
| 14 | - | - | - | PH1 | I/O | **X** | X | - | HS | O3 | X | X | **Port H1** | - | - |
| 15 | - | - | - | PH2 | I/O | **X** | X | - | - | O1 | X | X | **Port H2** | - | - |
| 16 | - | - | - | PH3 | I/O | **X** | X | - | - | O1 | X | X | **Port H3** | - | - |
| 17 | 13 | - | - | PF7/AIN15 | I/O | **X** | X | - | - | O1 | X | X | **Port F7** | Analog input 15 | - |
| 18 | 14 | - | - | PF6/AIN14 | I/O | **X** | X | - | - | O1 | X | X | **Port F6** | Analog input 14 | - |
| 19 | 15 | - | - | PF5/AIN13 | I/O | **X** | X | - | - | O1 | X | X | **Port F5** | Analog input 13 | - |
| 20 | 16 | - | 8 | PF4/AIN12 | I/O | **X** | X | - | - | O1 | X | X | **Port F4** | Analog input 12 | - |
| 21 | 17 | - | - | PF3/AIN11 | I/O | **X** | X | - | - | O1 | X | X | **Port F3** | Analog input 11 | - |

Table 9. STM8AF6388 pin description (continued)

| Pin number | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | LQFP48 | STM8AF62xx LQFP32/VFQFPN32 | | | Floating | Wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 22 | 18 | - | - | $V_{REF+}$ | S | - | - | - | - | - | - | - | ADC positive reference voltage | | - |
| 23 | 19 | 13 | 9 | $V_{DDA}$ | S | - | - | - | - | - | - | - | Analog power supply | | - |
| 24 | 20 | 14 | 10 | $V_{SSA}$ | S | - | - | - | - | - | - | - | Analog ground | | - |
| 25 | 21 | - | - | $V_{REF-}$ | S | - | - | - | - | - | - | - | ADC negative reference voltage | | - |
| 26 | 22 | - | - | PF0/AIN10 | I/O | **X** | X | - | - | O1 | X | X | **Port F0** | Analog input 10 | - |
| 27 | 23 | 15 | - | PB7/AIN7 | I/O | **X** | X | X | - | O1 | X | X | **Port B7** | Analog input 7 | - |
| 28 | 24 | 16 | - | PB6/AIN6 | I/O | **X** | X | X | - | O1 | X | X | **Port B6** | Analog input 6 | - |
| 29 | 25 | 17 | 11 | PB5/AIN5 | I/O | **X** | X | X | - | O1 | X | X | **Port B5** | Analog input 5 | $I^2C$_SDA [AFR6] |
| 30 | 26 | 18 | 12 | PB4/AIN4 | I/O | **X** | X | X | - | O1 | X | X | **Port B4** | Analog input 4 | $I^2C$_SCL [AFR6] |
| 31 | 27 | 19 | 13 | PB3/AIN3 | I/O | **X** | X | X | - | O1 | X | X | **Port B3** | Analog input 3 | TIM1_ETR [AFR5] |
| 32 | 28 | 20 | 14 | PB2/AIN2 | I/O | **X** | X | X | - | O1 | X | X | **Port B2** | Analog input | TIM1_CH3N [AFR5] |
| 33 | 29 | 21 | 15 | PB1/AIN1 | I/O | **X** | X | X | - | O1 | X | X | **Port B1** | Analog input 1 | TIM1_CH2N [AFR5] |
| 34 | 30 | 22 | 16 | PB0/AIN0 | I/O | **X** | X | X | - | O1 | X | X | **Port B0** | Analog input 0 | TIM1_CH1N [AFR5] |
| 35 | - | - | - | PH4/TIM1_ETR | I/O | **X** | X | - | - | O1 | X | X | **Port H4** | Timer 1 - trigger input | - |
| 36 | - | - | - | PH5/ TIM1_CH3N | I/O | **X** | X | - | - | O1 | X | X | **Port H5** | Timer 1 - inverted channel 3 | - |
| 37 | - | - | - | PH6/ TIM1_CH2N | I/O | **X** | X | - | - | O1 | X | X | **Port H6** | Timer 1 - inverted channel 2 | - |
| 38 | - | - | - | PH7/ TIM1_CH1N | I/O | **X** | X | - | - | O1 | X | X | **Port H7** | Timer 1 - inverted channel 2 | - |

Table 9. STM8AF6388 pin description (continued)

| Pin number | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | LQFP48 | STM8AF62xx LQFP32/VFQFPN32 | | | Floating | Wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 39 | 31 | 23 | - | PE7/AIN8 | I/O | **X** | X | - | - | O1 | X | X | **Port E7** | Analog input 8 | - |
| 40 | 32 | 24 | | PE6/AIN9 | I/O | **X** | X | X | - | O1 | X | X | **Port E6** | Analog input 9 | - |
| 41 | 33 | 25 | 17 | PE5/SPI_NSS | I/O | **X** | X | X | - | O1 | X | X | **Port E5** | SPI master/ slave select | - |
| 42 | - | - | - | PC0/ADC_ETR | I/O | **X** | X | X | - | O1 | X | X | **Port C0** | ADC trigger input | - |
| 43 | 34 | 26 | 18 | PC1/TIM1_CH1 | I/O | **X** | X | X | HS | O3 | X | X | **Port C1** | Timer 1 - channel 1 | - |
| 44 | 35 | 27 | 19 | PC2/TIM1_CH2 | I/O | **X** | X | X | HS | O3 | X | X | **Port C2** | Timer 1- channel 2 | - |
| 45 | 36 | 28 | 20 | PC3/TIM1_CH3 | I/O | **X** | X | X | HS | O3 | X | X | **Port C3** | Timer 1 - channel 3 | - |
| 46 | 37 | 29 | 21 | PC4/TIM1_CH4 | I/O | **X** | X | X | HS | O3 | X | X | **Port C4** | Timer 1 - channel 4 | - |
| 47 | 38 | 30 | 22 | PC5/SPI_SCK | I/O | **X** | X | X | - | O3 | X | X | **Port C5** | SPI clock | - |
| 48 | 39 | 31 | - | $V_{SSIO_2}$ | S | - | - | - | - | - | - | - | I/O ground | | - |
| 49 | 40 | 32 | - | $V_{DDIO_2}$ | S | - | - | - | - | - | - | - | I/O power supply | | - |
| 50 | 41 | 33 | 23 | PC6/SPI_MOSI | I/O | **X** | X | X | - | O3 | X | X | **Port C6** | SPI master out/ slave in | - |
| 51 | 42 | 34 | 24 | PC7/SPI_MISO | I/O | **X** | X | X | - | O3 | X | X | **Port C7** | SPI master in/ slave out | - |
| 52 | 43 | 35 | - | PG0 | I/O | **X** | X | - | - | O1 | X | X | **Port G0** | - | - |
| 53 | 44 | 36 | - | PG1 | I/O | **X** | X | - | - | O1 | X | X | **Port G1** | - | - |
| 54 | 45 | - | - | PG2 | I/O | **X** | X | - | - | O1 | X | X | **Port G2** | - | - |
| 55 | 46 | - | - | PG3 | I/O | **X** | X | - | - | O1 | X | X | **Port G3** | - | - |
| 56 | 47 | - | - | PG4 | I/O | **X** | X | - | - | O1 | X | X | **Port G4** | - | - |
| 57 | 48 | - | - | PI0 | I/O | **X** | X | - | - | O1 | X | X | **Port I0** | - | - |
| 58 | - | - | - | PI1 | I/O | **X** | X | - | - | O1 | X | X | **Port I1** | - | - |
| 59 | - | - | - | PI2 | I/O | **X** | X | - | - | O1 | X | X | **Port I2** | - | - |
| 60 | - | - | - | PI3 | I/O | **X** | X | - | - | O1 | X | X | **Port I3** | - | - |

Table 9. STM8AF6388 pin description (continued)

| Pin number | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | LQFP48 | STM8AF62xx LQFP32/VFQFPN32 | | | Floating | Wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 61 | - | - | - | PI4 | I/O | **X** | X | - | - | O1 | X | X | **Port I4** | - | - |
| 62 | - | - | - | PI5 | I/O | **X** | X | - | - | O1 | X | X | **Port I5** | - | - |
| 63 | 49 | - | - | PG5 | I/O | **X** | X | - | - | O1 | X | X | **Port G5** | - | - |
| 64 | 50 | - | - | PG6 | I/O | **X** | X | - | - | O1 | X | X | **Port G6** | - | - |
| 65 | 51 | - | - | PG7 | I/O | **X** | X | - | - | O1 | X | X | **Port G7** | - | - |
| 66 | 52 | - | - | PE4 | I/O | **X** | X | X | - | O1 | X | X | **Port E4** | - | - |
| 67 | 53 | 37 | - | PE3/TIM1_BKIN | I/O | **X** | X | X | - | O1 | X | X | **Port E3** | Timer 1 - break input | - |
| 68 | 54 | 38 | - | PE2/$I^2C$_SDA | I/O | **X** | - | X | - | O1 | T(2) | - | **Port E2** | $I^2C$ data | - |
| 69 | 55 | 39 | - | PE1/$I^2C$_SCL | I/O | **X** | - | X | - | O1 | T(2) | - | **Port E1** | $I^2C$ clock | - |
| 70 | 56 | 40 | - | PE0/CLK_CCO | I/O | **X** | X | X | - | O3 | X | X | **Port E0** | Configurable clock output | - |
| 71 | - | - | - | PI6 | I/O | **X** | X | - | - | O1 | X | X | **Port I6** | - | - |
| 72 | - | - | - | PI7 | I/O | **X** | X | - | - | O1 | X | X | **Port I7** | - | - |
| 73 | 57 | 41 | 25 | PD0/TIM3_CH2 | I/O | **X** | X | X | HS | O3 | X | X | **Port D0** | Timer 3 - channel 2 | TIM1_BKIN [AFR3]/ CLK_CCO [AFR2] |
| 74 | 58 | 42 | 26 | PD1/SWIM(3) | I/O | X | **X** | X | HS | O4 | X | X | **Port D1** | SWIM data interface | - |
| 75 | 59 | 43 | 27 | PD2/TIM3_CH1 | I/O | **X** | X | X | HS | O3 | X | X | **Port D2** | Timer 3 - channel 1 | TIM2_CH3 [AFR1] |
| 76 | 60 | 44 | 28 | PD3/TIM2_CH2 | I/O | **X** | X | X | HS | O3 | X | X | **Port D3** | Timer 2 - channel 2 | ADC_ETR [AFR0] |
| 77 | 61 | 45 | 29 | PD4/TIM2_CH1/ BEEP | I/O | **X** | X | X | HS | O3 | X | X | **Port D4** | Timer 2 - channel 1 | BEEP output [AFR7] |
| 78 | 62 | 46 | 30 | PD5/ LINUART_TX | I/O | **X** | X | X | - | O1 | X | X | **Port D5** | LINUART data transmit | - |
| 79 | 63 | 47 | 31 | PD6/ LINUART_RX | I/O | **X** | X | X | - | O1 | X | X | **Port D6** | LINUART data receive | - |
| 80 | 64 | 48 | 32 | PD7/TLI(4) | I/O | **X** | X | X | - | O1 | X | X | **Port D7** | Top level interrupt | - |

1. In Halt/Active-halt mode, this pin behaves as follows:
   - The input/output path is disabled.
   - If the HSE clock is used for wakeup, the internal weak pull-up is disabled.
   - If the HSE clock is off, the internal weak pull-up setting is used. It is configured through Px_CR1[7:0] bits of the corresponding port control register. Px_CR1[7:0] bits must be set correctly to ensure that the pin is not left floating in Halt/Active-halt mode.
2. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up and protection diode to $V_{DD}$ are not implemented)
3. The PD1 pin is in input pull-up during the reset phase and after reset release.
4. If this pin is configured as interrupt pin, it will trigger the TLI.

## 6.2 Alternate function remapping

As shown in the rightmost column of *Table 9*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 9: Option bytes on page 54*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

# 7 Memory and register map

## 7.1 Memory map

**Figure 8. Register and memory map**

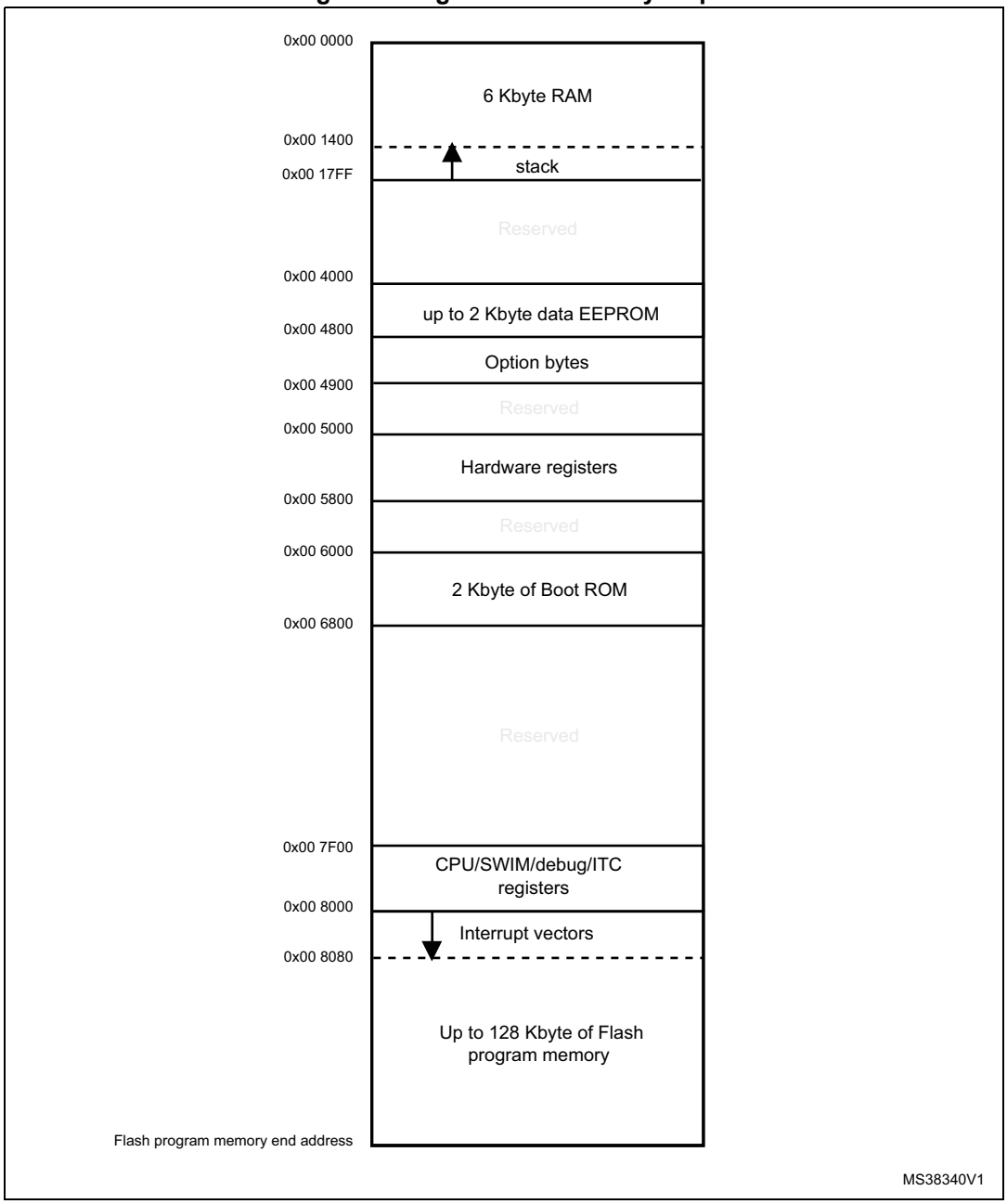


**Table 10. Memory model 128K**

| Flash program memory size | Flash program memory end address | RAM size | RAM end address | Stack roll-over address |
|---|---|---|---|---|
| 128 K | 0x00 27FFF | 6 K | 0x00 17FF | 0x00 1400 |
| 64 K | 0x00 17FFF | | | |
| 32 K | 0x00 0FFFF | | | |

## 7.2 Register map

In this section the memory and register map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016.

**Table 11. I/O port hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5000 | Port A | PA_ODR | Port A data output latch register | 0x00 |
| 0x00 5001 | | PA_IDR | Port A input pin value register | 0xXX(1) |
| 0x00 5002 | | PA_DDR | Port A data direction register | 0x00 |
| 0x00 5003 | | PA_CR1 | Port A control register 1 | 0x00 |
| 0x00 5004 | | PA_CR2 | Port A control register 2 | 0x00 |
| 0x00 5005 | Port B | PB_ODR | Port B data output latch register | 0x00 |
| 0x00 5006 | | PB_IDR | Port B input pin value register | 0xXX(1) |
| 0x00 5007 | | PB_DDR | Port B data direction register | 0x00 |
| 0x00 5008 | | PB_CR1 | Port B control register 1 | 0x00 |
| 0x00 5009 | | PB_CR2 | Port B control register 2 | 0x00 |
| 0x00 500A | Port C | PC_ODR | Port C data output latch register | 0x00 |
| 0x00 500B | | PB_IDR | Port C input pin value register | 0xXX(1) |
| 0x00 500C | | PC_DDR | Port C data direction register | 0x00 |
| 0x00 500D | | PC_CR1 | Port C control register 1 | 0x00 |
| 0x00 500E | | PC_CR2 | Port C control register 2 | 0x00 |
| 0x00 500F | Port D | PD_ODR | Port D data output latch register | 0x00 |
| 0x00 5010 | | PD_IDR | Port D input pin value register | 0xXX(1) |
| 0x00 5011 | | PD_DDR | Port D data direction register | 0x00 |
| 0x00 5012 | | PD_CR1 | Port D control register 1 | 0x02 |
| 0x00 5013 | | PD_CR2 | Port D control register 2 | 0x00 |

Table 11. I/O port hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5014 | Port E | PE_ODR | Port E data output latch register | 0x00 |
| 0x00 5015 | | PE_IDR | Port E input pin value register | 0xXX(1) |
| 0x00 5016 | | PE_DDR | Port E data direction register | 0x00 |
| 0x00 5017 | | PE_CR1 | Port E control register 1 | 0x00 |
| 0x00 5018 | | PE_CR2 | Port E control register 2 | 0x00 |
| 0x00 5019 | Port F | PF_ODR | Port F data output latch register | 0x00 |
| 0x00 501A | | PF_IDR | Port F input pin value register | 0xXX(1) |
| 0x00 501B | | PF_DDR | Port F data direction register | 0x00 |
| 0x00 501C | | PF_CR1 | Port F control register 1 | 0x00 |
| 0x00 501D | | PF_CR2 | Port F control register 2 | 0x00 |
| 0x00 501E | Port G | PG_ODR | Port G data output latch register | 0x00 |
| 0x00 501F | | PG_IDR | Port G input pin value register | 0xXX(1) |
| 0x00 5020 | | PG_DDR | Port G data direction register | 0x00 |
| 0x00 5021 | | PG_CR1 | Port G control register 1 | 0x00 |
| 0x00 5022 | | PG_CR2 | Port G control register 2 | 0x00 |
| 0x00 5023 | Port H | PH_ODR | Port H data output latch register | 0x00 |
| 0x00 5024 | | PH_IDR | Port H input pin value register | 0xXX(1) |
| 0x00 5025 | | PH_DDR | Port H data direction register | 0x00 |
| 0x00 5026 | | PH_CR1 | Port H control register 1 | 0x00 |
| 0x00 5027 | | PH_CR2 | Port H control register 2 | 0x00 |
| 0x00 5028 | Port I | PI_ODR | Port I data output latch register | 0x00 |
| 0x00 5029 | | PI_IDR | Port I input pin value register | 0xXX(1) |
| 0x00 502A | | PI_DDR | Port I data direction register | 0x00 |
| 0x00 502B | | PI_CR1 | Port I control register 1 | 0x00 |
| 0x00 502C | | PI_CR2 | Port I control register 2 | 0x00 |

1. Depends on the external circuitry.

**Table 12. General hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 505A | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 505B | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 505C | | FLASH_NCR2 | Flash complementary control register 2 | 0xFF |
| 0x00 505D | | FLASH_FPR | Flash protection register | 0x00 |
| 0x00 505E | | FLASH_NFPR | Flash complementary protection register | 0xFF |
| 0x00 505F | | FLASH_IAPSR | Flash in-application programming status register | 0x40 |
| 0x00 5060 to 0x005061 | Reserved area (2 bytes) | | | |
| 0x00 5062 | Flash | FLASH_PUKR | Flash Program memory unprotection register | 0x00 |
| 0x00 5063 | Reserved area (1 byte) | | | |
| 0x00 5064 | Flash | FLASH_DUKR | Data EEPROM unprotection register | 0x00 |
| 0x00 5065 to 0x00 509F | Reserved area (59 bytes) | | | |
| 0x00 50A0 | ITC | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 to 0x00 50B2 | Reserved area (17 bytes) | | | |
| 0x00 50B3 | RST | RST_SR | Reset status register | 0xXX(1) |
| 0x00 50B4 to 0x00 50BF | Reserved area (12 bytes) | | | |
| 0x00 50C0 | CLK | CLK_ICKR | Internal clock control register | 0x01 |
| 0x00 50C1 | | CLK_ECKR | External clock control register | 0x00 |
| 0x00 50C2 | Reserved area (1 byte) | | | |

Table 12. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 50C3 | CLK | CLK_CMSR | Clock master status register | 0xE1 |
| 0x00 50C4 | | CLK_SWR | Clock master switch register | 0xE1 |
| 0x00 50C5 | | CLK_SWCR | Clock switch control register | 0xXX |
| 0x00 50C6 | | CLK_CKDIVR | Clock divider register | 0x18 |
| 0x00 50C7 | | CLK_PCKENR1 | Peripheral clock gating register 1 | 0xFF |
| 0x00 50C8 | | CLK_CSSR | Clock security system register | 0x00 |
| 0x00 50C9 | | CLK_CCOR | Configurable clock control register | 0x00 |
| 0x00 50CA | | CLK_PCKENR2 | Peripheral clock gating register 2 | 0xFF |
| 0x00 50CB | | Reserved area (1 byte) | | |
| 0x00 50CC | | CLK_HSITRIMR | HSI clock calibration trimming register | 0x00 |
| 0x00 50CD | | CLK_SWIMCCR | SWIM clock control register | 0bXXXX XXX0 |
| 0x00 50CE to 0x00 50D0 | Reserved area (3 bytes) | | | |
| 0x00 50D1 | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D2 | | WWDG_WR | WWDR window register | 0x7F |
| 0x00 50D3 to 0x00 50DF | Reserved area (13 bytes) | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX(2) |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 bytes) | | | |
| 0x00 50F0 | AWU | AWU_CSR1 | AWU control/status register 1 | 0x00 |
| 0x00 50F1 | | AWU_APR | AWU asynchronous prescaler buffer register | 0x3F |
| 0x00 50F2 | | AWU_TBR | AWU timebase selection register | 0x00 |
| 0x00 50F3 | BEEP | BEEP_CSR | BEEP control/status register | 0x1F |
| 0x00 50F4 to 0x00 50FF | Reserved area (12 bytes) | | | |

Table 12. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5200 | SPI | SPI_CR1 | SPI control register 1 | 0x00 |
| 0x00 5201 | | SPI_CR2 | SPI control register 2 | 0x00 |
| 0x00 5202 | | SPI_ICR | SPI interrupt control register | 0x00 |
| 0x00 5203 | | SPI_SR | SPI status register | 0x02 |
| 0x00 5204 | | SPI_DR | SPI data register | 0x00 |
| 0x00 5205 | | SPI_CRCPR | SPI CRC polynomial register | 0x07 |
| 0x00 5206 | | SPI_RXCRCR | SPI Rx CRC register | 0xFF |
| 0x00 5207 | | SPI_TXCRCR | SPI Tx CRC register | 0xFF |
| 0x00 5208 to 0x00 520F | Reserved area (8 bytes) | | | |
| 0x00 5210 | I2C | I2C_CR1 | I2C control register 1 | 0x00 |
| 0x00 5211 | | I2C_CR2 | I2C control register 2 | 0x00 |
| 0x00 5212 | | I2C_FREQR | I2C frequency register | 0x00 |
| 0x00 5213 | | I2C_OARL | I2C own address register low | 0x00 |
| 0x00 5214 | | I2C_OARH | I2C own address register high | 0x00 |
| 0x00 5215 | | | | |
| 0x00 5216 | | I2C_DR | I2C data register | 0x00 |
| 0x00 5217 | | I2C_SR1 | I2C status register 1 | 0x00 |
| 0x00 5218 | | I2C_SR2 | I2C status register 2 | 0x00 |
| 0x00 5219 | | I2C_SR3 | I2C status register 3 | 0x00 |
| 0x00 521A | | I2C_ITR | I2C interrupt control register | 0x00 |
| 0x00 521B | | I2C_CCRL | I2C clock control register low | 0x00 |
| 0x00 521C | | I2C_CCRH | I2C clock control register high | 0x00 |
| 0x00 521D | | I2C_TRISER | I2C TRISE register | 0x02 |
| 0x00 521E to 0x00 522F | Reserved area (18 bytes) | | | |

Table 12. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5230 | USART | UART1_SR | USART status register | 0xC0 |
| 0x00 5231 | | UART1_DR | USART data register | 0xXX |
| 0x00 5232 | | UART1_BRR1 | USART baud rate register 1 | 0x00 |
| 0x00 5233 | | UART1_BRR2 | USART baud rate register 2 | 0x00 |
| 0x00 5234 | | UART1_CR1 | USART control register 1 | 0x00 |
| 0x00 5235 | | UART1_CR2 | USART control register 2 | 0x00 |
| 0x00 5236 | | UART1_CR3 | USART control register 3 | 0x00 |
| 0x00 5237 | | UART1_CR4 | USART control register 4 | 0x00 |
| 0x00 5238 | | UART1_CR5 | USART control register 5 | 0x00 |
| 0x00 5239 | | UART1_GTR | USART guard time register | 0x00 |
| 0x00 523A | | UART1_PSCR | USART prescaler register | 0x00 |
| 0x00 523B to 0x00 523F | Reserved area (5 bytes) | | | |
| 0x00 5240 | LINUART | UART3_SR | LINUART status register | 0xC0 |
| 0x00 5241 | | UART3_DR | LINUART data register | 0xXX |
| 0x00 5242 | | UART3_BRR1 | LINUART baud rate register 1 | 0x00 |
| 0x00 5243 | | UART3_BRR2 | LINUART baud rate register 2 | 0x00 |
| 0x00 5244 | | UART3_CR1 | LINUART control register 1 | 0x00 |
| 0x00 5245 | | UART3_CR2 | LINUART control register 2 | 0x00 |
| 0x00 5246 | | UART3_CR3 | LINUART control register 3 | 0x00 |
| 0x00 5247 | | UART3_CR4 | LINUART control register 4 | 0x00 |
| 0x00 5248 | | Reserved | | |
| 0x00 5249 | | UART3_CR6 | LINUART control register 6 | 0x00 |
| 0x00 524A to 0x00 524F | Reserved area (6 bytes) | | | |

Table 12. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5250 | TIM1 | TIM1_CR1 | TIM1 control register 1 | 0x00 |
| 0x00 5251 | | TIM1_CR2 | TIM1 control register 2 | 0x00 |
| 0x00 5252 | | TIM1_SMCR | TIM1 slave mode control register | 0x00 |
| 0x00 5253 | | TIM1_ETR | TIM1 external trigger register | 0x00 |
| 0x00 5254 | | TIM1_IER | TIM1 Interrupt enable register | 0x00 |
| 0x00 5255 | | TIM1_SR1 | TIM1 status register 1 | 0x00 |
| 0x00 5256 | | TIM1_SR2 | TIM1 status register 2 | 0x00 |
| 0x00 5257 | | TIM1_EGR | TIM1 event generation register | 0x00 |
| 0x00 5258 | | TIM1_CCMR1 | TIM1 capture/compare mode register 1 | 0x00 |
| 0x00 5259 | | TIM1_CCMR2 | TIM1 capture/compare mode register 2 | 0x00 |
| 0x00 525A | | TIM1_CCMR3 | TIM1 capture/compare mode register 3 | 0x00 |
| 0x00 525B | | TIM1_CCMR4 | TIM1 capture/compare mode register 4 | 0x00 |
| 0x00 525C | | TIM1_CCER1 | TIM1 capture/compare enable register 1 | 0x00 |
| 0x00 525D | | TIM1_CCER2 | TIM1 capture/compare enable register 2 | 0x00 |
| 0x00 525E | | TIM1_CNTRH | TIM1 counter high | 0x00 |
| 0x00 525F | | TIM1_CNTRL | TIM1 counter low | 0x00 |
| 0x00 5260 | | TIM1_PSCRH | TIM1 prescaler register high | 0x00 |
| 0x00 5261 | | TIM1_PSCRL | TIM1 prescaler register low | 0x00 |
| 0x00 5262 | | TIM1_ARRH | TIM1 auto-reload register high | 0xFF |
| 0x00 5263 | | TIM1_ARRL | TIM1 auto-reload register low | 0xFF |
| 0x00 5264 | | TIM1_RCR | TIM1 repetition counter register | 0x00 |
| 0x00 5265 | | TIM1_CCR1H | TIM1 capture/compare register 1 high | 0x00 |
| 0x00 5266 | | TIM1_CCR1L | TIM1 capture/compare register 1 low | 0x00 |
| 0x00 5267 | | TIM1_CCR2H | TIM1 capture/compare register 2 high | 0x00 |
| 0x00 5268 | | TIM1_CCR2L | TIM1 capture/compare register 2 low | 0x00 |
| 0x00 5269 | | TIM1_CCR3H | TIM1 capture/compare register 3 high | 0x00 |
| 0x00 526A | | TIM1_CCR3L | TIM1 capture/compare register 3 low | 0x00 |
| 0x00 526B | | TIM1_CCR4H | TIM1 capture/compare register 4 high | 0x00 |
| 0x00 526C | | TIM1_CCR4L | TIM1 capture/compare register 4 low | 0x00 |
| 0x00 526D | | TIM1_BKR | TIM1 break register | 0x00 |
| 0x00 526E | | TIM1_DTR | TIM1 dead-time register | 0x00 |
| 0x00 526F | | TIM1_OISR | TIM1 output idle state register | 0x00 |
| 0x00 5270 to 0x00 52FF | Reserved area (147 bytes) | | | |

Table 12. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5300 | TIM2 | TIM2_CR1 | TIM2 control register 1 | 0x00 |
| 0x00 5301 | | TIM2_IER | TIM2 interrupt enable register | 0x00 |
| 0x00 5302 | | TIM2_SR1 | TIM2 status register 1 | 0x00 |
| 0x00 5303 | | TIM2_SR2 | TIM2 status register 2 | 0x00 |
| 0x00 5304 | | TIM2_EGR | TIM2 event generation register | 0x00 |
| 0x00 5305 | | TIM2_CCMR1 | TIM2 capture/compare mode register 1 | 0x00 |
| 0x00 5306 | | TIM2_CCMR2 | TIM2 capture/compare mode register 2 | 0x00 |
| 0x00 5307 | | TIM2_CCMR3 | TIM2 capture/compare mode register 3 | 0x00 |
| 0x00 5308 | | TIM2_CCER1 | TIM2 capture/compare enable register 1 | 0x00 |
| 0x00 5309 | | TIM2_CCER2 | TIM2 capture/compare enable register 2 | 0x00 |
| 0x00 530A | | TIM2_CNTRH | TIM2 counter high | 0x00 |
| 0x00 530B | | TIM2_CNTRL | TIM2 counter low | 0x00 |
| 00 530C0x | | TIM2_PSCR | TIM2 prescaler register | 0x00 |
| 0x00 530D | | TIM2_ARRH | TIM2 auto-reload register high | 0xFF |
| 0x00 530E | | TIM2_ARRL | TIM2 auto-reload register low | 0xFF |
| 0x00 530F | | TIM2_CCR1H | TIM2 capture/compare register 1 high | 0x00 |
| 0x00 5310 | | TIM2_CCR1L | TIM2 capture/compare register 1 low | 0x00 |
| 0x00 5311 | | TIM2_CCR2H | TIM2 capture/compare reg. 2 high | 0x00 |
| 0x00 5312 | | TIM2_CCR2L | TIM2 capture/compare register 2 low | 0x00 |
| 0x00 5313 | | TIM2_CCR3H | TIM2 capture/compare register 3 high | 0x00 |
| 0x00 5314 | | TIM2_CCR3L | TIM2 capture/compare register 3 low | 0x00 |
| 0x00 5315 to 0x00 531F | Reserved area (11 bytes) | | | |

Table 12. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5320 | TIM3 | TIM3_CR1 | TIM3 control register 1 | 0x00 |
| 0x00 5321 | | TIM3_IER | TIM3 interrupt enable register | 0x00 |
| 0x00 5322 | | TIM3_SR1 | TIM3 status register 1 | 0x00 |
| 0x00 5323 | | TIM3_SR2 | TIM3 status register 2 | 0x00 |
| 0x00 5324 | | TIM3_EGR | TIM3 event generation register | 0x00 |
| 0x00 5325 | | TIM3_CCMR1 | TIM3 capture/compare mode register 1 | 0x00 |
| 0x00 5326 | | TIM3_CCMR2 | TIM3 capture/compare mode register 2 | 0x00 |
| 0x00 5327 | | TIM3_CCER1 | TIM3 capture/compare enable register 1 | 0x00 |
| 0x00 5328 | | TIM3_CNTRH | TIM3 counter high | 0x00 |
| 0x00 5329 | | TIM3_CNTRL | TIM3 counter low | 0x00 |
| 0x00 532A | | TIM3_PSCR | TIM3 prescaler register | 0x00 |
| 0x00 532B | | TIM3_ARRH | TIM3 auto-reload register high | 0xFF |
| 0x00 532C | | TIM3_ARRL | TIM3 auto-reload register low | 0xFF |
| 0x00 532D | | TIM3_CCR1H | TIM3 capture/compare register 1 high | 0x00 |
| 0x00 532E | | TIM3_CCR1L | TIM3 capture/compare register 1 low | 0x00 |
| 0x00 532F | | TIM3_CCR2H | TIM3 capture/compare register 2 high | 0x00 |
| 0x00 5330 | | TIM3_CCR2L | TIM3 capture/compare register 2 low | 0x00 |
| 0x00 5331 to 0x00 533F | Reserved area (15 bytes) | | | |
| 0x00 5340 | TIM4 | TIM4_CR1 | TIM4 control register 1 | 0x00 |
| 0x00 5341 | | TIM4_IER | TIM4 interrupt enable register | 0x00 |
| 0x00 5342 | | TIM4_SR | TIM4 status register | 0x00 |
| 0x00 5343 | | TIM4_EGR | TIM4 event generation register | 0x00 |
| 0x00 5344 | | TIM4_CNTR | TIM4 counter | 0x00 |
| 0x00 5345 | | TIM4_PSCR | TIM4 prescaler register | 0x00 |
| 0x00 5346 | | TIM4_ARR | TIM4 auto-reload register | 0xFF |
| 0x00 5347 to 0x00 53FF | Reserved area (185 bytes) | | | |

**Table 12. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5400 | ADC | ADC _CSR | ADC control/status register | 0x00 |
| 0x00 5401 | | ADC_CR1 | ADC configuration register 1 | 0x00 |
| 0x00 5402 | | ADC_CR2 | ADC configuration register 2 | 0x00 |
| 0x00 5403 | | ADC_CR3 | ADC configuration register 3 | 0x00 |
| 0x00 5404 | | ADC_DRH | ADC data register high | 0xXX |
| 0x00 5405 | | ADC_DRL | ADC data register low | 0xXX |
| 0x00 5406 | | ADC_TDRH | ADC Schmitt trigger disable register high | 0x00 |
| 0x00 5407 | | ADC_TDRL | ADC Schmitt trigger disable register low | 0x00 |
| 0x00 5408 to 0x00 57FF | Reserved area (1015 bytes) | | | |

1. Depends on the previous reset source.
2. Write only register.

**Table 13. CPU/SWIM/debug module/interrupt controller registers**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F00 | CPU(1) | A | Accumulator | 0x00 |
| 0x00 7F01 | | PCE | Program counter extended | 0x00 |
| 0x00 7F02 | | PCH | Program counter high | 0x80 |
| 0x00 7F03 | | PCL | Program counter low | 0x00 |
| 0x00 7F04 | | XH | X index register high | 0x00 |
| 0x00 7F05 | | XL | X index register low | 0x00 |
| 0x00 7F06 | | YH | Y index register high | 0x00 |
| 0x00 7F07 | | YL | Y index register low | 0x00 |
| 0x00 7F08 | | SPH | Stack pointer high | 0x17(2) |
| 0x00 7F09 | | SPL | Stack pointer low | 0xFF |
| 0x00 7F0A | | CC | Condition code register | 0x28 |
| 0x00 7F0B to 0x00 7F5F | Reserved area (85 bytes) | | | |
| 0x00 7F60 | CPU | CFG_GCR | Global configuration register | 0x00 |

**Table 13. CPU/SWIM/debug module/interrupt controller registers (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F70 | ITC | ITC_SPR1 | Interrupt software priority register 1 | 0xFF |
| 0x00 7F71 | | ITC_SPR2 | Interrupt software priority register 2 | 0xFF |
| 0x00 7F72 | | ITC_SPR3 | Interrupt software priority register 3 | 0xFF |
| 0x00 7F73 | | ITC_SPR4 | Interrupt software priority register 4 | 0xFF |
| 0x00 7F74 | | ITC_SPR5 | Interrupt software priority register 5 | 0xFF |
| 0x00 7F75 | | ITC_SPR6 | Interrupt software priority register 6 | 0xFF |
| 0x00 7F76 | | ITC_SPR7 | Interrupt software priority register 7 | 0xFF |
| 0x00 7F77 | | ITC_SPR8 | Interrupt software priority register 8 | 0xFF |
| 0x00 7F78 to 0x00 7F79 | Reserved area (2 bytes) | | | |
| 0x00 7F80 | SWIM | SWIM_CSR | SWIM control status register | 0x00 |
| 0x00 7F81 to 0x00 7F8F | Reserved area (15 bytes) | | | |
| 0x00 7F90 | DM | DM_BK1RE | DM breakpoint 1 register extended byte | 0xFF |
| 0x00 7F91 | | DM_BK1RH | DM breakpoint 1 register high byte | 0xFF |
| 0x00 7F92 | | DM_BK1RL | DM breakpoint 1 register low byte | 0xFF |
| 0x00 7F93 | | DM_BK2RE | DM breakpoint 2 register extended byte | 0xFF |
| 0x00 7F94 | | DM_BK2RH | DM breakpoint 2 register high byte | 0xFF |
| 0x00 7F95 | | DM_BK2RL | DM breakpoint 2 register low byte | 0xFF |
| 0x00 7F96 | | DM_CR1 | DM debug module control register 1 | 0x00 |
| 0x00 7F97 | | DM_CR2 | DM debug module control register 2 | 0x00 |
| 0x00 7F98 | | DM_CSR1 | DM debug module control/status register 1 | 0x10 |
| 0x00 7F99 | | DM_CSR2 | DM debug module control/status register 2 | 0x00 |
| 0x00 7F9A | | DM_ENFCTR | DM enable function register | 0xFF |
| 0x00 7F9B to 0x00 7F9F | Reserved area (5 bytes) | | | |

1. Accessible by debug module only
2. Product dependent value, see *Figure 8: Register and memory map*.

**Table 14. Temporary memory unprotection registers**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5800 | TMU | TMU_K1 | Temporary memory unprotection key register 1 | 0x00 |
| 0x00 5801 | | TMU_K2 | Temporary memory unprotection key register 2 | 0x00 |
| 0x00 5802 | | TMU_K3 | Temporary memory unprotection key register 3 | 0x00 |
| 0x00 5803 | | TMU_K4 | Temporary memory unprotection key register 4 | 0x00 |
| 0x00 5804 | | TMU_K5 | Temporary memory unprotection key register 5 | 0x00 |
| 0x00 5805 | | TMU_K6 | Temporary memory unprotection key register 6 | 0x00 |
| 0x00 5806 | | TMU_K7 | Temporary memory unprotection key register 7 | 0x00 |
| 0x00 5807 | | TMU_K8 | Temporary memory unprotection key register 8 | 0x00 |
| 0x00 5808 | | TMU_CSR | Temporary memory unprotection control and status register | 0x00 |

# 8 Interrupt table

**Table 15. STM8A interrupt table(1)**

| Priority | Source block | Description | Interrupt vector address | Wakeup from Halt | Comments |
|---|---|---|---|---|---|
| - | Reset | Reset | 0x00 8000 | Yes | - |
| - | TRAP | SW interrupt | 0x00 8004 | - | - |
| 0 | TLI | External top level interrupt | 0x00 8008 | - | - |
| 1 | AWU | Auto-wakeup from Halt | 0x00 800C | Yes | - |
| 2 | Clock controller | Main clock controller | 0x00 8010 | - | - |
| 3 | MISC | External interrupt E0 | 0x00 8014 | Yes | Port A interrupts |
| 4 | MISC | External interrupt E1 | 0x00 8018 | Yes | Port B interrupts |
| 5 | MISC | External interrupt E2 | 0x00 801C | Yes | Port C interrupts |
| 6 | MISC | External interrupt E3 | 0x00 8020 | Yes | Port D interrupts |
| 7 | MISC | External interrupt E4 | 0x00 8024 | Yes | Port E interrupts |
| 8 | Reserved | Reserved | 0x00 8028 | - | - |
| 9 | Reserved | Reserved | 0x00 802C | - | - |
| 10 | SPI | End of transfer | 0x00 8030 | Yes | - |
| 11 | Timer 1 | Update/overflow/ trigger/break | 0x00 8034 | - | - |
| 12 | Timer 1 | Capture/compare | 0x00 8038 | - | - |
| 13 | Timer 2 | Update/overflow | 0x00 803C | - | - |
| 14 | Timer 2 | Capture/compare | 0x00 8040 | - | - |
| 15 | Timer 3 | Update/overflow | 0x00 8044 | - | - |
| 16 | Timer 3 | Capture/compare | 0x00 8048 | - | - |
| 17 | USART | Tx complete | 0x00 804C | - | - |
| 18 | USART | Receive data full reg. | 0x00 8050 | - | - |
| 19 | $I^2C$ | $I^2C$ interrupts | 0x00 8054 | Yes | - |
| 20 | LINUART | Tx complete/error | 0x00 8058 | - | - |
| 21 | LINUART | Receive data full reg. | 0x00 805C | - | - |
| 22 | ADC | End of conversion | 0x00 8060 | - | - |
| 23 | Timer 4 | Update/overflow | 0x00 8064 | - | - |
| 24 | EEPROM | End of programming/ write in not allowed area | 0x00 8068 | - | - |

1. All unused interrupts must be initialized with ‘IRET’ for robust programming.

# 9 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Each option byte has to be stored twice, for redundancy, in a regular form (OPTx) and a complemented one (NOPTx), except for the ROP (read-out protection) option byte and option bytes 8 to 16.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 16: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be changed in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (PM0047) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

**Table 16. Option bytes**

| Addr. | Option name | Option byte no. | Option bits | | | | | | | | Factory default setting |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x00 4800 | Read-out protection (ROP) | OPT0 | ROP[7:0] | | | | | | | | 0x00 |
| 0x00 4801 | User boot code (UBC) | OPT1 | UBC[7:0] | | | | | | | | 0x00 |
| 0x00 4802 | | NOPT1 | NUBC[7:0] | | | | | | | | 0xFF |
| 0x00 4803 | Alternate function remapping (AFR) | OPT2 | AFR7 | AFR6 | AFR5 | AFR4 | AFR3 | AFR2 | AFR1 | AFR0 | 0x00 |
| 0x00 4804 | | NOPT2 | NAFR7 | NAFR6 | NAFR5 | NAFR4 | NAFR3 | NAFR2 | NAFR1 | NAFR0 | 0xFF |
| 0x00 4805 | Watchdog option | OPT3 | Reserved | | | | LSI_EN | IWDG_HW | WWDG_HW | WWDG_HALT | 0x00 |
| 0x00 4806 | | NOPT3 | Reserved | | | | NLSI_EN | NIWDG_HW | NWWDG_HW | NWWG_HALT | 0xFF |
| 0x00 4807 | Clock option | OPT4 | Reserved | | | | EXTCLK | CKAWUSEL | PRSC1 | PRSC0 | 0x00 |
| 0x00 4808 | | NOPT4 | Reserved | | | | NEXTCLK | NCKAWUSEL | NPRSC1 | NPRSC0 | 0xFF |
| 0x00 4809 | HSE clock startup | OPT5 | HSECNT[7:0] | | | | | | | | 0x00 |
| 0x00 480A | | NOPT5 | NHSECNT[7:0] | | | | | | | | 0xFF |

**Table 16. Option bytes (continued)**

| Addr. | Option name | Option byte no. | Option bits | | | | | | | | Factory default setting |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x00 480B | TMU | OPT6 | TMU[3:0] | | | | | | | | 0x00 |
| 0x00 480C | | NOPT6 | NTMU[3:0] | | | | | | | | 0xFF |
| 0x00 480D | Flash wait states | OPT7 | Reserved | | | | | | | WAIT STATE | 0x00 |
| 0x00 480E | | NOPT7 | Reserved | | | | | | | NWAIT STATE | 0xFF |
| 0x00 480F | Reserved | | | | | | | | | | |
| 0x00 4810 | TMU | OPT8 | TMU_KEY 1 [7:0] | | | | | | | | 0x00 |
| 0x00 4811 | | OPT9 | TMU_KEY 2 [7:0] | | | | | | | | 0x00 |
| 0x00 4812 | | OPT10 | TMU_KEY 3 [7:0] | | | | | | | | 0x00 |
| 0x00 4813 | | OPT11 | TMU_KEY 4 [7:0] | | | | | | | | 0x00 |
| 0x00 4814 | | OPT12 | TMU_KEY 5 [7:0] | | | | | | | | 0x00 |
| 0x00 4815 | | OPT13 | TMU_KEY 6 [7:0] | | | | | | | | 0x00 |
| 0x00 4816 | | OPT14 | TMU_KEY 7 [7:0] | | | | | | | | 0x00 |
| 0x00 4817 | | OPT15 | TMU_KEY 8 [7:0] | | | | | | | | 0x00 |
| 0x00 4818 | | OPT16 | TMU_MAXATT [7:0] | | | | | | | | 0xC7 |
| 0x00 4819 to 487D | Reserved | | | | | | | | | | |
| 0x00 487E | Boot-loader(1) | OPT17 | BL [7:0] | | | | | | | | 0x00 |
| 0x00 487F | | NOPT 17 | NBL [7:0] | | | | | | | | 0xFF |

1. This option consists of two bytes that must have a complementary value in order to be valid. If the option is invalid, it has no effect on EMC reset.

**Table 17. Option byte description**

| Option byte no. | Description |
|---|---|
| OPT0 | **ROP[7:0]: Memory readout protection (ROP)**<br>0xAA: Enable readout protection (write access via SWIM protocol)<br>*Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.* |
| OPT1 | **UBC[7:0]: User boot code area**<br>0x00: No UBC, no write-protection<br>0x01: Page 0 to 1 defined as UBC, memory write-protected<br>0x02: Page 0 to 3 defined as UBC, memory write-protected<br>0x03 to 0xFF: Pages 4 to 255 defined as UBC, memory write-protected<br>*Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.* |
| OPT2 | **AFR7: Alternate function remapping option 7**<br>0: Port D4 alternate function = TIM2_CH1<br>1: Port D4 alternate function = BEEP<br>**AFR6: Alternate function remapping option 6**<br>0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4<br>1: Port B5 alternate function = $I^2C$_SDA, port B4 alternate function = $I^2C$_SCL.<br>**AFR5: Alternate function remapping option 5**<br>0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0.<br>1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N.<br>**AFR4: Alternate function remapping option 4**<br>0: Port D7 alternate function = TLI<br>1: Reserved<br>**AFR3: Alternate function remapping option 3**<br>0: Port D0 alternate function = TIM3_CH2<br>1: Port D0 alternate function = TIM1_BKIN<br>**AFR2: Alternate function remapping option 2**<br>0: Port D0 alternate function = TIM3_CH2<br>1: Port D0 alternate function = CLK_CCO<br>*Note: AFR2 option has priority over AFR3 if both are activated*<br>**AFR1: Alternate function remapping option 1**<br>0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1.<br>1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3.<br>**AFR0: Alternate function remapping option 0**<br>0: Port D3 alternate function = TIM2_CH2<br>1: Port D3 alternate function = ADC_ETR |

Table 17. Option byte description (continued)

| Option byte no. | Description |
|---|---|
| OPT3 | **LSI_EN: Low speed internal clock enable**<br>0: LSI clock is not available as CPU clock source<br>1: LSI clock is available as CPU clock source |
| | **IWDG_HW: Independent watchdog**<br>0: IWDG Independent watchdog activated by software<br>1: IWDG Independent watchdog activated by hardware |
| | **WWDG_HW: Window watchdog activation**<br>0: WWDG window watchdog activated by software<br>1: WWDG window watchdog activated by hardware |
| | **WWDG_HALT: Window watchdog reset on Halt**<br>0: No reset generated on Halt if WWDG active<br>1: Reset generated on Halt if WWDG active |
| OPT4 | **EXTCLK: External clock selection**<br>0: External crystal connected to OSCIN/OSCOUT<br>1: External clock signal on OSCIN |
| | **CKAWUSEL: Auto-wakeup unit/clock**<br>0: LSI clock source selected for AWU<br>1: HSE clock with prescaler selected as clock source for AWU |
| | **PRSC[1:0]: AWU clock prescaler**<br>00: 24 MHz to 128 kHz prescaler<br>01: 16 MHz to 128 kHz prescaler<br>10: 8 MHz to 128 kHz prescaler<br>11: 4 MHz to 128 kHz prescaler |
| OPT5 | **HSECNT[7:0]: HSE crystal oscillator stabilization time**<br>This configures the stabilization time to 0.5, 8, 128, and 2048 HSE cycles with corresponding option byte values of 0xE1, 0xD2, 0xB4, and 0x00. |
| OPT6 | **TMU**[3:0]: Enable temporary memory unprotection<br>0101: TMU disabled (permanent ROP).<br>Any other value: TMU enabled. |
| OPT7 | **WAIT STATE: Wait state configuration**<br>This option configures the number of wait states inserted when reading from the Flash/data EEPROM memory.<br>0: No wait state<br>1: One wait state |
| OPT8 | **TMU_KEY 1 [7:0]: Temporary unprotection key 0**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT9 | **TMU_KEY 2 [7:0]: Temporary unprotection key 1**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT10 | **TMU_KEY 3 [7:0]: Temporary unprotection key 2**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT11 | **TMU_KEY 4 [7:0]: Temporary unprotection key 3**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |

Table 17. Option byte description (continued)

| Option byte no. | Description |
|---|---|
| OPT12 | **TMU_KEY 5 [7:0]: Temporary unprotection key 4**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT13 | **TMU_KEY 6 [7:0]: Temporary unprotection key 5**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT14 | **TMU_KEY 7 [7:0]: Temporary unprotection key 6**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT15 | **TMU_KEY 8 [7:0]: Temporary unprotection key 7**<br>Temporary unprotection key: Must be different from 0x00 or 0xFF |
| OPT16 | **TMU_MAXATT [7:0]: TMU access failure counter**<br>TMU_MAXATT can be initialized with the desired value only if TMU is disabled (TMU[3:0]=0101 in OPT6 option byte).<br>When TMU is enabled, any attempt to temporary remove the readout protection by using wrong key values increments the counter.<br>When the option byte value reaches 0x08, the Flash memory and data EEPROM are erased. |
| OPT17 | **BL[7:0]: Bootloader enable**<br>If this option byte is set to 0x55 (complementary value 0xAA) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0560). |

# 10 Electrical characteristics

## 10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to $V_{SS}$.

### 10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = -40 °C, $T_A$ = 25 °C, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

### 10.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

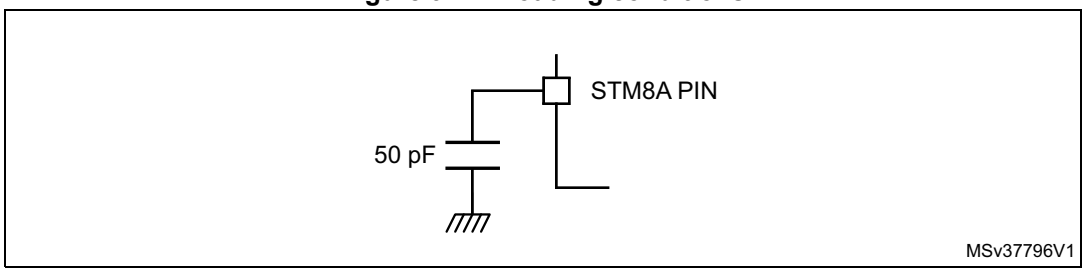
### 10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

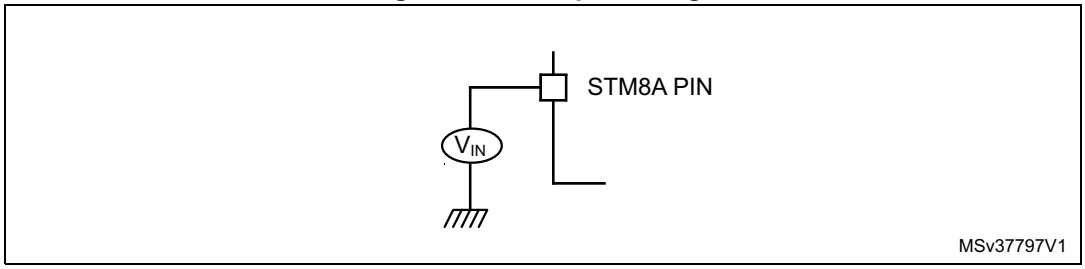
**Figure 9. Pin loading conditions**



### 10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

**Figure 10. Pin input voltage**




## 10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability. The device's mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

**Table 18. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DDx}$ - $V_{SS}$ | Supply voltage (including $V_{DDA}$ and $V_{DDIO}$)(1) | -0.3 | 6.5 | V |
| $V_{IN}$ | Input voltage on true open drain pins (PE1, PE2)(2) | $V_{SS}$ - 0.3 | 6.5 | |
| | Input voltage on any other pin(2) | $V_{SS}$ - 0.3 | $V_{DD}$ + 0.3 | |
| $\lvert V_{DDx} - V_{DD} \rvert$ | Variations between different power pins | - | 50 | mV |
| $\lvert V_{SSx} - V_{SS} \rvert$ | Variations between all the different ground pins | - | 50 | |
| $V_{ESD}$ | Electrostatic discharge voltage | see *Absolute maximum ratings (electrical sensitivity) on page 88* | | |

1. All power ($V_{DD}$, $V_{DDIO}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSIO}$, $V_{SSA}$) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding $V_{IN}$ maximum must always be respected

**Table 19. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDDIO}$ | Total current into $V_{DDIO}$ power lines (source)(1)(2)(3) | 100 | mA |
| $I_{VSSIO}$ | Total current out of $V_{SS\ IO}$ ground lines (sink)(1)(2)(3) | 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 20 | |
| | Output current source by any I/Os and control pin | -20 | |
| $I_{INJ(PIN)}$(4) | Injected current on any pin | ±10 | |
| $I_{INJ(TOT)}$ | Sum of injected currents | 50 | |

1. All power ($V_{DD}$, $V_{DDIO}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSIO}$, $V_{SSA}$) pins must always be connected to the external supply.
2. The total limit applies to the sum of operation and injected currents.
3. $V_{DDIO}$ includes the sum of the positive injection currents. $V_{SSIO}$ includes the sum of the negative injection currents.
4. This condition is implicitly insured if VIN maximum is respected. If VIN maximum cannot be respected, the injection current must be limited externally to the IINJ(PIN) value. A positive injection is induced by VIN > VDD while a negative injection is induced by VIN < VSS. For true open-drain pads, there is no positive injection current allowed and the corresponding VIN maximum must always be respected.

**Table 20. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to 150 | °C |
| $T_J$ | Maximum junction temperature | 160 | |

**Table 21. Operating lifetime(1)**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| OLF | Conforming to AEC-Q100 rev G | -40 to 125 °C | Grade 1 |
| | | -40 to 150 °C | Grade 0 |

1. For detailed mission profile analysis, please contact the nearest ST Sales Office.

## 10.3 Operating conditions

**Table 22. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CPU}$ | Internal CPU clock frequency | 1 wait state $T_A$ = -40 °C to 150 °C | 16 | 24 | MHz |
| | | 0 wait state $T_A$ = -40 °C to 150 °C | 0 | 16 | |
| $V_{DD}/V_{DDIO}$ | Standard operating voltage | - | 3.0 | 5.5 | V |
| $V_{CAP}$(1) | $C_{EXT}$: capacitance of external capacitor | - | 470 | 3300 | nF |
| | ESR of external capacitor | at 1 MHz(2) | - | 0.3 | Ω |
| | ESL of external capacitor | | - | 15 | nH |
| $T_A$ | Ambient temperature | Suffix A | - 40 | 85 | °C |
| | | Suffix C | | 125 | |
| | | Suffix D | | 150 | |
| $T_J$ | Junction temperature range | Suffix A | - 40 | 90 | |
| | | Suffix C | | 130 | |
| | | Suffix D | | 155 | |

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for $V_{CAP}$ parameters is given by design of internal regulator.

**Figure 11. $f_{CPUmax}$ versus $V_{DD}$**

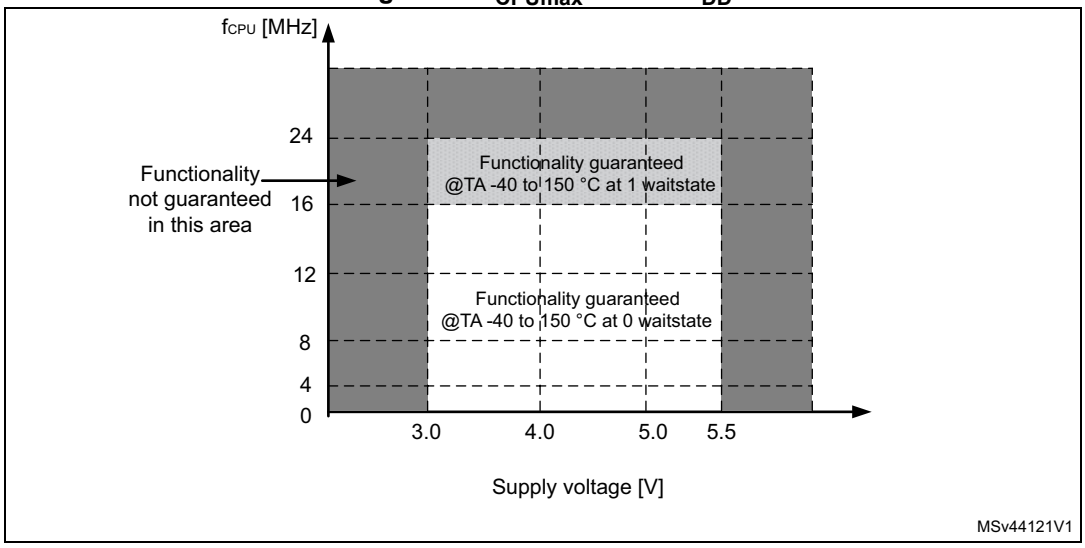


**Table 23. Operating conditions at power-up/power-down**

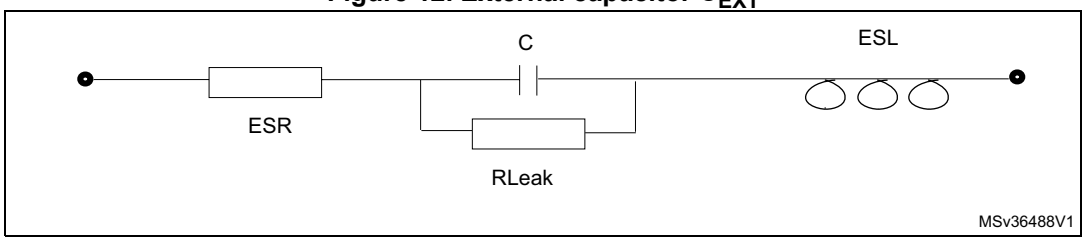
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | - | 2(1) | - | ∞ | µs/V |
| | $V_{DD}$ fall time rate | - | 2(1) | - | ∞ | |
| $t_{TEMP}$ | Reset release delay | $V_{DD}$ rising | - | 1 | 1.7 | ms |
| | Reset generation delay | $V_{DD}$ falling | - | 3 | - | µs |
| $V_{IT+}$ | Power-on reset threshold(2) (3) | - | 2.65 | 2.8 | 2.95 | V |
| $V_{IT-}$ | Brown-out reset threshold | - | 2.58 | 2.73 | 2.88 | |
| $V_{HYS(BOR)}$ | Brown-out reset hysteresis | - | - | 70(1) | - | mV |

1. Guaranteed by design, not tested in production.
2. If $V_{DD}$ is below 3 V, the code execution is guaranteed above the $V_{IT-}$ and $V_{IT+}$ thresholds. RAM content is kept. The EEPROM programming sequence must not be initiated.
3. There is inrush current into $V_{DD}$ present after device power on to charge $C_{EXT}$ capacitor. This inrush energy depends from $C_{EXT}$ capacitor value. For example, a $C_{EXT}$ of 1 µF requires Q=1 µF x 1.8 V = 1.8 µC.

### 10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor $C_{EXT}$ to the $V_{CAP}$ pin. $C_{EXT}$ is specified in *Table 22*. Care should be taken to limit the series inductance to less than 15 nH.

**Figure 12. External capacitor $C_{EXT}$**




1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

### 10.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 59* and *Figure 10 on page 60*.

If not explicitly stated, general conditions of temperature and voltage apply.

**Table 24. Total current consumption in Run, Wait and Slow mode. General conditions for $V_{DD}$ apply, $T_A$ = -40 °C to 150 °C**

| Symbol | Parameter | Conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(RUN)}$(1) | Supply current in Run mode | All peripherals clocked, code executed from Flash program memory, HSE external clock (without resonator) | $f_{CPU}$ = 24 MHz 1 ws | 8.8 | 16.9(2) | mA |
| | | | $f_{CPU}$ = 16 MHz | 7.5 | 14.1 | |
| | | | $f_{CPU}$ = 8 MHz | 4.1 | 7.5(2) | |
| | | | $f_{CPU}$ = 4 MHz | 2.5 | 4.2(2) | |
| | | | $f_{CPU}$ = 2 MHz | 1.6 | 2.6 | |
| $I_{DD(RUN)}$(1) | Supply current in Run mode | All peripherals clocked, code executed from RAM, HSE external clock (without resonator) | $f_{CPU}$ = 24 MHz | 4.5 | 6.1(2) | |
| | | | $f_{CPU}$ = 16 MHz | 3.8 | 5.1 | |
| | | | $f_{CPU}$ = 8 MHz | 2.3 | 3.1(2) | |
| | | | $f_{CPU}$ = 4 MHz | 1.5 | 2.1(2) | |
| | | | $f_{CPU}$ = 2 MHz | 1.1 | 1.6 | |
| $I_{DD(WFI)}$(1) | Supply current in Wait mode | CPU stopped, all peripherals off, HSE external clock | $f_{CPU}$ = 24 MHz | 2.5 | 3.2(2) | |
| | | | $f_{CPU}$ = 16 MHz | 1.75 | 2.6 | |
| | | | $f_{CPU}$ = 8 MHz | 1.25 | 2.0(2) | |
| | | | $f_{CPU}$ = 4 MHz | 1.0 | 1.7(2) | |
| | | | $f_{CPU}$ = 2 MHz | 0.90 | 1.6 | |
| $I_{DD(SLOW)}$(1) | Supply current in Slow mode | $f_{CPU}$ scaled down, all peripherals off, code executed from RAM | External clock 16 MHz $f_{CPU}$ = 125 kHz | 1.60 | 2.05 | |
| | | | LSI internal RC $f_{CPU}$ = 128 kHz | 1.60 | 1.90(2) | |

1. The current due to I/O utilization is not taken into account in these values.
2. Guaranteed by design, not tested in production.

**Table 25. Total current consumption in Halt and Active-halt modes. General conditions for $V_{DD}$ applied. $T_A$ = -40 °C to 55 °C unless otherwise stated**

| Symbol | Parameter | Conditions | | | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | Main voltage regulator (MVR)(1) | Flash mode(2) | Clock source and temperature condition | | | |
| $I_{DD(H)}$ | Supply current in Halt mode | Off | Power-down | Clocks stopped | 105 | 135(3) | µA |
| | | | | Clocks stopped, $T_A$ = 25 °C | 105 | 125 | |
| $I_{DD(AH)}$ | Supply current in Active-halt mode with regulator on | On | Power-down | External clock 16 MHz $f_{MASTER}$ = 125 kHz | 870 | 1000(3) | |
| | | | | LSI clock 128 kHz | 250 | 330(3) | |
| | Supply current in Active-halt mode with regulator off | Off | Power-down | LSI clock 128 kHz | 125 | 142(3) | |
| | | | | LSI clock 128 kHz, $T_A$ = 25 °C | 125 | 130 | |
| $t_{WU(AH)}$ | Wakeup time from Active-halt mode with regulator on | On | Operating mode | $T_A$ = -40 to 150 °C | 10 | 30(3) | µs |
| | Wakeup time from Active-halt mode with regulator off | Off | | | 50 | 80(3) | |

1. Configured by the REGAH bit in the CLK_ICKR register.
2. Configured by the AHALT bit in the FLASH_CR1 register.
3. Guaranteed by characterization results, not tested in production.

## Current consumption for on-chip peripherals

**Table 26. Oscillator current consumption**

| Symbol | Parameter | Conditions | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(OSC)}$ | HSE oscillator current consumption(2) | Quartz or ceramic resonator, CL = 33 pF $V_{DD}$ = 5 V | $f_{OSC}$ = 24 MHz | 1 | 2.0(3) | mA |
| | | | $f_{OSC}$ = 16 MHz | 0.6 | - | |
| | | | $f_{OSC}$ = 8 MHz | 0.57 | - | |
| $I_{DD(OSC)}$ | HSE oscillator current consumption(2) | Quartz or ceramic resonator, CL = 33 pF $V_{DD}$ = 3.3 V | $f_{OSC}$ = 24 MHz | 0.5 | 1.0(3) | |
| | | | $f_{OSC}$ = 16 MHz | 0.25 | - | |
| | | | $f_{OSC}$ = 8 MHz | 0.18 | - | |

1. During startup, the oscillator current consumption may reach 6 mA.
2. The supply current of the oscillator can be further optimized by selecting a high quality resonator with small $R_m$ value. Refer to crystal manufacturer for more details
3. Informative data.

**Table 27. Programming current consumption**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{DD(PROG)}$ | Programming current | $V_{DD}$ = 5 V, -40 °C to 150 °C, erasing and programming data or Flash program memory | 1.0 | 1.7 | mA |

**Table 28. Typical peripheral current consumption $V_{DD}$ = 5.0 V(1)**

| Symbol | Parameter | Typ. $f_{master}$ = 2 MHz | Typ. $f_{master}$ = 16 MHz | Typ. $f_{master}$ =24 MHz | Unit |
|---|---|---|---|---|---|
| $I_{DD(TIM1)}$ | TIM1 supply current(2) | 0.03 | 0.23 | 0.34 | mA |
| $I_{DD(TIM2)}$ | TIM2 supply current (2) | 0.02 | 0.12 | 0.19 | |
| $I_{DD(TIM3)}$ | TIM3 supply current(2) | 0.01 | 0.1 | 0.16 | |
| $I_{DD(TIM4)}$ | TIM4 supply current(2) | 0.004 | 0.03 | 0.05 | |
| $I_{DD(USART)}$ | USART supply current(2) | 0.03 | 0.09 | 0.15 | |
| $I_{DD(LINUART)}$ | LINUART supply current(2) | 0.03 | 0.11 | 0.18 | |
| $I_{DD(SPI)}$ | SPI supply current(2) | 0.01 | 0.04 | 0.07 | |
| $I_{DD(I^2C)}$ | $I^2C$ supply current(2) | 0.02 | 0.06 | 0.91 | |
| $I_{DD(AWU)}$ | AWU supply current(2) | 0.003 | 0.02 | 0.05 | |
| $I_{DD(TOT_DIG)}$ | All digital peripherals on | 0.22 | 1 | 2.4 | |
| $I_{DD(ADC)}$ | ADC supply current when converting(3) | 0.93 | 0.95 | 0.96 | |

1. Typical values not tested in production. Since the peripherals are powered by an internally regulated, constant digital supply voltage, the values are similar in the full supply voltage range.
2. Data based on a differential $I_{DD}$ measurement between no peripheral clocked and a single active peripheral. This measurement does not include the pad toggling consumption.
3. Data based on a differential $I_{DD}$ measurement between reset configuration and continuous A/D conversions.

### Current consumption curves

*Figure 13* to *Figure 18* show typical current consumption measured with code executing in RAM.

**Figure 13. Typ. $I_{DD(RUN)HSE}$ vs. $V_{DD}$ @$f_{CPU}$ = 16 MHz, peripherals = on**

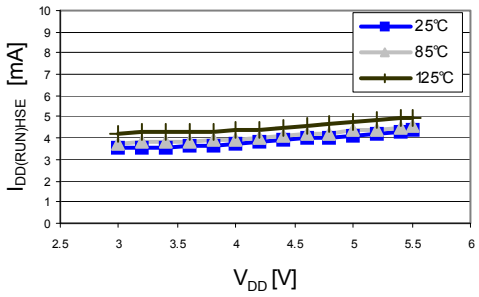



**Figure 14. Typ. $I_{DD(RUN)HSE}$ vs. $f_{CPU}$ @ $V_{DD}$ = 5.0 V, peripherals = on**

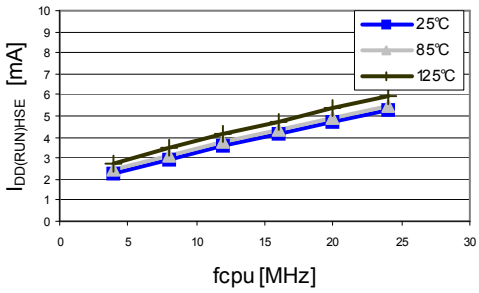



**Figure 15. Typ. $I_{DD(RUN)HSI}$ vs. $V_{DD}$ @ $f_{CPU}$ = 16 MHz, peripherals = off**

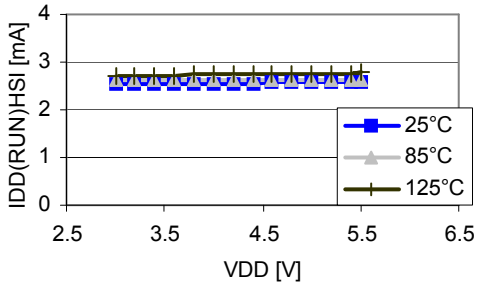



**Figure 16. Typ. $I_{DD(WFI)HSE}$ vs. $V_{DD}$ @ $f_{CPU}$ = 16 MHz, peripherals = on**

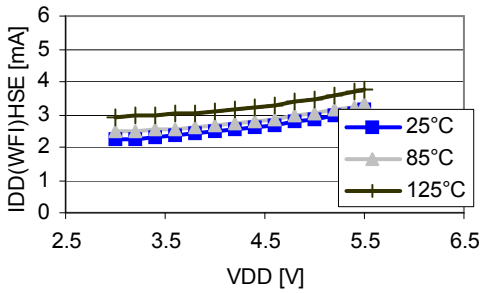



**Figure 17. Typ. $I_{DD(WFI)HSE}$ vs. $f_{CPU}$ @ $V_{DD}$ = 5.0 V, peripherals = on**

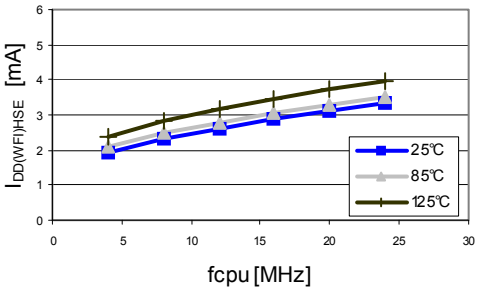
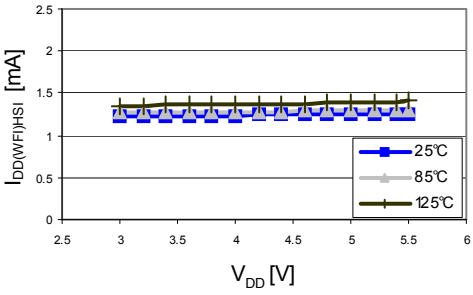



**Figure 18. Typ. $I_{DD(WFI)HSI}$ vs. $V_{DD}$ @ $f_{CPU}$ = 16 MHz, peripherals = off**



### 10.3.3 External clock sources and timing characteristics

#### HSE external clock

An HSE clock can be generated by feeding an external clock signal of up to 24 MHz to the OSCIN pin.

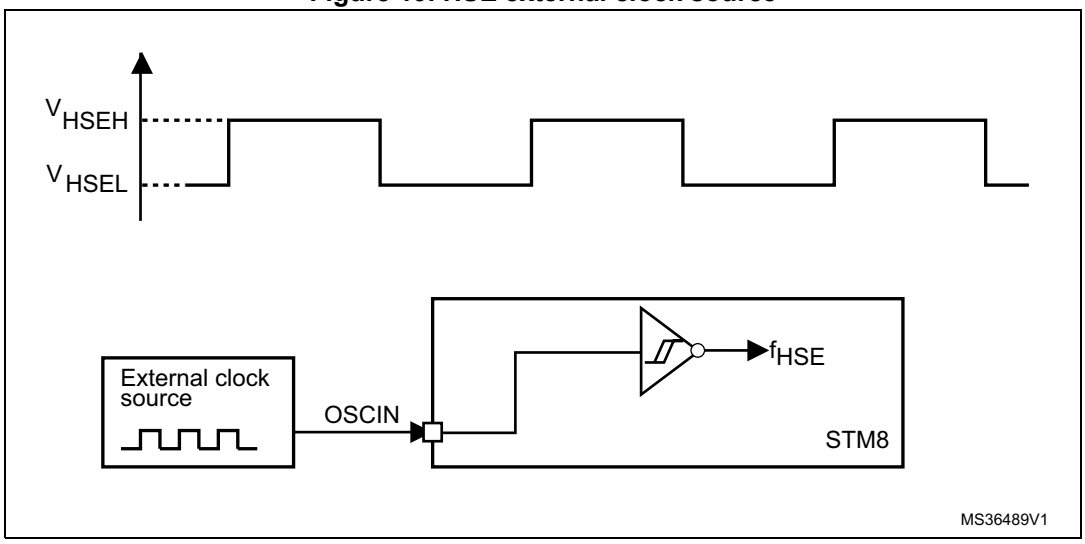
Clock characteristics are subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 29. HSE external clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE_ext}$ | User external clock source frequency | $T_A$ = -40 °C to 150 °C | 0(1) | - | 24 | MHz |
| $V_{HSEdHL}$ | Comparator hysteresis | - | 0.1 x $V_{DD}$ | - | - | V |
| $V_{HSEH}$ | OSCIN high-level input pin voltage | - | 0.7 x $V_{DD}$ | - | $V_{DD}$ | |
| $V_{HSEL}$ | OSCIN low-level input pin voltage | - | $V_{SS}$ | - | 0.3 x $V_{DD}$ | |
| $I_{LEAK_HSE}$ | OSCIN input leakage current | $V_{SS} < V_{IN} < V_{DD}$ | -1 | - | +1 | µA |

1. If CSS is used, the external clock must have a frequency above 500 kHz.

**Figure 19. HSE external clock source**




#### HSE crystal/ceramic resonator oscillator

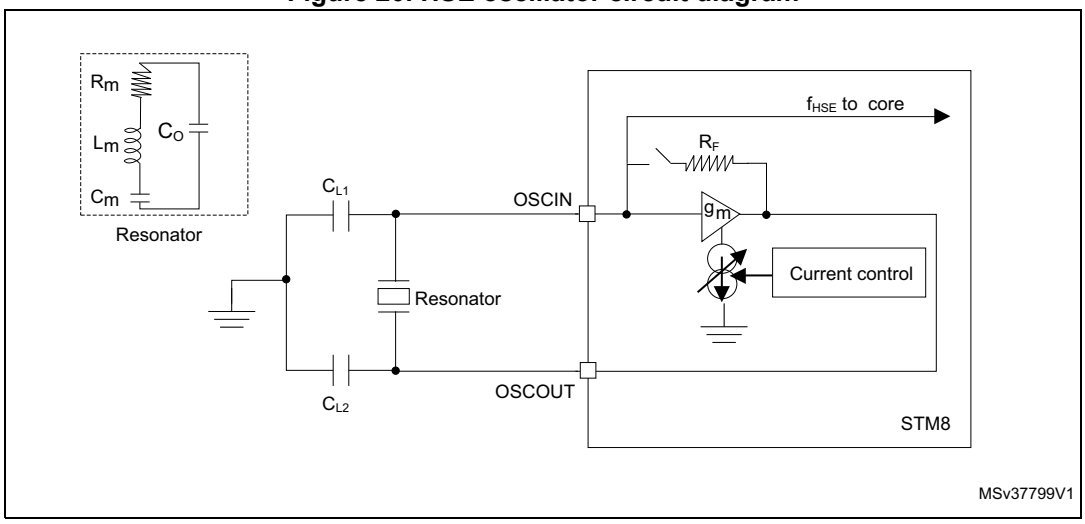
The HSE clock can be supplied using a crystal/ceramic resonator oscillator of up to 24 MHz. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

**Table 30. HSE oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | - | - | 220 | - | kΩ |
| $C_{L1}/C_{L2}$ (1) | Recommended load capacitance | - | - | - | 20 | pF |
| $g_m$ | Oscillator trans conductance | - | 5 | - | - | mA/V |
| $t_{SU(HSE)}$ (2) | Startup time | $V_{DD}$ is stabilized | - | 2.8 | - | ms |

1. The oscillator needs two load capacitors, $C_{L1}$ and $C_{L2}$, to act as load for the crystal. The total load capacitance ($C_{Load}$) is $(C_{L1} * C_{L2})/(C_{L1} + C_{L2})$. If $C_{L1} = C_{L2}$, $C_{load} = C_{L1/2}$. Some oscillators have built-in load capacitors, $C_{L1}$ and $C_{L2}$.
2. This value is the startup time, measured from the moment it is enabled (by software) until a stabilized 24 MHz oscillation is reached. It can vary with the crystal type that is used.

**Figure 20. HSE oscillator circuit diagram**




## HSE oscillator critical $g_m$ formula

The crystal characteristics have to be checked with the following formula:

**Equation 1**

$$g_m \gg g_{mcrit}$$

where $g_{mcrit}$ can be calculated with the crystal parameters as follows:

**Equation 2**

$$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$$

**$R_m$**: Notional resistance (see crystal specification)
**$L_m$**: Notional inductance (see crystal specification)
**$C_m$**: Notional capacitance (see crystal specification)
**Co**: Shunt capacitance (see crystal specification)
**$C_{L1} = C_{L2} = C$**: Grounded external capacitance

### 10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$.

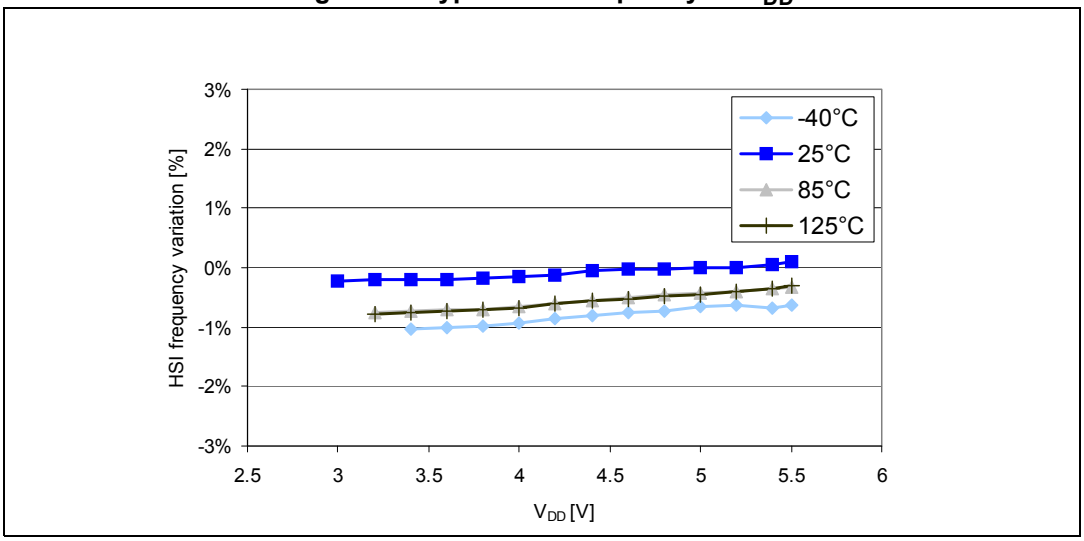
#### High-speed internal RC oscillator (HSI)

**Table 31. HSI oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 16 | - | MHz |
| $ACC_{HS}$ | HSI oscillator user trimming accuracy | Trimmed by the application for any $V_{DD}$ and $T_A$ conditions | -1 | - | 1 | % |
| | HSI oscillator accuracy (factory calibrated) | $V_{DD} = 3.0\ V \leq V_{DD} \leq 5.5\ V$, $-40\ °C \leq T_A \leq 150\ °C$ | -5 | - | 5 | |
| $t_{su(HSI)}$ | HSI oscillator wakeup time | - | - | - | 2(1) | µs |

1. Guaranteed by characterization results, not tested in production.

**Figure 21. Typical HSI frequency vs $V_{DD}$**



### Low-speed internal RC oscillator (LSI)

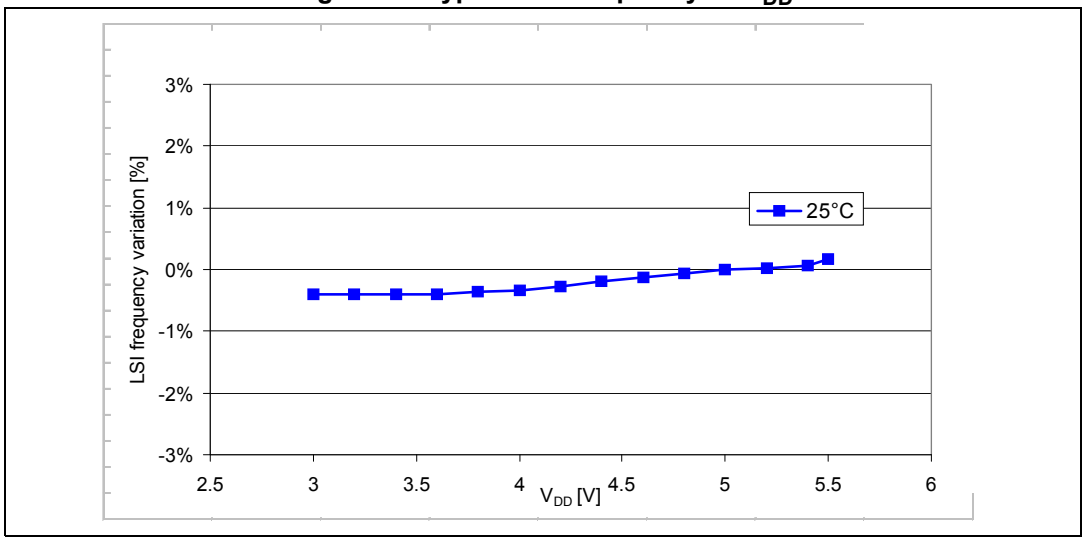
Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 32. LSI oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | Frequency | - | 112 | 128 | 144 | kHz |
| $t_{su(LSI)}$ | LSI oscillator wakeup time | - | - | - | 7(1) | µs |

1. Guaranteed by characterization results, not tested in production.

**Figure 22. Typical LSI frequency vs $V_{DD}$**



## 10.3.5 Memory characteristics

### Flash program memory/data EEPROM memory

General conditions: $T_A$ = -40 °C to 150 °C.

**Table 33. Flash program memory/data EEPROM memory**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage (all modes, execution/write/erase) | $f_{CPU}$ is 16 to 24 MHz with 1 ws<br>$f_{CPU}$ is 0 to 16 MHz with 0 ws | 3.0 | - | 5.5 | V |
| $V_{DD}$ | Operating voltage (code execution) | $f_{CPU}$ is 16 to 24 MHz with 1 ws<br>$f_{CPU}$ is 0 to 16 MHz with 0 ws | 2.6 | - | 5.5 | |
| $t_{prog}$ | Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes) | - | - | 6 | 6.6 | ms |
| | Fast programming time for 1 block (128 bytes) | - | - | 3 | 3.3 | |
| $t_{erase}$ | Erase time for 1 block (128 bytes) | - | - | 3 | 3.3 | |

1. Guaranteed by characterization results, not tested in production.

**Table 34. Flash program memory**

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{WE}$ | Temperature for writing and erasing | - | -40 | 150 | °C |
| $N_{WE}$ | Flash program memory endurance (erase/write cycles)(1) | $T_A$ = 25 °C | 1000 | - | cycles |
| $t_{RET}$ | Data retention time | $T_A$ = 25 °C | 40 | - | years |
| | | $T_A$ = 55 °C | 20 | - | |

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.

**Table 35. Data memory**

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{WE}$ | Temperature for writing and erasing | - | -40 | 150 | °C |
| $N_{WE}$ | Data memory endurance(1) (erase/write cycles) | $T_A$ = 25 °C | 300 k | - | cycles |
| | | $T_A$ = -40°C to 125 °C | 100 k(2) | - | |
| $t_{RET}$ | Data retention time | $T_A$ = 25 °C | 40(2)(3) | - | years |
| | | $T_A$ = 55 °C | 20(2)(3) | - | |

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

## 10.3.6 I/O port pin characteristics

### General characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 36. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage | - | -0.3 V | | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | High-level input voltage | | 0.7 x $V_{DD}$ | | $V_{DD}$ + 0.3 V | |
| $V_{hys}$ | Hysteresis(1) | | - | 0.1 x $V_{DD}$ | - | |
| $V_{OH}$ | High-level output voltage | Standard I/0, $V_{DD}$ = 5 V, I = 3 mA | $V_{DD}$ - 0.5 V | - | - | |
| | | Standard I/0, $V_{DD}$ = 3 V, I = 1.5 mA | $V_{DD}$ - 0.4 V | - | - | |
| $V_{OL}$ | Low-level output voltage | High sink and true open drain I/0, $V_{DD}$ = 5 V I = 8 mA | - | - | 0.5 | V |
| | | Standard I/0, $V_{DD}$ = 5 V I = 3 mA | - | - | 0.6 | |
| | | Standard I/0, $V_{DD}$ = 3 V I = 1.5 mA | - | - | 0.4 | |
| $R_{pu}$ | Pull-up resistor | $V_{DD}$ = 5 V, $V_{IN}$ = $V_{SS}$ | 35 | 50 | 65 | kΩ |
| $t_R$, $t_F$ | Rise and fall time (10% - 90%) | Fast I/Os Load = 50 pF | - | - | 35(2) | ns |
| | | Standard and high sink I/Os Load = 50 pF | - | - | 125(2) | |
| | | Fast I/Os Load = 20 pF | - | - | 20(2) | |
| | | Standard and high sink I/Os Load = 20 pF | - | - | 50(2) | |
| $I_{lkg}$ | Digital input pad leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |
| $I_{lkg\ ana}$ | Analog input pad leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < $T_A$ < 125 °C | - | - | ±250 | nA |
| | | $V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < $T_A$ < 150 °C | - | - | ±500 | |
| $I_{lkg(inj)}$ | Leakage current in adjacent I/O(3) | Injection current ±4 mA | - | - | ±1(3) | µA |
| $I_{DDIO}$ | Total current on either $V_{DDIO}$ or $V_{SSIO}$ | Including injection currents | - | - | 60 | mA |

1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.

2. Guaranteed by design.
3. Guaranteed by characterization results, not tested in production.

**Figure 23. Typical $V_{IL}$ and $V_{IH}$ vs $V_{DD}$ @ four temperatures**

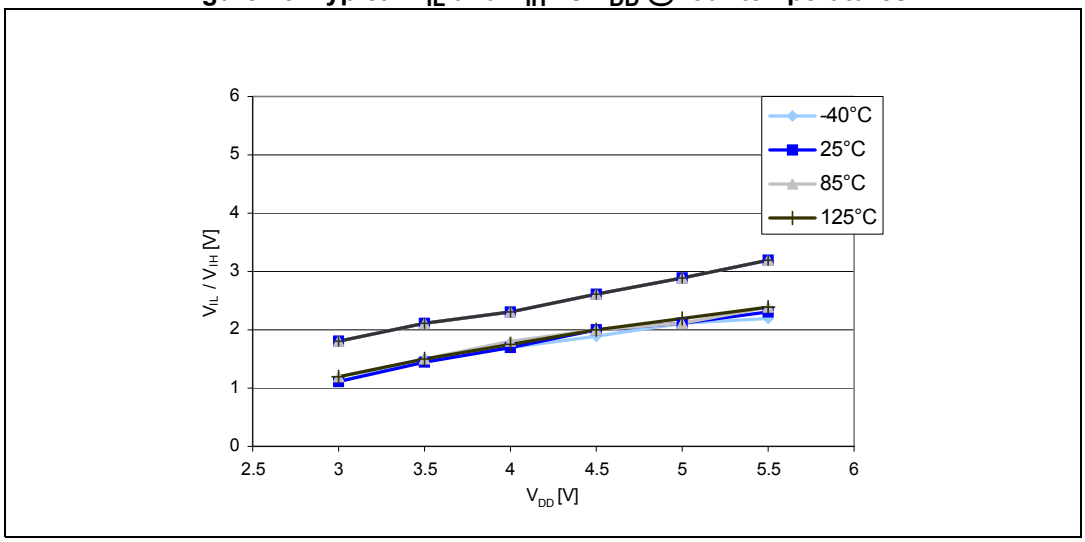



**Figure 24. Typical pull-up resistance $R_{PU}$ vs $V_{DD}$ @ four temperatures**

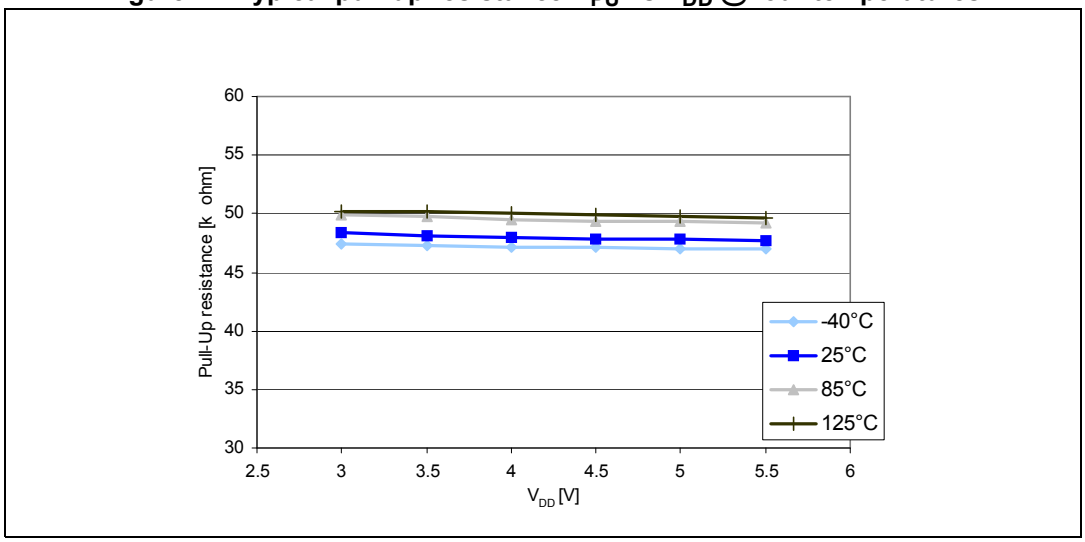
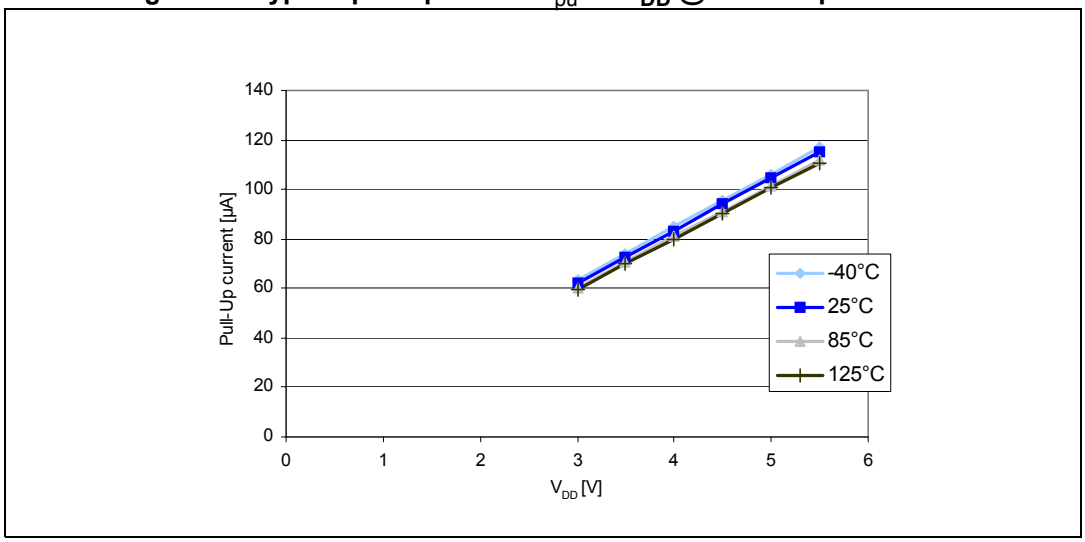


**Figure 25. Typical pull-up current $I_{pu}$ vs $V_{DD}$ @ four temperatures(1)**




1. The pull-up is a pure resistor (slope goes through 0).

## Typical output level curves

*Figure 26* to *Figure 35* show typical output level curves measured with output on a single pin.

**Figure 26. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (standard ports)**

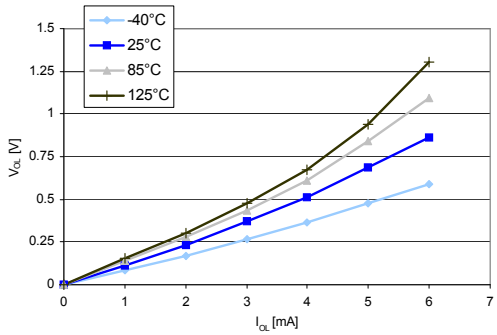



**Figure 27. Typ. $V_{OL}$ @ $V_{DD}$ = 5.0 V (standard ports)**

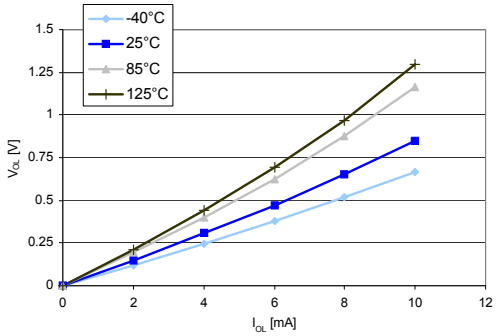



**Figure 28. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (true open drain ports)**

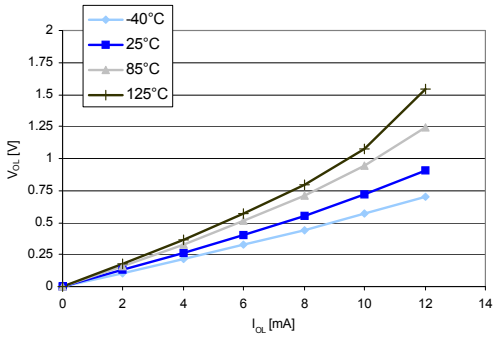



**Figure 29. Typ. $V_{OL}$ @ $V_{DD}$ = 5.0 V (true open drain ports)**

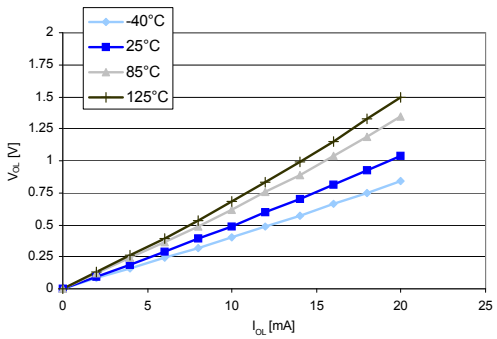


**Figure 30. Typ. $V_{OL}$ @ $V_{DD}$ = 3.3 V (high sink ports)**

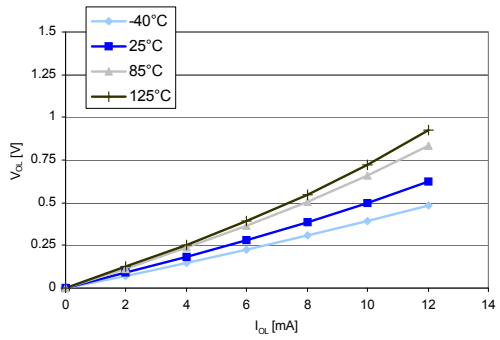



**Figure 31. Typ. $V_{OL}$ @ $V_{DD}$ = 5.0 V (high sink ports)**

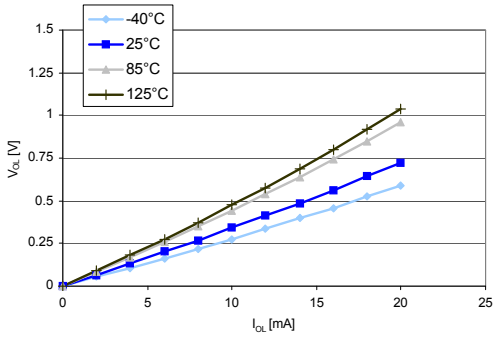



**Figure 32. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.3 V (standard ports)**

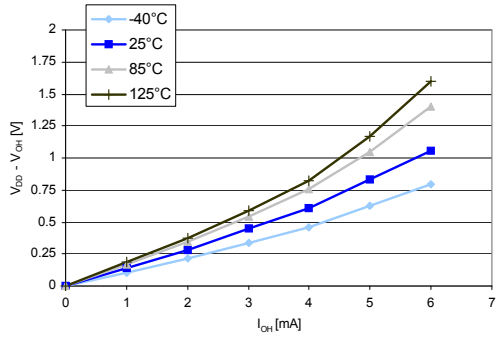



**Figure 33. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 5.0 V (standard ports)**

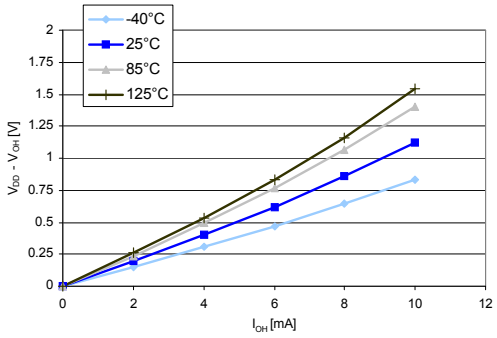



**Figure 34. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.3 V (high sink ports)**

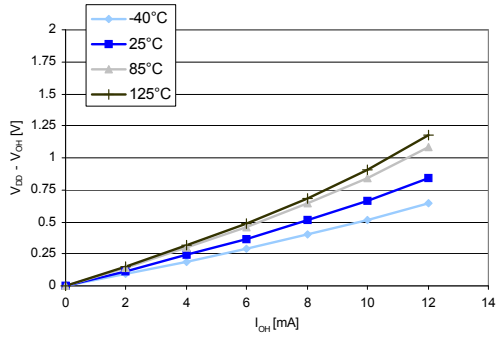
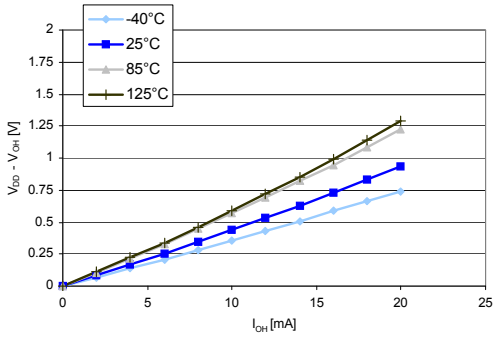



**Figure 35. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 5.0 V (high sink ports)**



### 10.3.7 Reset pin characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 37. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST low-level input voltage(1) | - | $V_{SS}$ | - | 0.3 x $V_{DD}$ | V |
| $V_{IH(NRST)}$ | NRST high-level input voltage(1) | - | 0.7 x $V_{DD}$ | - | $V_{DD}$ | |
| $V_{OL(NRST)}$ | NRST low-level output voltage(1) | $I_{OL}$ = 3 mA | - | - | 0.6 | |
| $R_{PU(NRST)}$ | NRST pull-up resistor | - | 30 | 40 | 60 | kΩ |
| $t_{IFP}$ | NRST input filtered pulse(1) | - | 85 | - | 315 | ns |
| $t_{INFP(NRST)}$ | NRST Input not filtered pulse duration(2) | - | 500 | - | - | |

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

**Figure 36. Typical NRST $V_{IL}$ and $V_{IH}$ vs $V_{DD}$ @ four temperatures**

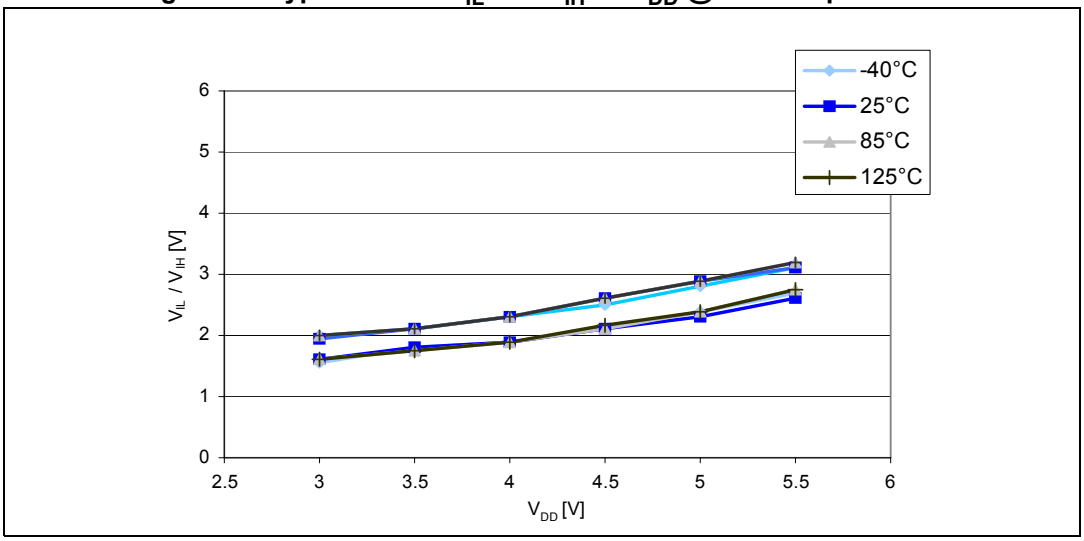


**Figure 37. Typical NRST pull-up resistance $R_{PU}$ vs $V_{DD}$**

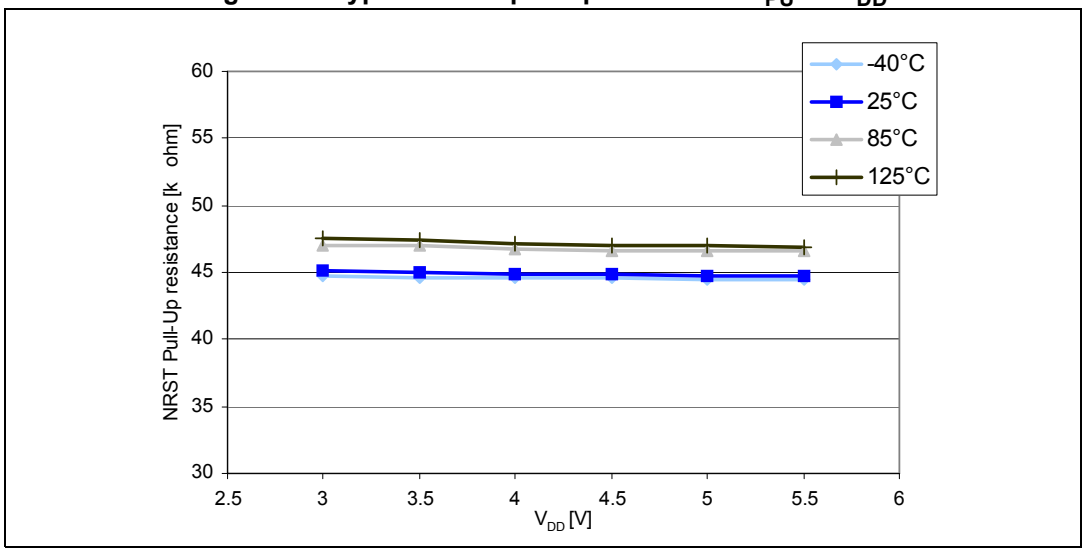
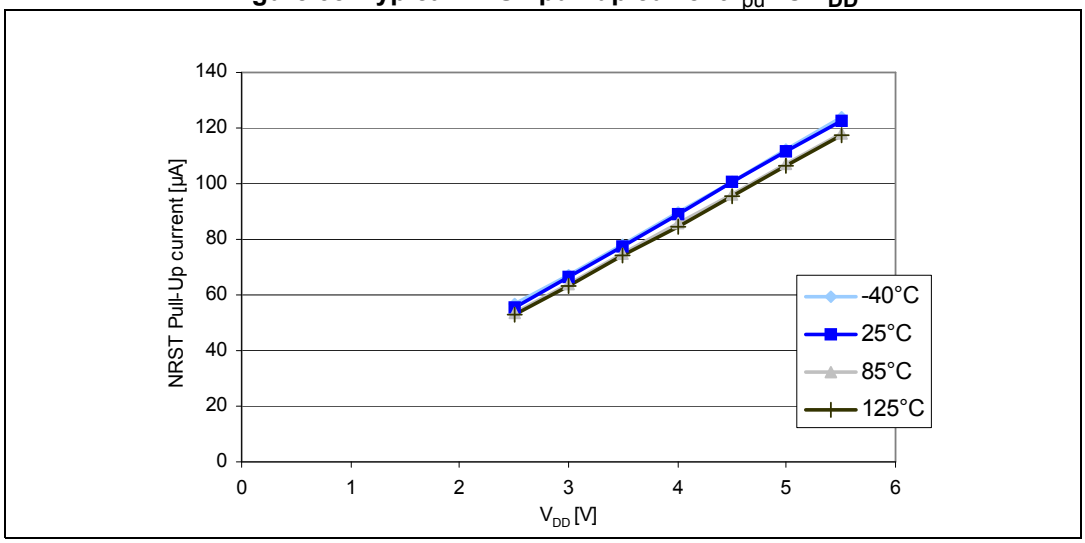


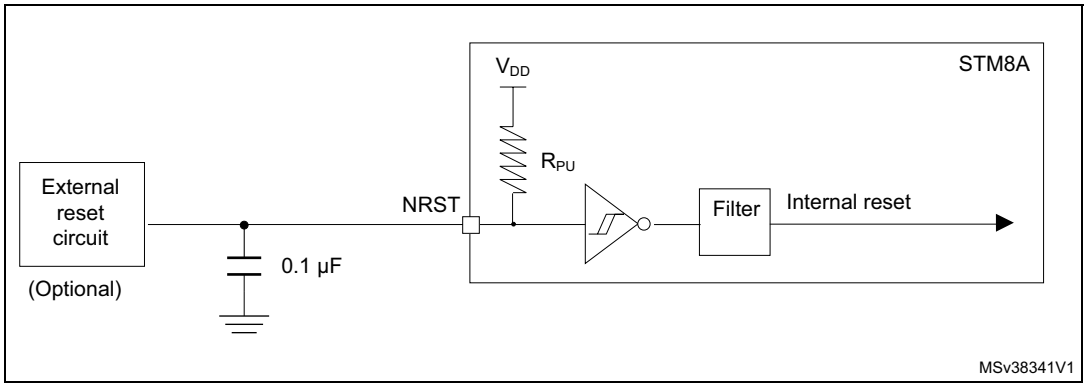

**Figure 38. Typical NRST pull-up current $I_{pu}$ vs $V_{DD}$**




The reset network shown in *Figure 39* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 37: NRST pin characteristics*), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 10 nF.

**Figure 39. Recommended reset pin protection**




### 10.3.8 TIM 1, 2, 3, and 4 electrical specifications

Subject to general operating conditions for $V_{DD}$, $f_{MASTER}$ and $T_A$.

**Table 38. TIM 1, 2, 3, and 4 electrical specifications**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{EXT}$ | Timer external clock frequency(1) | - | - | - | 24 | MHz |

1. Not tested in production.

### 10.3.9 SPI interface

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under ambient temperature, $f_{MASTER}$ frequency, and $V_{DD}$ supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

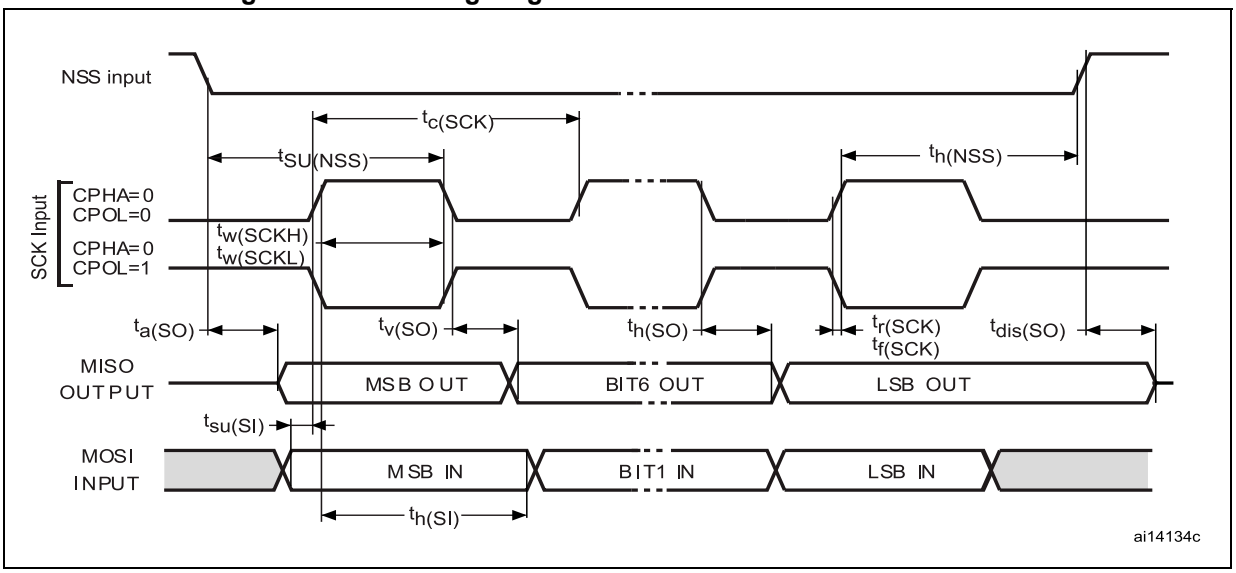
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 39. SPI characteristics**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | | 0 | 10 | MHz |
| | | Slave mode | $V_{DD}$ < 4.5 V | 0 | 6(1) | |
| | | | $V_{DD}$ = 4.5 V to 5.5 V | 0 | 8(1) | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | | - | 25(2) | ns |
| $t_{su(NSS)}$(3) | NSS setup time | Slave mode | | 4 * $t_{MASTER}$ | - | |
| $t_{h(NSS)}$(3) | NSS hold time | Slave mode | | 70 | - | |
| $t_{w(SCKH)}$(3)<br>$t_{w(SCKL)}$(3) | SCK high and low time | Master mode | $t_{SCK}/2$ - 15 | $t_{SCK}/2$ + 15 | $t_{w(SCKH)}$(3)<br>$t_{w(SCKL)}$(3) | |
| $t_{su(MI)}$(3)<br>$t_{su(SI)}$(3) | Data input setup time | Master mode | | 5 | - | |
| | | Slave mode | | 5 | - | |
| $t_{h(MI)}$(3)<br>$t_{h(SI)}$(3) | Data input hold time | Master mode | | 7 | - | |
| | | Slave mode | | 10 | - | |
| $t_{a(SO)}$(3)(4) | Data output access time | Slave mode | | - | 3* $t_{MASTER}$ | |
| $t_{dis(SO)}$(3)(5) | Data output disable time | Slave mode | | 25 | | |
| $t_{v(SO)}$(3) | Data output valid time | Slave mode (after enable edge) | $V_{DD}$ < 4.5 V | - | 75 | |
| | | | $V_{DD}$ = 4.5 V to 5.5 V | - | 53 | |
| $t_{v(MO)}$(3) | Data output valid time | Master mode (after enable edge) | | - | 30 | |
| $t_{h(SO)}$(3) | Data output hold time | Slave mode (after enable edge) | | 31 | - | |
| $t_{h(MO)}$(3) | | Master mode (after enable edge) | | 12 | - | |

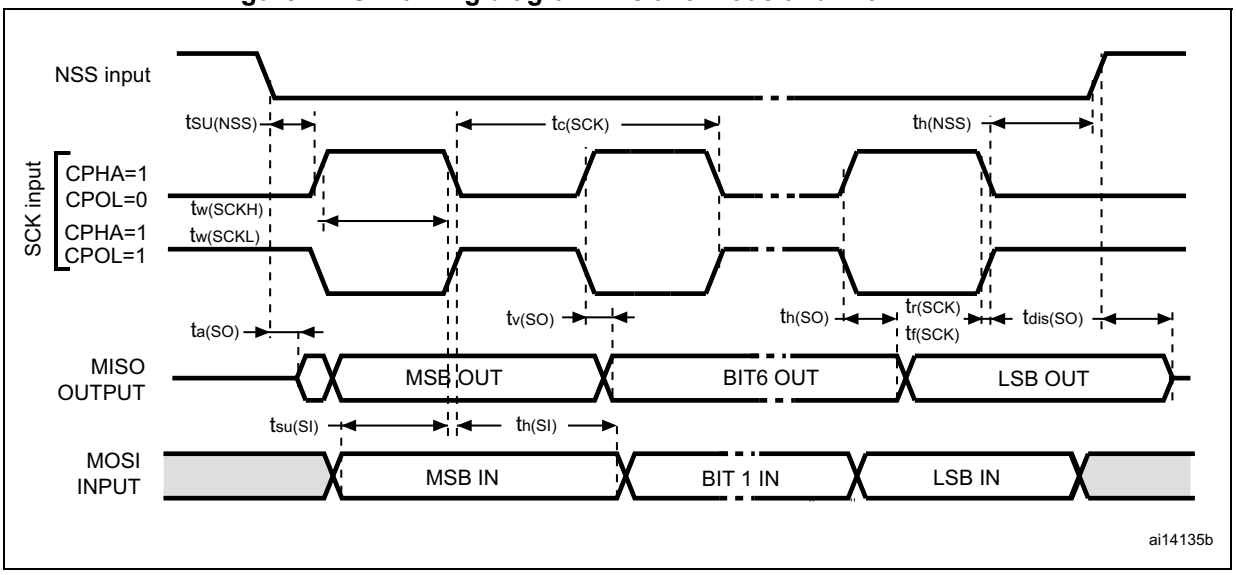
1. $f_{SCK} < f_{MASTER}/2$.
2. The pad has to be configured accordingly (fast mode).
3. Guaranteed by design or by characterization results, not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

**Figure 40. SPI timing diagram in slave mode and with CPHA = 0**



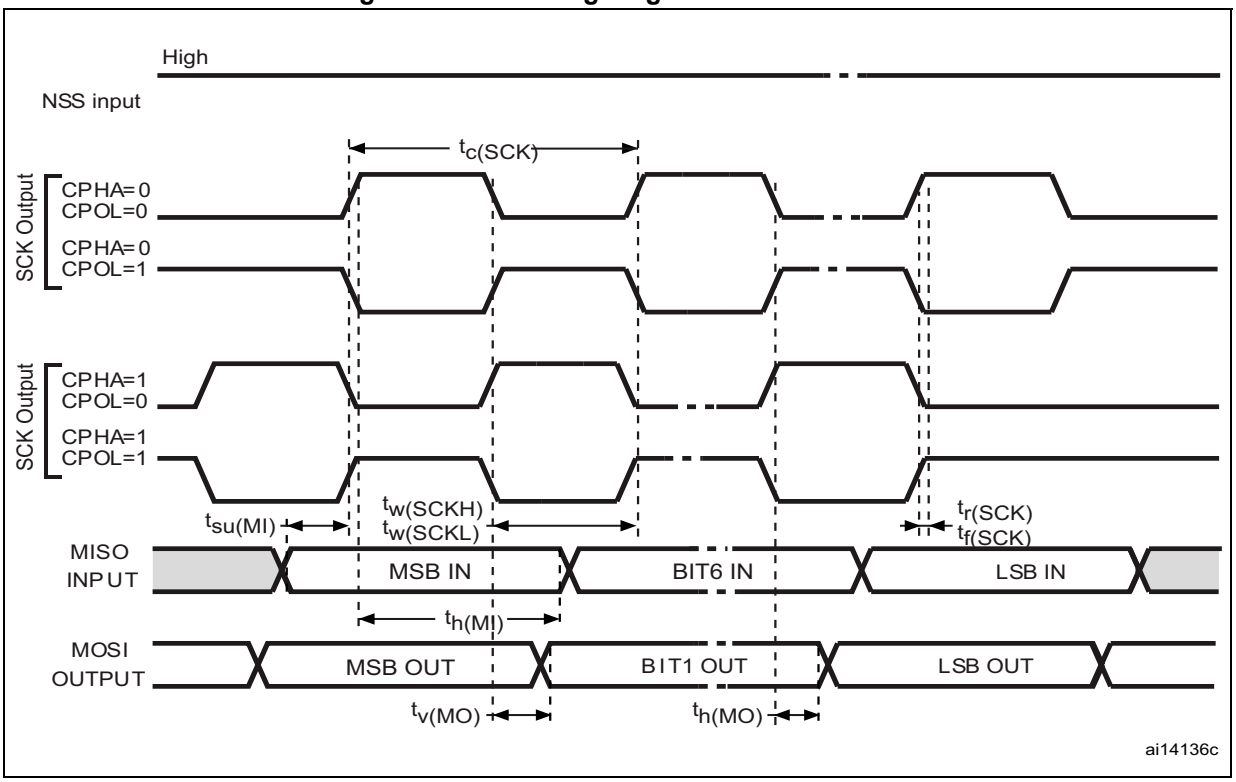

1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Figure 41. SPI timing diagram in slave mode and with CPHA = 1**




1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Figure 42. SPI timing diagram - master mode**




1. Measurement points are at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

### 10.3.10 I²C interface characteristics

**Table 40. I²C characteristics**

| Symbol | Parameter | Standard mode I²C | | Fast mode I²C(1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min(2) | Max(2) | Min(2) | Max(2) | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0(3) | - | 0(4) | 900(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time ($V_{DD}$ 3 V to 5.5 V) | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time ($V_{DD}$ 3 V to 5.5 V) | - | 300 | - | 300 | |
| $t_{h(STA)}$ | START condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | STOP condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | STOP to START condition time (bus free) | 4.7 | - | 1.3 | - | µs |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. $f_{MASTER}$, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

### 10.3.11 10-bit ADC characteristics

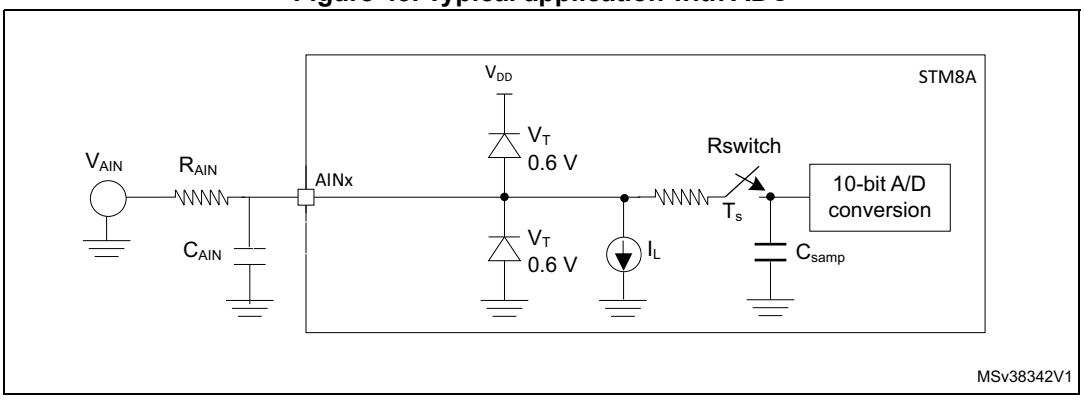
Subject to general operating conditions for $V_{DDA}$, $f_{MASTER}$ and $T_A$ unless otherwise specified.

**Table 41. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | - | 111 kHz | - | 4 MHz | kHz/MHz |
| $V_{DDA}$ | Analog supply | - | 3 | - | 5.5 | V |
| $V_{REF+}$ | Positive reference voltage | - | 2.75 | - | $V_{DDA}$ | |
| $V_{REF-}$ | Negative reference voltage | - | $V_{SSA}$ | - | 0.5 | |
| $V_{AIN}$ | Conversion voltage range(1) | - | $V_{SSA}$ | - | $V_{DDA}$ | |
| | | Devices with external $V_{REF+}$/ $V_{REF-}$ pins | $V_{REF-}$ | - | $V_{REF+}$ | |
| $C_{samp}$ | Internal sample and hold capacitor | - | - | - | 3 | pF |
| $t_S$(1) | Sampling time (3 x 1/$f_{ADC}$) | $f_{ADC}$ = 2 MHz | - | 1.5 | - | µs |
| | | $f_{ADC}$ = 4 MHz | - | 0.75 | - | |
| $t_{STAB}$ | Wakeup time from standby | $f_{ADC}$ = 2 MHz | - | 7 | - | |
| | | $f_{ADC}$ = 4 MHz | - | 3.5 | - | |
| $t_{CONV}$ | Total conversion time including sampling time (14 x 1/$f_{ADC}$) | $f_{ADC}$ = 2 MHz | - | 7 | - | |
| | | $f_{ADC}$ = 4 MHz | - | 3.5 | - | |
| $R_{switch}$ | Equivalent switch resistance | - | - | - | 30 | kΩ |

1. During the sample time, the sampling capacitance, $C_{samp}$ (3 pF typ), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_S$. After the end of the sample time $t_S$, changes of the analog input voltage have no effect on the conversion result.

**Figure 43. Typical application with ADC**



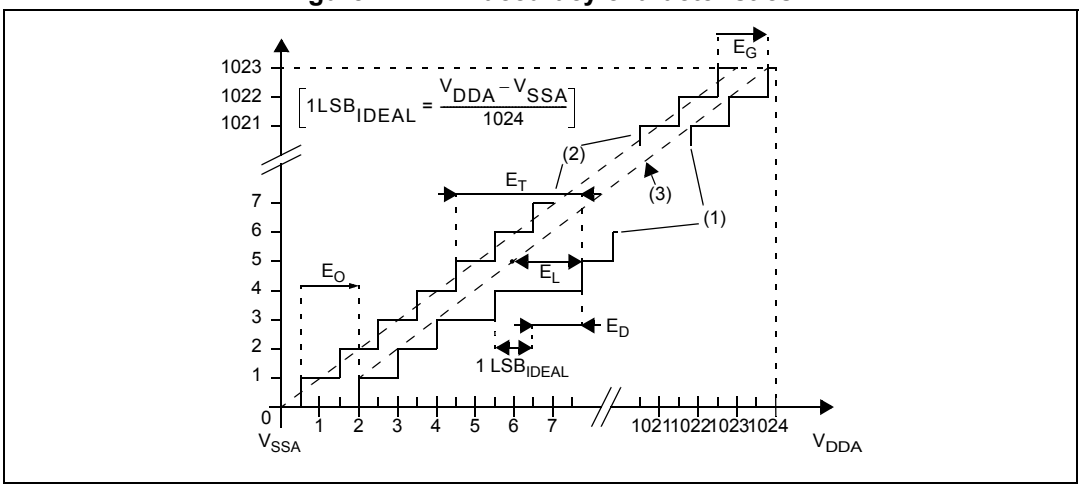

1. Legend: $R_{AIN}$ = external resistance, $C_{AIN}$ = capacitors, $C_{samp}$ = internal sample and hold capacitor.

**Table 42. ADC accuracy for $V_{DDA}$ = 5 V**

| Symbol | Parameter | Conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $\|E_T\|$ | Total unadjusted error(2) | $f_{ADC}$ = 2 MHz | 1.4 | 3(3) | LSB |
| $\|E_O\|$ | Offset error(2) | | 0.8 | 3 | |
| $\|E_G\|$ | Gain error(2) | | 0.1 | 2 | |
| $\|E_D\|$ | Differential linearity error(2) | | 0.9 | 1 | |
| $\|E_L\|$ | Integral linearity error(2) | | 0.7 | 1.5 | |
| $\|E_T\|$ | Total unadjusted error(2) | $f_{ADC}$ = 4 MHz | 1.9(4) | 4(4) | |
| $\|E_O\|$ | Offset error(2) | | 1.3(4) | 4(4) | |
| $\|E_G\|$ | Gain error(2) | | 0.6(4) | 3(4) | |
| $\|E_D\|$ | Differential linearity error(2) | | 1.5(4) | 2(4) | |
| $\|E_L\|$ | Integral linearity error(2) | | 1.2(4) | 1.5(4) | |

1. Guaranteed by characterization results, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific sales types on the whole temperature range.
4. Target values.

**Figure 44. ADC accuracy characteristics**




1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   **$E_T$** = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   **$E_O$** = Offset error: Deviation between the first actual transition and the first ideal one.
   **$E_G$** = Gain error: Deviation between the last ideal transition and the last actual one.
   **$E_D$** = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   **$E_L$** = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

### 10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

#### Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- ***ESD***: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- ***FTB***: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

***Software recommendations***

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

***Prequalification trials***

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Table 43. EMS data**

| Symbol | Parameter | Conditions | Level/class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$= 25 °C, $f_{MASTER}$ = 16 MHz (HSI clock), Conforms to IEC 1000-4-2 | 3/B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$= 3.3 V, $T_A$= 25 °C, $f_{MASTER}$ = 16 MHz (HSI clock), Conforms to IEC 1000-4-4 | 4/A |

### Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

**Table 44. EMI data**

| Symbol | Parameter | Conditions | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | General conditions | Monitored frequency band | Max $f_{CPU}$(1) | | | |
| | | | | 8 MHz | 16 MHz | 24 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 5 V, $T_A$ = 25 °C, LQFP80 package conforming to IEC 61967-2 | 0.1 MHz to 30 MHz | 15 | 17 | 22 | dBµV |
| | | | 30 MHz to 130 MHz | 18 | 22 | 16 | |
| | | | 130 MHz to 1 GHz | -1 | 3 | 5 | |
| | EMI level | | - | 2 | 2.5 | 2.5 | |

1. Guaranteed by characterization results, not tested in production.

### Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

### Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

**Table 45. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = 25 °C, conforming to JESD22-A114 | 3A | 4000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = 25 °C, conforming to JESD22-C101 | 3 | 500 | |
| $V_{ESD(MM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = 25 °C, conforming to JESD22-A115 | B | 200 | |

1. Guaranteed by characterization results, not tested in production

### Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

**Table 46. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class(1) |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = 25 °C | A |
| | | $T_A$ = 85 °C | |
| | | $T_A$ = 125 °C | |
| | | $T_A$ = 150 °C | |

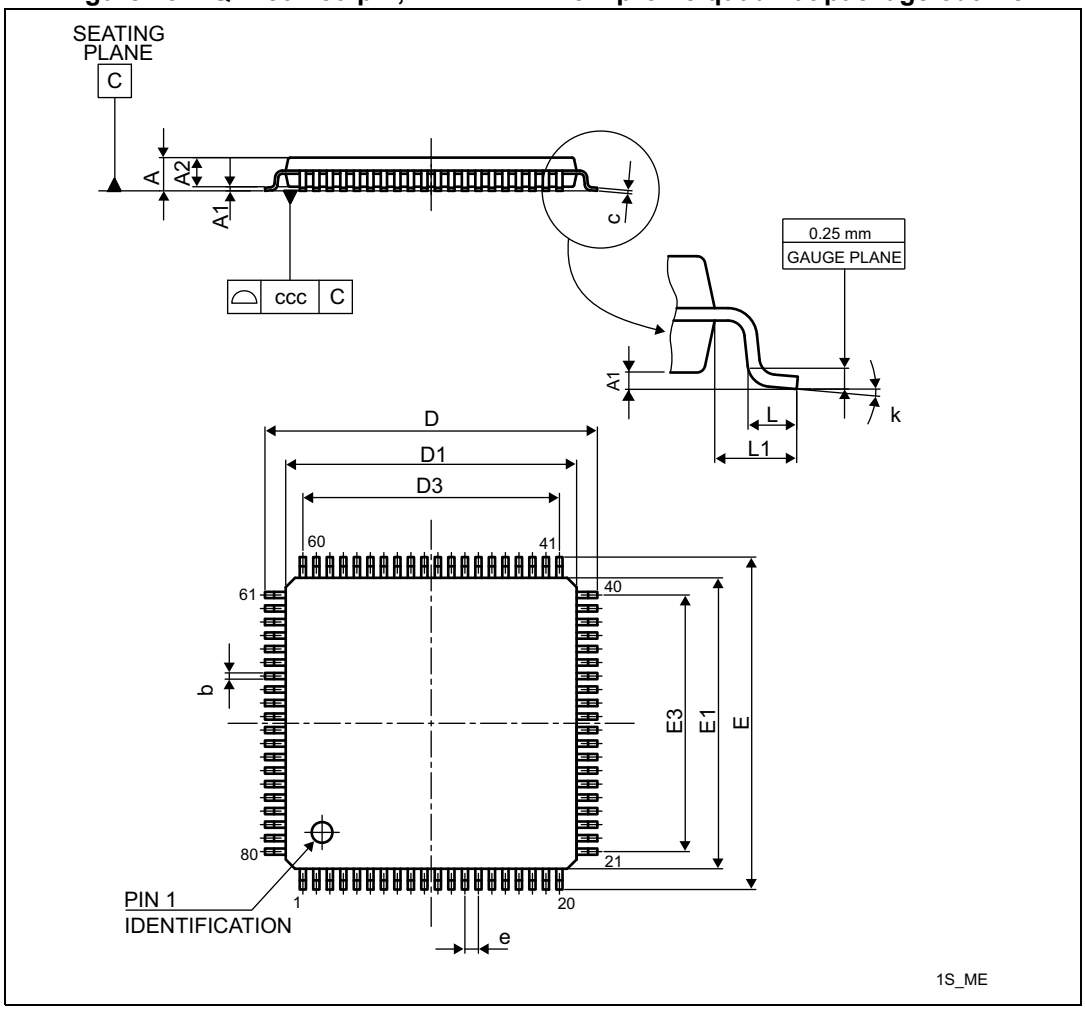
1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

# 11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 11.1 LQFP80 package information

**Figure 45. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline**



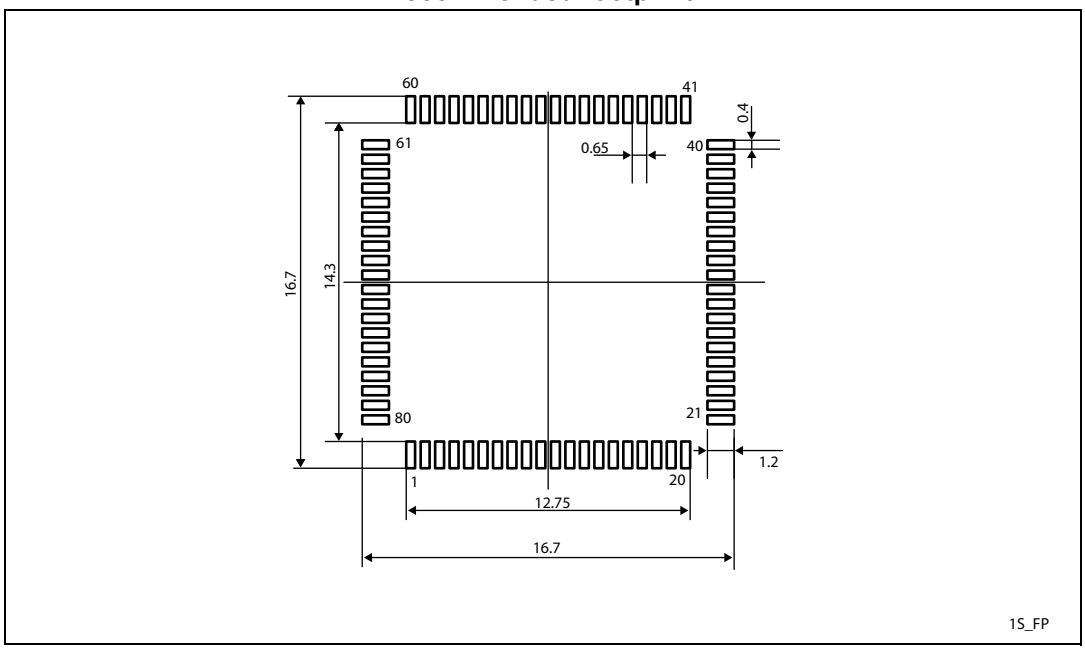

1. Drawing is not to scale.

**Table 47. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1)**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.220 | 0.320 | 0.380 | 0.0087 | 0.0126 | 0.0150 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | - | 12.350 | - | - | 0.4862 | - |
| E | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | - | 12.350 | - | - | 0.4862 | - |
| e | - | 0.650 | - | - | 0.0256 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 46. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint**



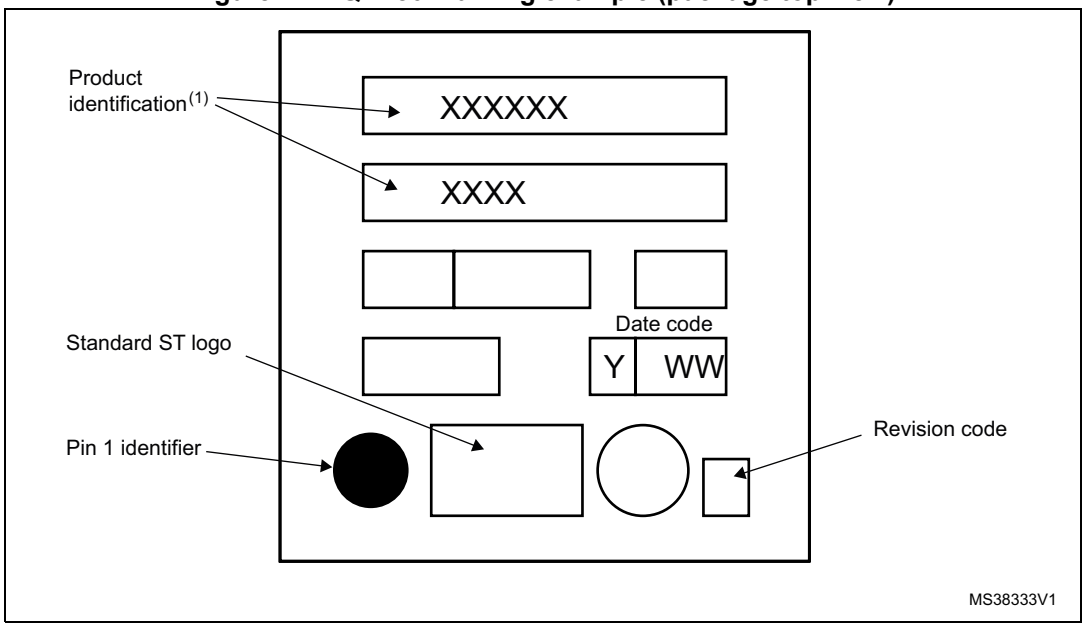

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

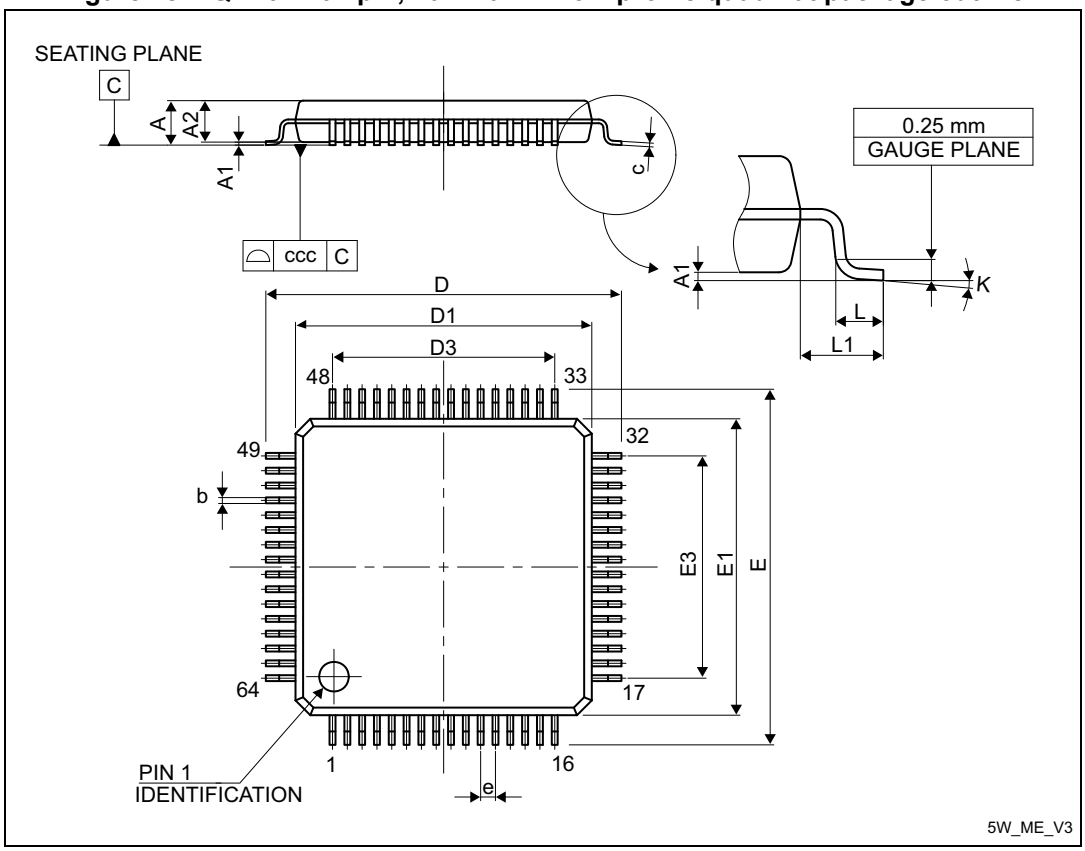
**Figure 47. LQFP80 marking example (package top view)**




1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

## 11.2 LQFP64 package information

**Figure 48. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 48. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data**

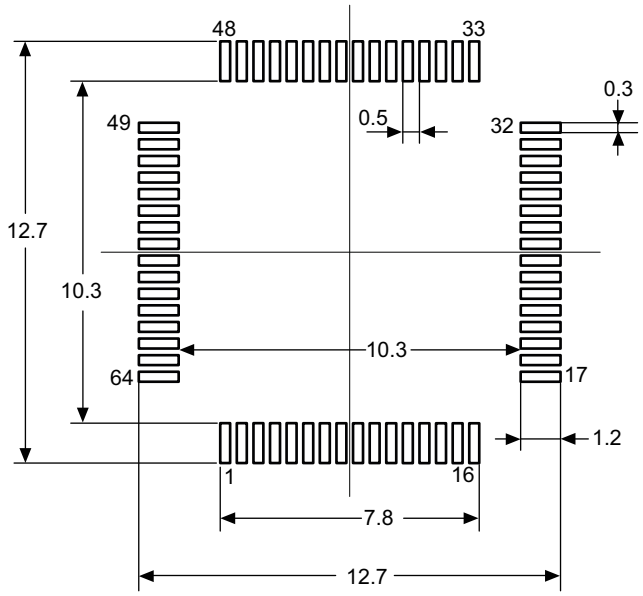
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |

**Table 48. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint**



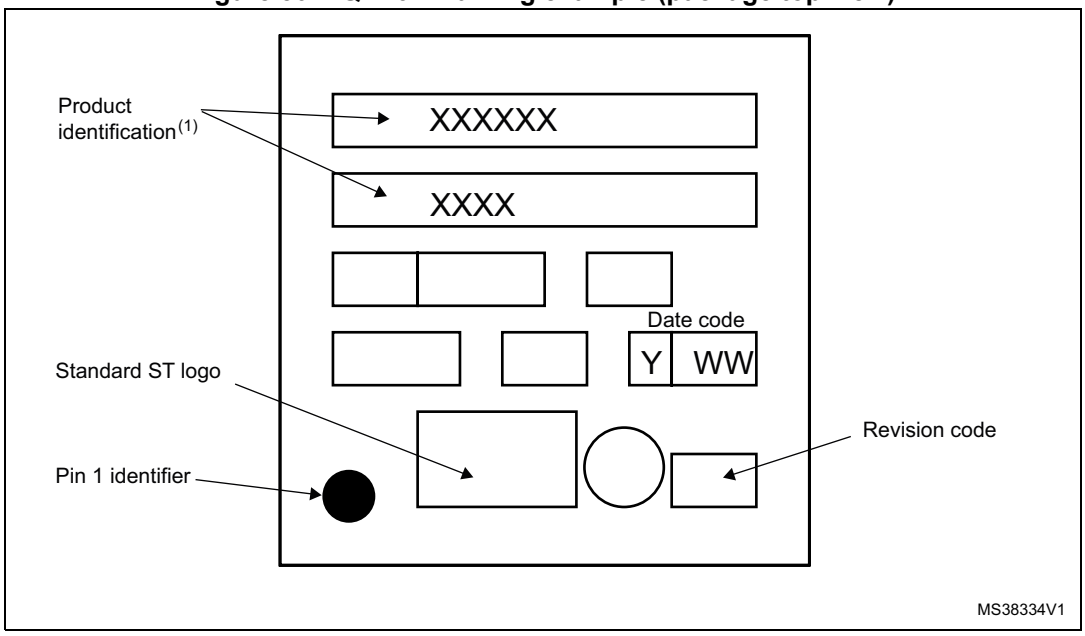

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

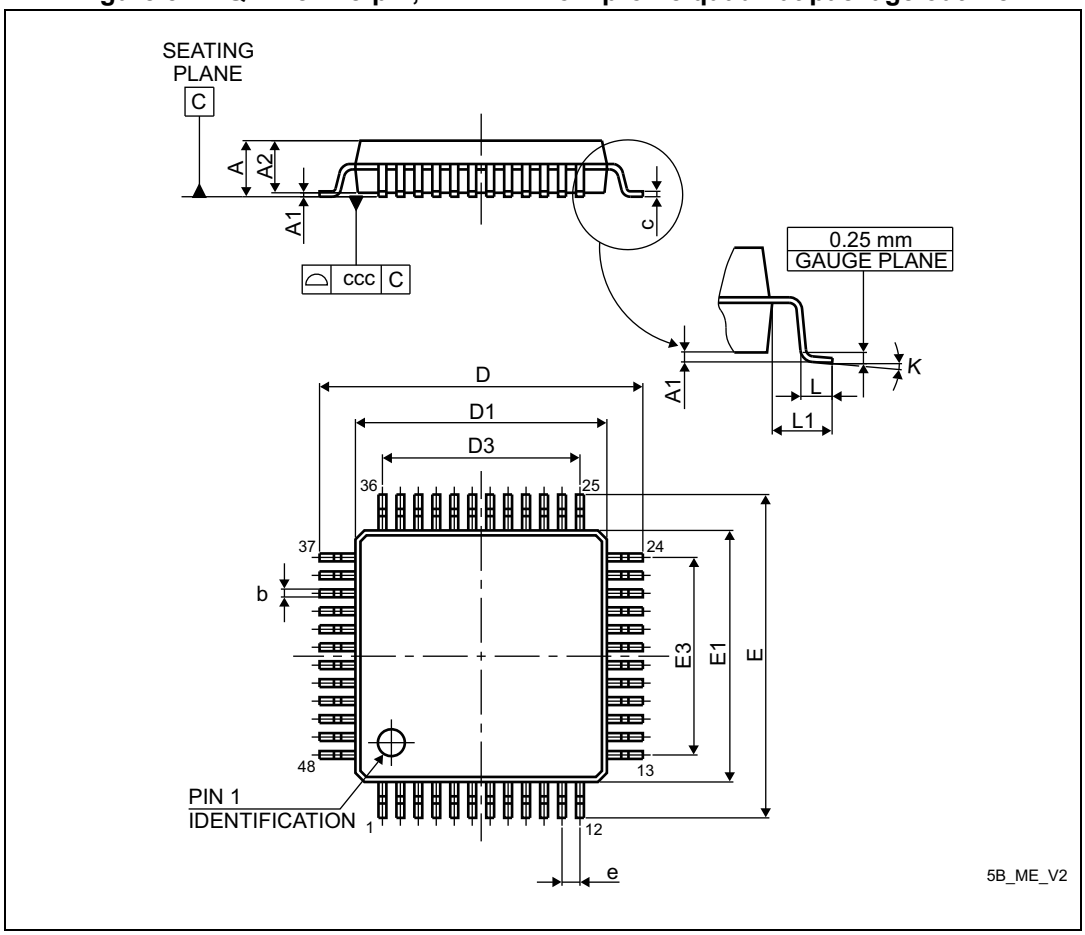
**Figure 50. LQFP64 marking example (package top view)**




1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

## 11.3 LQFP48 package information

**Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline**



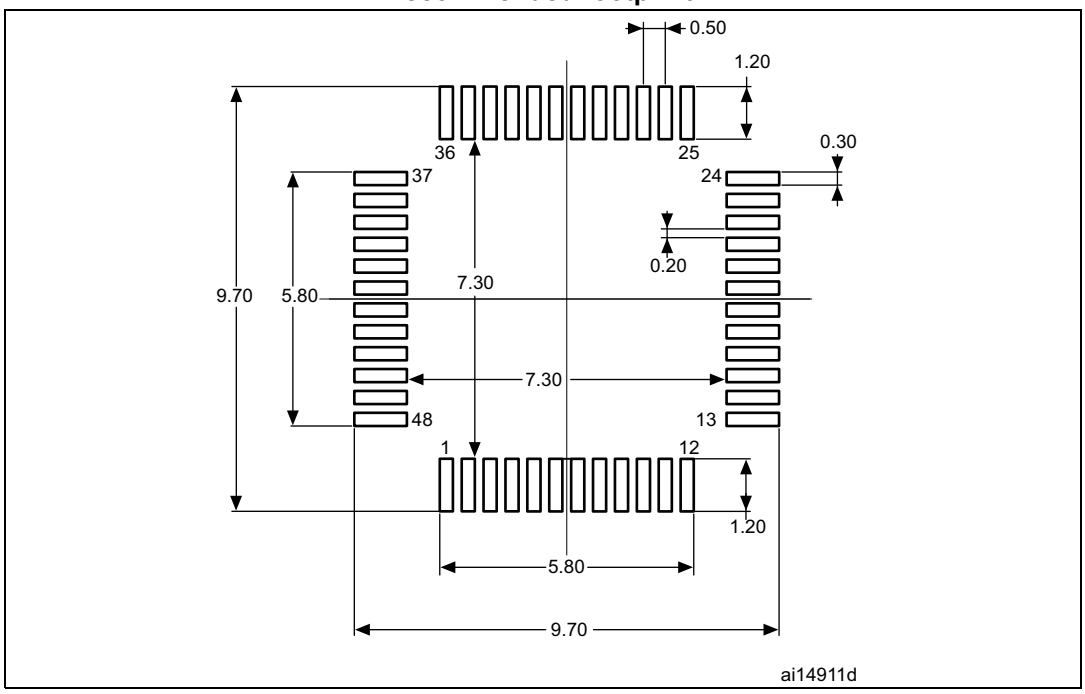

1. Drawing is not to scale.

**Table 49. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint**



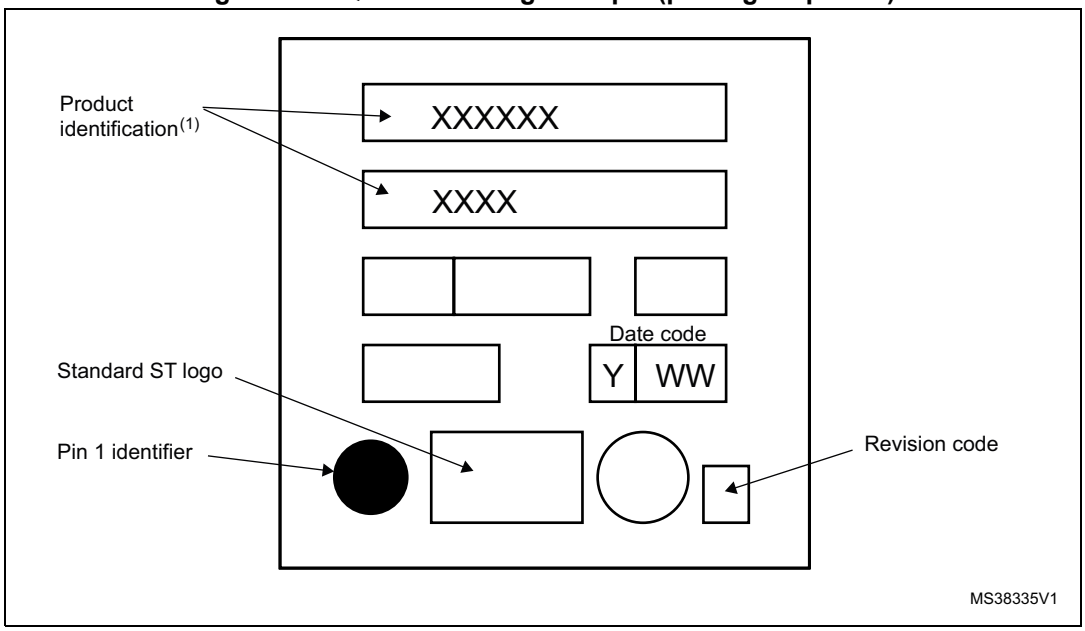

1. Dimensions are expressed in millimeters.

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

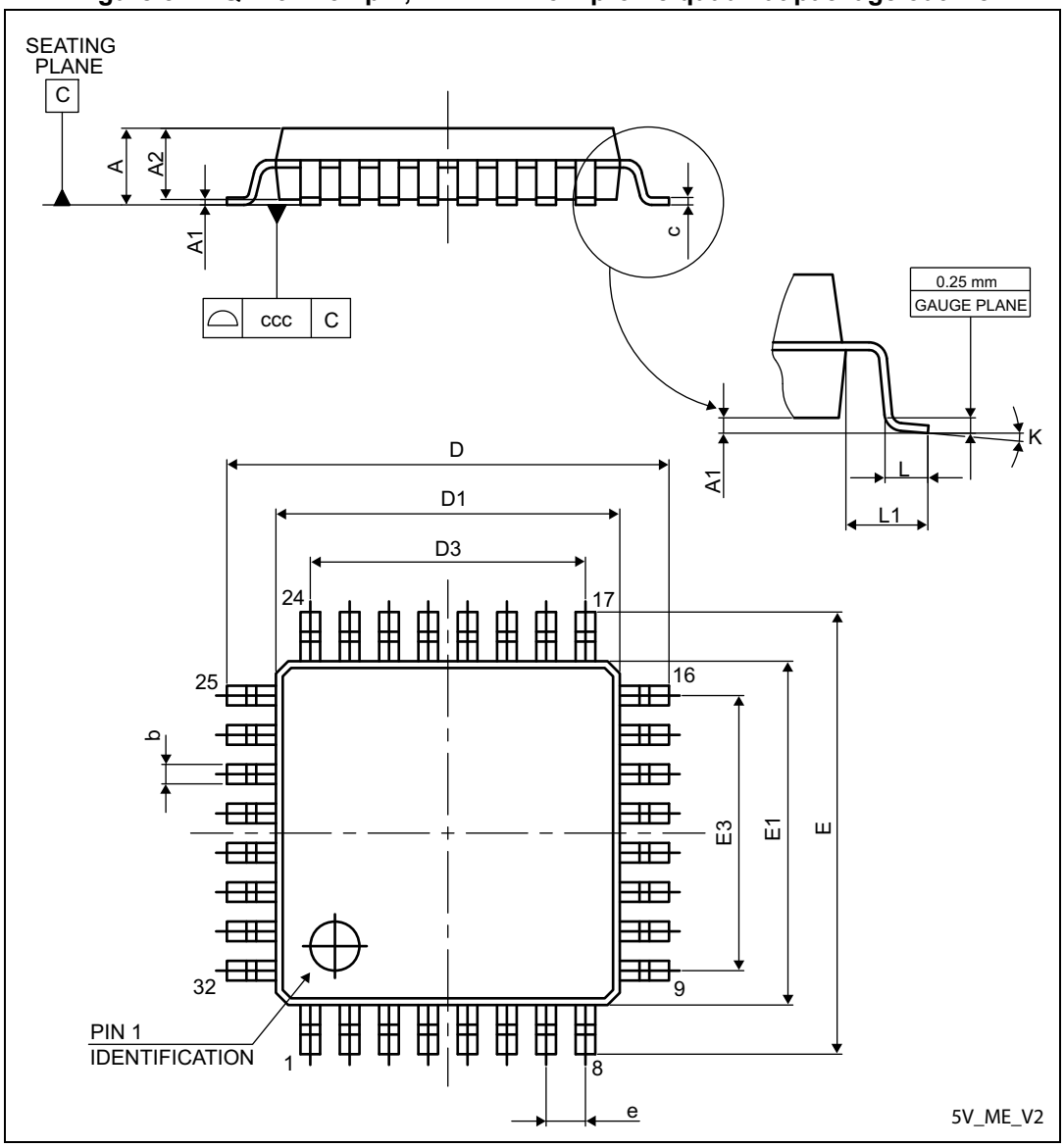
**Figure 53. LQFP48 marking example (package top view)**




1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

## 11.4 LQFP32 package information

**Figure 54. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline**



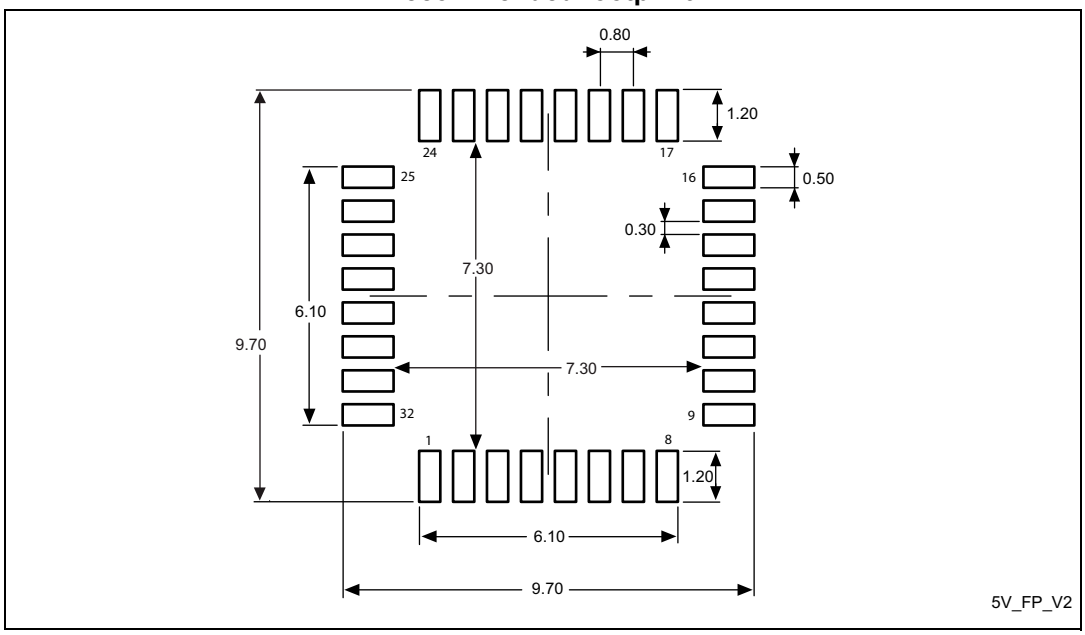

1. Drawing is not to scale.

**Table 50. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.300 | 0.370 | 0.450 | 0.0118 | 0.0146 | 0.0177 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.600 | - | - | 0.2205 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.600 | - | - | 0.2205 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 55. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint**



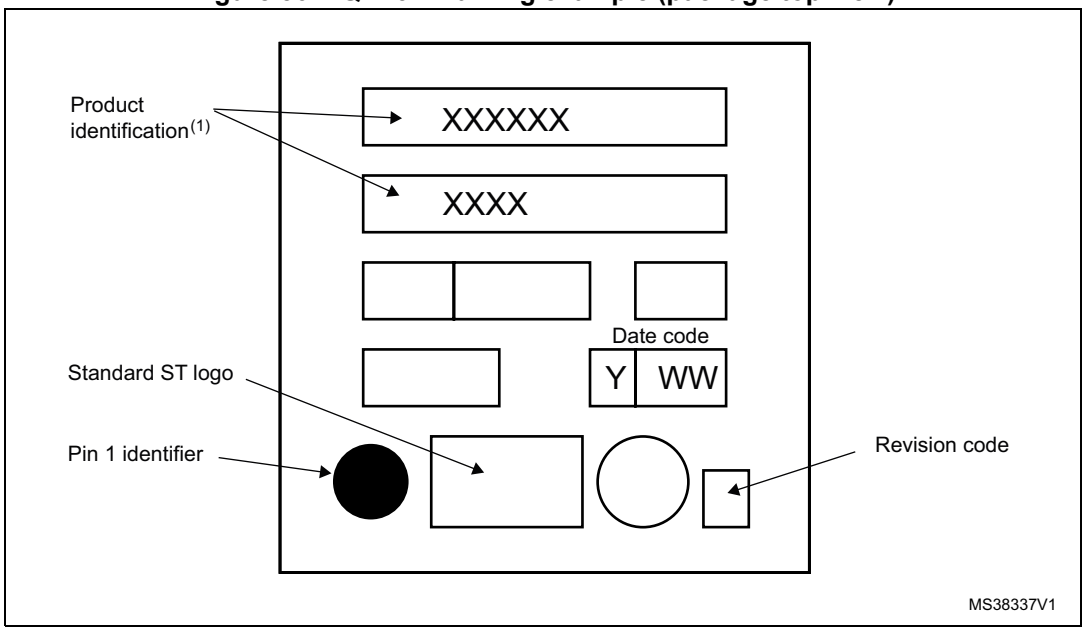

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

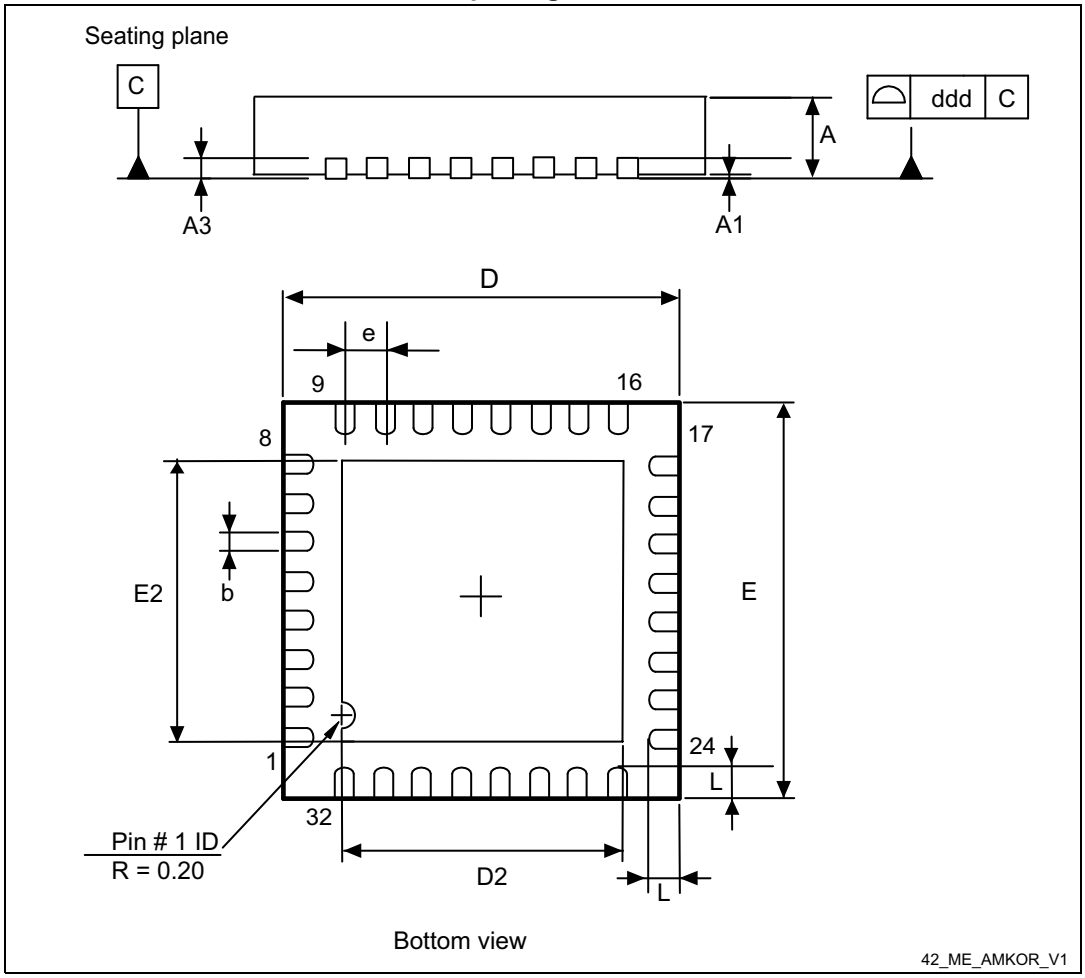
**Figure 56. LQFP32 marking example (package top view)**




1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

## 11.5 VFQFPN32 package information

**Figure 57. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline**



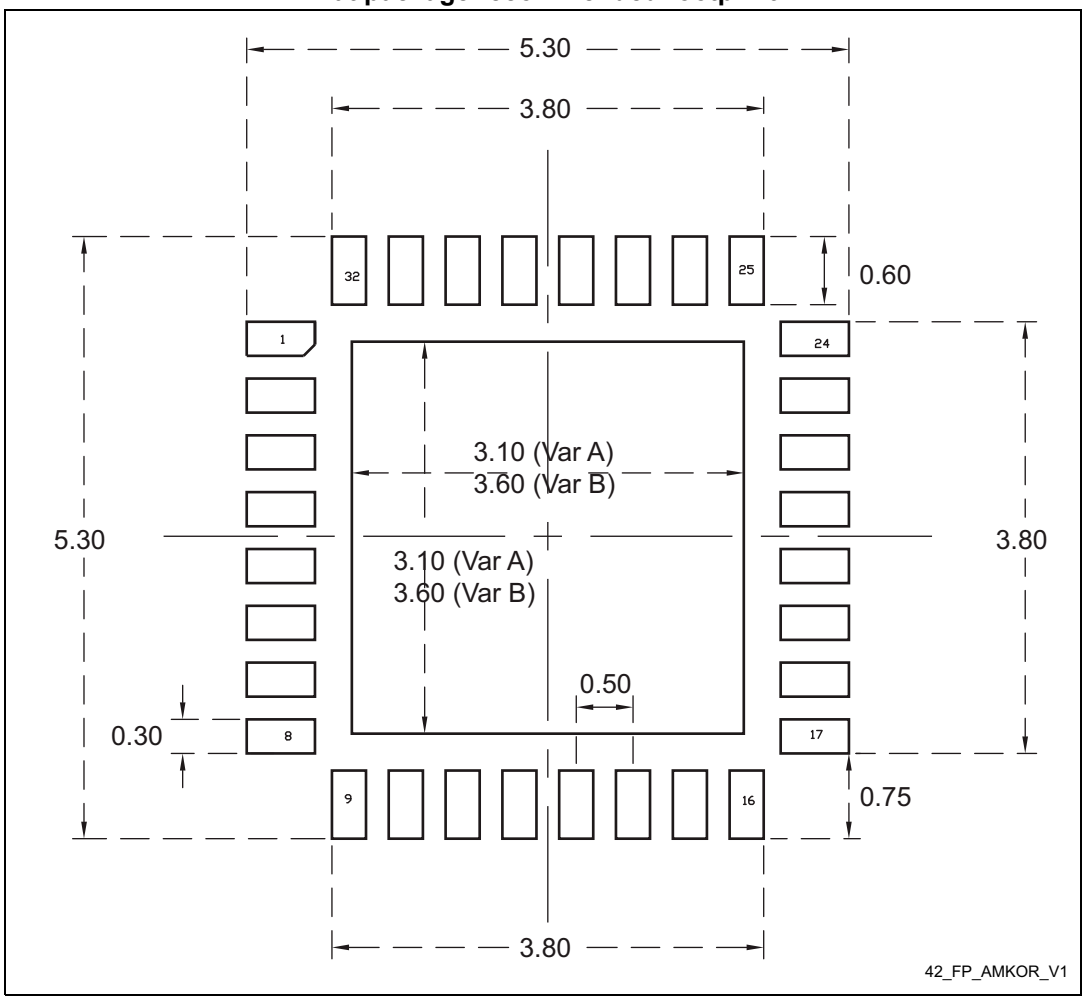

1. Drawing is not to scale.

**Table 51. VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.800 | 0.900 | 1.000 | 0.0315 | 0.0354 | 0.0394 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| A3 | - | 0.200 | - | - | 0.0079 | - |
| b | 0.180 | 0.250 | 0.300 | 0.0071 | 0.0098 | 0.0118 |
| D | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| D2 | 3.500 | 3.600 | 3.700 | 0.1378 | 0.1417 | 0.1457 |
| E | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| E2 | 3.500 | 3.600 | 3.700 | 0.1378 | 0.1417 | 0.1457 |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 58. VFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint**



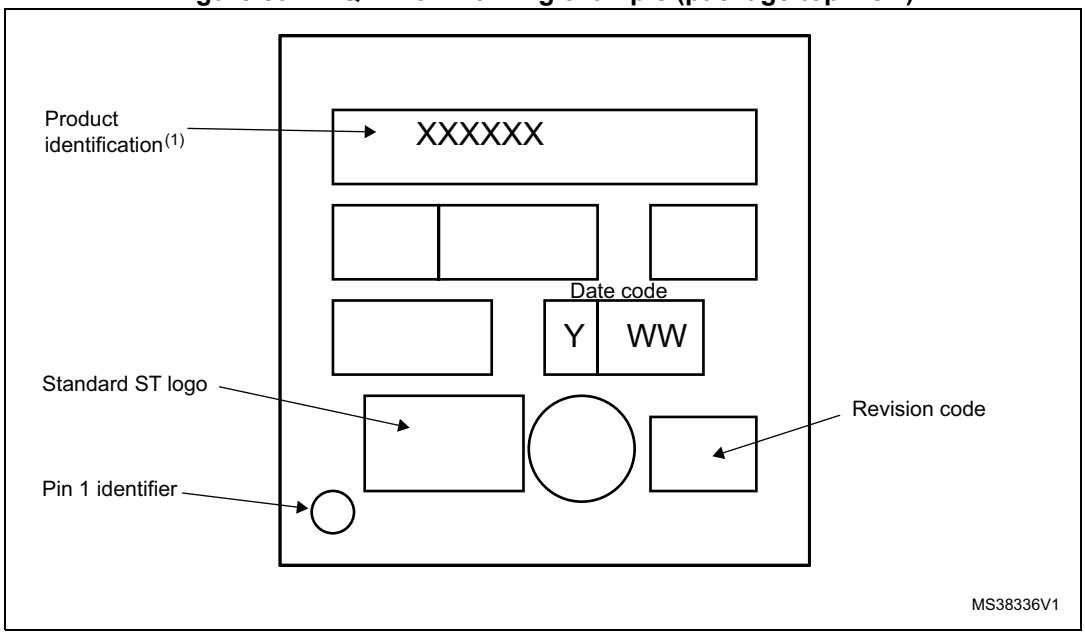

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 59. VFQFPN32 marking example (package top view)**




1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

## 11.6 Thermal characteristics

In case the maximum chip junction temperature ($T_{Jmax}$) specified in *Table 22: General operating conditions* is exceeded, the functionality of the device cannot be guaranteed.

$T_{Jmax}$, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

where:

**$T_{Amax}$** is the maximum ambient temperature in °C

**$\Theta_{JA}$** is the package junction-to-ambient thermal resistance in ° C/W

**$P_{Dmax}$** is the sum of $P_{INTmax}$ and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)

**$P_{INTmax}$** is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

**$P_{I/Omax}$** represents the maximum power dissipation on output pins

where:

$$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma((V_{DD} - V_{OH}) * I_{OH})$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low- and high-level in the application.

**Table 52. Thermal characteristics(1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm | 38 | °C/W |
| | Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm | 46 | |
| | Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm | 57 | |
| | Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm | 59 | |
| | Thermal resistance junction-ambient VFQFPN 32 - 5 x 5 mm | 25 | |

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

### 11.6.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

### 11.6.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 60: STM8AF6388 ordering information scheme[1] on page 111*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2)
- $I_{DDmax}$ = 8 mA
- $V_{DD}$ = 5 V
- maximum 20 I/Os used at the same time in output at low-level with $I_{OL}$ = 8 mA
- $V_{OL}$ = 0.4 V

$P_{INTmax}$ = 8 mA x 5 V = 400 mW

$P_{IOmax}$ = 20 x 8 mA x 0.4 V = 64 mW

This gives:

$P_{INTmax}$ = 400 mW and $P_{IOmax}$ 64 mW

$P_{Dmax}$ = 400 mW + 64 mW

Thus:

$P_{Dmax}$ = 464 mW.

Using the values obtained in *Table 52: Thermal characteristics* $T_{Jmax}$ is calculated as follows:

For LQFP64 46 °C/W

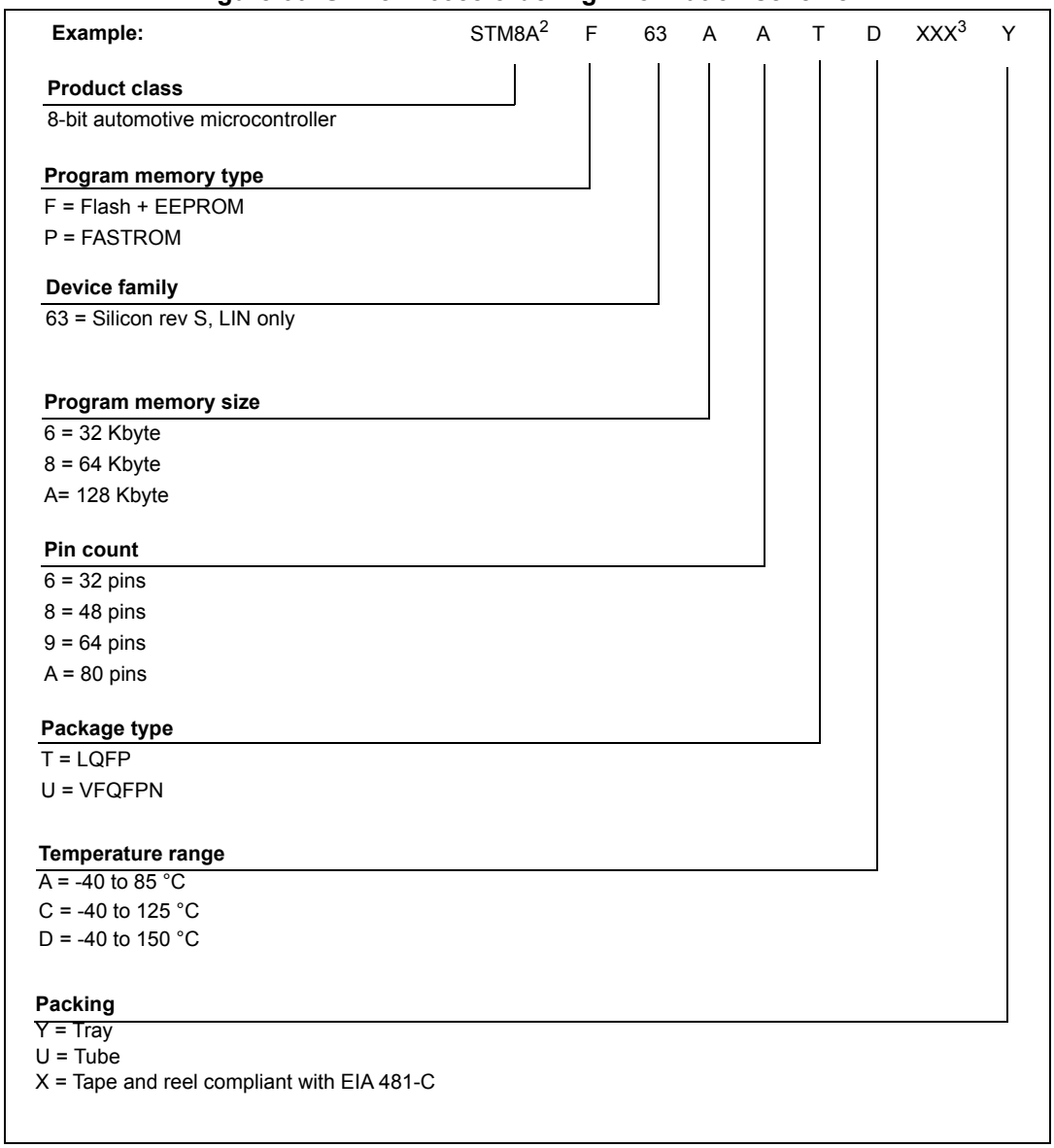
$$T_{jmax} = 82\ °C + (46\ °C/W \times 464\ mW) = 82\ °C + 21\ °C = 103\ °C$$

This is within the range of the suffix C version parts (-40 °C < $T_j$ < 125 ° C).

Parts must be ordered at least with the temperature range suffix C.

# 12 Ordering information

**Figure 60. STM8AF6388 ordering information scheme[1]**




1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.
3. Customer specific FASTROM code or custom device configuration. This field shows 'SSS' if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.

# 13 STM8 development tools

Development tools for the STM8A microcontrollers include the

- STice emulation system offering tracing and code profiling
- STVD high-level language debugger including assembler and visual development environment - seamless integration of third party C compilers
- STVP Flash programming software

In addition, the STM8A comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

## 13.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8A application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full-featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including tracing, profiling and code coverage analysis to help detect execution bottlenecks and dead code.

In addition, STice offers in-circuit debugging and programming of STM8A microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

### 13.1.1 STice key features

- Program and data trace recording up to 128 K records
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Real-time read/write of all device resources during emulation
- Occurrence and time profiling and code coverage analysis (new features)
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- USB 2.0 high-speed interface to host PC
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows users to specify the components they need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

## 13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

### 13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

#### ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

#### ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

### 13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface. Available toolchains include:

#### C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

#### STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows users to assemble and link their application source code.

## 13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

# 14 Revision history

Table 53. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 24-Oct-2017 | 1 | Initial release |

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