TC35680FSG-002/ TC35681FSG-002

Bluetooth® Low Energy IC

Rev 1.0

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- TC35680/TC35681-002 Programming Guide
- TC35680/TC35681-002 Known Issues
- **Bluetooth**® Core Specification

Technical Terms and Abbreviations

The following technical terms and abbreviations are used in this document.

Terms or Abbreviations	Description
Active mode	Normal operating mode. The packet transmission and reception procedure of the **Bluetooth**® connection and the other internal CPU activities are executed in this mode. Refer to Section 3.6.
Sleep mode	One of the low power modes. The reference clock stops to save power. The **Bluetooth**® **connection** is kept in this mode. Refer to Section 3.6.
Backup mode	One of the low power modes. This mode consumes same or less power than the Sleep mode. The power supply of the CPU stops as well as the reference clock. Refer to Section 3.6.
Complete mode	One of the operating modes. A host operates this device using TCU commands (Control API in the GATT/SM layer). Refer to Section 3.4.
Deep Sleep mode	One of the low power modes. This mode saves more power than the Backup mode. The Sleep clock stops as well as the power supply of the CPU and the reference clock. Refer to Section 3.6.
HCI mode	One of the operating modes. A host operates this device using HCI commands. Refer to Section 3.4.
PMU	Power Management Unit. Integrated PMU controls the power save procedure of this device. In order to save power, it switches the built-in DC/DC converter and the LDO regulator properly, and also controls the output voltage at the same time. Refer to Section 3.1 and Section 3.6.
User-App mode	One of the operating modes. A user application is executed by the built-in CPU in this device. Refer to Section 3.4.
Auto-Advertising function	Advertising packets are transmitted without software control in the Backup mode. This function enables the packet transmission even in the low power mode.

1. Function Outlines and Features

1.1. Function Outlines

TC35680FSG/TC35681FSG series (hereafter, TC35680/TC35681 series) are compliant with 2.4 GHz wireless communication **Bluetooth**® Low Energy Ver.5.0 specification. Each device has an MCU based on Arm® Cortex-M0® processor and integrates RF analog circuit and baseband digital circuits. The following functions in the **Bluetooth**® core specifications are supported; the LE Long Range feature, LE 2-Mbps feature, HCI (Host Control Interface) feature, Low Energy GATT Profile feature, and others.

The TC35680/TC35681 series line-up is as follows:

- ✓ TC35680FSG (hereafter, TC35680): Flash memory is included to store user application program.
- ✓ TC35681FSG (hereafter, TC35681): Flash memory is not included.

TC35680/TC35681 series support both controlled by an external CPU and standalone operation.

Table 1-1 shows the main application and features of each device.

Table 1-1 Applications and features of TC35680/TC35681 series

Product	TC35680FSG	TC35681FSG
Main application	• General-purpose (Note 1) • Standalone	• General-purpose (Note 1) • Standalone (Note 2) • Host-controlled system
Flash memory	Built-in	None
No. 27 pin	VDDIOFQ	VSSD1
Minimum VBAT operation voltage (VBATopr)	1.9 V	1.8 V (-40 to 105°C) 2.0 V (-40 to 120°C)
Ambient temperature	-40°C to +85°C	
Number of General-purpose I/O (GPIO)	18	
Number of UART channels (Note 3)	2	
Number of I^2C channels (Note 3)	2	
Number of SPI channels (Note 3)	2	
Number of AD Converter channels (Note 3)	5	
Number of PWM channels (Note 3)	4	
Sleep clock output function (Note 3)	Yes	
Package	QFN40 5.0 mm × 5.0 mm × 0.9 mm 0.4-mm pitch	

Note 1: Except "UNINTENDED USE" described in “RESTRICTIONS ON PRODUCT USE”

Note 2: An external EEPROM is necessary in the standalone system.

Note 3: These pins are shared with the GPIO pins.

1.2. Features

- Wireless communication function
  - Compliant with **Bluetooth**® Low Energy Ver.5.0 specification.
    - Built-in **Bluetooth**® baseband circuit
    - Built-in **Bluetooth**® RF circuit
      - Maximum output power: +8 dBm
      - Maximum RX sensitivity: -105.0 dBm (in case of Coded PHY and S = 8)
      - RSSI accuracy: ±2 dB (in case of -90 to -10 dBm input)
    - HCI commands/Extended HCI commands (implemented in the mask ROM)
    - Control API in GATT/SM layer (TCU commands: Toshiba Command Unit) (implemented in the mask ROM)
    - Auto-advertising feature
    - Output power setting feature
- Microcontroller unit
  - Built-in Arm® Cortex®-M0 processor (Maximum operating frequency is 32 MHz.)
  - Built-in mask ROM
    - Boot loader
    - API for the hardware control
    - **Bluetooth**® wireless function API
    - **Bluetooth**® protocol stack
  - Built-in retention SRAM (User area is 76 KB out of total 144 KB.)
  - Built-in serial Flash memory (TC35680 only)
    - Memory capacity: 128 KB
    - Sector size: 4 KB
    - Endurance: 100,000 times
- Interface, AD converter, and Debug function
  - General-purpose I/O (GPIO) (18 pins)
  - General-purpose serial interfaces
    - UART interface (2 channels. Shared with the GPIO pins.)
      - HCI mode: One channel is used as a host interface (9600 bps to 921.6 kbps)
      - User-App mode: 600 to 2000 kbps (Maximum baudrate may be 2000 kbps or less and depends on user-application program.)
    - SPI interface (2 channels. Shared with the GPIO pins.)
    - I^2C interface (2 channels. Shared with the GPIO pins.)
      - TC35681 uses one channel as the interface to the EEPROM for User-App mode.
  - PWM interface (4 channels. Shared with the GPIO pins.)
    - Pulse generation function
    - "Rhythm function" (function to mask a pulse signal)
  - AD converter (ADC)
    - General-purpose voltage measurement (5 channels. Shared with the GPIO pins.)
    - Power supply voltage (VBAT) measurement (1 channel. Connected internally.)
  - Interface for Emulator debug control
    - SWD (Serial Wire Debug): 2-wire system (1 channel)
- Clock
  - Reference clock (32 MHz)
    - Built-in crystal oscillator with a frequency adjustment function
  - Sleep clock (32.768 kHz)
    - Built-in crystal oscillator with a frequency adjustment function
    - External clock input is supported.
    - Built-in silicon oscillator (SiOSC)
  - Sleep clock output function (Shared with the GPIO pins.)

- Power supply
  - Power supply circuit
    - Support for wide range of the input power voltage
    - DC/DC converter and LDO regulator are integrated.
      - Built-in Power Management Unit for the low power consumption function.
    - Independent power pins for the I/O circuits (VDDIO)
- System function
  - 2 system configurations are supported.
    - Host-controlled system (A host CPU controls this device.)
    - Standalone system (The operation of this device is controlled by its own CPU.)
  - 3 operating modes are supported.
    - HCI mode
      - Control by HCI and Extended HCI commands
      - User application (firmware) programming
      - For radio certification tests in different countries and regions
      - For **Bluetooth**® qualification test
      - For other RF tests
    - Complete mode
      - Control of this device by the TCU commands (Control commands in the GATT/SM layer)
    - User-App mode
      - Download function of a user application program to this device
        - Download from the built-in Flash memory or host CPU (TC35680)
        - Download from an external EEPROM or a host CPU (TC35681)
      - Execution of a user application program
  - Low power system feature
    - 3 low power modes (Sleep, Backup, and Deep Sleep)
  - Support for Interrupts
  - Patch support
    - Patch function (maximum 4)
    - Auto-patch function
  - DMA support
    - Built-in 7-channel DMA controller (2 to 6 channels are available for a user.)
- Clock and Timer
  - RTC
    - RTC function with the accuracy of sleep clock frequency
    - Clock and Calendar function: YY/MM/DD hh:mm:ss (24-hour clock) and day of the week
    - Alarm function: Alarm setting by hh:mm and either a date or a day, and an interrupt by the alarm generation
    - Leap year function (the exceptional procedure for every 100 years is not supported.)
    - RTC is working even in the Sleep and Backup modes.
  - Timer
    - BCTimer
      - 3-channel hardware timer (One channel is dedicated to the system.)
      - 16-bit counter which can be loaded automatically every 1 µs at minimum.
      - The count of the timer stops in low power mode.
    - GTimer
      - 1-channel hardware timer
      - Built-in prescaler to divide the clock (1 to 1024 division). The minimum interval is 38 ns to 39 µs.
      - 16-bit counter which can be loaded automatically.
      - The count of the timer stops in low power mode.
    - OS timer (1-second timer and 1-ms timer)
      - Timer controlled by the OS
    - Watchdog timer (WDT) function

- Security
  - True Random Number Generator (TRNG)
    - A random number of 256 bits at maximum is generated by DRBG and ESG.
    - Compliant with NIST SP800-22 and BSI random number test.
  - Hardware encryption engine (AES128, only encryption)
- Package
  - TC35680FSG/TC35681FSG: QFN package [40 pins, 5 mm x 5 mm, 0.4-mm pitch, and 0.9-mm thickness]

2. Pin Assignment

2.1. Pin Assignment of TC35680FSG (Top View)

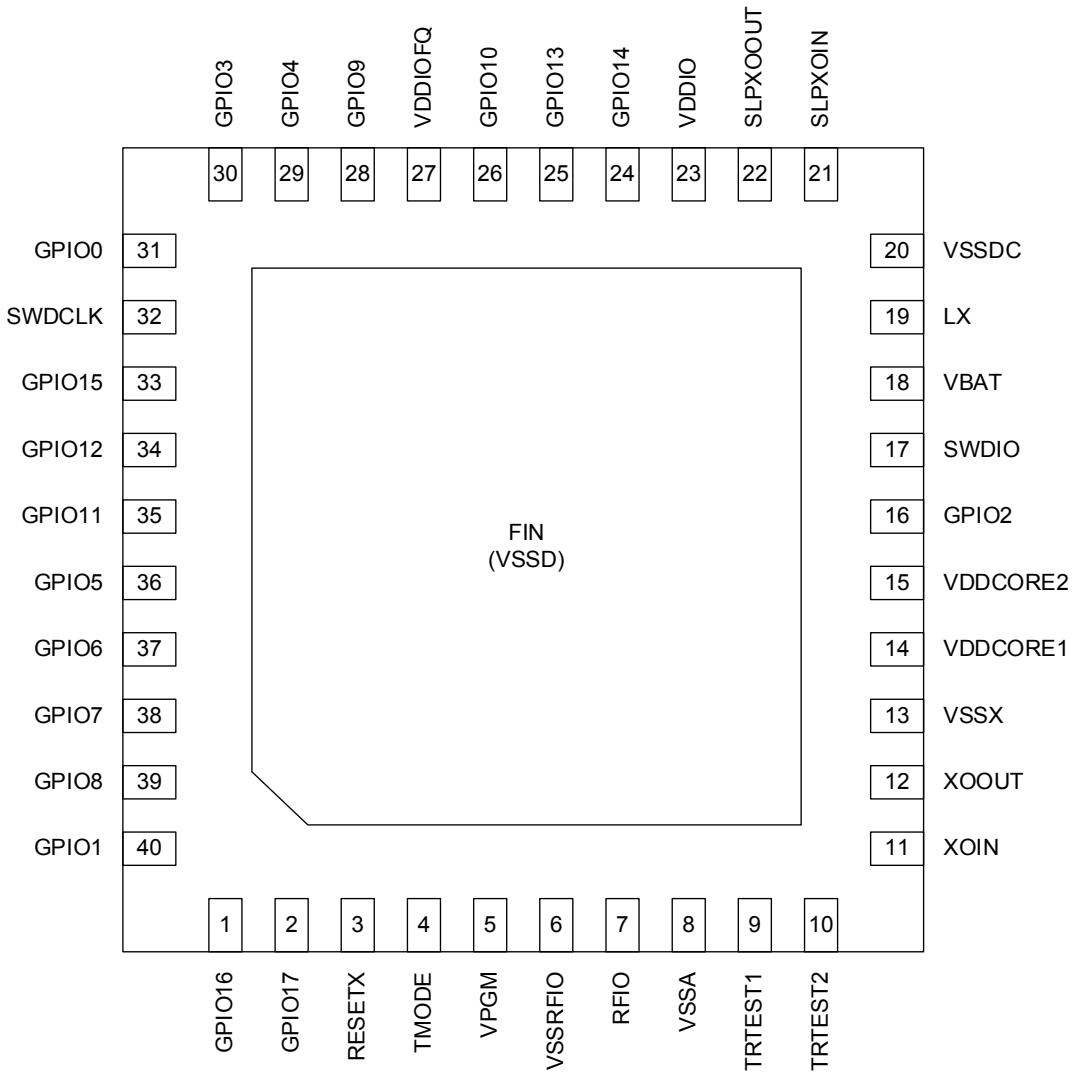


Figure 2-1 Pin assignment of TC35680FSG (Top view)

2.2. Pin Assignment of TC35681FSG (Top View)

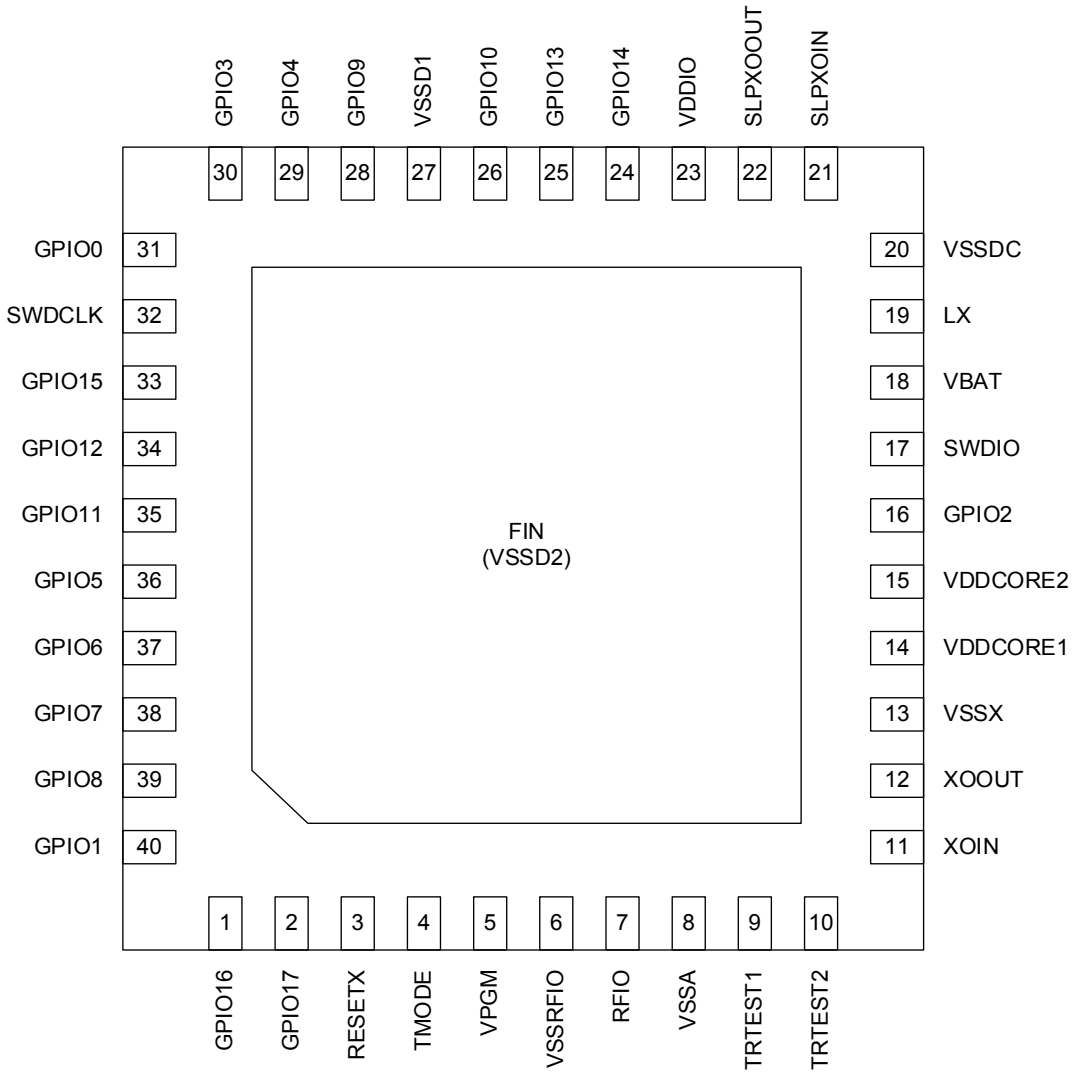


Figure 2-2 Pin assignment of TC35681FSG (Top view)

2.3. Function of Each Pin

The attribute, the status as output or input, and other functions of each pin are shown in Table 2-1.

The power supply pins are shown in Table 2-6.

Table 2-1 Function of each pin

Pin name	Pin No. QFN Package	Attribute Power supply group Signal direction I/O Type	Description
RESETX	3	VDDIO IN Schmitt trigger	Hardware reset input pin. Low level asserts the reset.
XOIN	11	VDDCORE1 IN OSC	Input pin for the reference clock oscillation. A 32-MHz crystal resonator with accuracy of ± 50 ppm or less should be connected to the XOIN pin and the XOOUT pin. The crystal oscillation circuit includes a variable capacitor (a capacitor array) to adjust the oscillation frequency.
XOOUT	12	VDDCORE1 OUT OSC	Output (feedback) pin for the reference clock oscillation.
SLPXOIN	21	VDDIO IN OSC	Input pin for the sleep clock oscillation by a crystal resonator. A 32.768-kHz crystal resonator with accuracy of ± 500 ppm or less should be connected to the SLPXOIN pin and the SLPXOOUT pin. The crystal oscillation circuit includes a variable capacitor (a capacitor array) to adjust the oscillation frequency. When an external clock is used, the clock should be input to this pin.
SLPXOOUT	22	VDDIO OUT OSC	Output (feedback) pin for the 32.768-kHz oscillation.
RFIO	7	VDDCORE1 IN/OUT Analog	RF signal input and output pin. The impedance matching of 50 Ω can be done by connecting a proper capacitor between the RFIO pin and GND. When this pin is connected to an antenna for communication, a series capacitor should be connected, because the signal of this pin has a DC bias. For the details, refer to the “Hardware Application Note” of this device.
GPIO0 GPIO15	31 33	VDDIO IN/OUT Pull-up/Pull-down resistors Schmitt trigger	General-purpose I/O pins. Following functions can be set by software; ✓ Switch as input or output. ✓ Connection or disconnection of a pull-up and a pull-down resistors (Note 1) ✓ Selection of output drivability. ✓ Setting of an interrupt. The interrupt can also be used to wake up from the Deep Sleep mode to the Active mode. For details of the function assignment, the low power consumption function, and the interrupt, refer to Section 2.4, Section 3.6, and Section 4.6, respectively.

Pin name	Pin No. QFN Package	Attribute Power supply group Signal direction I/O Type	Description
GPIO1 GPIO2 GPIO5 GPIO6 GPIO7 GPIO8 GPIO11 GPIO12 GPIO13 GPIO16 GPIO17	40 16 36 37 38 39 35 34 25 1 2	VDDIO IN/OUT Pull-up/Pull-down resistors Schmitt trigger	General-purpose I/O pins. Following functions can be set by software; ✓ Switch as input or output. ✓ Connection or disconnection of a pull-up and a pull-down resistors (Note 1) ✓ Selection of output drivability. ✓ Setting of an interrupt. For details of the function assignment, the low power consumption function, and the interrupt, refer to Section 2.4, Section 3.6, and Section 4.6, respectively.
GPIO3 GPIO4 GPIO9 GPIO10 GPIO14	30 29 28 26 24	VDDIO IN/OUT Pull-up/Pull-down resistors Schmitt trigger	ADC input and general-purpose I/O pins. Following functions can be set by software; ✓ Switch of input or output. ✓ Connection or disconnection of a pull-up and a pull-down resistors (Note 1) ✓ Selection of output drivability. ✓ Setting of an interrupt. ✓ ADC input For the details of the function assignment, the low power consumption function, the interrupt, and the ADC, refer to Section 2.4, Section 3.6, Section 4.6, and Section 4.11, respectively.
SWDCLK	32	VDDIO IN Pull-up/Pull-down resistors Schmitt trigger	SWD clock pin. Input pin of the Serial Wire Debug clock. When the function is not used, this pin should be open.
SWDIO	17	VDDIO IN/OUT Pull-up/Pull-down resistors Schmitt trigger	SWD data pin or Operating mode switching pin. Input or output data pin for the Serial Wire Debug. When the functions of this pin are not used, this pin should be open. This pin is also used to switch an operating mode. For the details of switching the operation mode, refer to Section 3.4.
TMODE	4	VDDIO IN Schmitt trigger	Test setting pin. This pin is used for a manufacturing test. It should be connected to GND when this device is used.
TRTEST1 TRTEST2	9 10	VDDCORE1 IN/OUT Analog	Test pins for analog. This pin is used for a manufacturing test. It should be connected to GND when this device is used.

Note 1: The values of the built-in pull-up and pull-down resistors vary widely; about 20 kΩ to 100 kΩ.

2.4. List of Functions of GPIO Pins

Some GPIO pins are used as multiplexed function pins. They have multiple functions such as a serial interface and others as well as a general-purpose I/O. The basic setting of the assignment of the function is done at boot timing by the built-in firmware program in the mask ROM. After boot up, a user application or a proper command from the host CPU can set expected functions to the corresponding GPIO pins.

Table 2-2 shows the status of each GPIO pin before the built-in firmware finishes the boot setting. And the functions which can be assigned to each GPIO by a user application program are shown in the same table. Unused pins can be open. “Disable” in the table means that both the input and output functions are disabled.

Some examples of the function setting are shown in Table 2-3.

Since it is not possible to assign one function to multiple GPIO pins simultaneously, care should be taken in function assignment for GPIO pins.

For details of the GPIO function, refer also to Section 4.6.

Table 2-2 Multiple functions of GPIO

Pin name (Function 0)	I/O function/Pin status		Function 1	Function 2	Function 3	Function 4	ADC
	During reset	Boot setting					
GPIO0	Disable/Hi-Z		—	—	—	—	—
GPIO1 (Note 1)	Disable/ Pull-up	Input/Pull-up or Input/Pull-down (Note 2)	—	—	—	—	—
GPIO2	Disable/Pull-up		PWM1 output	—	—	—	—
GPIO3	Disable/Hi-Z		PWM2 output	SPI-DOUT1 output	—	—	ADC1 input
GPIO4	Disable/Hi-Z		PWM3 output	SPI-DIN1 input	—	—	ADC2 input
GPIO5	Disable/Pull-up (Note 3)		UART1-TX output	—	—	—	—
GPIO6	Disable/Pull-up (Note 4)		UART1-RX input	—	—	—	—
GPIO7	Disable/Pull-up (Note 5)		I2C-SCL1 input and output	—	SPI-SCS1 input and output	UART1-RTSX output	—
GPIO8	Disable/Pull-up (Note 5)		I2C-SDA1 input and output	—	SPI-SCLK1 output	UART1-CTSX input	—
GPIO9	Disable/Hi-Z		I2C-SCL2 input and output	—	—	—	ADC3 input
GPIO10	Disable/Hi-Z		I2C-SDA2 input and output	—	—	—	ADC4 input
GPIO11	Disable/Pull-up		I2C-SCL2 input and output	SPI-DOUT2 output	—	—	—
GPIO12	Disable/Pull-up		I2C-SDA2 input and output	SPI-DIN2 input	—	—	—
GPIO13	Disable/Pull-up		UART1-RTSX output	PWM0 output	SPI-SCS2 input and output	UART2-RTSX output	—
GPIO14	Disable/Hi-Z		UART1-CTSX input	SLEEPCLK output	SPI-SCLK2 output	UART2-CTSX input	ADC5 input
GPIO15	Disable/Hi-Z		—	—	—	—	—
GPIO16	Disable/Pull-up		UART2-TX output	—	—	—	—
GPIO17	Disable/Pull-up		UART2-RX input	—	—	—	—

Note 1: This pin is used to switch an operating mode at the reset deassertion.
Note 2: “Input/Pull-up” in the User-App mode, and “Input/Pull-down” in the HCI mode or the Complete mode.
Note 3: “Disable/Pull-up” in the User-App mode, and “Output” in the HCI mode and the Complete mode. Function 1 is assigned.
Note 4: “Disable/Pull-up” in the User-App mode, and “Input/Pull-up” in the HCI mode and the Complete mode. Function 1 is assigned.
Note 5: When TC35681 is used, Function 1 is assigned in the User-App mode.

2.4.1. Example of GPIO Function Setting

Table 2-3 shows examples of the GPIO function settings.

Table 2-3 Example of GPIO function setting (QFN package)

Function setting	Function setting 1	Function setting 2	Function setting 3	Function setting 4	Function setting 5
Application	UART: 1 channel (4-wire system) UART: 1 channel (2-wire system) SPI: 1 channel ADC: 2 channels PWM: 3 channels	UART: 1 channel (4-wire system) I²C: 1 channel ADC: 2 channels PWM: 3 channels	UART: 1 channel (4-wire system) I²C: 1 channel ADC: 2 channels PWM: 3 channels	UART: 1 channel (4-wire system) I²C: 1 channel SPI: 1 channel ADC: 2 channels	UART: 1 channel (2-wire system) I²C: 1 channel
GPIO0	GPIO0	GPIO0	GPIO0	GPIO0	GPIO0
GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1
GPIO2	PWM1	PWM1	PWM1	GPIO2	GPIO2
GPIO3	PWM2	PWM2	PWM2	SPI-DOUT1	GPIO3
GPIO4	PWM3	PWM3	PWM3	SPI-DIN1	GPIO4
GPIO5	UART1-TX	UART1-TX	UART1-TX	UART1-TX	UART1-TX
GPIO6	UART1-RX	UART1-RX	UART1-RX	UART1-RX	UART1-RX
GPIO7	UART1-RTSX	UART1-RTSX	I2C-SCL1	SPI-SCS1	I2C-SCL1
GPIO8	UART1-CTSX	UART1-CTSX	I2C-SDA1	SPI-SCLK1	I2C-SDA1
GPIO9	ADC3	ADC3	ADC3	ADC3	GPIO9
GPIO10	ADC4	ADC4	ADC4	ADC4	GPIO10
GPIO11	SPI-DOUT2	I2C-SCL2	GPIO11	I2C-SCL2	GPIO11
GPIO12	SPI-DIN2	I2C-SDA2	GPIO12	I2C-SDA2	GPIO12
GPIO13	SPI-SCS2	GPIO13	UART1-RTSX	UART1-RTSX	GPIO13
GPIO14	SPI-SCLK2	GPIO14	UART1-CTSX	UART1-CTSX	GPIO14
GPIO15	GPIO15	GPIO15	GPIO15	GPIO15	GPIO15
GPIO16	UART2-TX	GPIO16	GPIO16	GPIO16	GPIO16
GPIO17	UART2-RX	GPIO17	GPIO17	GPIO17	GPIO17

2.4.2. Limitation on Assignment of UART Function to GPIO

The UART which can be assigned to GPIO in TC35680/TC35681 is shown in Table 2-4. The GPIO's which can be assigned to the UART interface depend on an operating mode.

Table 2-4 GPIO assignment of 2 UART interfaces (QFN package)

Operating mode	HCI mode/Complete mode	User-App mode
UART1-TX	GPIO5 is used. (Non-modifiable)	GPIO5 can be used.
UART1-RX	GPIO6 is used. (Non-modifiable)	GPIO6 can be used.
UART1-RTSX	Only GPIO7 can be used.	Either GPIO7 or GPIO13 can be used. (Note 1)
UART1-CTSX	Only GPIO8 can be used.	Either GPIO8 or GPIO14 can be used. (Note 1)
UART2-TX	Not assigned	GPIO16 can be used.
UART2-RX	Not assigned	GPIO17 can be used.
UART2-RTSX	Not assigned	GPIO13 can be used. (Note 1)
UART2-CTSX	Not assigned	GPIO14 can be used. (Note 1)

Note 1: GPIO13 cannot be assigned to both UART1-RTSX and UART2-RTSX at the same time.
GPIO14 cannot be assigned to both UART1-CTSX and UART2-CTSX at the same time.

2.4.3. Limitation on Assignment of I^2C Function to GPIO

TC35681 uses GPIO7 and GPIO8 as the channel 1 of I^2C1 interface to an EEPROM which stores a user application program. Another channel of the I^2C interface cannot be assigned in the start-up sequence.

Table 2-5 Assignment of 2 I^2C interfaces

Product	TC35680		TC35681	
Operating mode	HCI mode/ Complete mode	User-App mode	HCI mode/ Complete mode	User-App mode
I2C-SCL1	GPIO7 can be used.		GPIO7 can be used.	GPIO7 is used. (Non-modifiable)
I2C-SDA1	GPIO8 can be used.		GPIO8 can be used.	GPIO8 is used. (Non-modifiable)
I2C-SCL2	GPIO9 and GPIO11 can be used.		GPIO9 and GPIO11 can be used.	
I2C-SDA2	GPIO10 and GPIO12 can be used.		GPIO10 and GPIO12 can be used.	

2.5. Power Supply Pins

The attribute and the normal operation voltage of each power supply pin are shown in Table 2-6.

Table 2-6 Power supply pin

Pin name	Pin No. QFN Package	Attribute Type VDD/GND	Description
VDD/GND			
VPGM	5	TEST —	Power supply pin for test. This pin should be connected to GND.
VBAT	18	VBAT VDD	Power supply pin for DC/DC converter/LDO regulator and the sleep circuit. An external power supply should be connected to this pin to operate the built-in DC/DC converter and LDO regulator.
LX	19	VBAT VDD	DC/DC converter output pin. When the DC/DC converter is used, the power is supplied to VDDCORE1 and VDDCORE2 from this pin. An external coil for the DC/DC converter should be connected. For details, refer to Section 4.4. Any other use is not possible.
VDDCORE1	14	— VDD	Power supply input pin for the analog circuit. The LX pin supplies power when the DC/DC converter is used. And the VDDCORE2 pin supplies power when the transition to a low power mode is done or when the LDO is used. This pin should be connected to the VDDCORE2 pin. For details, refer to Section 4.4. Any other use is not possible.
VDDCORE2	15	— VDD	A feedback input pin for the DC/DC converter. It is also a power supply pin for the analog and digital circuits, and the output pin of the built-in LDO regulator, as well. When the DC/DC converter is used, this pin is a feedback input pin. A coil should be connected between this pin and the LX pin. When the built-in LDO regulator is used, this pin is an output pin of the regulator. The internal circuits connected to VDDCORE1 and VDDCORE2 are supplied with the power. For details, refer to Section 4.4. Any other use is not possible.
VDDIO	23	VDDIO VDD	Power supply pin for I/O. The power of the proper voltage for the GPIO circuits should be supplied. The voltage should not exceed the VBAT value. For details, refer to Section 4.4. Any other use is not possible.

Pin name	Pin No. QFN Package	Attribute Type VDD/GND	Description
VDD/GND			
VDDIOFQ	27	VDDIOFQ VDD	(Only TC35680) This pin should be connected to an external capacitor for the power supply of the built-in Flash memory (output). This pin is connected to the power supply of the built-in Flash memory. A load capacitor of 0.1 μF or more in the operation temperature range should be connected for the LDO regulator. Any other use is not possible.
VSSD1	27	Digital GND	(Only TC35681) This pin should be connected to GND.
VSSA	8	Analog GND	GND pin for the analog circuits. This pin should be connected to GND.
VSSRFIO	6	Analog GND	GND pin for RFIO. This pin should be connected to GND.
VSSX	13	Analog GND	GND pin for OSC. This pin should be connected to GND.
VSSDC	20	Digital GND	GND pin for the DC/DC converter. This pin should be connected to GND.
VSSD VSSD2(Note1)	FIN	Digital GND	Die pad GND (FIN). This pin is shared with the GND of the digital circuits. The die pad on the bottom of the package should be connected to GND.

Note1:Only TC35681

3. Device Overview

3.1. Internal Block Diagram

The internal block diagrams of TC35680 and TC35681 are shown in Figure 3-1 and Figure 3-2, respectively. An example of connection of main components is shown in each figure, as well.

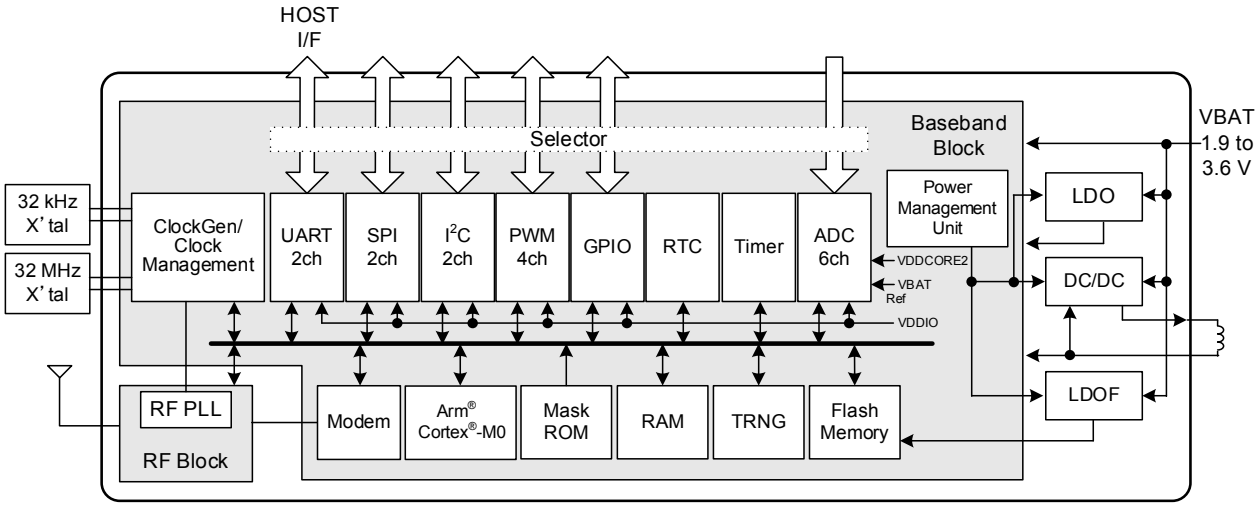


Figure 3-1 Internal block diagram of TC35680 and an example of connection of main components

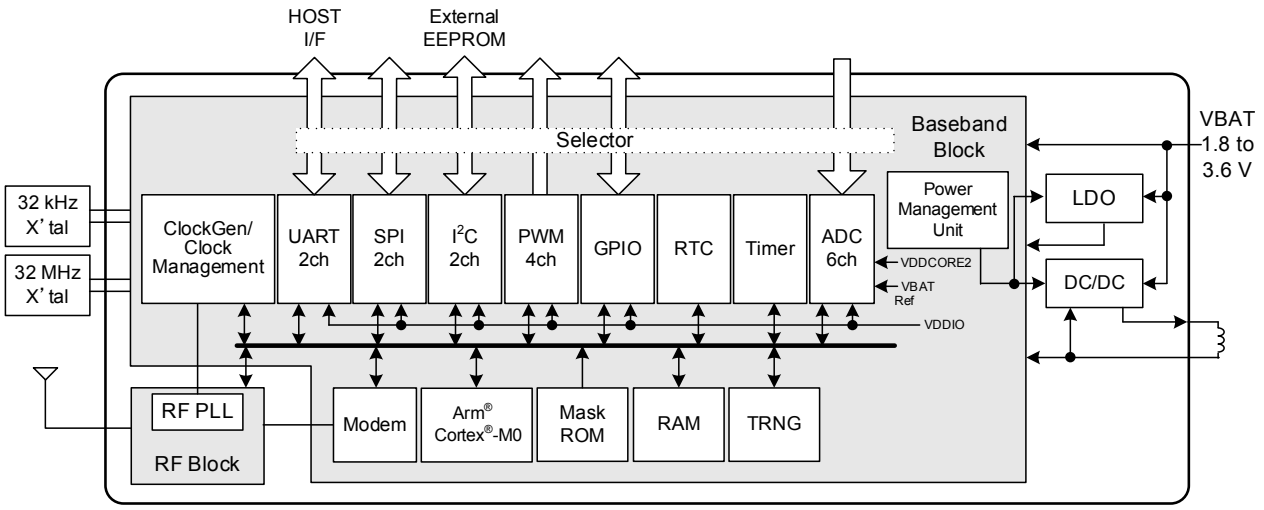


Figure 3-2 Internal block diagram of TC35681 and an example of connection of main components

3.1.1. Power Supply System

TC35680/TC35681 integrate a DC/DC converter and multiple LDO regulators. Many circuits in the device are supplied with power from step-down power supply. Power Management Unit (PMU) switches the power supplies dynamically and controls the output voltage to optimize power efficiency according to low power modes.

The power dedicated to the digital interface can be supplied on the VDDIO pin. So system design or user application need not care about the power control done by the PMU.

For details of the power supply system, refer also to Section 3.6 and Section 4.4.

3.1.2. Clock System

The frequency of the reference operation clock is 32 MHz. And the frequency of the sleep clock is 32.768 kHz. Each clock circuit has its own clock divider, so each block including the CPU can be supplied with an optimized clock. For the setting parameters for each block, refer to the function description in Chapter 4. For the details of the reference clock and the sleep clock, refer to Section 4.12 and Section 4.13, respectively.

The source of the sleep clock of TC35680/TC35681 can be selected from among the following three clock sources. At start-up, the built-in silicon oscillator (hereafter, SiOSC) is used.

- SiOSC
- Crystal resonator (A crystal oscillation circuit is used.)
- External sleep clock input

The frequency accuracy of the SiOSC is not compliant with the **Bluetooth®** connection. It cannot be used for the application which executes the **Bluetooth® connection**. The SiOSC can be used for application which includes advertising only, and others.

For the details of the sleep clock, refer to Section 4.13.

3.1.3. Hardware Start-up Sequence

The sequence of the start-up of the power supply and the reset deassertion are shown in Figure 3-3. For sequence of the start-up of the built-in firmware, refer to Section 3.5. For details of the reset, refer to Section 4.5.

The VBAT power should be supplied first. The VDDIO power can be supplied simultaneously. The voltage of the VDDIO, however, should not exceed the voltage of the VBAT. The reset should be deasserted after the voltage of the VBAT reaches the minimum value of VBATopr in Section 5.2 and the voltage of the VDDIO also reaches the minimum value of VDDIOopr.
When the reset is deasserted, the crystal oscillator for the reference clock starts to operate.
And the SiOSC starts oscillating to supply the sleep clock.
The reference clock should become stable in 1.5 ms for a circuit of TC35680/TC35681. It is needed that a stable time of the reference clock keeps within1.5 ms

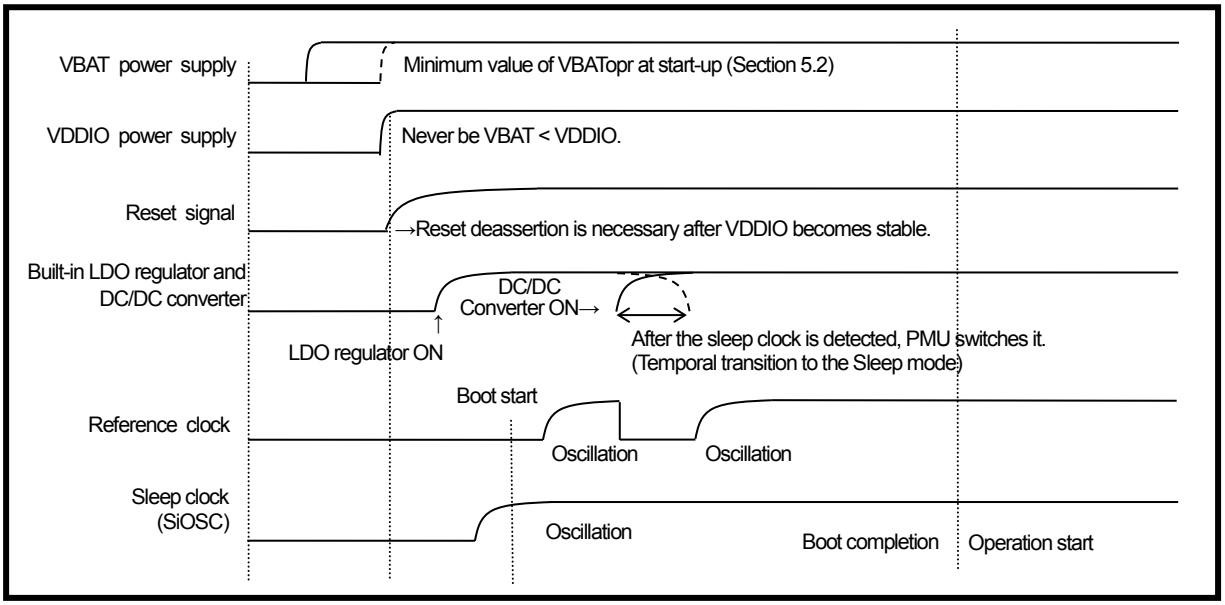


Figure 3-3 Hardware start-up sequence

3.2. System Configuration and Operating Mode

TC35680/TC35681 support two system configurations and three operating modes, as shown in Figure 3-4.

- System configuration
  - Configuration that this device is controlled by an external host CPU (Host-controlled system)
  - Configuration that this device is controlled by its own CPU using a user application program (Standalone system)

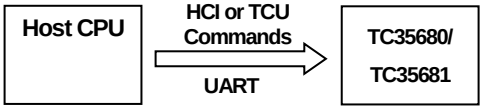
- Operating mode
  - Controlled by HCI/Extended HCI commands in the Host-controlled system (HCI mode).
  - Controlled by TCU commands in the Host-controlled system (Complete mode).
  - Controlled by the built-in CPU in TC35680 or TC35681 using a user application program (User-App mode)

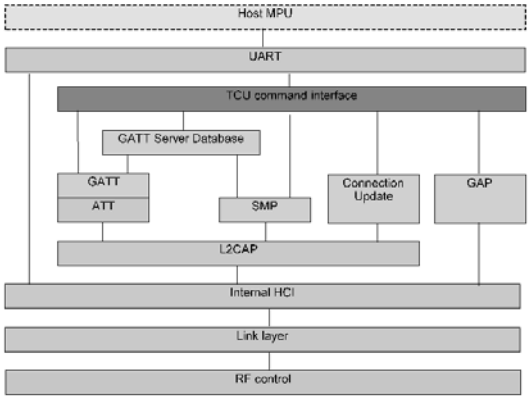
    Following 3 methods are available to download a user application program;
    - ✓ Download from the built-in Flash memory (TC35680)
    - ✓ Download from an external EEPROM (TC35681)
    - ✓ Download via the UART interface (TC35680/TC35681)

For the details of the selection of the operating mode, refer to Section 3.4.

■ **HCI mode/Complete mode**

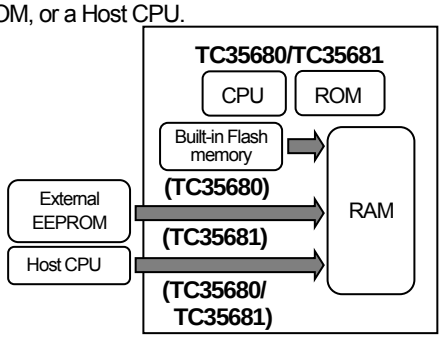
Controlled by a host CPU.





■ **User-App mode**

Controlled by a user application program in the built-in Flash ROM, an external EEPROM, or a Host CPU.



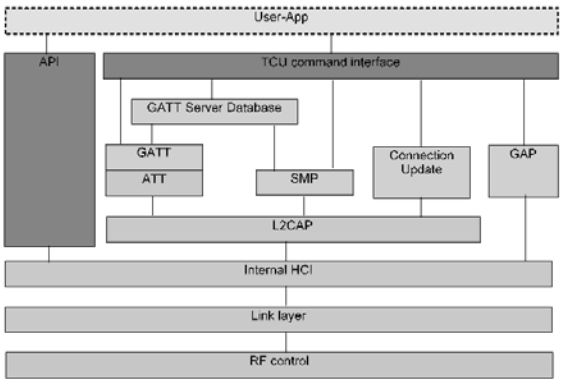


Figure 3-4 Example of system configuration of TC35680/TC35681

3.3. System Configuration

3.3.1. Standalone System

When the standalone system is configured, a user application program should be stored in the built-in Flash memory (TC35680) or an external EEPROM (TC35681) in the User-App mode.

In the User-App mode, a boot loader in the mask ROM reads the user application program from the built-in Flash memory or an external EEPROM and writes to the RAM in the standalone system, then the user application program is executed. An external CPU is not necessary in the system. Then, the standalone operation is enabled.

3.3.2. Host-Controlled System

The host-controlled system can be configured by the following three methods;

- ✓ Using the HCI mode.
- ✓ Using the Complete mode.
- ✓ Using the User-App mode.

The built-in firmware is used to configure the system in the HCI and the Complete modes.

In the User-App mode, a user application program is executed by the CPU in TC35680/TC35681. And in the system, the host can operate together with it.

3.4. Selection and Setting of Operating Mode

The following two methods are available to set an operating mode.

- ✓ Setting is done by the status of the GPIO1 and SWDIO pins at start-up
- ✓ Setting is done by the HCI_SET_MODE command after start-up in the HCI mode. (The Complete mode or the User-App mode can be selected.)

Table 3-1 shows the application of each operating mode and its setting at start-up.

When the User-App mode is selected at start-up, it is not possible to switch directly to the HCI mode. A restart (a hardware reset assertion) is necessary to switch from the User-App mode or the Complete mode to another operating mode.

Table 3-1 Application of each operating mode and its setting at start-up

Operating mode	Setting at start-up		Application
	GPIO1	SWDIO	
User-App mode	H	—	✓ Execution of a user application program
HCI mode	L	H	✓ RF test ✓ Radio Frequency (RF) Certification test ✓ **Bluetooth**® Qualification test ✓ Programming of a user application program (firmware) ✓ Control by HCI/Extended HCI commands
Complete mode	L	H	✓ Device control by TCU commands (Control commands in the GATT/SM layer)
Test mode	L	L	This setting is prohibited.

Note: The built-in firmware assigns the input function with the pull-up resistor ON to the GPIO1 pin at start-up. So, when the pin is open at start-up, the User-App mode is selected. When the setting pins are pulled down with external resistors, respectively, the values of the resistors should be sufficiently lower than the values of the internal pull-up resistors. 1 kΩ, for example, is OK.

3.4.1. HCI Mode

In the HCI mode, a host CPU controls TC35680/TC35681 using the HCI commands and the Extended HCI commands which are stored in the built-in firmware. The host CPU is connected to TC35680/TC35681 with the UART interface. The HCI mode is used for the following purposes;

- TC35680/TC35681 are controlled using the HCI commands and the Extended HCI commands.
- **Bluetooth**® Qualification test and Radio Frequency (RF) Certification test in different countries and regions.
- A user application program (firmware) is programmed to the built-in Flash memory.
- RF test is done.
- The operating mode is changed by the HCI command.

The program for the HCI mode is stored in the mask ROM as a built-in firmware. So, in HCI mode, the TC35680/TC35681 do not execute a user application program which is executed by the CPU of the TC35680/TC35681. After start-up, the GPIO5 pin (UART1-TX) and the GPOO6 pin (UART1-RX) are assigned to the UART interface pins by the built-in firmware.

The initial setting of the UART interface in the HCI mode is shown in Table 3-2.

Table 3-2 Initial setting of UART interface in HCI mode

Baud rate	115.2 kbps
Parity bit	None
Data length	8 bits
Stop bit	1 bit
Flow control	None
Protocol	HCI

3.4.2. Complete Mode

After start-up in the HCI mode, a proper command can switch to the Complete mode. Then a TCU command can be used to control the system. The TCU command is a control API in the GATT/SM layer, and it is stored in the mask ROM.
The HCI_SET_MODE command is used to switch the HCI mode to the Complete mode.

3.4.3. User-App Mode

In the User-App mode, a user application program is executed by the CPU in TC35680/TC35681. The user application program can use the **Bluetooth**® Low Energy protocol stack and a hardware control API in the built-in firmware. In this document, the control function that can be used in the User-App mode is described as “API”.
TC35680/TC35681 download a user application program with one of the following methods, and execute the program.

- ✓ Download of the user application program which is stored in the built-in Flash memory (TC35680) or an external EEPROM (TC35681) in the proper format
- ✓ Download of a user application program from the host CPU via the UART interface

The storage memory of a user application program is the built-in Flash memory in TC35680 or an external EEROM for T35681. TC35681 and the EEPROM should be connected with the I^2C interface (GPIO7 and GPIO8).

A user application program cannot occupy all resources of the CPU. The built-in firmware also uses resources of the CPU. So user should fully evaluate that a desired functions are executed as expected and the performance reaches the target level.

3.5. Start-up Sequence

The boot loader and the built-in firmware in TC35680/TC35681 recognize the operating mode and complete the start-up procedure, as shown in Figure 3-5.

The download procedure via the UART interface and the execution procedure are done by the HCI command after TC35680/TC35681 start up in the HCI mode.

3.5.1. Details of Start-up Sequence

(1) Reset is deasserted.
(2) “enable” or “disable” setting of SWD in this device is checked.
(3) When the result is “disable”, the SWD function is set to disabled.
(4) When the result is “enable”, the SWD function is set to enabled.
(5) The firmware start-up is executed.
(6) The password for the SWD in the built-in Flash memory is checked.
(7) When the password for the SWD is stored in the built-in Flash memory, an access to the built-in Flash memory and RAM spaces are restricted.
(8) When the password for the SWD is not stored in the built-in Flash memory, the SWD is set to being enabled.
(9) The presence of the auto-patch programs are checked.
  ✓ For the details of the auto-patch function, refer to Section 4.16.
(10) When the auto-patch programs are present in the built-in Flash memory or the external EEPROM, the auto-patch programs are adopted.
(11) When the auto-patch programs have been adopted or when the auto-patch programs are not present, the status of the GPIO1 pin is checked.
(12) When the GPIO1 pin is Low, the status of the SWDIO pin is checked.
(13) When the SWDIO pin is Low, this device enters a test mode. This setting is not usable.
(14) When the SWDIO pin is High, this device starts up in the HCI mode.
(15) When the GPIO1 pin is High, “Check word” in the user application program stored in the built-in Flash memory or the external EEPROM is read.
(16) A match between “Check word” and a preset value is checked.
When “Check word” does not match with the preset value, this device starts up in the HCI mode.
(17) When “Check word” matches with the preset value, the user application program in the built-in Flash memory or the external EEPROM is downloaded to TC35680/TC35681.
(18) A checksum value stored in the built-in Flash memory or the external EEPROM is compared with the checksum value which is calculated using the downloaded user application program.
(19) When those checksum values matched, the built-in firmware executes the user application program.
(20) When those checksum values did not match, the error occurs. The hardware reset is needed.

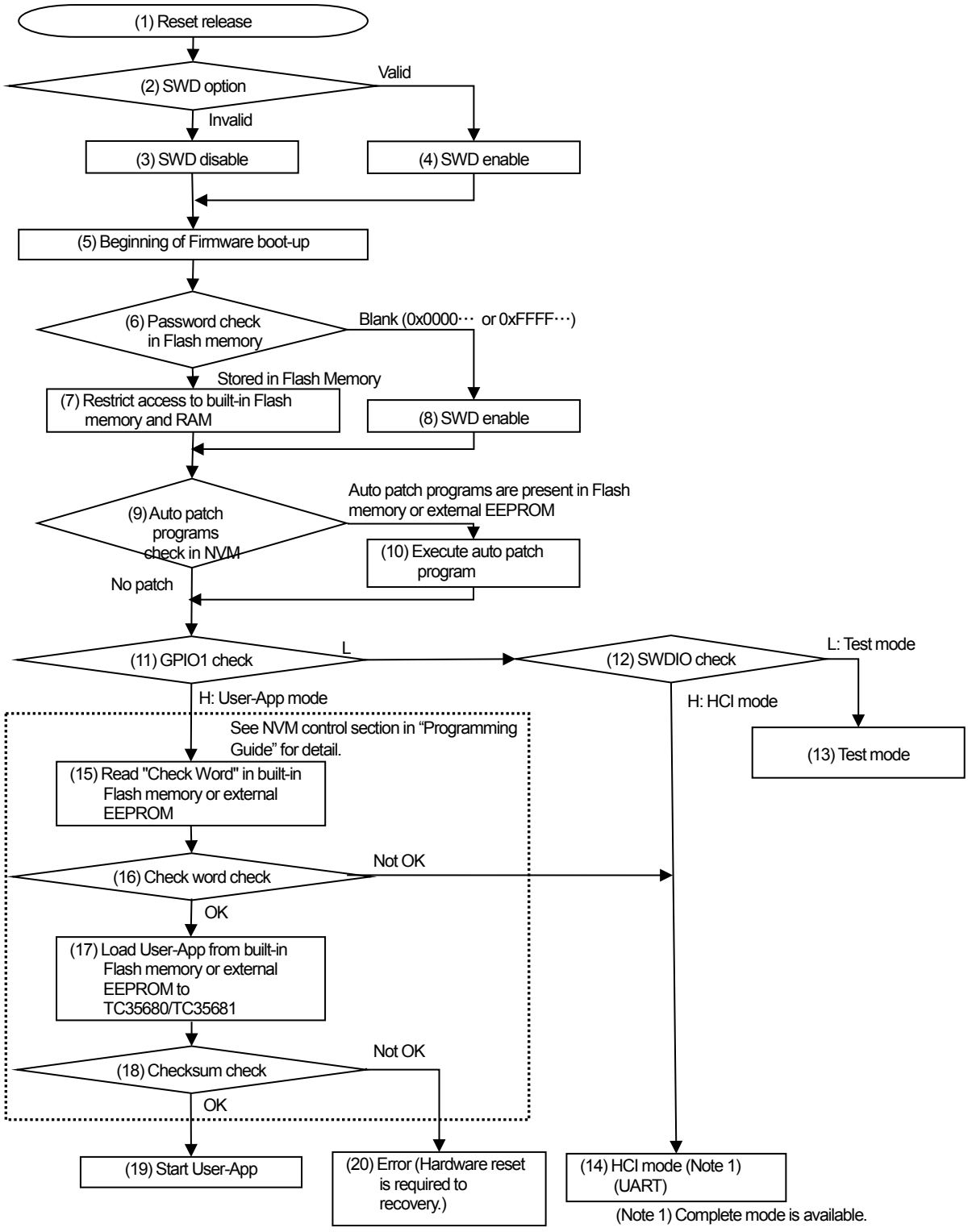


Figure 3-5 TC35680/TC35681 boot sequence

3.6. Low Power System

TC35680/TC35681 support the following three low power modes to save power consumption.

- Sleep
- Backup
- Deep Sleep

The power consumption decreases in the order of the Sleep, the Backup, and the Deep Sleep modes. The lowest power consumption is realized in the Deep Sleep mode.

The low power consumption function are independent of the operation mode (the HCI mode, the Complete mode or the User-App mode).

3.6.1. State Transition

Figure 3-6 shows the state transition diagram of TC35680/TC35681. There are three main states.

- Active mode
- Reset
- Low power mode

The Active mode is a normal operating state. The Reset is the state when a hardware reset is asserted. The Low power mode is either the Sleep, the Backup or the Deep Sleep state.

In this document, the transition from the Low power mode to the Active mode is defined as “Wake-up”. And the transition from the Active mode to the Low power mode is defined as “Sleeping”.

The transition from the Active mode to the Low power mode can be done by Sleeping. The direct transition among the low power states is not possible.

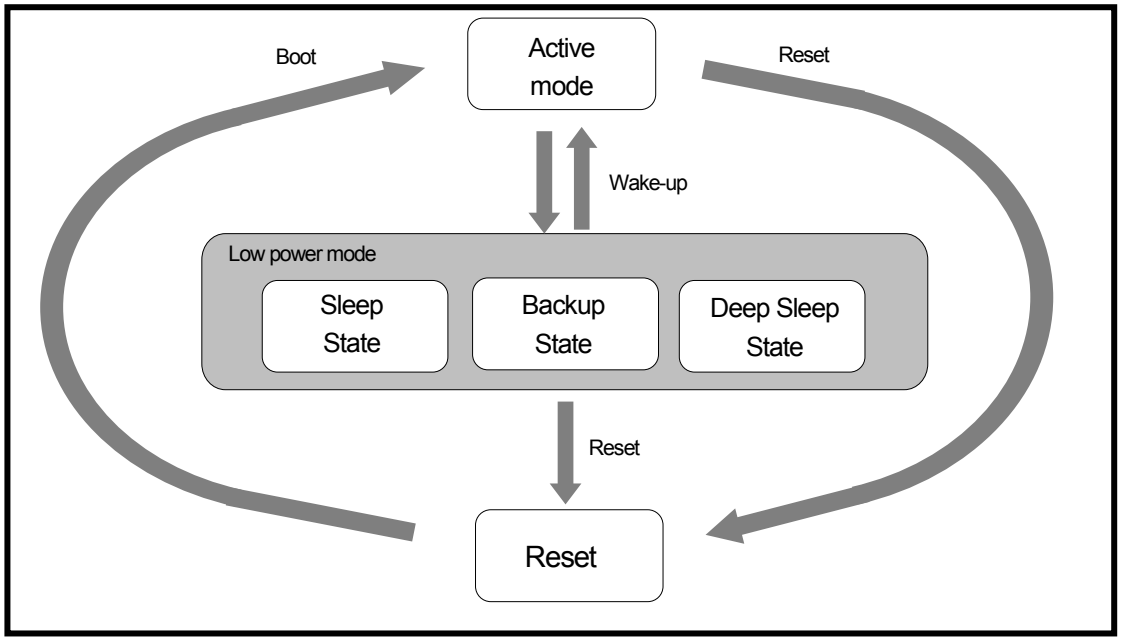


Figure 3-6 State transition diagram

3.6.2. Available Functions in Each Low Power Mode

Available functions in each low power mode are shown in Table 3-3.

A suitable low power mode should be selected. For the details of the current consumption, refer to Section 5.3.

Table 3-3 Available functions

Function		Active mode	Sleep mode	Backup mode	Deep Sleep mode (Note 1)
Reference clock		Oscillation	Stop	Stop	Stop
Sleep clock		Oscillation	Oscillation	Oscillation	Stop
CPU power supply		ON	ON	OFF	OFF
CPU clock		16 MHz/32 MHz	Stop	Stop	Stop
Built-in power supply		DC/DC converter: 1.2 V (Commodity devices) or LDO regulator: 1.2 V (Customized devices)	LDO regulator: 0.85 V	LDO regulator: 0.85 V	DC/DC converter: OFF LDO regulator: OFF
RAM		Whole data is retained.	Whole or part of the data before entering this mode is retained. Or, no data is retained. (Note 2)	Whole or part of the data before entering this mode is retained. Or, no data is retained. (Note 2)	No data before entering this mode is retained. (Note 2)
Bluetooth® wireless	Connection	Available	Available	TC35680/TC35681 do not enter this mode during communicating.	Not available
	Scan		Available	TC35680/TC35681 do not enter this mode during scanning.	
	Advertise		Available	Available (Note3)	
	Initiating		Available	TC35680/TC35681 do not enter this mode during initiating.	
Hardware reset		Available	Available	Available	Available
GPIO		Available	Except the ANYKEY wake-up, the GPIO0 wake-up and the GPIO15 wake-up, other GPIO functions are not executed in this mode. After a wake-up, the settings before entering this mode are resumed.		Except the GPIO0 wake-up and the GPIO15 wake-up, other GPIO functions are not executed in this mode. Before entering this mode, the status is retained.
UART		Available	This IC does not enter this mode during communication. In this mode, any UART functions are not executed. Only when the API described in the “Programming Guide” is used to control the UART, the settings before entering this mode are resumed.		Deactivated.
SPI		Available	This IC does not enter this mode during communication. In this mode, any SPI functions are not executed. After a wake-up, the settings before entering this mode are resumed.		Deactivated.
I^2C		Available	This IC does not enter this mode during communication. In this mode, any I^2C functions are not executed. After a wake-up, the settings before entering this mode are resumed.		Deactivated.
PWM		Available	Before entering this mode, this PWM function should be stopped. After wake-up, the settings before entering this mode are resumed.		Deactivated.
ADC		Available	This IC does not enter this mode during ADC is operated. In this mode, ADC functions are not executed. After wake-up, the settings before entering this mode are resumed.		Deactivated.

Function	Active mode	Sleep mode	Backup mode	Deep Sleep mode (Note 1)
TRNG	Available (execution together with a wireless communication is not recommended.)	In this mode, TRNG functions are not executed. The random number seed before entering this mode is not resumed after a wake-up.		Deactivated.
Sleep clock output function	Available	In this mode, this function is not executed. After a wake-up, the settings before entering this mode are resumed.		Deactivated.
BCTIMER and GTIMER	Available	In this mode, functions of BCTIMER and GTIMER are not executed. After a wake-up, the settings before entering this mode are resumed and each counter is initialized.		Deactivated.
OS timer (1-second timer and 1-ms timer)	Available	Available	This OS timer does not enter this mode during counting.	Deactivated.
RTC	Available	Available		Deactivated.
WDT	Available	In this mode, WDT functions are not executed. After wake-up, the settings before entering this mode are resumed and the counter is initialized.		Deactivated.
DMAC	Available	In this mode, DMAC functions are not executed. Only when the API is used to control the UART or the **Bluetooth® connection**, the settings before entering this mode are resumed.		Deactivated.
SWD	Available	Deactivated.		Deactivated.
Built-in Flash memory (Note 4)	Available	This IC does not enter this mode when the accessing to the built-in Flash memory is opened (“SYS_API_QSPI_SrorageClose()” or ”SYS_API_QSPIDirectStorageClose() is not done)”.		Deactivated.

Note 1: The same procedure is necessary as the procedure for the return from the cold boot, after the Deep Sleep mode id switched to the Active mode.

Note 2: The same procedure is necessary as the procedure for the return from the cold boot, when the RAM data has not been retained before entering this mode.

Note 3: In the case that the auto-advertise function is used. For the details, refer to Section 4.3.

Note 4: Only for TC35680.

3.6.3. Condition on Transition to Low Power Mode

The transition to a low power mode is enabled by the HCI command "HCI_M2_BTL_LOW_POWER_MODE" and API "SYS_API_SetBlesglSleepCtrl()". The several low power modes can be enabled.

When a multiple low power modes are enabled, TC35680/TC35681 can select among them the smallest power mode which meets the conditions.

TC35680/TC35681 transition to a low power mode automatically when all the following conditions are met.

- Transition to one or more low power modes is enabled.
- The other tasks which are controlled by the built-in firmware are in the idle state.
- When GPIO0 or GPIO15 is set to a wake-up input, an appropriate signal is input to the pin.
- Neither UART, SPI, nor I^2C interface transfers any data.
  - ✓ If the UART is not transferring just using "uart1_Open()", the transition to a low power mode can be done.
- AD convertor is not operated.
- The accessing to built-in Flash memory is closed. ("SYS_API_QSPI_SrorageClose()" or "SYS_API_QSPIDirectStorageClose()" is done.)
- **Bluetooth®** Advertising is not ongoing (the condition to transit to the Deep Sleep mode).
- The **Bluetooth® connection** has not been established (the condition to transit to the Backup or the Deep Sleep mode).

The followings are the conditions to transit to a low power mode in the User-App mode.

- The user application task waits for an event using the API "OS_API_WaitEventFlg()".
- Neither 1-second timer nor 1-ms timer operates (the condition to transit to the Backup or the Deep Sleep mode).

3.6.4. Condition on Return from Low Power Mode

The low power mode of TC35680/TC35681 can be enabled to switch to the Active mode by the following condition.

- ✓ One of the triggers in Table 3-4 occurs in the corresponding low power mode.

Even if TC35680/TC35681 is in the Low power mode, they temporarily return to the Active mode at the timing of the Bluetooth® connection or the timing of Advertising or Scanning without the wake-up notification to the host CPU and user application. After executing the communicating, they enter the Low power mode again.

Table 3-4 Wake-up and boot factors

Sleep mode	Backup mode	Deep Sleep mode	Reset mode
✓ GPIO0 interrupt or GPIO15 interrupt ✓ ANYKEY wake-up interrupt ✓ RTC alarm ✓ Expiration of the counter of the 1-second timer or the 1-ms timer. ✓ Reception of a packet from a remote device. ✓ Hardware reset deassertion. ✓ One hour elapses after the transition to the Sleep mode. (Note 2)	✓ GPIO0 interrupt or GPIO15 interrupt ✓ ANYKEY wake-up interrupt ✓ RTC alarm ✓ Connection request from a remote device (Note 3) ✓ The number of the auto-advertising becomes a set value. (Note 1) ✓ Hardware reset deassertion	✓ GPIO0 interrupt or GPIO15 interrupt ✓ Hardware reset deassertion	✓ Hardware reset deassertion

Note 1: When the Auto-Advertising function is set before the transition to the Backup mode, TC35680/TC35681 wake up themselves after a set number of the Advertising packets are transmitted.

Note 2: If there is counter which can count more than one hour using the 1-second timer, TC35680/TC35681 wake up themselves temporarily every hour in the Sleep mode. This wake-up notification isn't sent to the user application. The time interval cannot be changed.

Note 3: In the case that the Auto-Advertising function is used. For the details, refer to Section 4.3.

3.6.5. Acquisition of Wake-up Factor and Return from Low Power Mode

The user application can acquire a wake-up factor by using the API "SYS_API_GetWakeUpCauseValue()". After the acquisition of the wake-up factor, a proper procedure in the user software program should be done. For details of the wake-up factors and the API, refer to the "Programming Guide".

The procedure for wake-up in the Deep Sleep mode is the same as that of the cold boot. It can be recognized that the wake-up is done at the Deep Sleep mode.

If the retention of the RAM data is not set before Sleeping, the data is lost at the wake-up in a low power mode.

4. Functions

4.1. Bluetooth® Wireless Communication

For certain comer cases, either the industry standard of its implementation for **Bluetooth® connection** functions in TC35680/TC35681 series has some known issue. The issues and their countermeasures are summarized in Known Issues document which a user should refer to.

The **Bluetooth® connection** is performed by the hardware which is configured by an RF circuit and a baseband circuit as well as the built-in firmware. The wireless communication can be realized by this device and the external components such as a crystal resonator and other discrete devices.

4.1.1. Supported Functions

The list of the functions supported by TC35680/TC35681 is shown in Table 4-1.

TC35680/TC35681 of ROM version 002 operates as the Central or the Peripheral and they are connected to one device.

Table 4-1 List of supported functions

Bluetooth® core spec. feature	Description	Notes
v4.0 features	Central	Supported
	Peripheral	Supported
	Multi point connections	Not supported
	Connection Update	Supported
	Random Address	Supported
	WhiteList	Supported
	Security Property (Just Works)	Supported
	Security Property (PassKey Entry)	Supported
	Security Property (OOB)	Not supported
	Security Property (Numeric Comparison)	Supported
	GATT-Client	Supported
	GATT-Server	Supported
	Broadcaster	Supported
	Observer	Supported
v4.1 features	Low Duty Cycle Directed Advertising	Supported
	32-bit UUID support in LE	Supported
	LE L2CAP Connection Oriented Channel Support	Not supported
	LE Privacy v1.1	Not supported
	Connection Parameter Request Procedure	Supported
	Extended Reject Indication	Supported
	Slave-initiated Features Exchange	Supported
	LE Ping	Supported
	Act as LE Master and LE Slave at the same time	Not Supported
	Act as LE Slave to more than one LE Master at the same time	Not Supported
v4.2 features	LE Data Packet Length Extension (Max payload length 255 bytes)	Supported
	LE Secure Connections	Supported
	Link Layer Privacy	Supported
	Link Layer Extended Scanner Filter Policies	Supported
v5.0 features	LE 2M PHY	Supported
	LE Coded PHY	Supported
	Channel Selection Algorithm #2	Supported
	LE Extended Advertising(Max 1650 bytes)	Supported
	LE Extended Scanning(Max 1650 bytes)	Supported
	Stable Modulation Index - Transmitter	Not supported
	Stable Modulation Index - Receiver	Not supported
	LE Periodic Advertising	Not supported
	Minimum Number of Used Channels Procedure	Supported
	High Duty Cycle Non-Connectable Advertising	Supported

4.1.2. RF Function

The RF function in TC35680/TC35681 has the following features;

- Built-in transmission and reception circuits
- Built-in balun
- Built-in RF switch circuit
- Output power setting
- ±2 dB (typical) accuracy for the receive signal level

The impedance matching can be done by connecting a proper capacitor between the RFIO pin and GND. The signal of this pin has a DC bias during communication. It is recommended that a series capacitor should be connected to cut the DC bias. For details, refer to the design guide in the "Hardware Application Note" of this device.

4.2. Output Power Setting

The output power can be selected from among +8, +7, +6, +4, 0, -6, and -20 dBm (typ.) using the HCI command or the API "SYS_API_SetTransmitPowerLevel()". The default value is +8 dBm.

This function can set a specific output power for a recipient device.

The RSSI has an accuracy of ±2 dB (typ.) for the input signal strength in the range of -90 to -10 dBm.

4.3. Auto-advertise Function

The auto-advertise function repeatedly transfers an Advertising packet with very low power consumption (except for Extended Advertising operation) in the Backup mode.

The auto-advertise function has the following features;

- An Advertising packet is transmitted with a set interval time in the Backup mode.
- The scan request and the connection request are accepted while this function is executed.
- When the scan request is received, a preset scan response data is transmitted by the corresponding hardware.
- When the connection request is received, TC35680/TC35681 wakes up from Backup mode and return to Active mode. Then the software procedure can be executed.
- The interval time of the transmission and the transmission count of the Advertising packet can be set. After the set count of Advertising packets have been transmitted, the CPU starts up.
  - ✓ This function is convenient for the CPU to execute a low frequency procedure such as detection of the low voltage of a battery and others.

The advertisement count in the Backup mode can be set by the HCI command "HCI_M2_BTL_SET_BACKUP_AUTO_WAKEUP" or the API "SYS_API_SetDozeLAdverisingCount()". The set value is 0 to 0xFFFFFFFF. When 0 is set, the advertising continues until any other factor suspends it. The initial value is 0.

The following conditions are necessary to execute this function.

- The conditions to enter the Backup mode are met.
- Valid set of conditions to start the auto-advertise are configured and advertising starts.

4.4. Power Supply

4.4.1. VBAT and VDDIO

TC35680/TC35681 have a main power supply VBAT and an I/O power supply VDDIO. VBAT and VDDIO can be supplied with one power source or with individual power sources.

When the source of the VDDIO is different from the source of the VBAT, the voltage of the VDDIO should not exceed the voltage of the VBAT. For each range of the operation voltage, refer to Section 5.2. For the example of the connection, refer to Chapter 6.

4.4.2. Voltage Step-Down DC/DC Converter and LDO Regulator

TC35680/TC35681 integrate a DC/DC converter and multiple LDO regulators. The DC/DC converter or the LDO regulator can be selected as the power supply source in the normal operating mode (the Active mode). The selection is done at the shipment of a device. So, it cannot be done by an external control in software. A commodity product uses the DC/DC converter. The LDO regulator can be used by a customized product.

The DC/DC converter reduces the power consumption. It needs an external inductor. On the other hand, the LDO regulator needs no inductors, which reduces some discrete components and the area of the board. The power source should be selected to optimize the performance of the application system.

As a low power consumption function, the PMU switches automatically the power source between the DC/DC converter and the LDO regulator to save power efficiently. And it changes the voltage of the source at the same time to reduce more power consumption. When a user only sets a mode of a low power consumption function, the PMU controls the power source automatically to save the power. For the details of the low power consumption function, refer to Section 3.6. And, for the details of the output voltage, refer to Chapter 5.

Table 4-2 shows the output and input pins of the power supply when the DC/DC converter or the LDO regulator is used.

Table 4-2 Input and output pins of power supply

Pin name	DC/DC converter operation	LDO regulator operation
LX	Output	Hi-Z
VDDCORE1	Input	Input
VDDCORE2	Input	Output

When the output power of the RF wireless communication is 8 dBm, it is strongly recommended that a proper LC filter is connected to the VDDCORE1 and VDDCORE2 pins, respectively, to reduce the noise which affects the RF characteristics. The details of the connection of the LC filter, refer to Chapter 6 and the “Hardware Application Note”.

4.5. Reset Interface

4.5.1. Feature

The reset interface has the following features;

- Reference I/O power supply: VDDIO
- Level sensitive asynchronous reset (Low level is active.)

After the power is supplied, the external reset signal should be deasserted (RESETX pin = High) when the VBAT reaches the minimum value of the VBATopr shown in Section 5.2 and the VDDIO reaches the minimum value of the VDDIOopr. After the external reset is deasserted, the crystal resonator of the reference clock starts oscillation. The internal reset is deasserted after the time interval for the oscillation of a crystal resonator stability elapses (a built-in timer measures the interval).
The reset signal, RESETX should be asserted (Low level) for 1 μs or more.

4.5.2. Connection Example

The reset signal can be generated by an RC time constant circuit or can be supplied by the device which generates a level sensitive asynchronous reset signal. The RC time constant circuit can generate a delay signal for the start-up of the power supply.
"Reset in the User-App mode" in Figure 4-1 shows an example of this connection.
And "Reset by Host CPU" in Figure 4-1 shows an example of the connection of the device which generates a level sensitive asynchronous reset signal. When a JTAG emulator is connected, the reset pin of the host CPU is connected to the reset pin of the JTAG emulator using a wired-OR connection. The reset of this device is asserted by the low level output of either the host CPU or the JTAG emulator.

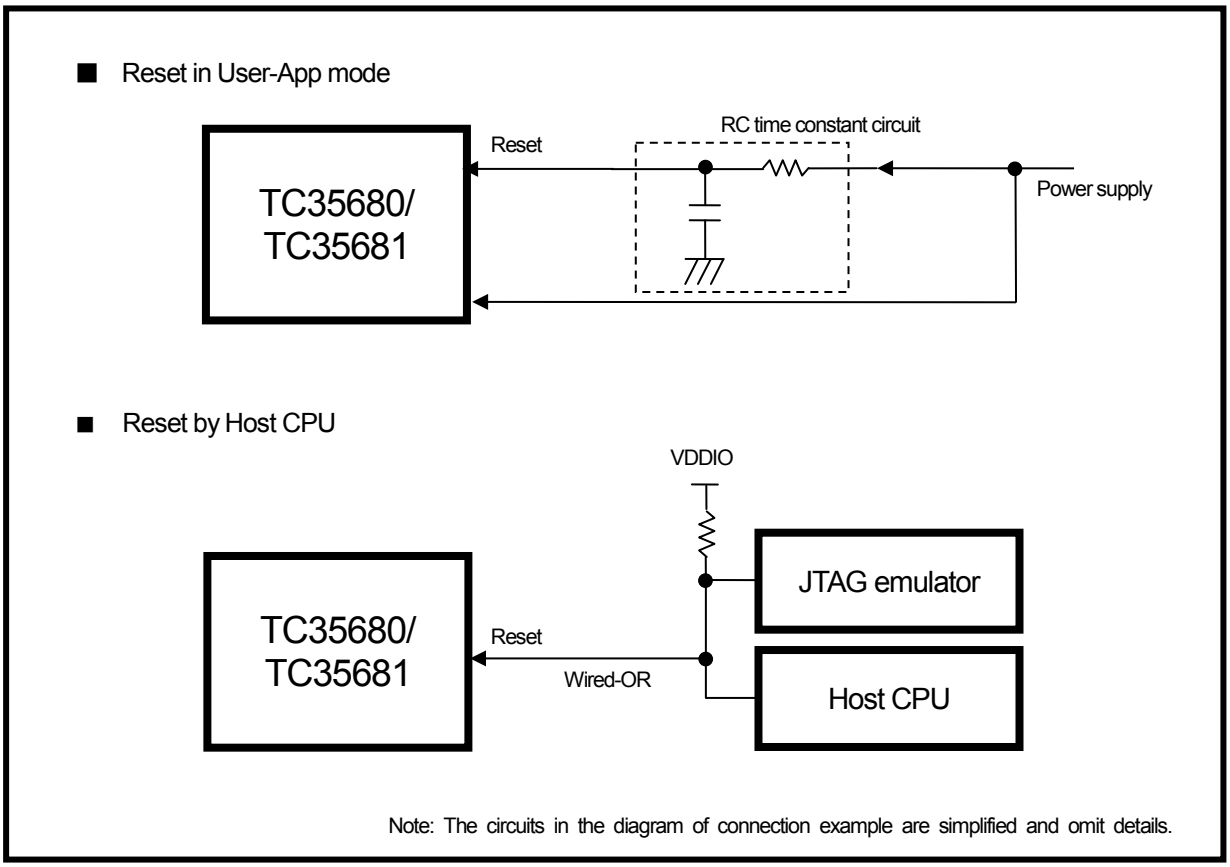


Figure 4-1 Example of Reset signal connection

4.6. General-purpose I/O (GPIO) Function

4.6.1. Feature

The GPIO pin has the following features;

- ✓ Reference I/O power supply: VDDIO
- ✓ Pin number: 18 for QFN package
- ✓ General-purpose I/O function. The ON/OFF control of input and output can be done individually.
- ✓ Reading input data and writing output data can be done for each pin or a group of several pins.
- ✓ Interrupt function is supported. The detection method can be selected from among the followings;
  - ✧ Edge detection (a rising edge, a falling edge, and both edges)
  - ✧ Level detection (High level and Low level)
- ✓ Built-in programmable pull-up and pull-down resistors.
- ✓ Output drive current can be selected (1 mA, 1.5 mA (initial), 2 mA, and 4 mA).
- ✓ Before the transition to a low power mode, each GPIO holds the status of the I/O (I/O latch function).

The diagram of the GPIO pin which supports an ADC input signal is shown in Figure 4-2.

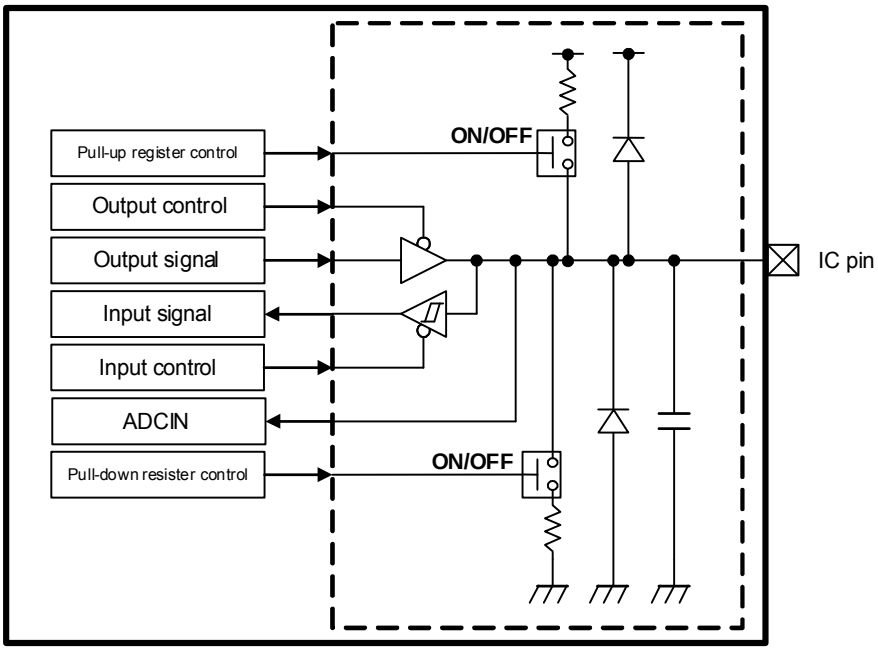


Figure 4-2 Diagram of the GPIO which supports ADC input signal

4.6.2. GPIO Pin Setting

The following settings of each GPIO pin can be done by software. And they are also held after this device enters a low power mode. The setting method of the GPIO function is shown in Table 4-3.

- ✓ Some GPIO pins have multiplexed functions. For details, refer to Section 2.4. The general-purpose I/O (GPIO) function can be assigned by setting the function 0.
- ✓ The input or output function can be assigned to a GPIO pin.
- ✓ The input of each GPIO can be enabled or disabled. When another multiplexed function is used and it is an input function, the input standby of the pin should be released because the input standby function fixes the internal input signal to Low level.
- ✓ The connection or disconnection of a built-in pull-up resistor can be selected. And the connection or disconnection of a built-in pull-down resistor can be also selected. The initial value of each pin is shown in Table 2-3. The pull-up resistor and the pull-down resistor should not be simultaneously connected to the same pin.
- ✓ The pull-up resistor and the pull-down resistor are disconnected regardless of the settings when the pin is set to an output one. When the output is disabled, the last settings are restored.
- ✓ The drive current can be selected from these options: 1 mA, 1.5 mA, 2 mA, and 4 mA.
- ✓ An external interrupt request can be accepted when the GDIO pin is set to an input one. The detection of the interrupt request can be selected from an edge detection (a rising edge, a falling edge, or both edges) and a level detection (High level or Low level) per pin. And no detection can be also selected.

Table 4-3 Setting method of GPIO

Setting	Setting method		
	HCI command	API	Register
Input or Output setting	HCI_M2_BTL_READ_MEMORY reads the data and HCI_M2_BTL_WRITE_MEMORY sets the data.	SYS_API_SetGpioEn	GPIO_OUT_EN (output setting) GPIO_OUT_EN_WRAP (output setting)
Input standby		—	PMU_IOSTANDBYX
Pull-up resistor and Pull-down resistor settings		SYS_API_SetGpioCfgReg	GPIO_CFG
Drive current setting		SYS_API_SetGpioCfgReg	GPIO_CFG
Interrupt setting		SYS_API_SetGpioCfgReg	GPIO_CFG
Input data read		—	GPIO_MON and GPIO_MON_WRAP
Output data setting		—	GPIO_OUT and GPIO_OUT_WRAP

4.6.3. General-purpose Input Function

The general-purpose input of a GPIO pin is enabled when the function 0 in Table 2-2 is assigned to the pin and the input standby is released according to the setting in Table 4-3. When the input standby is set, the general-purpose input is disabled. The internal input data is fixed to Low level. The input standby setting is held after this device enters a low power mode.

When a GPIO pin is used as a CMOS input, the fixed level of the external input signal should be High level or Low level. If the input standby is set to the pin, the pin does not work as the CMOS input. When the pin is open or when the pin is used for the ADC function, the input standby of the pin should be set.

When both the input standby and the output disable are set, the input and output of the GPIO pin are disabled (“Disable” state). When, additionally, the built-in pull-up and pull-down resistors are disconnected, the pin becomes Hi-Z.

The connection or disconnection of the built-in pull-up and pull-down resistors is set by the API or the corresponding register in Table 4-3.

The input data can be read using “Input data read” method described in Table 4-3.

4.6.4. General-purpose Output Function

The general-purpose output of a GPIO pin is enabled by the API or the corresponding register in Table 4-3 when the function 0 in Table 2-2 is assigned to the pin. The output data can be set to a GPIO pin, or to multiple pins at once, using the register described in Table 4-3. The output settings of the pin and the output data are held even after this device enters a low power mode.

4.6.5. I/O Latch Function

When TC35680/TC35681 enter a low power mode such as the Sleep mode, the Backup mode, or the Deep Sleep mode, the devices latch the setting data of the GPIO pins which are described in Section 4.6.2.

This function is also done when another multiplexed function is set to the GPIO pin.

The latch data is initialized by the hardware reset.

4.6.6. Interrupt Function

4.6.6.1. Interrupt in Active Mode

Every GPIO pin can be set to receiving an external interrupt request. The setting method and others are shown in Table 4-4.

One of the following detections of the interrupt request can be assigned to the pin.

- Edge detection of the interrupt request (a rising edge, a falling edge, or both edges)
- Level detection of the interrupt request (High level or Low level)
- Interrupt disable (No detection)

The initial setting is “Interrupt disable”.

Proper API’s can set the interrupt and get the interrupt cause. It is unnecessary to control the corresponding register directly.

TC35680/TC35681 do not detect the interrupt request during a transition to low power mode.

Table 4-4 Getting interrupt cause, clearing, and Call-back function

Item	Setting method	
	API	Register
Interrupt setting	SYS_API_SetGpioCfgReg	GPIO_CFG
Getting interrupt cause	The information of the generated GPIO interrupt is sent to the argument in the call-back function which is registered by a user. SYS_API_HwGpioIntHandlerInstall should be used.	—
Interrupt cause clear	The factor is cleared automatically by the built-in firmware.	—
Call-back function	SYS_API_HwGpioIntHandlerInstall	—

4.6.6.2. Wake-up in Sleep Mode or Backup Mode

The ANYKEY wake-up function has some known issue. The issue and their countermeasures are summarized in Known Issues which a user should refer to.

Every GPIO pin can receive a signal to wake up TC35680/TC35681 in the Sleep mode or the Backup mode (ANYKEY wake-up). The ANYKEY wake-up function is available in the User-App mode (in the HCI mode, it is disabled).
Table 4-5 shows the interrupt setting, the getting interrupt cause, the interrupt cause clear, and the API of the call-back function for ANYKEY wake-up.
The ANYKEY wake-up can be set by the HCI command or the API in Table 4-5, and one of the following detections of the interrupt request can be assigned to the pin.

- Edge detection of the interrupt request (a rising edge, a falling edge, or both edges)
- Interrupt disable (No detection)

When the external wake-up request is detected before the transition to a low power mode, the wake-up sequence begins after the transition completes.
It should be noted that the ANYKEY wake-up is detected when the ANYKEY wake-up is set in the following conditions;

- The wake-up is set within 2 clock cycles (= $1/f_{SLEEPCLK} \times 2$) after the oscillation of the sleep clock becomes stable.
- The rising edge detection is set while the external input is High to the pin.
- The falling edge detection is set while the external input is Low to the pin.

When an ANYKEY wake-up interrupt is detected, the interval of $1/f_{SLEEPCLK}$ or more is necessary to accept the next interrupt.

Table 4-5 Getting interrupt cause, clearing, and Call-back function for ANYKEY wake-up

Item	API
Interrupt setting	SYS_API_SetWakeInt()
Getting interrupt cause	SYS_API_GetWakeUpCauseValue()
Interrupt cause clear	The cause is cleared automatically by the built-in firmware.
Call-back function	SYS_API_SetCallbackPMUTimInt()

The GPIO0 or GPIO15 wake-up function described next is available in the Sleep mode, the Backup mode, and the Deep Sleep mode.

4.6.6.3. Wake-up in Deep Sleep Mode (GPIO0 and GPIO15 Wake-up)

Only the GPIO0 or GPIO15 pin can receive an external wake-up request in the Deep Sleep mode. Table 4-6 shows the interrupt setting, the getting interrupt cause, the interrupt cause clear, and the API of the call-back function for GPIO0 or GPIO15 wake-up. The wake-up function can be set to the GPIO0 or GPIO15 pin, respectively, by the API in Table 4-6, and one of the following detections of the interrupt request can be assigned to the pin.

- ✓ Level detection of the interrupt request (High level or Low level)
- ✓ Detection disable

When the external wake-up request is detected before the transition to a low power mode, the wake-up sequence begins after the transition completes.

Table 4-6 Getting interrupt cause, clearing, and Call-back function for GPIO0 or GPIO15 wake-up

Item	API
Interrupt setting	SYS_API_SetDeepSleep()
Getting interrupt cause	SYS_API_GetWakeUpCauseValue()
Interrupt cause clear	None
Call-back function	None

4.7. UART Interface

4.7.1. Feature

The UART interface has the following features;

- ✓ Reference I/O power supply: VDDIO
- ✓ Full duplex and 2-wire start-stop synchronous data transfer (Reception data and Transmission data)
- ✓ Full duplex and 4-wire start-stop synchronous data transfer (Reception data, Transmission data, Input flow control, and Output flow control)
- ✓ 2-wire start-stop synchronous data transfer or 4-wire start-stop synchronous data transfer can be selected by a setting.
- ✓ Channel number: 2 for QFN package
- ✓ Frame format:
  - ✧ Data: 8 bits (LSB first)
  - ✧ Parity: No parity, odd, and even
  - ✧ Stop bit: 1 bit and 2 bits
  - ✧ Flow control (optional): RTSX and CTSX
- ✓ Programmable setting of Baud rate
  - ✧ HCI mode and Complete mode: 9600 bps to 921.6 kbps
  - ✧ User-App mode: 600 to 2000 kbps (Maximum baudrate may be 2000 kbps or less and depends on user-application program.)
- ✓ Error detection function
  - ✧ Reception timeout error
  - ✧ Timeout setting (HCI mode: 5 ms (Initial value), Complete mode and User-App mode: 1.04 ms (when the baud rate is 115.2 kbps))
  - ✧ Reception overrun error
  - ✧ Reception framing error
- ✓ Host wake-up function

TC35680/TC35681 transfer the commands, the status, and the data to/from a host CPU through a UART interface in the HCI mode or the Complete mode.

In the mode, the built-in firmware assigns the UART1 function to the corresponding GPIOs as the host interface. (assigned as function1) For the details, refer to Section 2.4 and Section 3.4.1.

In the User-App mode, 2 channels of the UART can be used. For the GPIO pin assignment, refer to Section 2.4.

In the HCI mode, the setting of baud rate and flow control can be configured.

The UART interface operates at the VDDIO power supply voltage. Because the power supply pin is shared with other hardware interfaces, the voltage of the UART interface cannot be independently different.

The UART interface pins are shared with GPIO's general-purpose I/O pins. The function assignment can be done by software.

4.7.2. Connection Example (Host Interface in HCI Mode)

The UART interface can be connected with a UART interface on a host CPU.

Figure 4-3 shows an example of the connection with an external host CPU for the 2-wire start-stop synchronization data transfer (Reception data and Transmission data). When the HCI mode is selected, the built-in firmware assigns the UART function to the corresponding GPIO pins. Figure 4-4 shows the timing of the assignment when the UART function is assigned to the GPIO pins in the HCI mode.

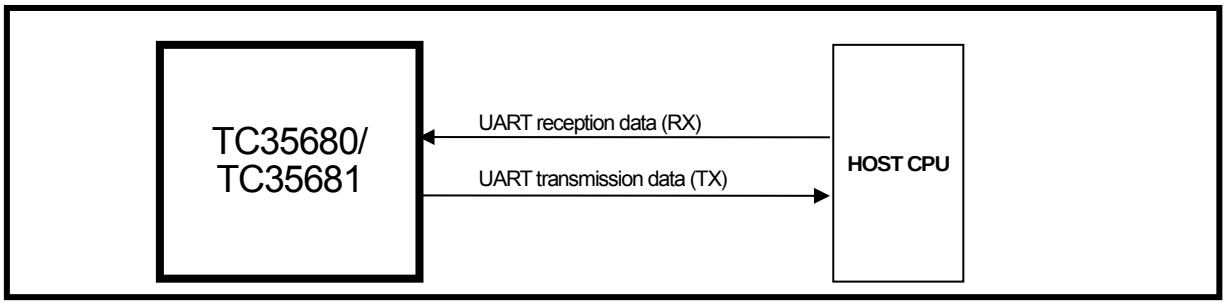


Figure 4-3 UART connection example

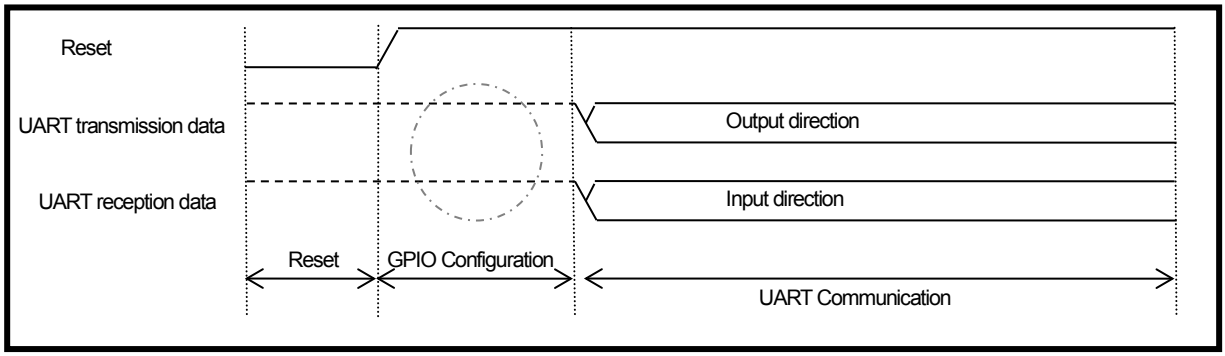


Figure 4-4 Timing of assignment of UART function

4.7.3. Frame Format

TC35680/TC35681 support the following formats;

- ✓ Data bit length: 8 bits (LSB first)
- ✓ Parity bit: No parity, odd, or even
- ✓ Stop bit length: 1 bit or 2 bits
- ✓ Flow control: RTSX and CTSX (optional)

An example of the UART data frame is shown in Figure 4-5.

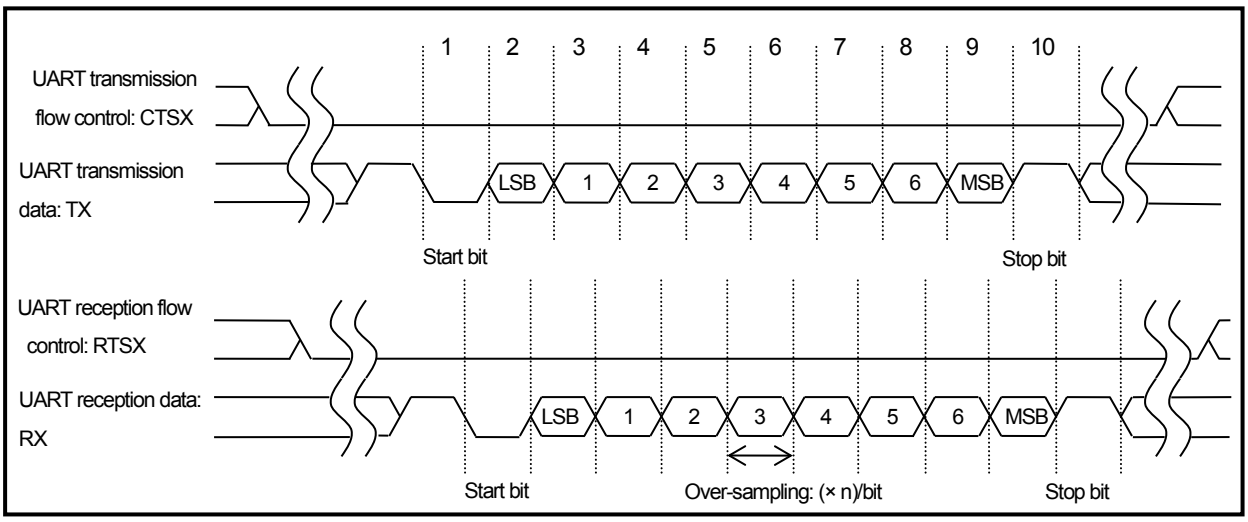


Figure 4-5 Data frame

4.7.4. Flow Control Function

The hardware flow control is available when the GPIOs of TC35680/TC35681 are assigned to the UART interface of the 4-wire. The signal directions are shown in Figure 4-6.

The flow control can be used to prevent from the overflow of the data buffers.

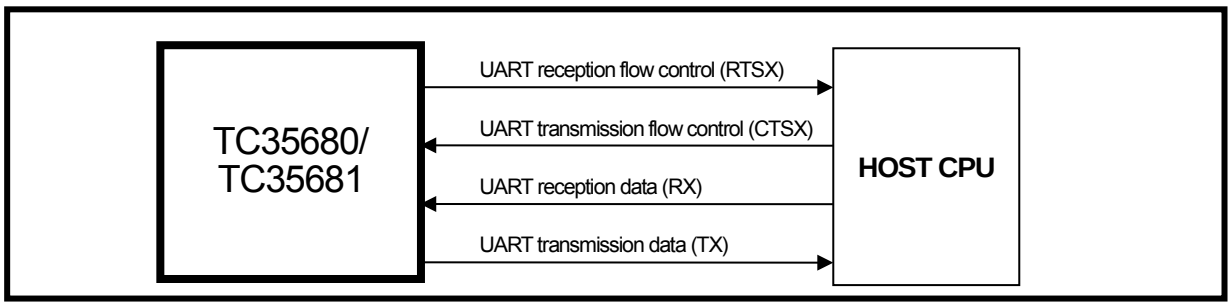


Figure 4-6 Example of UART connection

When the CTSX (Clear to Send) input signal is High, TC35680/TC35681 complete the transmission of a current frame of data and then stops. When the CTSX input is Low, the devices start to transmit data. If no transmission data is present, the transmission is not done.

When the RTSX (Request to Send) output signal is High, it requests the host CPU to stop the data transmission.

When the RTSX output is Low, the data transmission from the host CPU is permitted.

The response time of the UART data transmission and reception to the flow control signals is the interval between 1-frame time (minimum) and 4-frame time (maximum). It depends on the baud rate and the internal procedure status of the frame.

4.7.5. Baud Rate Setting

(1) Setting by an HCI command (HCI mode)

The HCI command “HCI_M2_BTL_SET_BAUDRATE” can set the baud rate. For the details, refer to the “Command Document”.

The baud rate can be set by the following command.

Extended HCI command: HCI_M2_BTL_SET_BAUDRATE

(2) Setting by API (only UART1) (User-App mode)

The baud rate of UART1 in TC35680/TC35681 can be set by the API “uart1_Set_BaudRate()”. The current baud rate can be checked by the API “uart1_Read_BaudRate()”.

For details, refer to the “Programming Guide”.

(3) Setting by a register (User-App mode)

The UART clock in TC35680/TC35681 is generated by the reference clock (32 MHz). The baud rate can be set by the UARTx_IBRD register, the UARTx_OVCR register, and the UARTx_FBRD register (x = 1 means UART1 and x = 2, UART2).

The typical values of actual and ideal baud rates in TC35680/TC35681, and the error values are shown in Table 4-7.

TC35680/TC35681 can receive the data of which baud rate error is within ±2%. The baud rate error of the host CPU should be in the range.

Table 4-7 Typical UART baud rate

Ideal baud rate [bps]	Actual baud rate [bps]	UARTx_IBRD register	UARTx_FBRD register	UARTx_OVCR register	Error [%]
600	600.01	0x115c	—	0x25	0.01
1200	1200.12	0x08ae	—	0x25	0.01
2400	2400.24	0x0457	—	0x25	0.01
4800	4801.92	0x01dc	—	0x37	0.04
7200	7207.21	0x0172	—	0x25	0.1
9600	9603.84	0x00ee	—	0x37	0.0400
14400	14414.41	0x00b9	—	0x25	0.1001
19200	19207.68	0x0077	—	0x37	0.0400
28800	28828.83	0x004a	—	0x48	0.1001
38400	38415.37	0x0031	—	0x5a	0.0400
57600	57657.66	0x0025	—	0x48	0.1001
76800	76923.08	0x0020	—	0x36	0.1603
115200	115211.52	0x0011	0x17	0x49	0.0100
153600	153615.36	0x0011	0x17	0x25	0.0100
230400	230319.39	0x000b	0x25	0x25	-0.0350
307200	306954.44	0x0008	0x2c	0x25	-0.0799
460800	460638.78	0x0005	0x16	0x36	-0.0350
921600	920863.31	0x0002	0x0b	0x49	-0.0799
1843200	1845045.05	0x0001	0x0a	0x48	0.1001
2000000	2000000	0x0001	—	0x49	0.0000

Note: x = 1 means UART1 and x = 2 means UART2

4.7.6. UART Message Recognition Function (Spacing between Messages)

In order to recognize the boundary of a UART message, a message time space is inserted between the messages transferred through the UART interface of TC35680/TC35681 in the Complete mode. In the message time space, no data is transferred on the UART interface. One message consists of one or more frames which exist between two message spaces.

In the HCI mode, the data transfer can be done without the massage time space. But the maximum number of the continuous HCI command is limited to 8.

The message configured by the frames and the boundary of the message are illustrated in Figure 4-7 (Transmission frame) and Figure 4-8 (Reception frame). If the space of the neighboring frames is less than 12-frame length (an initial setting), the transmission data or the reception data is processed as one message. If the space length is 12-frame length or more, the data is processed as two messages.

The host CPU can recognize the message boundary by measuring the length of the message time space. For example, when the baudrate is 115.2 kbps, the message time space of the neighboring frames should be (0.087 ms × 12) = 1.04 ms or more (0.087 ms is one frame time length).

TC35680/TC35681 measure the time space of the neighboring frames using an internal timer to recognize the boundary. TC35680/TC35681 notify of the reception timeout error when the devices detect a message space time in a message. The default time of the reception timeout is 12-frame length (1.04ms at 115.2-kbps baud rate) in the User-App mode. This time can be changed

For the reception timeout error, refer to Section 4.7.7.

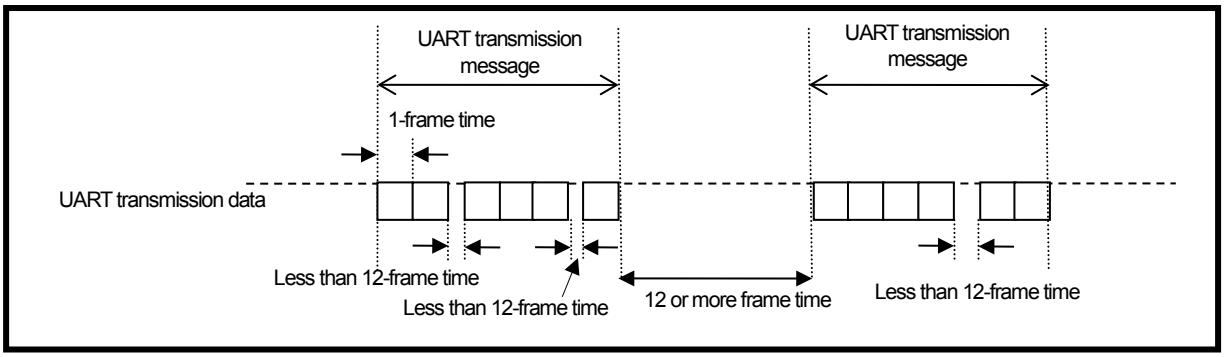


Figure 4-7 Transmission frame and Transmission message

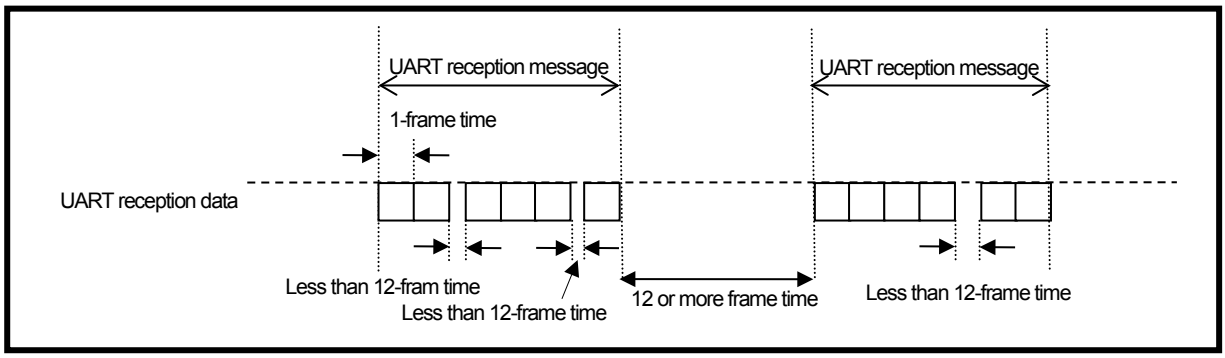


Figure 4-8 Reception frame and Reception message

4.7.7. Error Detection Function

The UART interface in TC35680/TC35681 can detect 3 following errors;

- ✓ Reception timeout error
- ✓ Reception overrun error
- ✓ Reception framing error

4.7.7.1. Reception Timeout Error

The availability of the timeout setting depends on an operating mode and a setting target interface. Table 4-8 shows the availability of the timeout setting.

When the reception timeout is enabled, no data reception notifies the timeout error. The setting can be disabled.

Table 4-8 Availability of the timeout setting and the initial value

Operating mode	HCI mode	Complete mode	User-App mode	
Setting method	HCI command	HCI command	API	Register
Setting target	Only UART1	Only UART1	Only UART1 (Note 2)	UART1 and UART2
Initial timeout setting	Disabled.	Enabled	Disabled	Disabled
Initial timeout value	5 ms (Note 1)	1.04 ms	User setting value	Initial vale of register
Reception	Configurable	Configurable	Configurable	Configurable

Note 1: The error occurs when the value exceeds 5 ms.

Note 2: Only UART1 can be set by the API in the User-App mode. When UART2 is used, the setting should be done by the register.

4.7.7.2. Reception Overrun Error

The reception overrun error occurs when the UART reception frame buffer in TC35680/TC35681 overflows. Normally, this overflow error does not occur when the flow control described in Section 4.7.4 is used for data transfer.

4.7.7.3. Reception Framing Error

The reception framing error occurs when “0” is detected at the stop bit.

4.7.8. Host Wake-up Function

TC35680/TC35681 can issue the signal to wake up the host CPU before they transmit a message through the UART interface. This host wake-up function is disabled by default, but it can be assigned to a GPIO pin which is selected by a HCI command or API.

The host wake-up time can be changed by a HCI command, API or register (the default is 10 ms).

This function is available in the Complete mode.

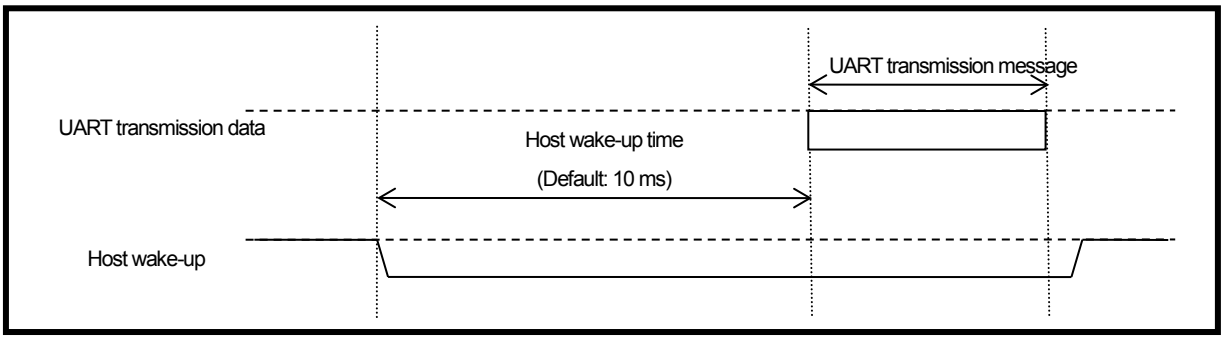


Figure 4-9 Host wake-up

4.8. SPI Interface

4.8.1. Feature

The serial peripheral interface has the following features;

- ✓ Reference I/O power supply: VDDIO
- ✓ Channel number: 2 for QFN package
- ✓ SPI function
  - ✧ Chip select: 2 channels for QFN package
  - ✧ Chip select polarity: High active or Low active can be selected.
  - ✧ Serial clock of Master: The clock polarity and the phase can be adjusted (selectable from among 4 combinations)
  - ✧ Serial clock frequency: 8 kHz to 16 MHz
  - ✧ Serial data transfer: Both MSB first and LSB first are available.

The SPI interface operates at the VDDIO power supply voltage. Because the power supply pin is shared with other hardware interfaces, the voltage of the SPI interface cannot be independently different.

4.8.2. Connection Example

The SPI interface can be connected to a serial EEPROM and a serial Flash memory.

The SPI interface has one chip select pin. Figure 4-10 shows an example of the connection with a serial Flash ROM through the SPI interface of TC35680/TC35681.

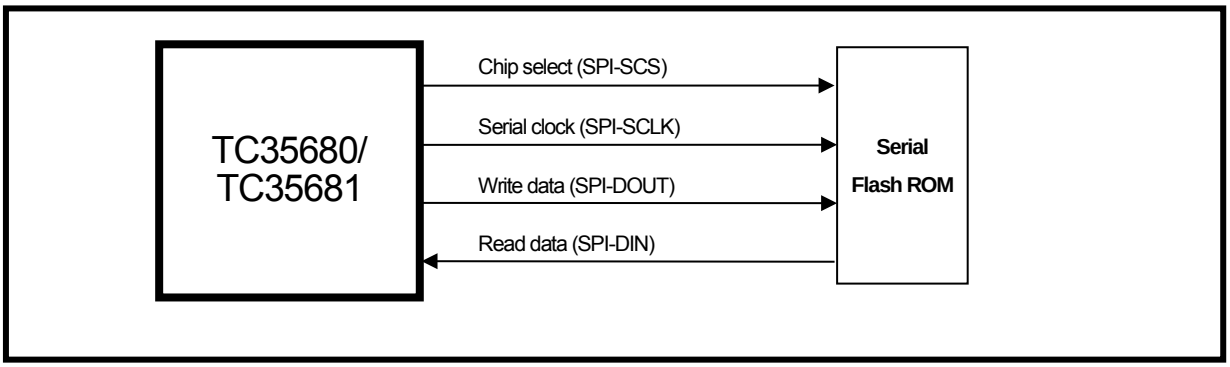


Figure 4-10 Connection example of SPI interface to Serial Flash ROM

4.8.3. Frame Format

When the SPI interface is connected to an external device, the first 8 bits (X7 to X0) specify an address and the mode of read or write. The type of the command recognition code and the bit width of the address should match those of the external device. For the details of the format, refer to a technical document of the external device.

Figure 4-11 shows an example where an 8-bit address is written and then its 8-bit data is read.

Figure 4-12 shows an example where an 8-bit address is written and then its 8-bit data is written.

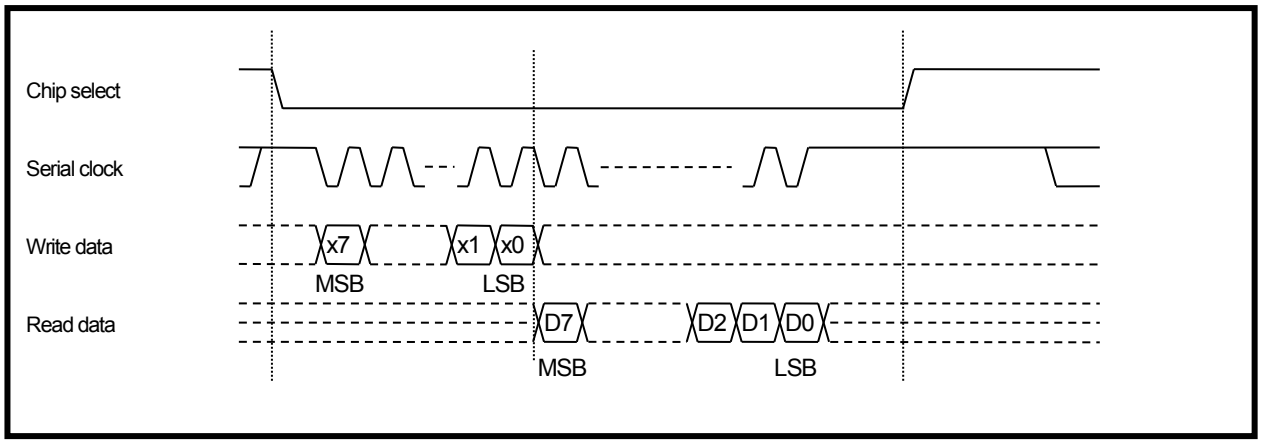


Figure 4-11 SPI format (Single Byte read)

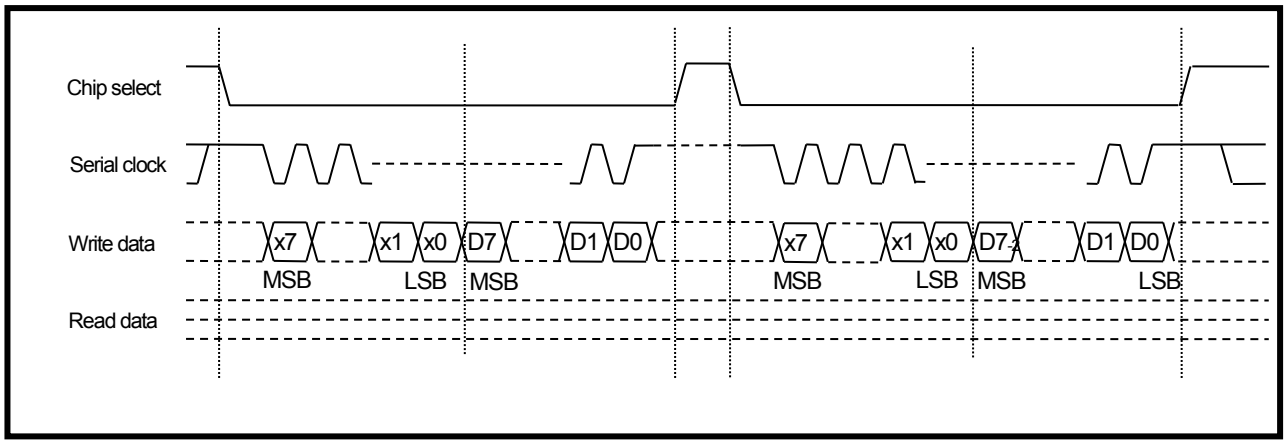


Figure 4-12 SPI format (Single Byte write)

4.8.4. SPI Clock

The SPI clock can be set by the SPI timing control register (SPI_TIMINGCONTROL).

The SPI clock frequency can be set by 1-bit "div" field, 2-bit "PRS" field, and 8-bit "BASE" filed in the SPI_TIMINGCONTROL register.

Table 4-9 shows the equation to calculate the SPI clock frequency.

Table 4-9 Equation to calculate SPI clock frequency

div field	PRS field	BASE field	SPI clock frequency [MHz]
0 (Initial value)	00 (Initial value) and 01	1 to 255 (0: Setting is prohibited.) 1: (Initial value)	Reference clock frequency ÷ (2^{PRS} × BASE × 2)
	02 and 03		Reference clock frequency ÷ {(2^{PRS} × BASE × 2) + 2}
1	00 to 03		Reference clock frequency ÷ (2^{PRS} × BASE × 2)

Table 4-10 and Table 4-11 show the typical frequency for the SPI clock at 32 MHz of the reference clock frequency.

Table 4-10 SPI clock frequency (MHz) at div = 0

BASE	PRS			
	0	1	2	3
1	16.000	8.000	3.200	1.778
2	8.000	4.000	1.778	0.941
3	5.333	2.667	1.231	0.640
4	4.000	2.000	0.941	0.485
5	3.200	1.600	0.762	0.390
6	2.667	1.333	0.640	0.327
7	2.286	1.143	0.552	0.281
8	2.000	1.000	0.485	0.246
9	1.778	0.889	0.432	0.219
10	1.600	0.800	0.390	0.198
16	1.000	0.500	0.246	0.124
32	0.500	0.250	0.124	0.062
64	0.250	0.125	0.062	0.031
128	0.125	0.063	0.031	0.016
255	0.063	0.031	0.016	0.008

Table 4-11 SPI clock frequency (MHz) at div = 1

BASE	PRS			
	0	1	2	3
1	16.000	8.000	4.000	2.000
2	8.000	4.000	2.000	1.000
3	5.333	2.667	1.333	0.667
4	4.000	2.000	1.000	0.500
5	3.200	1.600	0.800	0.400
6	2.667	1.333	0.667	0.333
7	2.286	1.143	0.571	0.286
8	2.000	1.000	0.500	0.250
9	1.778	0.889	0.444	0.222
10	1.600	0.800	0.400	0.200
16	1.000	0.500	0.250	0.125
32	0.500	0.250	0.125	0.063
64	0.250	0.125	0.063	0.031
128	0.125	0.063	0.031	0.016
255	0.063	0.031	0.016	0.008

4.9. I²C Interface

4.9.1. Feature

The I²C interface has the following features;

- ✓ Reference I/O power supply: VDDIO
- ✓ Channel number: 2 for QFN package
- ✓ I²C bus interface
  - ✧ I²C bus master operation and slave operation (not support the multi master operation)
  - ✧ Cross stretch is supported.
  - ✧ Serial clock frequency: Standard mode (Max. 100 kHz) and Fast mode (Max. 400 kHz)
  - ✧ Serial clock output mode: Open-drain output or CMOS output can be selected.
  - ✧ Device address format: 7-bit address (10-bit address is not supported.)

The I²C interface operates at the VDDIO power supply voltage. Because the power supply pin is shared with other hardware interfaces, the voltage of the I²C interface cannot be independently different.

When TC35681 is used in the User-App mode, Channel 1 is occupied as an interface to the memory which stores a user application program. For the details, refer to Section 3.4.3.

4.9.2. Connection Example

Figure 4-13 and Figure 4-14 show examples of the connections with serial EEPROM's through the I²C interfaces. When two or more EEPROM's are connected, the least three bits of the slave address should be different to identify each EEPROM.

When the I²C interface is used in the open-drain output mode, external resistors (Rext) should be connected to the serial clock line and the data line, as shown in Figure 4-13.

On the other hand, when the I²C interface is used in the CMOS output mode, the pull-up resistor for the clock line is not necessary because the TC35680/TC35681 always drive the clock line to High level or Low level. But the pull-up resistor (Rext) for the data line should be connected.

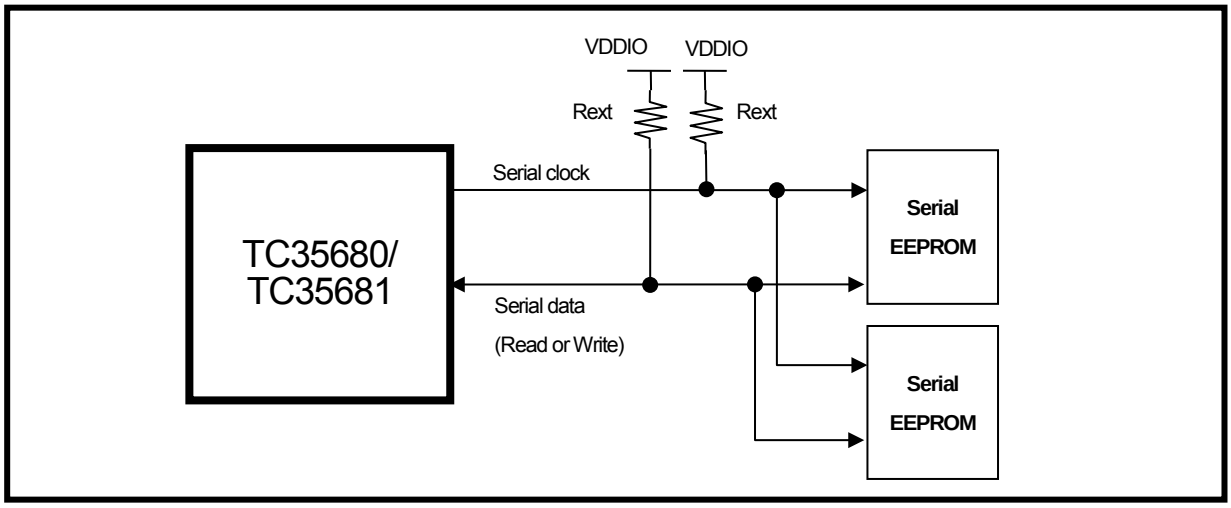


Figure 4-13 Example of the connection with serial EEPROM's through I²C interface (open-drain output mode)

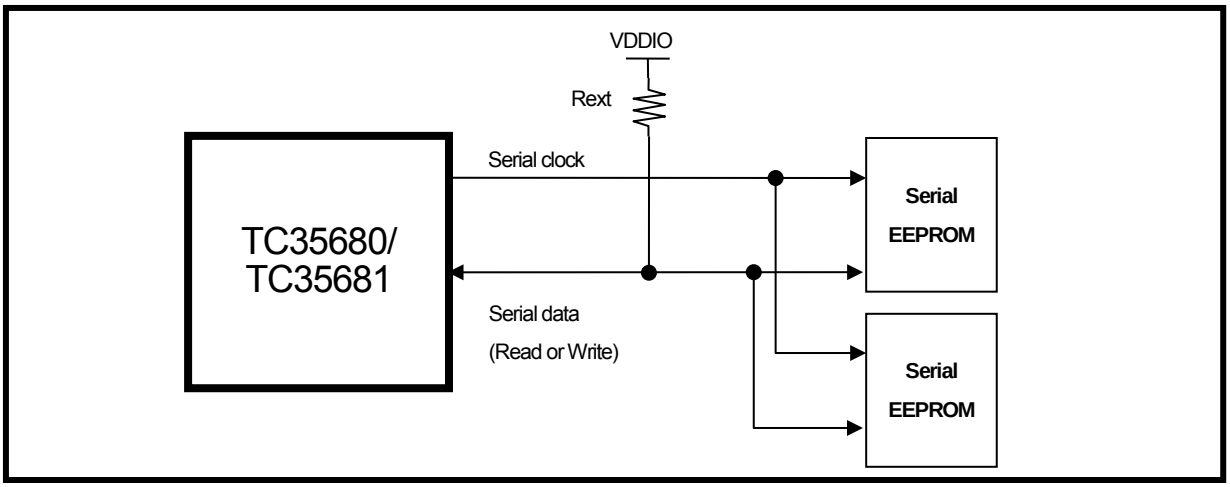


Figure 4-14 Example of the connection with serial EEPROM's through I²C interface (CMOS output mode)

4.9.3. Value of External Pull-up Resistor

A suitable value of the external pull-up resistor for the I²C interface should be determined to execute a correct operation.

The maximum value (Rext_max) is defined by the equation (1), in which "tr" is the rising time of the serial clock and the serial data signals specified in the I²C bus standard, and "Cb" is the I²C bus capacity.

On the other hand, the minimum value (Rext_min) is defined by the equation (2), in which "VDDIO", "Vol_max", and "Iol" are the supply voltage, the maximum value of the low level output voltage, and the low level output current, respectively. The pull-up resistor value should be a value between the minimum and the maximum ones.

$$\text{Rext\_max} = \frac{\text{tr}}{0.8473 \times \text{Cb}} \quad (1)$$

$$\text{Rext\_min} = \frac{\text{VDDIO} - \text{Vol\_max}}{\text{Iol}} \quad (2)$$

The TC35680/TC35681 support the I²C bus standard mode (the maximum frequency of 100 kHz) and I²C bus fast mode (the maximum frequency of 400 kHz). The rising time tr should be 1000 ns or less for the standard mode and 300 ns or less for the fast mode. The Cb value varies depending on the PCB design and implementation. Table 4-12 and Table 4-13 show the Rext_max and Rext_min values for the Cb of 20 pF.

Table 4-12 External Pull-up resistor value in I²C standard mode (I²C bus capacitance: 20 pF)

I²C bus frequency	Max. 100 kHz								
tr [ns]	1000								
Cb [pF]	20								
VDDIO [V]	1.8			3.0			3.6		
Vol_max [V]	0.3			0.4			0.4		
Iol [mA]	1	2	4	1	2	4	1	2	4
Rext_min [kΩ]	1.50	0.75	0.38	2.60	1.30	0.65	3.20	1.60	0.80
Rext_max [kΩ]	59.01								

Table 4-13 External Pull-up resistor value in I²C fast mode (I²C bus capacitance: 20 pF)

I²C bus frequency	Max. 400 kHz								
tr [ns]	300								
Cb [pF]	20								
VDDIO [V]	1.8			3.0			3.6		
Vol_max [V]	0.3			0.4			0.4		
Iol [mA]	1	2	4	1	2	4	1	2	4
Rext_min [kΩ]	1.50	0.75	0.38	2.60	1.30	0.65	3.20	1.60	0.80
Rext_max [kΩ]	17.70								

4.9.4. Transfer Format

In the I²C format, every data is sent as MSB first.

And, every device which is connected to bus has a unique device recognition address (slave address). It has been determined in accordance with the specifications of the connected device.

A master device sends the START condition, a slave address, and R/$\overline{W}$ bit first. Next, the slave device which has the slave address sent by a master device returns a reception acknowledge bit (ACK: Acknowledge bit). When the master device received ACK, it begins to transfer data depend on the transmitted R/$\overline{W}$ bit.

During transferring data, the device which receives data returns an ACK or a reception Not Acknowledge bit (NACK: Not Acknowledge bit) every time it receives one Byte data.

When the device which transmits data received an ACK, it transmits the next data. And when it received a NACK, it stops to transmit the next data and releases SDA to Hi-Z.

When all data are transferred, the master device generates the STOP condition in order to complete the transfer of I²C.

Figure 4-15 shows an example of the format when TC35680/TC35681 read two-Byte data with the serial memory. And Figure 4-16 shows an example of the format when TC35680/TC35681 write two-Byte data.

The gray texts and lines in these figures indicate that the signals are output by the serial memory.

For the read operation, after sending a slave address, TC35680/TC35681 send the First Byte address ([B7:B0]) of the reading data. After this, TC35680/TC35681 generate re-START condition in order to change the transfer direction from a transmission to a reception, they read data from the serial memory. TC35680/TC35681 return NACK to the serial memory after receiving 2nd data. And they generate the STOP condition. The read operation of I²C is completed.

For the write operation, after sending a slave address, TC35680/TC35681 send the First Byte address ([B7:B0]) of the writing data. After this, they transmit the data to serial memory. TC35680/TC35681 receive an ACK from the serial memory and generate the STOP condition. The write operation of I²C is completed.

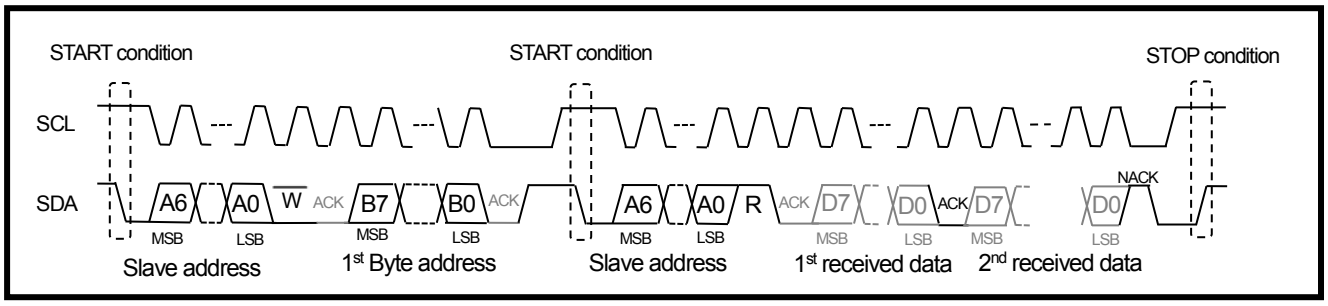


Figure 4-15 I²C transfer format (read 2-byte data from serial memory)

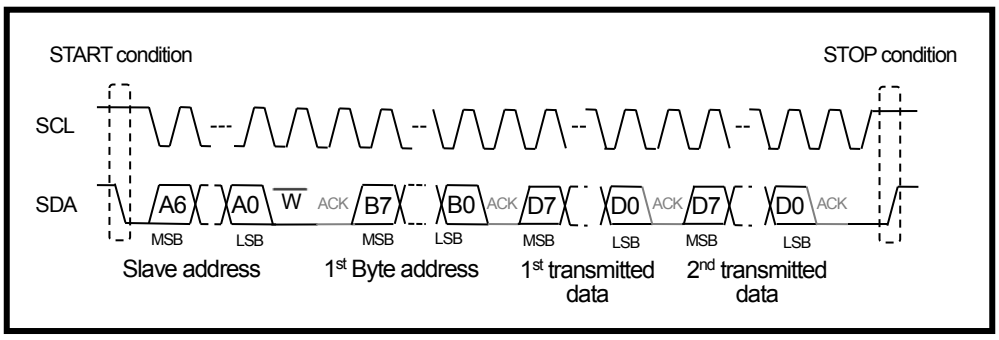


Figure 4-16 I²C transfer format (write 2-byte data to serial memory write)

4.10. PWM Interface

4.10.1. Feature

The PWM interface has the following features;

- ✓ Reference I/O power supply: VDDIO
- ✓ Pulse generation function
- ✓ Channel number: 4 for QFN package
- ✓ The clock source to generate pulses can be selected between a 16-MHz clock (2-division of the reference clock) and a 32.768-kHz clock.
- ✓ The following output frequencies can be selected using a clock divider.
  - ✧ 8 Hz to 16.384 kHz (the 32.768-kHz clock is used. 12-bit divider: the maximum division is 1/4096.)
  - ✧ 0.954 Hz to 8 MHz (the 16-MHz clock is used. 12-bit × 2 divider: the maximum division is 1/16777216)
- ✓ A pulse output can be masked with a 50-ms unit width (as example) by a regular pattern signal whose period is one second (Rhythm function).
- ✓ An interrupt can be generated every 1 second of the rhythm pattern period.
- ✓ The pulse can be reversed.
- ✓ The duty ratio of the pulse output can be adjusted.
- ✓ Each PWM output can be synchronized by the pulse output synchronization function.

TC35680/TC35681 have a PWM interface that can be used for the LED control, the buzzer control, and others.
The PWM interface operates at the VDDIO power supply voltage. Because the power supply pin is shared with other hardware interfaces, the voltage of the PWM interface cannot be independently different.

4.10.2. Pulse Generation Function

Figure 4-17 shows a PWM pulse waveform.
The frequency of the pulse signal is adjusted by changing the cycle time. The ON/OFF ratio can be adjusted by changing the duty ratio.
The frequency can be set to the value from 8 Hz to 16.384 kHz (in use of the 32.768-kHz clock), and from 0.954 Hz to 8 MHz (in use of the 16-MHz clock).
The duty ratio can be set to the value from 0 % to 100 %.

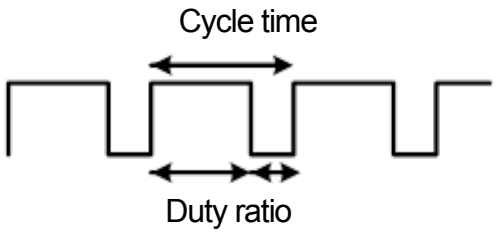
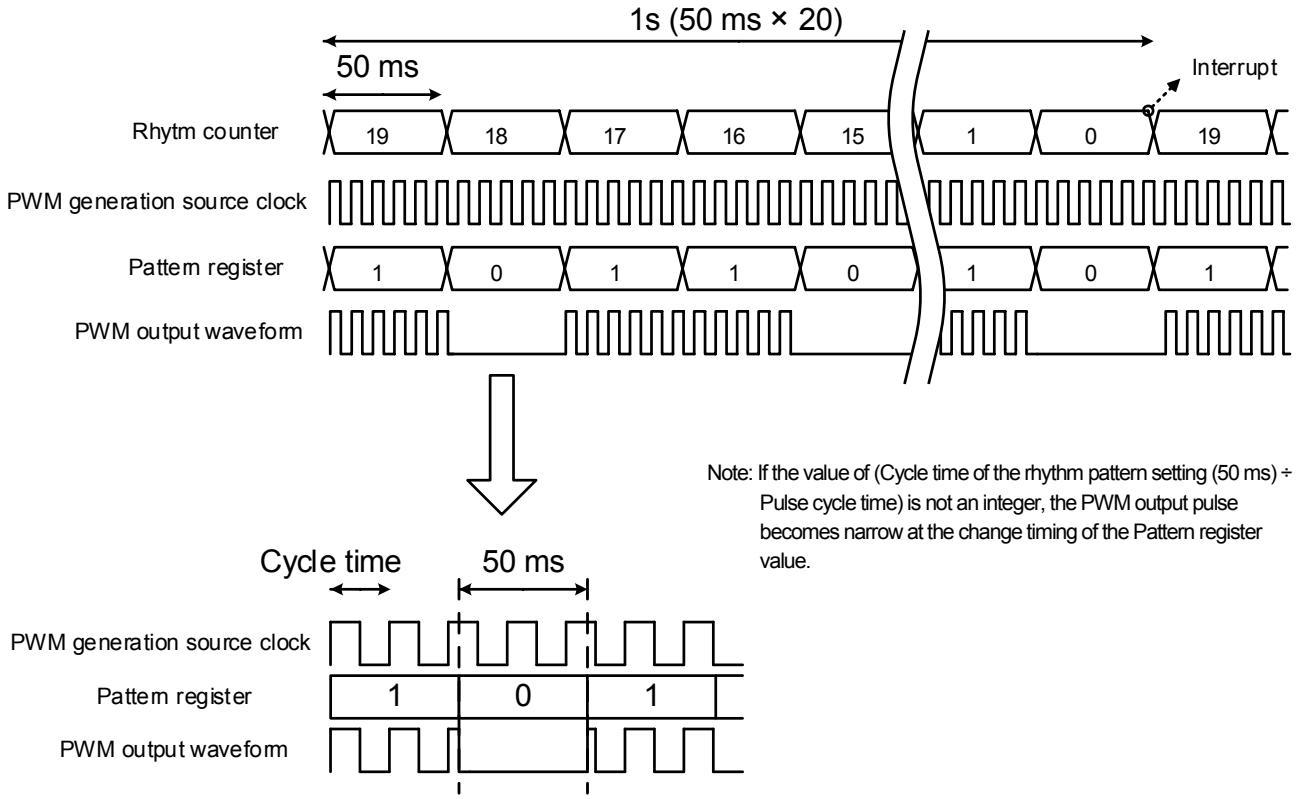


Figure 4-17 PWM pulse waveform

4.10.3. Rhythm Function (Output Masking)

Figure 4-18 illustrates the outlines of the PWM rhythm function. TC35680/TC35681 integrate a rhythm counter whose clock source cycle is 50 ms (as example). The counter is independent of the pulse generation function. A 20-bit register (Pattern register) is also built in, and each bit of the register corresponds to the content of the rhythm counter which counts down every 50 ms. When a bit of the Pattern register is 0, the corresponding PWM output is masked and fixed to 0 or 1. This function can generate a 1-scond periodic waveform which is implemented to blink a LED or to sound a buzzer.



Note: If the value of (Cycle time of the rhythm pattern setting (50 ms) ÷ Pulse cycle time) is not an integer, the PWM output pulse becomes narrow at the change timing of the Pattern register value.

Figure 4-18 Output masking by PWM rhythm function

4.11. ADC (AD Converter)

4.11.1. Feature

The TC35680/TC35681 integrates a 10/12-bit AD converter (ADC) that can be used for power supply voltage measurement and measurement of General-purpose voltage such as an input voltage from an external sensor.

The ADC has the following features;

- ✓ Reference I/O power supply: VDDIO
- ✓ General-purpose voltage input pin count (shared with GPIO pins): 5 for QFN package
- ✓ Power supply voltage measurement: 1 channel (ADC0) This pin is connect to VDDCORE2 (1.2-V voltage supply) internally.
- ✓ Maximum sampling rate: 1 MS/s (But the function which coverts an analog signal continuously is not supported)
- ✓ 10-bit conversion or 12-bit conversion can be selected (default is 10 bits).

For the general-purpose voltage input, the channels except channel 0 which is connected to VDDCORE2 can be used.

These channels are shared with the GPIO pins. When the ADC function is assigned to one of the GPIO pins, the corresponding pin should be set to input standby and the pull-up and pull-down resistors should be disconnected. For the details of the GPIO pins, refer to Section 2.4. And for the setting method of the pin, refer to Section 4.6.2.

The ADC function is set by the GPADCC_CTRL register. One of the channels is selected by the GPADCC_SELAIN register to convert the analog signal input from the channel. The result data can be read from the GPADCC_DATA register. The 10-bit conversion result is set to 11-bit to 2-bit in GPADCC_DATA register when the data length of the conversion result is specified as 10 bits. And the 12-bit conversion result is set to 11-bit to 0-bit in GPADCC_DATA register when the data length of the conversion result is specified as 12 bits.

All channel data cannot be read out at the same time. The conversion end can be detected using a corresponding interrupt or the polling method. The maximum sampling rate depends on the CPU utilization.

The pin of AD convertor for the measurement of General-purpose voltage should not be input the signal whose voltage is higher than the voltage of the VDDIO.

4.11.2. Function

An analog signal in the range of 0 to VDDIO (V) can be input into an analog input channel of the general-purpose voltage measurement. The reference voltage (VREFH) of the ADC is connected to VBAT internally, so the result of AD conversion is shown as a relative value against the VBAT voltage as in the following equation.

$$\text{Result of AD conversion} = 4095 \times \frac{\text{Input voltage to a channel of ADC}}{\text{VREFH}(= \text{VBAT voltage})}$$

ADC0 for the power supply voltage measurement is connected to VDDCORE2 (1.2-V voltage supply) internally. The VBAT voltage is shown by the channel 0's result of AD conversion.

$$\text{VBAT} = 4095 \times \frac{1.2\ \text{V}}{\text{Result of AD conversion of channel 0}}$$

The absolute voltage of the analog input signal for the general-purpose voltage measurement is calculated using the following equation.

$$\text{ADCn input voltage [V]} = \frac{\text{Result of AD conversion of channel n}}{\text{Result of AD conversion of channel 0}} \times 1.2\ \text{[V]}$$

The concept of the voltage conversion is shown in Figure 4-19.

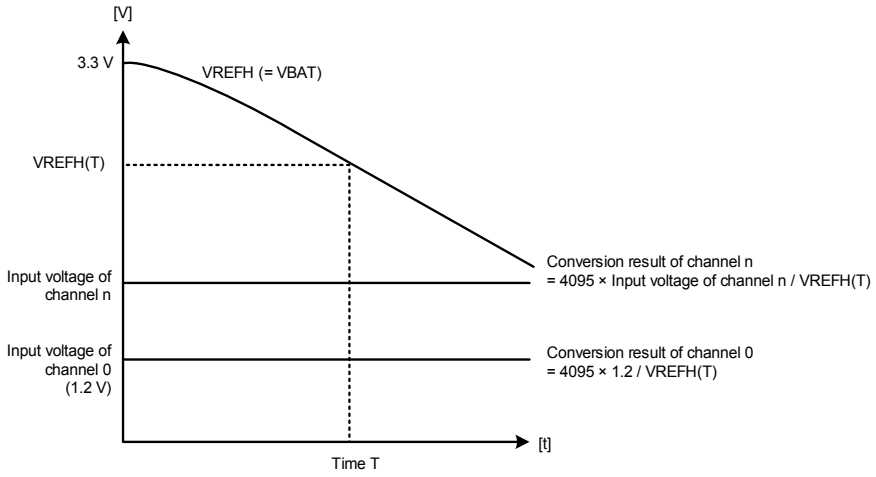


Figure 4-19 Conceptual diagram of the voltage conversion

4.12. Reference Clock Interface

4.12.1. Feature

The reference clock interface has the following features;

- ✓ Reference clock frequency: 32 MHz
- ✓ Clock frequency accuracy: ±50 ppm or less is necessary. (in operating environment)
- ✓ Built-in 128-step variable capacitor (1.24 to 20.4 pF)
- ✓ Load capacitance and equivalent series resistance of the crystal resonator
  - ✧ Load capacitance: 6 pF
  - ✧ Equal series resistance: 50 Ω (recommended)

An external feedback resistor and external capacitors are unnecessary for the crystal oscillation circuit in TC35680/TC35681, because the devices integrate the feedback resistor and a variable capacitor (1.24 to 20.4 pF) on the input and output pins of the crystal resonator. A crystal resonator which has a load capacitance of 6 pF should be connected between the XOIN and XOOUT pins, and the capacitance of the variable capacitor should be adjusted so that the frequency deviation does not exceed ±50 ppm under the use environment.

The recommended equivalent series resistance of the crystal resonator is 50 Ω. The oscillation margin should be evaluated sufficiently when a crystal resonator with a larger equivalent series resistance is used. And the interval time for the oscillation stability should be 1.5 ms or less.

4.12.2. Adjustment of Oscillation Frequency of Reference Clock

The adjustment of the oscillation frequency is done by the modification of the capacitance of the variable capacitor. It is done by the setting of the 7-bit XO_FREQ_TUNE field in the PMU_XOSC_TRIMIN register. When a value between 0x00 and 0x7F (2's complement) is set, the capacitance of the variable capacitors on the input and output pins changes with a step of approximately 0.15 pF. Then, the value 0x40 gives the minimum frequency and 0x3F, the maximum frequency.

The value of XO_FREQ_TUNE is 0x00 just after the hardware reset is deasserted or while the cold boot is done. It is set to 0x1A by the built-in firmware after the oscillation becomes stable. Then the value can be modified by a software procedure.

For the details of the adjustment of the variable capacitor, refer to the "Hardware Application Note".

4.12.3. Low Power Mode and Adjustment Value

The oscillation stops in a low power mode. When the wake-up is done in the Sleep mode or the Backup mode, the oscillation start is controlled by the value in the XO_FREQ_TUNE field which is set before the transition to the low power mode. So the value is different from the value in the XO_FREQ_TUNE field in the cold boot procedure. Then the interval time for oscillation stability is also different. The time should not exceed 1.5 ms.

Table 4-14 shows the oscillation condition and the value in the XO_FREQ_TUNE field.

Table 4-14 Oscillation condition of the reference clock and XO_FREQ_TUNE value

Oscillation condition	Value in XO_FREQ_TUNE
Just after hardware reset is deasserted or wake-up from the Deep Sleep mode.	0x00 (the initial value at start-up) 0x1A (the initial value after the oscillation becomes stable)
Wake-up from the Sleep or Backup mode	User setting value (Initial value is 0x1A)

4.12.4. Connection of Crystal Resonator

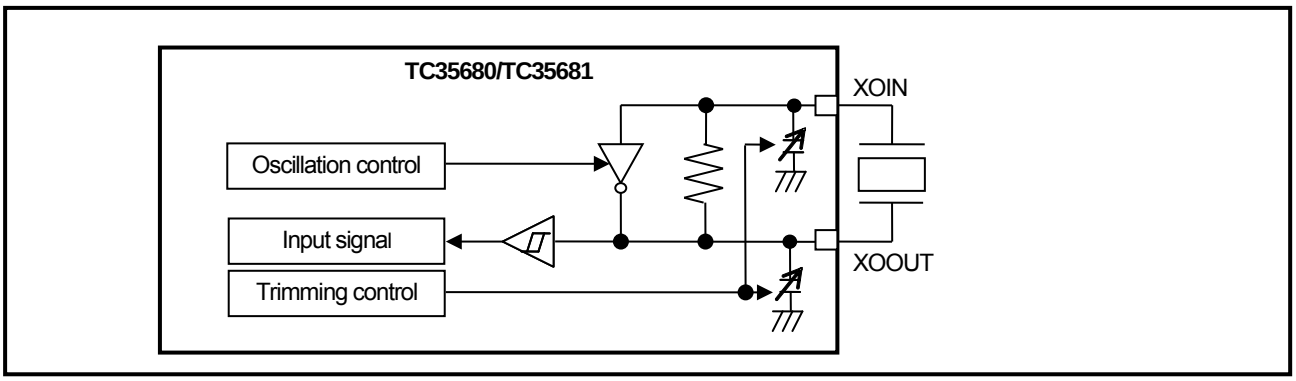


Figure 4-20 Connection of a crystal resonator

4.13. Sleep Clock Interface

4.13.1. Feature

The sleep clock interface has the following features;

- ✓ Selection source clock of sleep clock from among the following three clocks
  - ✧ Crystal resonator
  - ✧ External oscillator
  - ✧ Built-in silicon oscillator (SiOSC)
- ✓ Frequency: 32.768 kHz
- ✓ Frequency accuracy: ±500 ppm or less (in operating environment)
- ✓ Built-in 32-step variable capacitor (0 to 15.56 pF)
- ✓ Load capacitance and equivalent series resistance of the crystal resonator
  - ✧ Load capacitance: 4 pF
  - ✧ Equivalent series resistance: 80 kΩ (recommended)

The SiOSC oscillates at start-up. After the start-up, the clock source can be changed to the crystal resonator or an external oscillator. The jitter of the oscillation of the SiOSC is too large to comply with the **Bluetooth®** specification. So it is necessary that the clock source is changed to the crystal resonator or an external oscillator for the **Bluetooth®** communication.

4.13.2. Selection of Sleep Clock Source

The sleep clock source of TC35680/TC35681 can be selected from among the three clocks. The command and the API to change the source are shown in Table 4-15.

After start-up, the selection of the sleep clock source is done only once.

Table 4-15 Command and API to change a clock source

Operating mode	Command and API
HCI mode	HCI_M2_BTL_SET_LOW_POWER_CLOCK
User-App mode	SYS_API_SetBlesglSleepClock

4.13.3. Use of Crystal Resonator

An external feedback resistor and external capacitors are unnecessary for the crystal oscillation circuit in TC35680/TC35681, because the devices integrate the feedback resistor and a variable capacitor (0 to 15.56 pF) on the input and output pins of the crystal resonator. A crystal resonator which has a load capacitance of 4 pF should be connected between the SLPXOIN and SLPXOOUT pins, and the capacitance of the variable capacitor should be adjusted so that the frequency deviation does not exceed ±500 ppm under the use environment.

The recommended equivalent series resistance of the crystal resonator is 80 kΩ. The oscillation margin should be evaluated sufficiently when a crystal resonator with a larger equivalent series resistance is used.

For the details of the adjustment of the variable capacitor, refer to the “Hardware Application Note”.

4.13.4. Adjustment of Oscillation Frequency of Sleep Clock

The adjustment of the oscillation frequency is done by the modification of the capacitance of the variable capacitor. It is done by the setting of the 5-bit FREQTUNE_OSC32K field in the PMU_OSC32K_TRIMIN register. When a value between 0x00 and 0x1F (2's complement) is set, the capacitance of the variable capacitors on the input and output pins changes with a step of about 0.5 pF. Then, the value 0x0F gives the minimum frequency and 0x10, the maximum frequency.

The value in the FREQTUNE_OSC32K field is 0x00 just after the reset is deasserted or while the cold boot is done. It is set to 0x18 after the oscillation becomes stable. Then the value can be modified by a software procedure.

The oscillation of the sleep clock stops at the transition to the Deep Sleep mode.

Table 4-16 Oscillation condition of Sleep clock and FREQTUNE_OSC32K field value

Oscillation condition	Value in FREQTUNE_OSC32K field
J Just after hardware reset is deasserted or wake-up from the Deep Sleep mode.	0x00 (the initial value at start-up) 0x18 (the initial value after the oscillation becomes stable)

4.13.5. Connection of Crystal Resonator

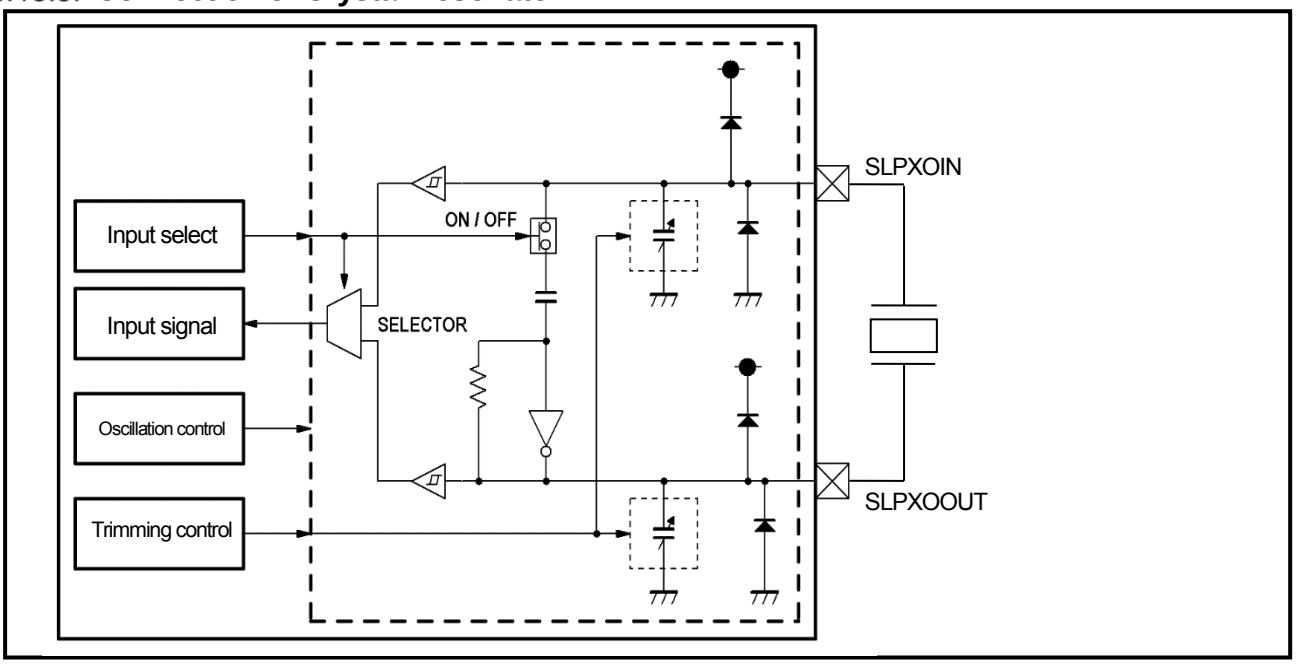


Figure 4-21 Connection of Crystal resonator

4.13.6. Use of External Crystal Oscillator

An external clock should be supplied to the SLPXOIN pin after the clock source is assigned to "Direct Input mode" by the command or the API in Table 4-15. The voltage range of the supplied clock is 0 to VDDIO (V).

A clock should not be supplied to the SLPXOIN pin before "Input from external" is set. The SLPXOOUT pin should be open or be connected to GND.

In order to supply the clock, the output of the external crystal oscillator should be controlled by the general-purpose output function of GPIO after the clock change procedure is done.

The external crystal oscillator can be used in Sleep mode and Backup mode. It cannot be used in Deep Sleep mode.

4.13.7. Built-in Silicon Oscillator (SiOSC)

TC35680/TC35681 integrates an oscillator “SiOSC” for the sleep clock. The SiOSC oscillates at start-up. The SiOSC’s jitter of the frequency, however, is larger than ±500 ppm which is the specified value by the **Bluetooth®** specification.

When the **Bluetooth®** communication is done, the clock source should be changed to the crystal resonator or the external oscillator. The change can be done by the command in the HCI mode or the API in the User-App mode shown in Table 4-15. When, however, an application is not timing-critical such as frequent transmission of an Advertising packet (Non connection), the SiOSC can be used because the accuracy of the SiOSC is enough. The crystal resonator and the external oscillator are unnecessary.

4.14. Sleep Clock Output Function

The sleep clock (32.768 kHz) can be issued from a GPIO pin. A corresponding API assigns the function to the GPIO14 pin. The output of the sleep clock stops in a low power mode.

The API “SYS_API_SetGpioMux()” can control the clock output enable and the stop of the output.

4.15. TRNG (True Random Number Generator) Function

TC35680/TC35681 include the TRNG (True Random Number Generator) function controlled by an oscillator sampling method. This function is composed of an ESG (Entropy Seed Generator) hardware and a DRBG (Deterministic Random Bit Generator) program in the built-in firmware.

The 256-bit random numbers generated by the TRNG function comply with the NIST SP800-22 and the BSI test standards.

The ESG starts up every boot and stops after it generates a random number seed. There is no need to input any random number seeds from outside, and, usually, the regeneration of the seed by the API control is not necessary, either. The random number seed can be regenerated by the API “SYS_API_ReseedRandData()”.

The random number seed should not be regenerated during wireless communication, otherwise the ESG operation noise may degrade the wireless performance.

The DRBG scrambles the random number seed to generate 256-bit length random numbers. Even during wireless communication, it does not affect the wireless communication performance. 8- to 256-bit length random numbers can be acquired by the API “SYS_API_GetRandData()”. The DRBG can repeat to generate the random numbers using the random number seed obtained at the boot. There is no need to regenerate the seed after a random number is acquired.

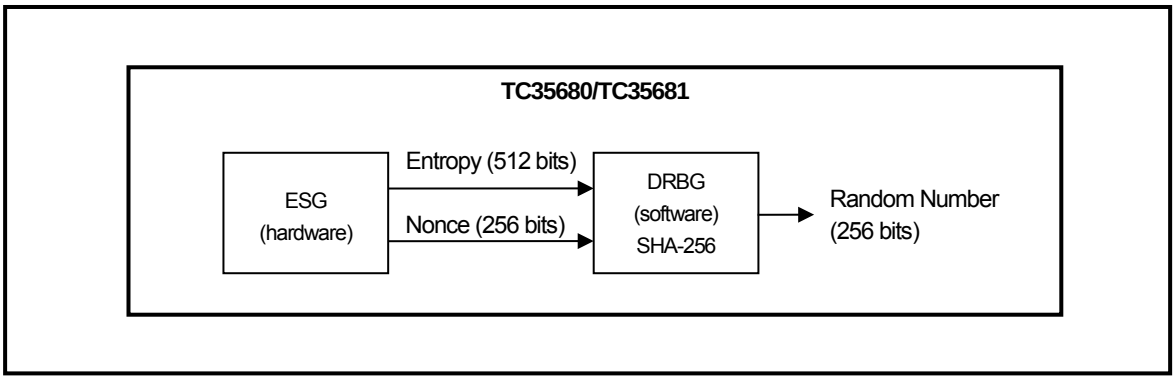


Figure 4-22 Configuration of TRNG

4.16. Auto-patch Function

TC35680/TC35681 provides an auto-patch function which is executed by the built-in firmware in the boot-up sequence.

The auto-patch programs should be stored in the built-in Flash memory or an external EEPROM together with a user application program. This function is available in the User-App mode (TC35680 and TC35681) and the HCI mode (TC35680 only). TC35681 in the HCI mode can be patched by the HCI command.

Table 4-17 shows the availability of the auto-patch function in each operating mode.

Table 4-17 Availability of the auto-patch function

Operating mode	HCI mode	Complete mode	User-App mode
TC35680	Yes	Yes	Yes
TC35681	No	No	Yes

The auto-patch function is executed by the built-in firmware in the following cases;

- ✓ During assertion of the hardware reset
- ✓ During assertion of the software reset
- ✓ During assertion of the reset by the watchdog timer
- ✓ Return procedure from the Deep Sleep mode

To activate the auto-patch function, the entry of the auto patch program should be done to a corresponding address in the built-in Flash memory. A desired value can be written in the RAM or a register at start-up before a host CPU or a user application program acquires the permission to control TC35680/TC35681.

This function is effective when a desired value should be written to the register for the adjustment of the clock frequency of the oscillator before the system is started up, and others.

4.17. Patch Function

The patch function is effective for repairing or improving the built-in firmware.

It is available in the HCI mode, the Complete mode, and the User-App mode. This function enables the modification of data in desired addresses in the memory space including the mask ROM. The size of the modification data is 32 Bytes.

We provides the patch programs in the source code. A necessary patch program should be selected and embedded to the proper locations in a user application program. The TC35680/TC35681 support 4 patch programs at maximum. The auto-patch programs are not included in this number.

4.18. CPU

The Arm® Cortex®-M0 processor is embedded in TC35680/TC35681.

The CPU in TC35680/TC35681 uses the reference clock. The clock frequency is 32 MHz at start-up.

API “SYS_API_ChangeSystemClock()” can select the clock frequency of 16 MHz or 32 MHz dynamically.

The 16MHz clock can be used only when the **Bluetooth® connection** of the advertising function does not operate.

5. Electrical Characteristics (TC35680FSG/TC35681FSG)

5.1. Absolute Maximum Ratings

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these ratings would be exceeded during operation, the electrical characteristics of the device may be irreparably altered, and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break-down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each absolute maximum rating will never be exceeded in any operating conditions.

Table 5-1 Absolute maximum ratings (VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Item	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	VBAT and VDDIO (Note 1)	-0.3	+3.9	V
I/O pin input voltage	VIN	-0.3	VDDIO + 0.3 (Note 2)	V
I/O pin input current	IIN	-10	+10	mA
Input power	RFIO	—	+10	dBm
Storage temperature	Tstg	-40	+125	°C

Note 1: Do not connect the VBAT pin to GND while the VDDIO pin is supplied with power. The current flow from the VDDIO pin to the VBAT pin in the device may cause damage, break-down, and/or degradation.
Please make sure that the VDDIO voltage should never exceed the VBAT voltage.

Note 2: VDDIO + 0.3 V should never exceed 3.9 V.

5.2. Operating Condition (Design Target Value)

The operating conditions are the conditions where this product can operate correctly with good quality. Malfunction may occur when even one of the conditions is not kept during operation. Please keep all specified conditions when an application equipment using this product is designed to avoid unexpected or poor results.

Table 5-2 Operation range (VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Item		Symbol (Pin name or Condition)	Rating			Unit
			Min.	Typ.	Max.	
Power supply voltage	VBAT operation voltage	VBATopr (TC35680)	1.9	3.0	3.6	V
		VBATopr (TC35681: Ta max. 105 °C)	1.8			
		VBATopr (TC35681: Ta max. 120 °C)	2.0			
	VDDIO operation voltage (Note 1)	VDDIOopr	1.8	3.0	3.6	V
	VDDIOFQ output voltage (Note 1) (Note 2)	VDDIOFQ (Note 2)	—	1.7	—	V
	VDDCORE voltage (Note 1)	VDDCORE1/VDDCORE2 (Active mode)	—	1.2	—	V
		VDDCORE1/VDDCORE2 (Low power mode)	—	0.85	—	V
RF frequency		Fc	2400	—	2483.5	MHz
Input frequency		Reference clock Fck	31.9984	32.00000	32.00160	MHz
		Sleep clock fslclk	32.751616	32.768000	32.784384	kHz
Ambient temperature		Ta (TC35680)	-40	+25	+85	°C
		Ta (TC35681)			+120	

Note 1: For the examples of recommended connections of the power supply pins, refer to the “Hardware Application Note”.

Note 2: The VDDIOFQ pin is an internal LDO regulator output. So do not connect an external power supply. Please connect an external by-pass capacitor to this pin (for TC35680).

5.3. DC Characteristics

5.3.1. Current Consumption (Design Target Value)

Table 5-3 shows a list of the current consumption values. Each value is an average operating value with a recommended connection of each power supply pin. For the measured values, the measurement is done under our company's evaluation environment.

The current consumption characteristics are based on the following conditions, unless specified otherwise.

- ✓ Ambient temperature (Ta): 25°C
- ✓ CPU clock frequency: 32 MHz
- ✓ Sleep clock frequency: 32.768 kHz, using a crystal resonator
- ✓ Power supply source in the normal operating mode: DC/DC convertor
- ✓ VBAT = VDDIO = 3.0 V
- ✓ VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V

Table 5-4 shows a list of DC characteristic values for each pin

Table 5-3 Current consumption

Item	Symbol	Condition		Measured pin (Note 1)	Rating			Unit
					Min.	Typ.	Max.	
Current consumption of the digital circuits at operation	IDD_{DIG} (Active1)	**Bluetooth**® wireless: not used Built-in Flash memory: not used		VBAT	—	1.2	—	mA
	IDD_{IO}	All GPIO is Hi-Z		VDDIO	—	0.3	—	μA
Digital circuit current consumption of the built-in Flash memory (Note 2)	IDD_{RD} (Read)	Reading		VBAT	—	3.8	—	mA
	IDD_{WR} (Write)	Programming			—	16.2	—	
	IDD_{ER} (Erase)	Erasing			—	16.2	—	
Data reception current consumption	IDD_{RX} (Active2)	125 kbps			—	5.2	—	
		500 kbps				5.2		
		1 Mbps				5.1		
		2 Mbps				5.6		
Data transmission current consumption	IDD_{TX} (Active3)	Output Power = 0 dBm	1 Mbps		—	5.2	—	
			2 Mbps		—	5.4	—	
		Output Power = +8 dBm	125 kbps		—	11.3	—	
			500 kbps		—		—	
			1 Mbps		—		—	
			2 Mbps		—	11.5	—	
		Output Power = +8 dBm Frequency of reference clock = 16 MHz	1 Mbps		—	11.0	—	
		Output Power = +8 dBm Power supply source: LDO regulator	1 Mbps		—	26.0	—	
Low power mode	—	Common condition: The oscillation of the reference clock is stopped.			—			μA
Current consumption in Low power mode (Sleep mode)	IDDS1	Power supply of CPU: on The oscillation of the sleep clock is operated. Whole of the data is retained.			—	2.5	—	
Current consumption in Low power mode (Backup mode)	IDDS2	Power supply of CPU: off The oscillation of the sleep clock is operated. Whole of the data is retained.			—	2.5	—	
Current consumption in Low power mode (Deep Sleep mode)	IDDS	Power supply of CPU: off The oscillation of the sleep clock is stopped. No data is retained.			—	0.05	—	

Note 1: The operating current consumption of a GPIO circuit depends on a load capacitance of its pin.

Note 2: Only for TC35680.

Table 5-4 DC characteristics (VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Item	Symbol	Condition		Measured pin (Note)	Rating			Unit
		I/F voltage	Other condition		Min.	Typ.	Max.	
High level input voltage	VIH	—	LVCMOS	VDDIO system	0.8 × VDDIO	—	—	V
Low level input voltage	VIL	—	LVCMOS	VDDIO system	—	—	0.2 × VDDIO	
High level input current	IIH	VDDIO = Input voltage to each pin	Pull-down resistor OFF	VDDIO system	-10	—	10	μA
			Pull-down resistor ON		10	—	200	
Low level input current	IIL		Pull-up resistor OFF		-10	—	10	
			Pull-up resistor ON		-200	—	-10	
High level output voltage	VOH	—	IOH = 1 mA	VDDIO system	VDDIO - 0.6	—	—	V
Low level output voltage	VOL	—	IOL = 1 mA	VDDIO system	—	—	0.4	V

Note: For the details of the power system pins, refer to Table 2-6 in which the power system of each function pin is shown.

5.4. Built-in Regulator Characteristics

Table 5-5 Built-in regulator characteristics (VBATopr: Min. to 3.6 V and VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Item	Symbol	Pin name or Condition	Rating			Unit
			Min.	Typ.	Max.	
Output voltage	Vout1	VDDCORE2	—	1.2 0.85 (Note 1)	—	V

Note 1: The output voltage in a low power mode.

Table 5-6 Built-in regulator characteristics (VBATopr: Min. to 3.6 V and VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Item	Symbol	Pin name or Condition	Rating			Unit
			Min.	Typ.	Max.	
Output voltage	Vout2	VDDIOFQ	—	1.7	—	V

5.5. ADC Characteristics

Table 5-7 ADC characteristics (VBATopr: Min. to 3.6 V and VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Analog reference voltage	VREFH	TC35680	1.9	3.0	3.6	V
		TC35681	1.8			
Analog input voltage	VAIN	—	VSSD	—	VREFH	V

5.6. RF Characteristics (Design Target Values)

The RF characteristics are based on the following conditions, unless otherwise specified.

- ✓ Ta = 25 °C
- ✓ VBAT = 3.0 V
- ✓ XOIN = 32 MHz (The frequency accuracy should be adjusted to ±2 ppm at room temperature)
- ✓ PAOUT = 8 dBm

Table 5-8 shows the RF transmission characteristics which are compliant with the **Bluetooth**® Core Specification Version 5.0 standard. Table 5-9 shows the RF reception characteristics. Some values in those tables are design target values.

Table 5-8 RF transmission characteristics

Item	Packet	Modulation condition	Channel	Condition	Rating			Unit
					Min.	Min.	Min.	
Output Power	255 octets	PRBS9	0, 12, 19, 39	Peak (Ppk)	—	0.4	Pavg+ 3 dB	dBm
				average (Pavg)	—	8	—	
In-band Emissions Uncoded data at 1 Ms/s	255 octets	PRBS9	0, 12, 19, 39	-4 MHz	—	-49	-30	dBm
				-3 MHz	—	-41	-30	
				-2 MHz	—	-40	-20	
				2 MHz	—	-40	-20	
				3 MHz	—	-41	-30	
				4 MHz	—	-49	-30	
In-band Emissions at 2 Ms/s	255 octets	PRBS9	0, 12, 19, 39	-6 MHz	—	-52	-30	dBm
				-5 MHz	—	-49	-20	
				-4 MHz	—	-50	-20	
				4 MHz	—	-50	-20	
				5 MHz	—	-50	-20	
				6 MHz	—	-52	-30	
Modulation Characteristics Uncoded data at 1 Ms/s	255 octets	11110000	0, 12, 19, 39	Δf1avg	225	244	275	kHz
		10101010		Δf2max	185	204	—	kHz
		—		Δf2avg/Δf1avg	0.8	0.90	—	Ratio
Modulation Characteristics at 2 Ms/s	255 octets	11110000	0, 12, 19, 39	Δf1avg	450	482	550	kHz
		10101010		Δf2max	370	415	—	kHz
		—		Δf2avg/Δf1avg	0.8	0.90	—	Ratio
Carrier frequency offset	255 octets	10101010	0, 12, 19, 39	average	-150	4	150	kHz
Carrier frequency drift	255 octets	10101010		worst	—	4	50	kHz
Carrier frequency drift Rate LE Coded (S=8)	255 octets	11110000		Absolute maximum	—	6	19.2	kHz/48 µs

Table 5-9 RF reception characteristics

Test item	Condition 1	Packet	Modulation condition	Channel	Condition 2	Rating			Unit
						Min.	Min.	Max.	
Rx Sensitivity	PER = 30.8 % at 1500 packets with dirty	37 octets	—	0, 12, 19, 39	2 Mbps	—	-93.2	—	dBm
					1 Mbps	—	-95.6	—	
					500 kbps (Coded PHY, S = 2)	—	-101.2	—	
					125 kbps (Coded PHY, S = 8)	—	-105.2	—	
		255 octets	—	0, 12, 19, 39	2 Mbps	—	-91.3	—	
					1 Mbps	—	-93.8	—	
					500 kbps (Coded PHY, S = 2)	—	-100.0	—	
					125 kbps (Coded PHY, S = 8)	—	-105.1	—	
C/I and Receiver Selectivity Performance, uncoded data at 1 Ms/s	PER = 30.8 % at 1500 packets	255 octets	Wanted signal: Bluetooth LE modulation PRBS9 Interferer: Bluetooth LE Modulation PRBS15	0, 2, 12, 19, 37, 39	-7 MHz	—	-42	—	dB
					-6 MHz	—	-32	-32	
					-5 MHz	—	-27	-26	
					-4 MHz	—	-29	-30	
					-3 MHz	—	-29	-32	
					-2 MHz	—	-26	-35	
					-1 MHz	—	-3	-2	
					0 MHz	—	8	8	
					1 MHz	—	-2	-2	
					2 MHz	—	-25	-30	
					3 MHz	—	-33	-38	
					4 MHz	—	-39	-40	
					5 MHz	—	-40	-44	
					6 MHz	—	-41	—	
C/I and Receiver Selectivity Performance, uncoded data at 2 Ms/s	PER = 30.8 % at 1500 packets	255 octets	Wanted signal: Bluetooth LE modulation PRBS9 Interferer: Bluetooth LE Modulation PRBS15	0, 2, 2, 19, 37, 39	-14 MHz	—	-43	-15	dB
					-12 MHz	—	-35	—	
					-10 MHz	—	-30	—	
					-8 MHz	—	-32	—	
					-6 MHz	—	-36	-15	
					-4 MHz	—	-30	—	
					-2 MHz	—	-7	15	
					0 MHz	—	5	21	
					2 MHz	—	-8	15	
					4 MHz	—	-29	-17	
					6 MHz	—	-37	—	
					8 MHz	—	-39	-27	
C/I and Receiver Selectivity Performance, LE Coded (S=2)	PER = 30.8 % at 1500 packets	255 octets	Wanted signal: Bluetooth LE modulation PRBS9 Interferer: Bluetooth LE Modulation PRBS15	0, 2, 12, 19, 37, 39	-7 MHz	—	-52	-31	dB
					-6 MHz	—	-36	-19	
					-5 MHz	—	-30	-13	
					-4 MHz	—	-33	-19	
					-3 MHz	—	-36	-31	
					-2 MHz	—	-34	-21	
					-1 MHz	—	-5	11	
					0 MHz	—	6	17	
					1 MHz	—	-5	11	
					2 MHz	—	-30	-21	
					3 MHz	—	-37	-31	
					4 MHz	—	-43	-31	
					5 MHz	—	-49	-31	
					6 MHz	—	-51	-31	

Test item	Condition 1	Packet	Modulation condition	Channel	Condition 2	Rating			Unit
						Min.	Min.	Max.	
C/I and Receiver Selectivity Performance, LE Coded (S=8)	PER = 30.8 % at 1500 packets	255 octets	Wanted signal: Bluetooth LE modulation PRBS9 Interferer: Bluetooth LE Modulation PRBS15	0, 2, 12, 19, 37, 39	-7 MHz	—	-52	-36	dB
					-6 MHz	—	-40	-24	
					-5 MHz	—	-29	-18	
					-4 MHz	—	-36	-24	
					-3 MHz	—	-42	-36	
					-2 MHz	—	-36	-26	
					-1 MHz	—	-10	6	
					0 MHz	—	5	12	
					1 MHz	—	-9	6	
					2 MHz	—	-32	-26	
					3 MHz	—	-37	-36	
					4 MHz	—	-51	-36	
					5 MHz	—	-52	-36	
					6 MHz	—	-52	-36	
Blocking Performance	PER = 30.8 % at 1500 packets	255 octets	Wanted signal: Bluetooth LE modulation PRBS9 Interferer: Unmodulated carrier	12	30 to 2000 MHz	-30	—	—	dBm
					2003 to 2399 MHz	-35	—	—	
					2484 to 2997 MHz	-35	—	—	
					3000 M to 12.75 GHz	-30	—	—	
Intermodulation Performance, 1 Ms/s	1500 packets	255 octets	Wanted signal: Bluetooth LE modulation PRBS9, -64 dBm Interferer #1: Bluetooth LE modulation PRBS15, -50 dBm Interferer #2: Unmodulated carrier, -50 dBm	0, 12, 19, 39	n=3	30.8	0	—	%
Intermodulation Performance, 2 Ms/s	1500 packets	255 octets	fWanted signal: Bluetooth LE modulation PRBS9, -64 dBm Interferer #1: Bluetooth LE modulation PRBS1, -50 dBm Interferer #2: Unmodulated carrier, -50 dBm	0, 12, 19, 39	n=3	30.8	0	—	%
Maximum input signal level	PER	255 octets	PRBS9	0, 12, 19, 39	-10 dBm	30.8	0	—	%
PER Report Integrity	PER	255 octets	PRBS9	0, 12, 19, 39	-30 dBm	50	50	65.4	%

Note: To the C/I characteristic and the blocking characteristic, the relaxed specifications of the certification test of **Bluetooth**® specification may be applied.

5.7. AC Characteristics (Design Target Values)

5.7.1. UART Interface

Table 5-10 AC characteristics of UART interface

Symbol	Item	Rating			Unit
		Min.	Typ.	Max.	
tCLDTDLY	CTSX falling edge to data transmission start	192	—	—	ns
tCHDTDLY	CTSX rising edge to data transmission completion	—	—	2	Byte
tRLDTDLY	RTSX falling edge to data reception start	0	—	—	ns
tRHDTDLY	RTSX rising edge to data reception completion	—	—	8	Byte

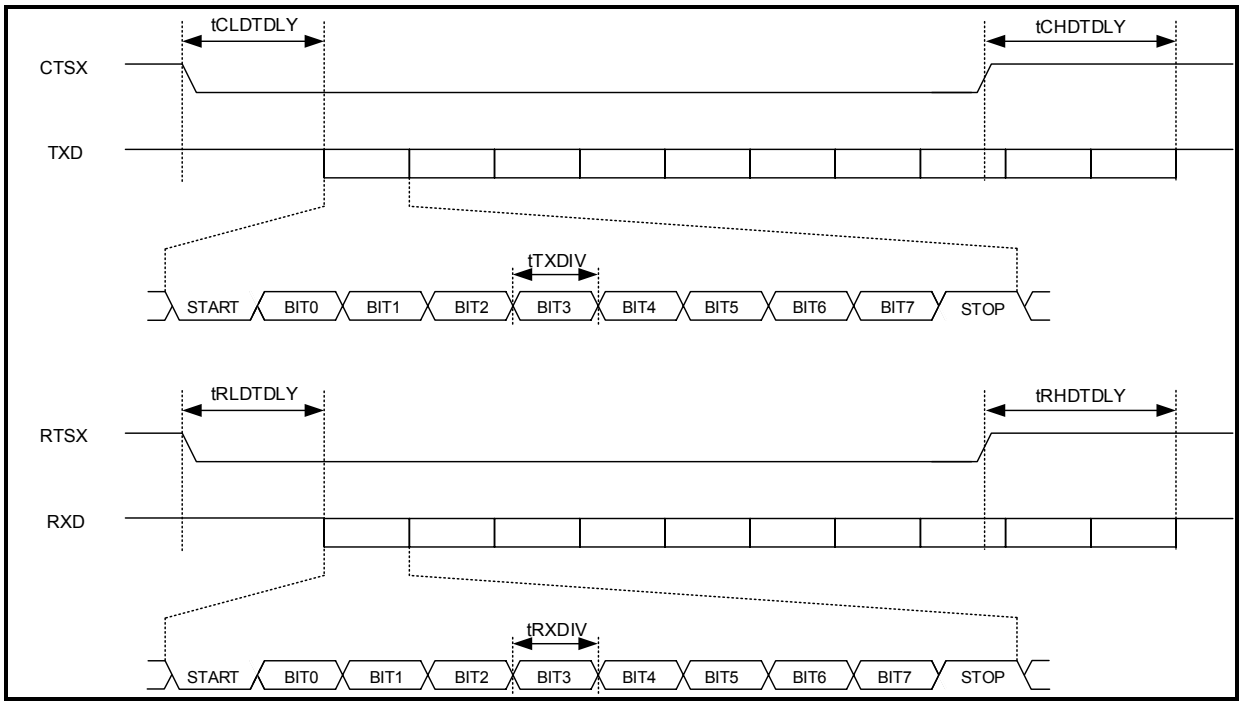


Figure 5-1 Timing chart of UART interface

5.7.2. I²C Interface

5.7.2.1. Standard Mode

Table 5-11 AC characteristics of I²C interface (Standard mode)

Symbol	Item	Rating			Unit
		Min.	Typ.	Max.	
tDATS	Data setup time	250	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Data validity period	—	—	3450	ns
tACKVD	ACK validity period	—	—	3450	ns
tSTAS	Restart condition setup time	4700	—	—	ns
tSTAH	Restart condition hold time	4000	—	—	ns
tSTOS	Stop condition setup time	4000	—	—	ns
tBUF	Bus release interval time between Stop condition and Start condition	4700	—	—	ns
tr	Rising time	—	—	1000	ns
tf	Falling time	—	—	300	ns
tHIGH	Serial clock High period	4000	—	—	ns
tLOW	Serial clock Low period	4700	—	—	ns
Cb	Bus load capacitance	—	—	400	pF

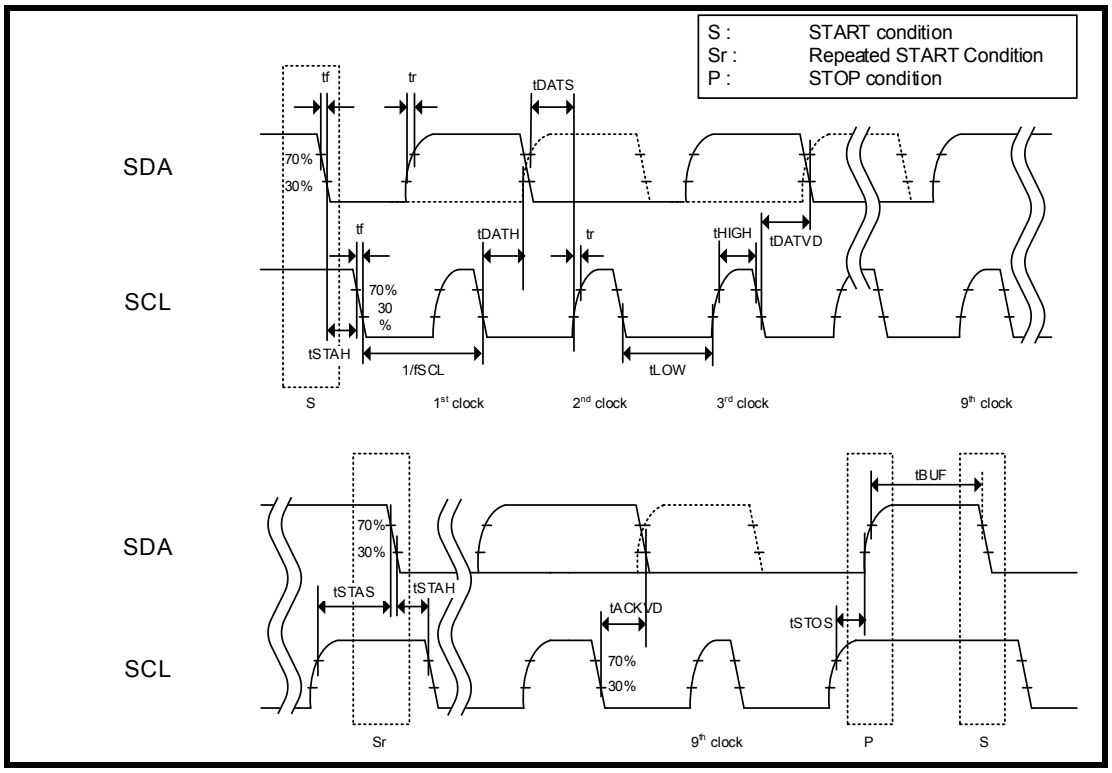


Figure 5-2 Timing chart of I²C interface (Standard mode)

5.7.2.2. Fast mode

Table 5-12 AC characteristics of I²C interface (Fast mode)

Symbol	Item	Rating			Unit
		Min.	Typ.	Max.	
tDATS	Data setup time	100	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Data validity period	—	—	900	ns
tACKVD	ACK validity period	—	—	900	ns
tSTAS	Restart condition setup time	600	—	—	ns
tSTAH	Restart condition hold time	600	—	—	ns
tSTOS	Stop condition setup time	600	—	—	ns
tBUF	Bus release interval time between Stop condition and Start condition	1300	—	—	ns
tr	Rising time	20 + 0.1 Cb	—	300	ns
tf	Falling time	20 + 0.1 Cb	—	300	ns
tSP	Removable spike pulse width	0	—	50	ns
tHIGH	Serial clock High period	—	1423	—	ns
tLOW	Serial clock Low period	—	1423	—	ns
Cb	Bus load capacitance	—	—	400	pF

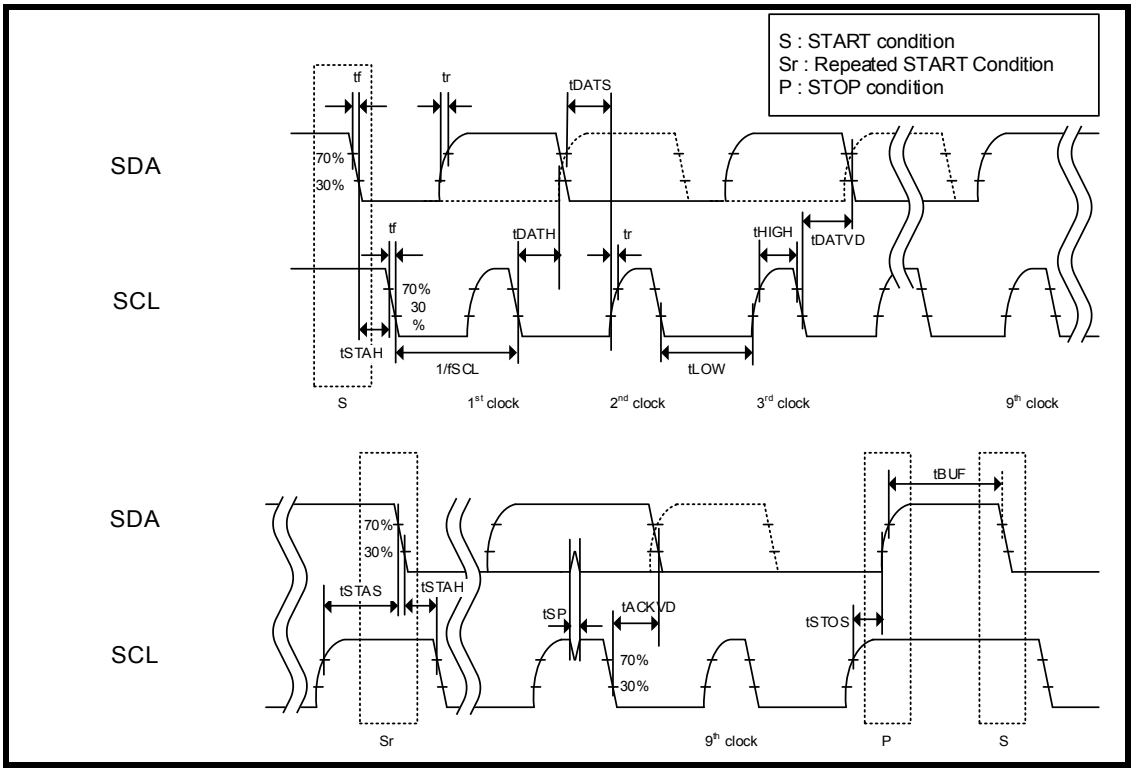


Figure 5-3 Timing chart of I²C interface (Fast mode)

5.7.3. SPI Interface

Table 5-13 AC characteristics of SPI interface

Symbol	Item	Rating			Unit
		Min.	Typ.	Max.	
tSPICLKCYC	SPI clock cycle	125	—	—	ns
tSPICLKHPW	SPI clock High pulse width	62	—	—	ns
tSPICLKLPW	SPI clock Low pulse width	62	—	—	ns
tSPICSS	SPI chip select setup time	31	—	—	ns
tSPICSH	SPI chip select hold time	62	—	—	ns
tSPIIW	SPI transfer idle pulse width	62	—	—	ns
tSPIAS	SPI address setup time	31	—	—	ns
tSPIAH	SPI address hold time	62	—	—	ns
tSPIDS	SPI data setup time	31	—	—	ns
tSPIDH	SPI data hold time	62	—	—	ns

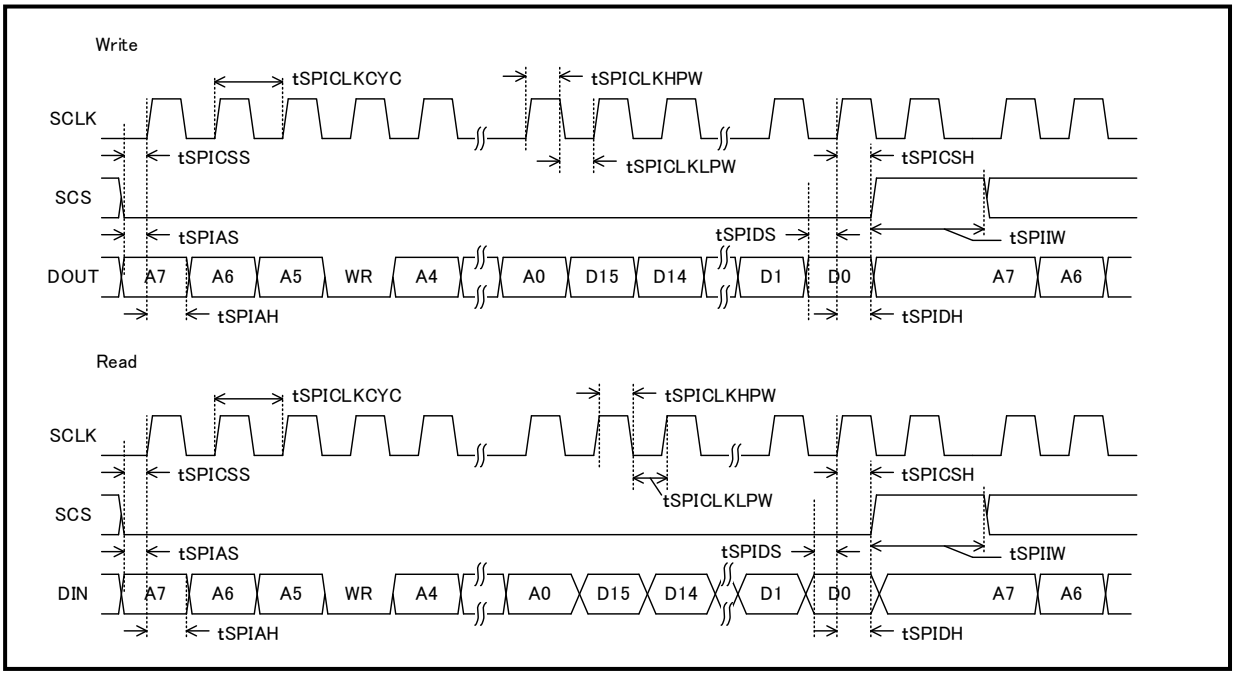


Figure 5-4 Timing chart of SPI interface

5.8. Characteristics of Flash Memory (Only TC35680)

Table 5-14 Characteristics of Flash memory (VBATopr: Min. to 3.6 V and VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Number of erase and programming cycles	—	Ta = 25 °C	10^5	—	—	Cycle

6. System Configuration Example

System configuration diagrams are shown in following subsections.

6.1. Configuration Example for User-App Mode (TC35680)

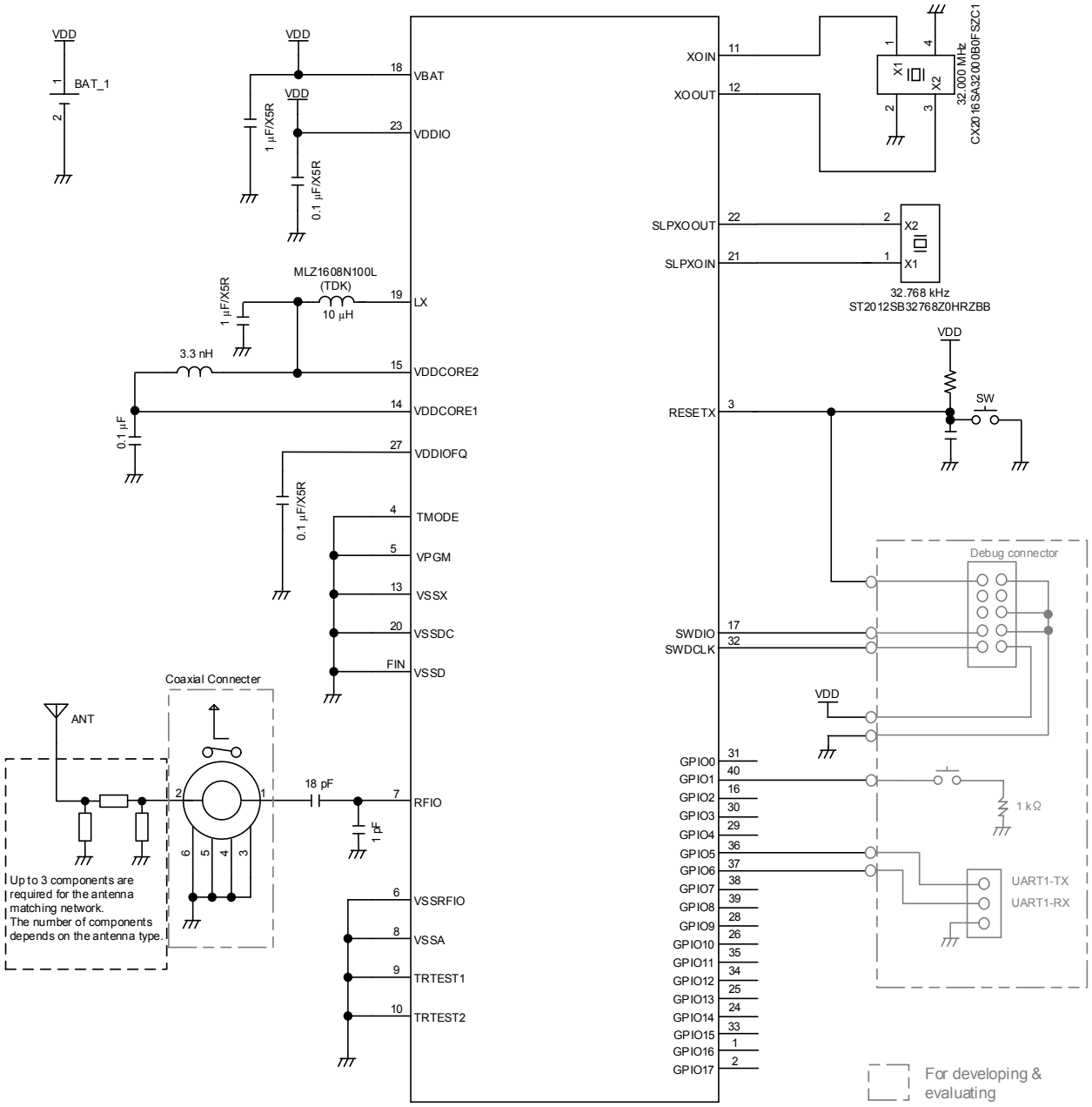


Figure 6-1 Example circuit for system configuration for TC35680FSG (User-App mode)

6.2. Configuration Example for HCI Mode (TC35680)

This example uses the UART interface to connect a host CPU.

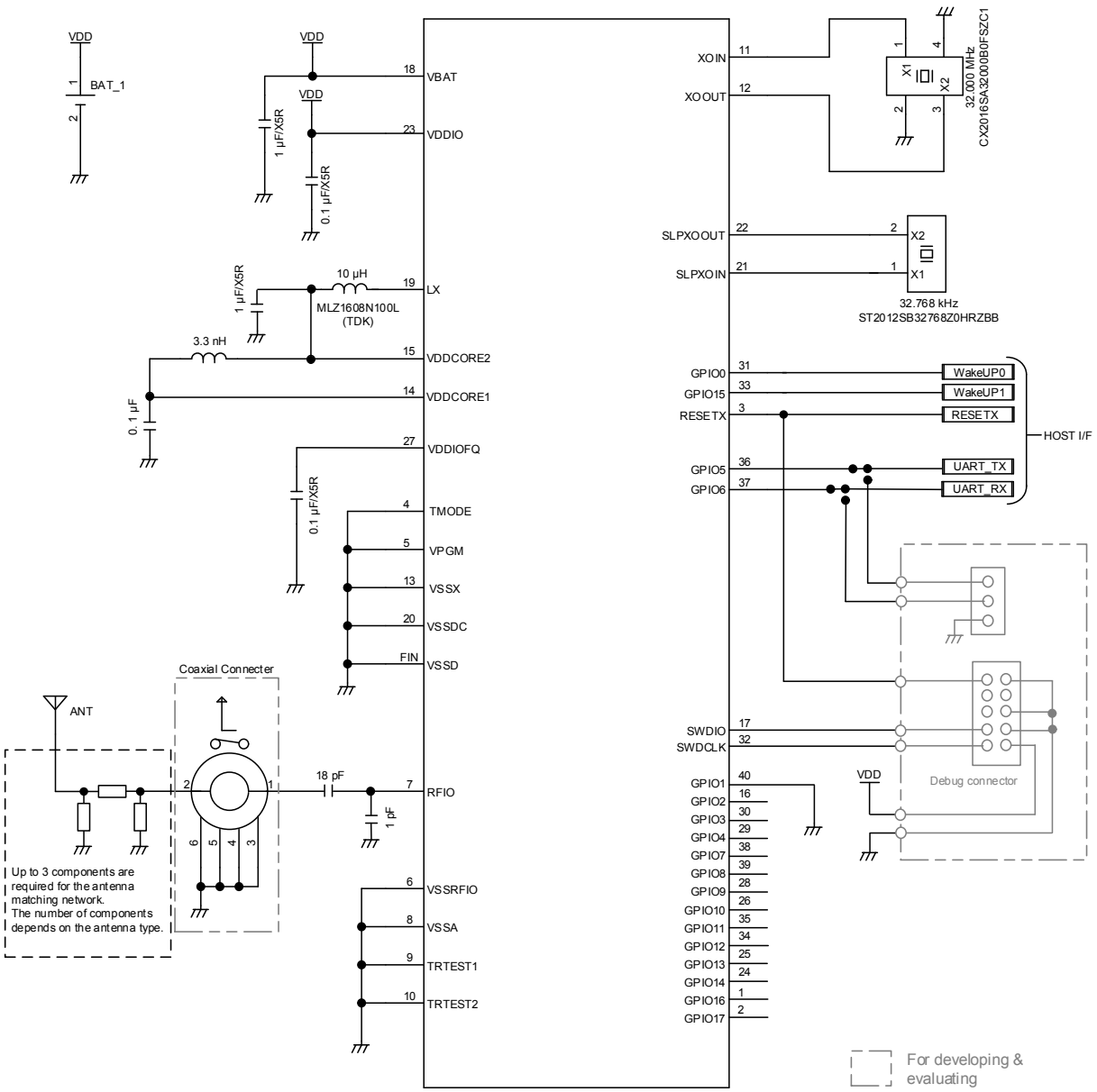


Figure 6-2 Example circuit for system configuration for TC35680FSG (HCI mode)

6.3. Connection Example for User-App Mode (TC35681 downloads a user application program from an external EEPROM)

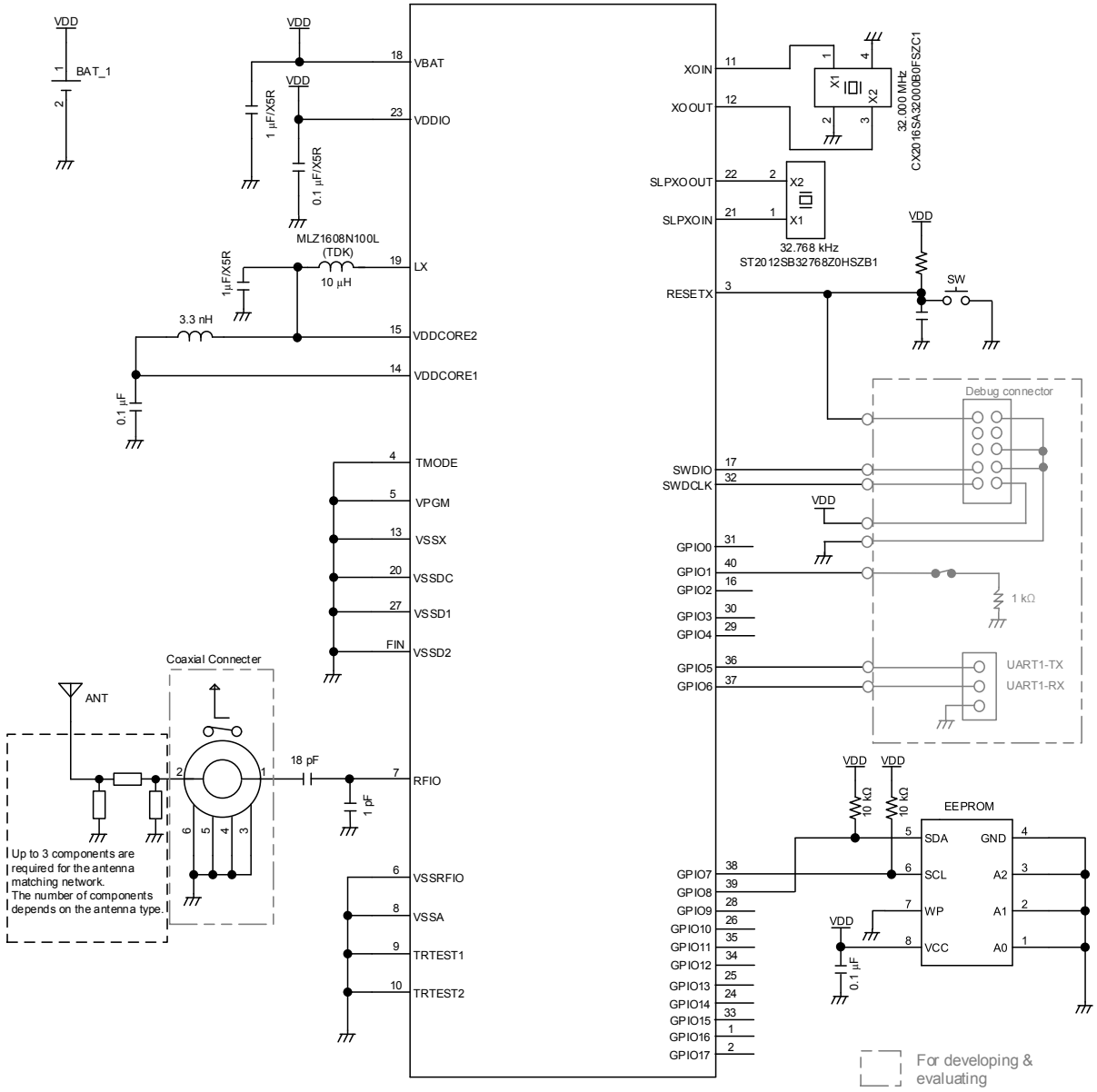


Figure 6-3 Example circuit for system configuration for TC35681FSG (User-App mode)

6.4. Connection Example for User-App Mode (TC35681 downloads a user application program from a host)

Refer to 6.5 “Connection Example for HCI Mode”.

6.5. Connection Example for HCI Mode (TC35681)

This example uses the UART interface to connect a host CPU.

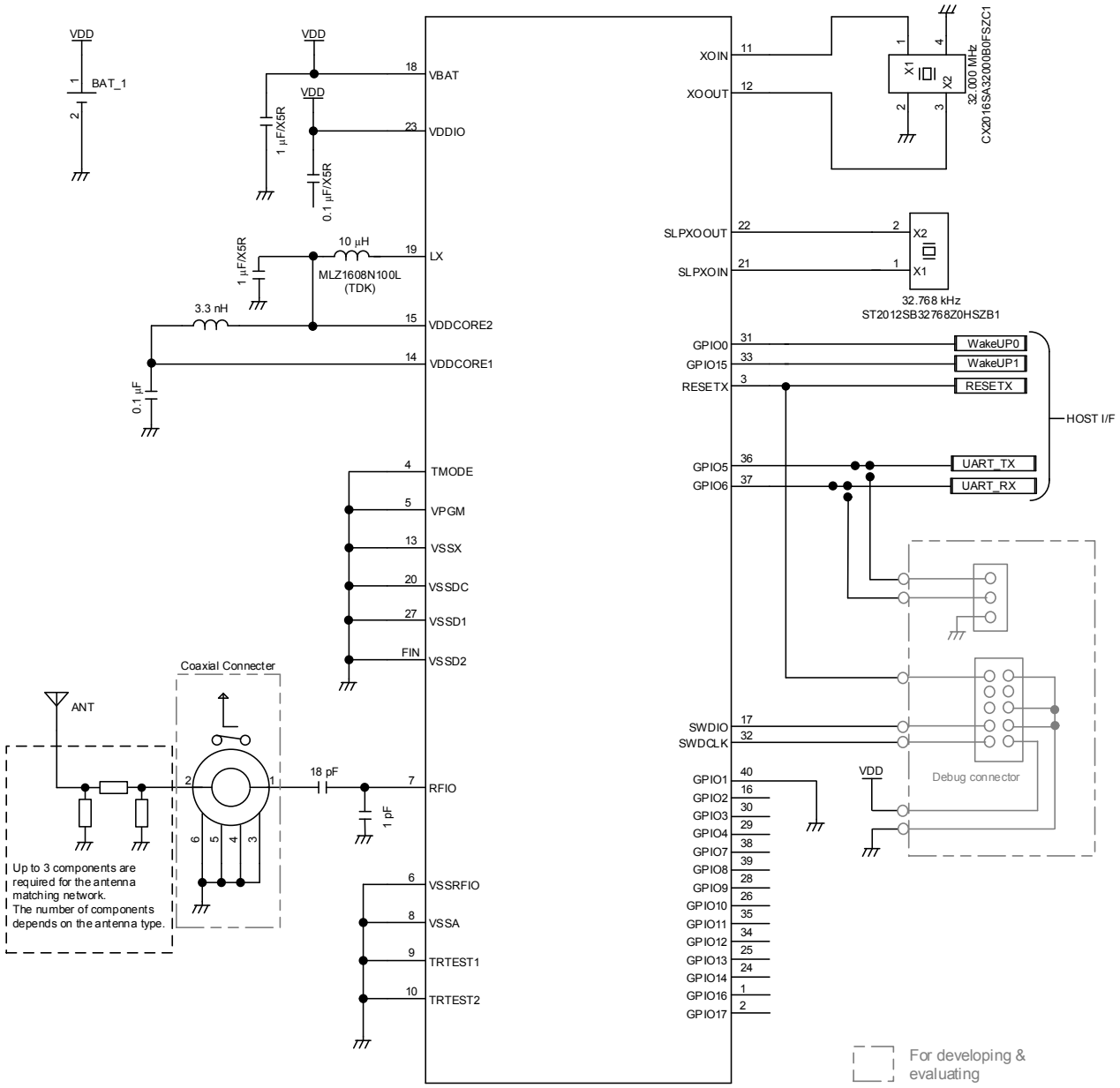


Figure 6-4 Example circuit for system configuration for TC35681FSG (HCI mode)

6.6. External Circuit Configuration for LDO Regulator (Common to TC35680 and TC35681)

The selection of the DC/DC converter or the LDO regulator is done by the setting at shipment. The LDO regulator is generally not selected for a standard product.

When the LDO regulator is used, a 0.1-μF capacitor, a 1-μF capacitor, and a 3.3-nH inductor are recommended to be connected with the VDDCORE1 pin and the VDDCORE2 pin, as shown in Figure 6-5.

The LX pin becomes Hi-Z when the LDO regulator is used. The pin can be open without any inductors.

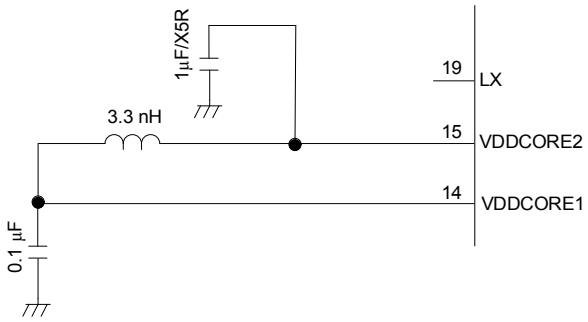
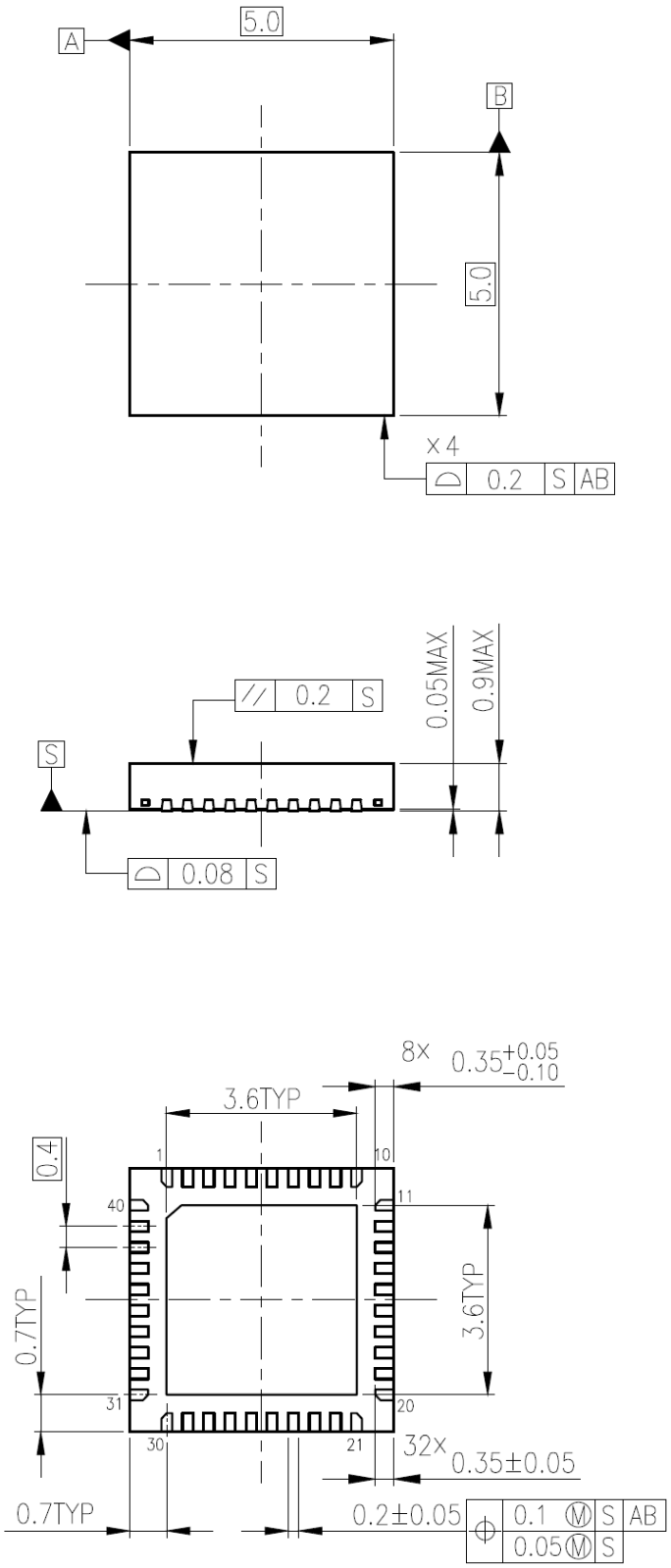


Figure 6-5 Circuit for LDO regulator

7. Package

7.1. Package Outline of TC35680FSG/TC35681FSG (P-VQFN40-0505-0.40-005/F01)

Unit: mm



Weight: 0.068 g (typ.)

Figure 7-1 Package outline (P-VQFN40-0505-0.40-005/F01)

7.2. Marking

7.2.1. Marking of TC35680FSG

Figure 7-2 shows a marking of the TC35680FSG.

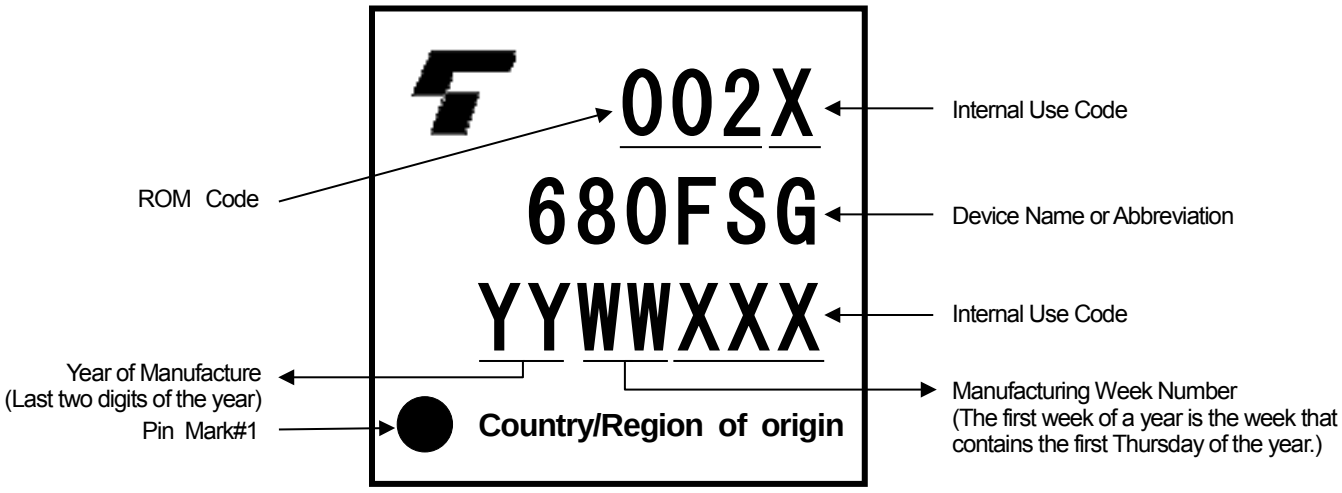


Figure 7-2 Marking (TC35680FSG)

7.2.2. Marking of TC35681FSG

Figure 7-3 shows a marking of the TC35681FSG.

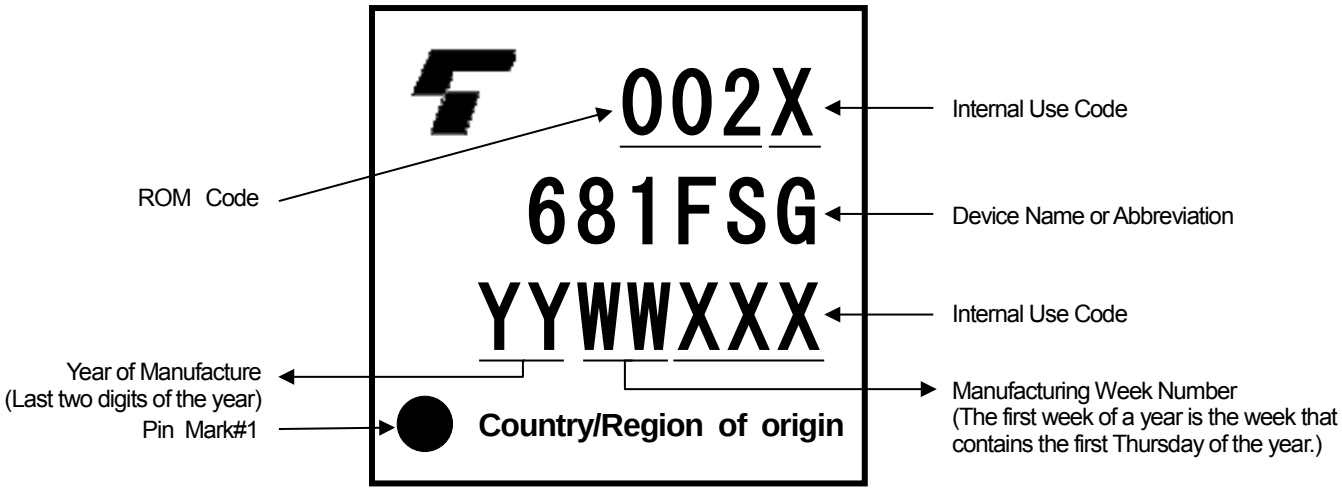


Figure 7-3 Marking (TC35681FSG)

8. List of Products

The line-up of the TC35680/TC35681 series is shown in Table 8-1.

Table 8-1 Product line-up

Product	Description
TC35680FSG-002(ELG	A unique BD address is added. DC/DC converter is used. SWD can be set. (Note 1) Minimum Order Quantity (MOQ) 2,000 units
TC35680FSG-002(E1C	A unique BD address is added. DC/DC converter is used. SWD can be set. (Note 1) MOQ 100 units
TC35681FSG-002(ELC	A unique BD address is added. DC/DC converter is used. SWD enabled. MOQ 2,000 units
TC35681FSG-002(E1C	A unique BD address is added. DC/DC converter is used. SWD enabled. MOQ 100 units

Note 1: When an SWD password is not set, the SWD function is not available. And even when the SWD password is set, the SWD function cannot be used until a password which is identical to the SWD password is set.

9. Revision History

Revision	Date	Description
1.0	2018-09-13	First release

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