# IS61WV25616ALL/ALS
# IS61WV25616BLL/BLS
# IS64WV25616BLL/BLS

## 256K x 16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM

**JULY 2010**

## FEATURES

HIGH SPEED: (IS61/64WV25616ALL/BLL)

- High-speed access time: 8, 10, 20 ns
- Low Active Power: 85 mW (typical)
- Low Standby Power: 7 mW (typical) CMOS standby

LOW POWER: (IS61/64WV25616ALS/BLS)

- High-speed access time: 25, 35, 45 ns
- Low Active Power: 35 mW (typical)
- Low Standby Power: 0.6 mW (typical) CMOS standby
- Single power supply
  - — $V_{DD}$ 1.65V to 2.2V (IS61WV25616Axx)
  - — $V_{DD}$ 2.4V to 3.6V (IS61/64WV25616Bxx)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial and Automotive temperature support
- Lead-free available

## DESCRIPTION

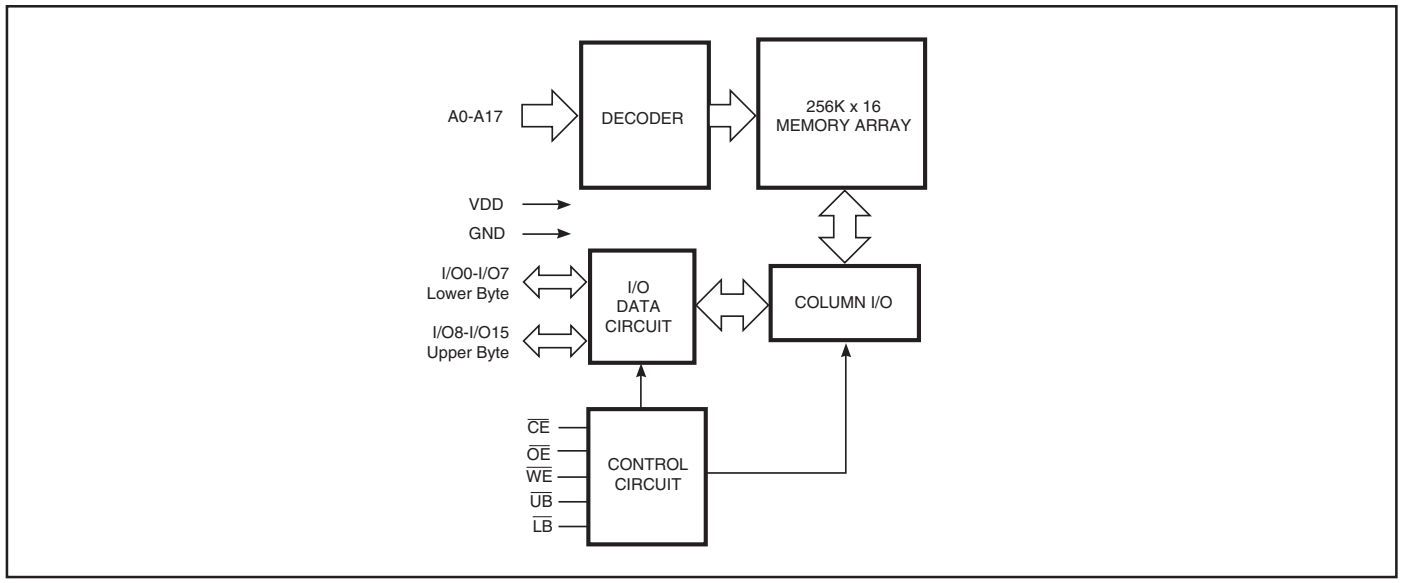
The *ISSI* IS61WV25616Axx/Bxx and IS64WV25616Bxx are high-speed, 4,194,304-bit static RAMs organized as 262,144 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS61WV25616Axx/Bxx and IS64WV25616Bxx are packaged in the JEDEC standard 44-pin TSOP Type II and 48-pin Mini BGA (6mm x 8mm).

## FUNCTIONAL BLOCK DIAGRAM

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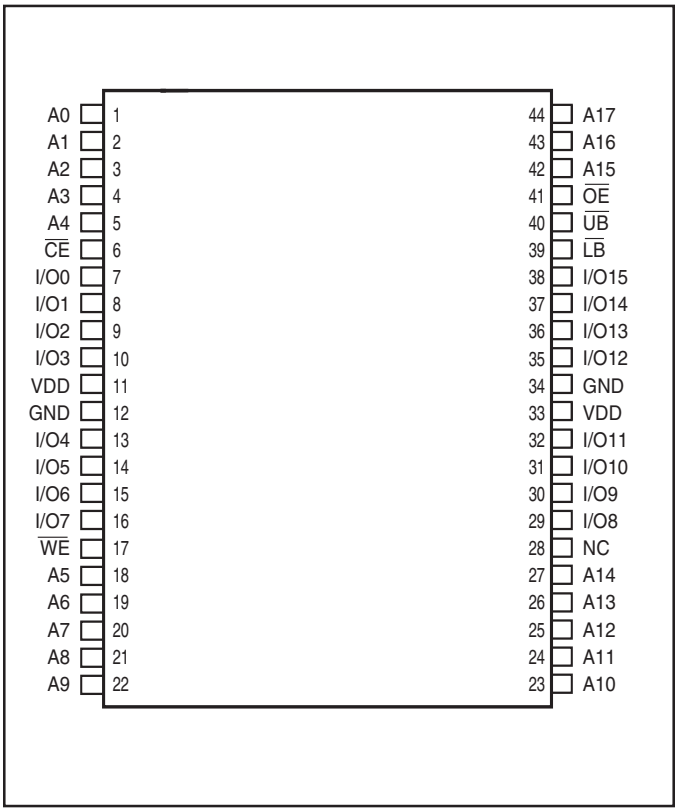
a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

## TRUTH TABLE

| Mode | $\overline{WE}$ | $\overline{CE}$ | $\overline{OE}$ | $\overline{LB}$ | $\overline{UB}$ | I/O PIN I/O0-I/O7 | I/O PIN I/O8-I/O15 | $V_{DD}$ Current |
|---|---|---|---|---|---|---|---|---|
| Not Selected | X | H | X | X | X | High-Z | High-Z | $I_{SB1}$, $I_{SB2}$ |
| Output Disabled | H | L | H | X | X | High-Z | High-Z | $I_{CC}$ |
| | X | L | X | H | H | High-Z | High-Z | |
| Read | H | L | L | L | H | $D_{OUT}$ | High-Z | $I_{CC}$ |
| | H | L | L | H | L | High-Z | $D_{OUT}$ | |
| | H | L | L | L | L | $D_{OUT}$ | $D_{OUT}$ | |
| Write | L | L | X | L | H | $D_{IN}$ | High-Z | $I_{CC}$ |
| | L | L | X | H | L | High-Z | $D_{IN}$ | |
| | L | L | X | L | L | $D_{IN}$ | $D_{IN}$ | |

## PIN CONFIGURATIONS

### 44-Pin TSOP (Type II) and SOJ



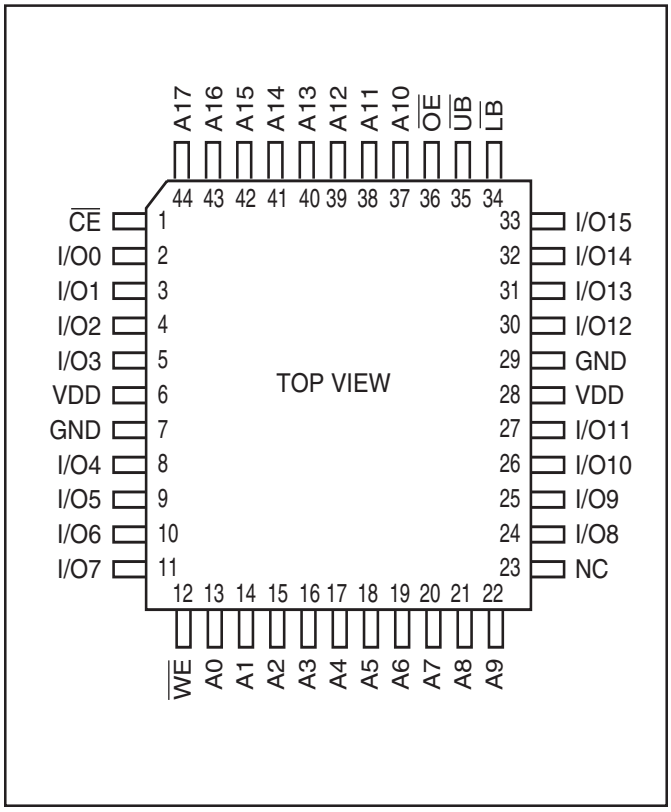

*SOJ package under evaluation.

## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A17 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{WE}$ | Write Enable Input |
| $\overline{LB}$ | Lower-byte Control (I/O0-I/O7) |
| $\overline{UB}$ | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| $V_{DD}$ | Power |
| GND | Ground |

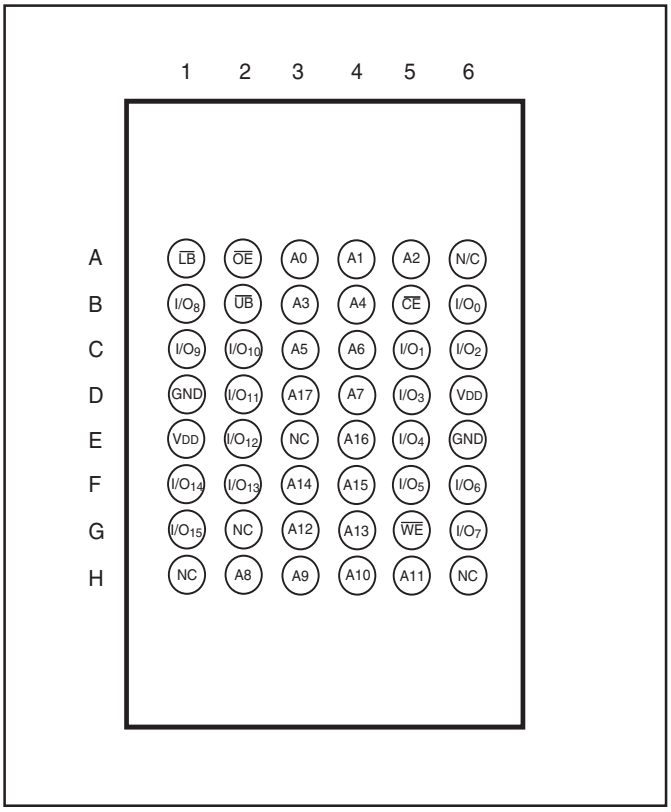
## PIN CONFIGURATIONS

### 44-Pin LQFP




*LQFP package under evaluation.

### 48-Pin mini BGA (6mm x 8mm)




## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A17 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{WE}$ | Write Enable Input |
| $\overline{LB}$ | Lower-byte Control (I/O0-I/O7) |
| $\overline{UB}$ | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| $V_{DD}$ | Power |
| GND | Ground |

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

### $V_{DD}$ = 3.3V ± 5%

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = Min., $I_{OH}$ = –4.0 mA | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $I_{OL}$ = 8.0 mA | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[1] | | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND ≤ $V_{IN}$ ≤ $V_{DD}$ | –1 | 1 | µA |
| $I_{LO}$ | Output Leakage | GND ≤ $V_{OUT}$ ≤ $V_{DD}$, Outputs Disabled | –1 | 1 | µA |

**Note:**
1. $V_{IL}$ (min.) = –0.3V DC; $V_{IL}$ (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   $V_{IH}$ (max.) = $V_{DD}$ + 0.3V DC; $V_{IH}$ (max.) = $V_{DD}$ + 2.0V AC (pulse width < 10 ns). Not 100% tested.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

### $V_{DD}$ = 2.4V-3.6V

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = Min., $I_{OH}$ = –1.0 mA | 1.8 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $I_{OL}$ = 1.0 mA | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[1] | | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND ≤ $V_{IN}$ ≤ $V_{DD}$ | –1 | 1 | µA |
| $I_{LO}$ | Output Leakage | GND ≤ $V_{OUT}$ ≤ $V_{DD}$, Outputs Disabled | –1 | 1 | µA |

**Note:**
1. $V_{IL}$ (min.) = –0.3V DC; $V_{IL}$ (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   $V_{IH}$ (max.) = $V_{DD}$ + 0.3V DC; $V_{IH}$ (max.) = $V_{DD}$ + 2.0V AC (pulse width < 10 ns). Not 100% tested.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

### $V_{DD}$ = 1.65V-2.2V

| Symbol | Parameter | Test Conditions | $V_{DD}$ | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = -0.1 mA | 1.65-2.2V | 1.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1 mA | 1.65-2.2V | — | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | 1.65-2.2V | 1.4 | $V_{DD}$ + 0.2 | V |
| $V_{IL}$[1] | Input LOW Voltage | | 1.65-2.2V | –0.2 | 0.4 | V |
| $I_{LI}$ | Input Leakage | GND ≤ $V_{IN}$ ≤ $V_{DD}$ | | –1 | 1 | µA |
| $I_{LO}$ | Output Leakage | GND ≤ $V_{OUT}$ ≤ $V_{DD}$, Outputs Disabled | | –1 | 1 | µA |

**Note:**
1. $V_{IL}$ (min.) = –0.3V DC; $V_{IL}$ (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   $V_{IH}$ (max.) = $V_{DD}$ + 0.3V DC; $V_{IH}$ (max.) = $V_{DD}$ + 2.0V AC (pulse width < 10 ns). Not 100% tested.

## AC TEST CONDITIONS

| Parameter | Unit (2.4V-3.6V) | Unit (3.3V ± 10%) | Unit (1.65V-2.2V) |
|---|---|---|---|
| Input Pulse Level | 0V to 3V | 0V to 3V | 0V to 1.8V |
| Input Rise and Fall Times | 1V/ns | 1V/ns | 1V/ns |
| Input and Output Timing and Reference Level ($V_{Ref}$) | 1.5V | 1.5V | 0.9V |
| Output Load | See Figures 1 and 2 | See Figures 1 and 2 | See Figures 1 and 2 |

## AC TEST LOADS

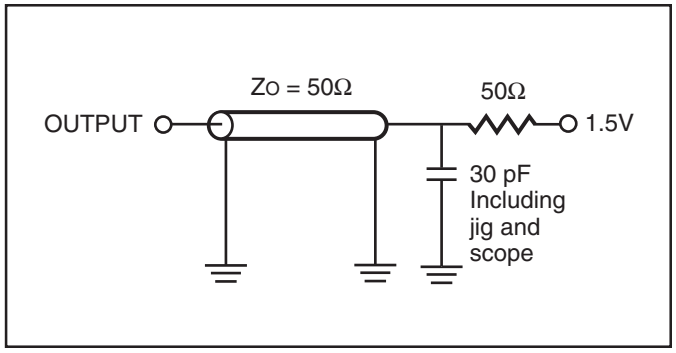



**Figure 1.**

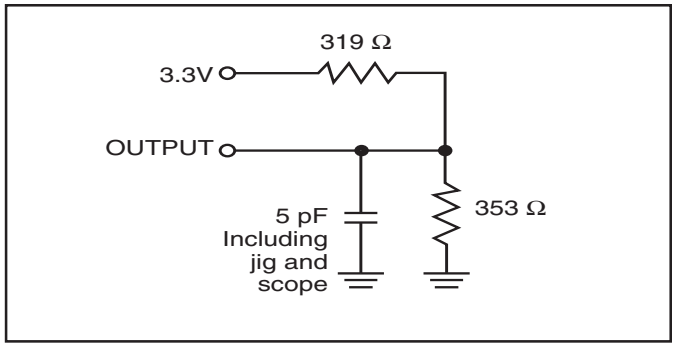



**Figure 2.**

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to $V_{DD}$ + 0.5 | V |
| $V_{DD}$ | $V_{DD}$ Relates to GND | –0.3 to 4.0 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |

**Notes:**
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE[1,2]

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{OUT}$ = 0V | 8 | pF |

**Notes:**
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = 3.3V.

# HIGH SPEED (IS61WV25616ALL/BLL)

## OPERATING RANGE ($V_{DD}$) (IS61WV25616ALL)

| Range | Ambient Temperature | $V_{DD}$ | Speed |
|---|---|---|---|
| Commercial | 0°C to +70°C | 1.65V-2.2V | 20ns |
| Industrial | –40°C to +85°C | 1.65V-2.2V | 20ns |
| Automotive | –40°C to +125°C | 1.65V-2.2V | 20ns |

## OPERATING RANGE ($V_{DD}$) (IS61WV25616BLL)[1]

| Range | Ambient Temperature | $V_{DD}$ (8 ns)[1] | $V_{DD}$ (10 ns)[1] |
|---|---|---|---|
| Commercial | 0°C to +70°C | 3.3V $\pm$ 5% | 2.4V-3.6V |
| Industrial | –40°C to +85°C | 3.3V $\pm$ 5% | 2.4V-3.6V |

**Note:**
1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V $\pm$ 5%, the device meets 8ns.

## OPERATING RANGE ($V_{DD}$) (IS64WV25616BLL)

| Range | Ambient Temperature | $V_{DD}$ (10 ns) |
|---|---|---|
| Automotive | –40°C to +125°C | 2.4V-3.6V |

## POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -8 Min. | -8 Max. | -10 Min. | -10 Max. | -20 Min. | -20 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | $V_{DD}$ Dynamic Operating Supply Current | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ | Com. | — | 50 | — | 40 | — | 35 | mA |
| | | | Ind. | — | 55 | — | 45 | — | 40 | |
| | | | Auto. | — | — | — | 65 | — | 60 | |
| | | | typ.[2] | | | 25 | | | | |
| $I_{CC1}$ | Operating Supply Current | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = 0 | Com. | — | 35 | — | 35 | — | 30 | mA |
| | | | Ind. | — | 40 | — | 40 | — | 40 | |
| | | | Auto. | — | — | — | 60 | — | 60 | |
| $I_{SB1}$ | TTL Standby Current (TTL Inputs) | $V_{DD}$ = Max., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\overline{CE} \geq V_{IH}$, f = 0 | Com. | — | 10 | — | 10 | — | 10 | mA |
| | | | Ind. | — | 15 | — | 15 | — | 15 | |
| | | | Auto. | — | — | — | 30 | — | 30 | |
| $I_{SB2}$ | CMOS Standby Current (CMOS Inputs) | $V_{DD}$ = Max., $\overline{CE} \geq V_{DD}$ – 0.2V, $V_{IN} \geq V_{DD}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0 | Com. | — | 8 | — | 8 | — | 8 | mA |
| | | | Ind. | — | 9 | — | 9 | — | 9 | |
| | | | Auto. | — | — | — | 20 | — | 20 | |
| | | | typ.[2] | | | 2 | | | | |

**Note:**
1. At f = $f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at $V_{DD}$ = 3.0V, $T_A$ = 25°C and not 100% tested.

# LOW POWER (IS61WV25616ALS/BLS)

## OPERATING RANGE ($V_{DD}$) (IS61WV25616ALS)

| Range | Ambient Temperature | $V_{DD}$ | Speed |
|---|---|---|---|
| Commercial | 0°C to +70°C | 1.65V-2.2V | 45ns |
| Industrial | –40°C to +85°C | 1.65V-2.2V | 45ns |
| Automotive | –40°C to +125°C | 1.65V-2.2V | 45ns |

## OPERATING RANGE ($V_{DD}$) (IS61WV25616BLS)

| Range | Ambient Temperature | $V_{DD}$ (25 ns) |
|---|---|---|
| Commercial | 0°C to +70°C | 2.4V-3.6V |
| Industrial | –40°C to +85°C | 2.4V-3.6V |

## OPERATING RANGE ($V_{DD}$) (IS64WV25616BLS)

| Range | Ambient Temperature | $V_{DD}$ (35 ns) |
|---|---|---|
| Automotive | –40°C to +125°C | 2.4V-3.6V |

## POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -25 Min. | -25 Max. | -35 Min. | -35 Max. | -45 Min. | -45 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | $V_{DD}$ Dynamic Operating Supply Current | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ | Com. | — | 20 | — | 20 | — | 15 | mA |
| | | | Ind. | — | 25 | — | 25 | — | 20 | |
| | | | Auto. | — | 50 | — | 50 | — | 40 | |
| | | | typ.[2] | | 11 | | | | | |
| $I_{CC1}$ | Operating Supply Current | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = 0 | Com. | — | 10 | — | 10 | — | 10 | mA |
| | | | Ind. | — | 12 | — | 12 | — | 12 | |
| | | | Auto. | — | 20 | — | 20 | — | 20 | |
| $I_{SB1}$ | TTL Standby Current (TTL Inputs) | $V_{DD}$ = Max., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\overline{CE} \geq V_{IH}$, f = 0 | Com. | — | 5 | — | 5 | — | 5 | mA |
| | | | Ind. | — | 7 | — | 7 | — | 7 | |
| | | | Auto. | — | 10 | — | 10 | — | 10 | |
| $I_{SB2}$ | CMOS Standby Current (CMOS Inputs) | $V_{DD}$ = Max., $\overline{CE} \geq V_{DD}$ – 0.2V, $V_{IN} \geq V_{DD}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0 | Com. | — | 1 | — | 1 | — | 1 | mA |
| | | | Ind. | — | 2 | — | 2 | — | 2 | |
| | | | Auto. | — | 10 | — | 10 | — | 10 | |
| | | | typ.[2] | | 0.2 | | | | | |

**Note:**

1. At f = $f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at $V_{DD}$ = 3.0V, $T_A$ = 25°C and not 100% tested.

## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | -8 Min. | -8 Max. | -10 Min. | -10 Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 8 | — | 10 | — | ns |
| $t_{AA}$ | Address Access Time | — | 8 | — | 10 | ns |
| $t_{OHA}$ | Output Hold Time | 2.0 | — | 2.0 | — | ns |
| $t_{ACE}$ | $\overline{CE}$ Access Time | — | 8 | — | 10 | ns |
| $t_{DOE}$ | $\overline{OE}$ Access Time | — | 4.5 | — | 4.5 | ns |
| $t_{HZOE}$[2] | $\overline{OE}$ to High-Z Output | — | 3 | — | 4 | ns |
| $t_{LZOE}$[2] | $\overline{OE}$ to Low-Z Output | 0 | — | 0 | — | ns |
| $t_{HZCE}$[2 | $\overline{CE}$ to High-Z Output | 0 | 3 | 0 | 4 | ns |
| $t_{LZCE}$[2] | $\overline{CE}$ to Low-Z Output | 3 | — | 3 | — | ns |
| $t_{BA}$ | $\overline{LB}$, $\overline{UB}$ Access Time | — | 5.5 | — | 6.5 | ns |
| $t_{HZB}$[2] | $\overline{LB}$, $\overline{UB}$ to High-Z Output | 0 | 3 | 0 | 3 | ns |
| $t_{LZB}$[2] | $\overline{LB}$, $\overline{UB}$ to Low-Z Output | 0 | — | 0 | — | ns |
| $t_{PU}$ | Power Up Time | 0 | — | 0 | — | ns |
| $t_{PD}$ | Power Down Time | — | 8 | — | 10 | ns |

**Notes:**
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

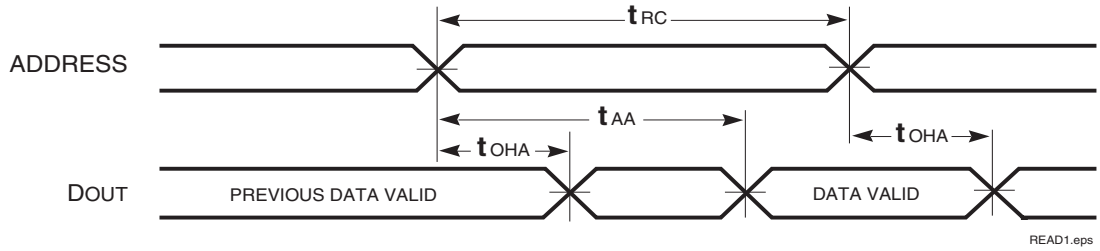
## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | -20 ns | | -25 ns | | -35 ns | | -45ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 20 | — | 25 | — | 35 | — | 45 | — | ns |
| $t_{AA}$ | Address Access Time | — | 20 | — | 25 | — | 35 | — | 45 | ns |
| $t_{OHA}$ | Output Hold Time | 2.5 | — | 4 | — | 4 | — | 7 | — | ns |
| $t_{ACE}$ | $\overline{CE}$ Access Time | — | 20 | — | 25 | — | 35 | — | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ Access Time | — | 8 | — | 12 | — | 15 | — | 20 | ns |
| $t_{HZOE}$[2] | $\overline{OE}$ to High-Z Output | 0 | 8 | 0 | 8 | 0 | 10 | 0 | 15 | ns |
| $t_{LZOE}$[2] | $\overline{OE}$ to Low-Z Output | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{HZCE}$[2 | $\overline{CE}$ to High-Z Output | 0 | 8 | 0 | 8 | 0 | 10 | 0 | 15 | ns |
| $t_{LZCE}$[2] | $\overline{CE}$ to Low-Z Output | 3 | — | 10 | — | 10 | — | 15 | — | ns |
| $t_{BA}$ | $\overline{LB}$, $\overline{UB}$ Access Time | — | 8 | — | 25 | — | 35 | — | 45 | ns |
| $t_{HZB}$ | $\overline{LB}$, $\overline{UB}$ to High-Z Output | 0 | 8 | 0 | 8 | 0 | 10 | 0 | 15 | ns |
| $t_{LZB}$ | $\overline{LB}$, $\overline{UB}$ to Low-Z Output | 0 | — | 0 | — | 0 | — | 0 | — | ns |

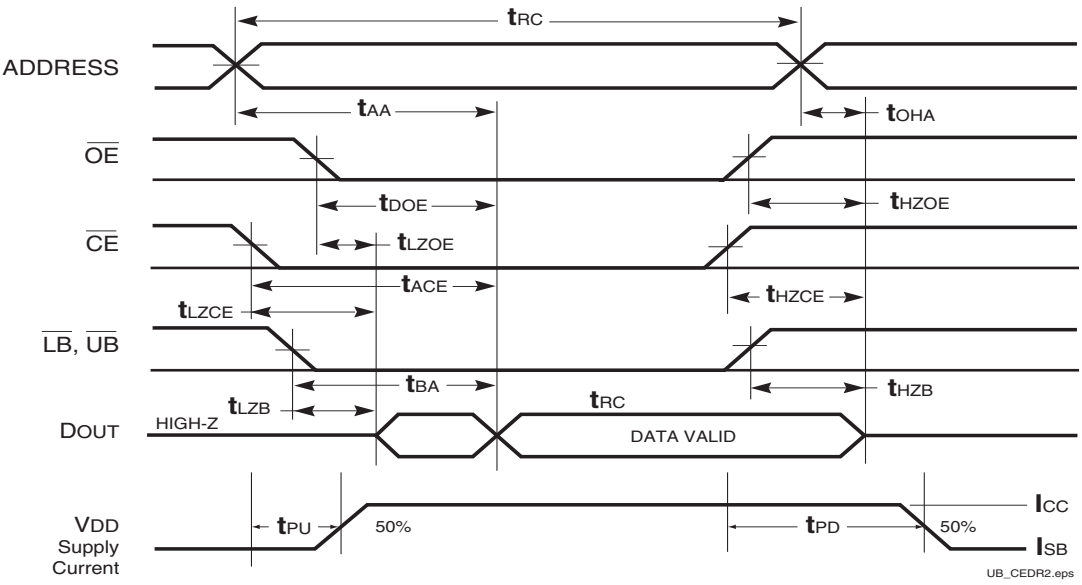
**Notes:**
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to $V_{DD}$-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

## AC WAVEFORMS

### READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{UB}$ or $\overline{LB}$ = $V_{IL}$)




### READ CYCLE NO. 2[1,3]




**Notes:**
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = $V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

## WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

| Symbol | Parameter | -8 Min. | -8 Max. | -10 Min. | -10 Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | 8 | — | 10 | — | ns |
| $t_{SCE}$ | $\overline{CE}$ to Write End | 6.5 | — | 8 | — | ns |
| $t_{AW}$ | Address Setup Time to Write End | 6.5 | — | 8 | — | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | — | 0 | — | ns |
| $t_{SA}$ | Address Setup Time | 0 | — | 0 | — | ns |
| $t_{PWB}$ | $\overline{LB}$, $\overline{UB}$ Valid to End of Write | 6.5 | — | 8 | — | ns |
| $t_{PWE1}$ | $\overline{WE}$ Pulse Width | 6.5 | — | 8 | — | ns |
| $t_{PWE2}$ | $\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW) | 8.0 | — | 10 | — | ns |
| $t_{SD}$ | Data Setup to Write End | 5 | — | 6 | — | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | — | 0 | — | ns |
| $t_{HZWE}$[2] | $\overline{WE}$ LOW to High-Z Output | — | 3.5 | — | 5 | ns |
| $t_{LZWE}$[2] | $\overline{WE}$ HIGH to Low-Z Output | 2 | — | 2 | — | ns |

**Notes:**
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

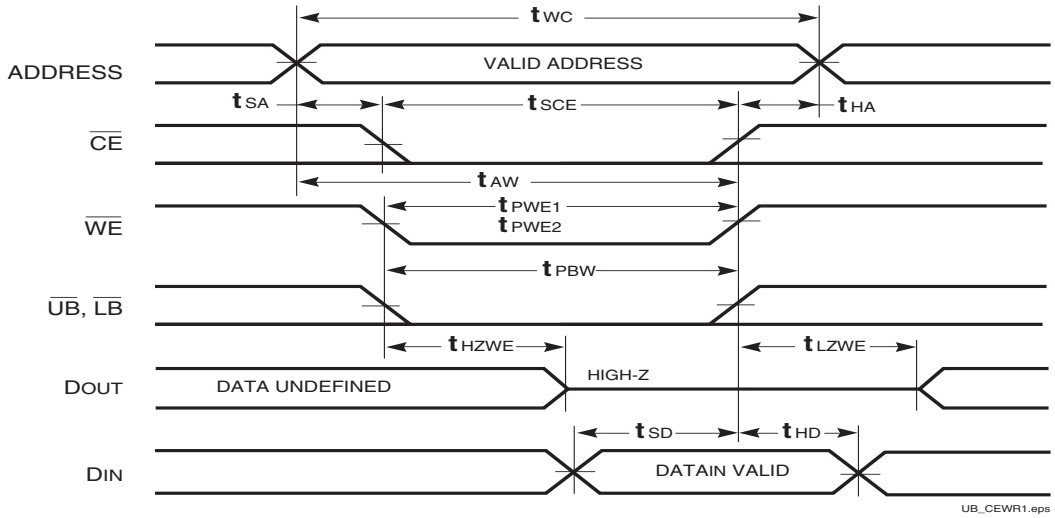
## WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

| Symbol | Parameter | -20 ns | | -25 ns | | -35 ns | | -45ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{WC}$ | Write Cycle Time | 20 | — | 25 | — | 35 | — | 45 | — | ns |
| $t_{SCE}$ | $\overline{CE}$ to Write End | 12 | — | 18 | — | 25 | — | 35 | — | ns |
| $t_{AW}$ | Address Setup Time to Write End | 12 | — | 15 | — | 25 | — | 35 | — | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{SA}$ | Address Setup Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PWB}$ | $\overline{LB}$, $\overline{UB}$ Valid to End of Write | 12 | — | 18 | — | 30 | — | 35 | — | ns |
| $t_{PWE1}$ | $\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH) | 12 | — | 18 | — | 30 | — | 35 | — | ns |
| $t_{PWE2}$ | $\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW) | 17 | — | 20 | — | 30 | — | 35 | — | ns |
| $t_{SD}$ | Data Setup to Write End | 9 | — | 12 | — | 15 | — | 20 | — | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{HZWE}$[3] | $\overline{WE}$ LOW to High-Z Output | — | 9 | — | 12 | — | 20 | — | 20 | ns |
| $t_{LZWE}$[3] | $\overline{WE}$ HIGH to Low-Z Output | 3 | — | 5 | — | 5 | — | 5 | — | ns |

**Notes:**
1. Test conditions assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to $V_{DD}$-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

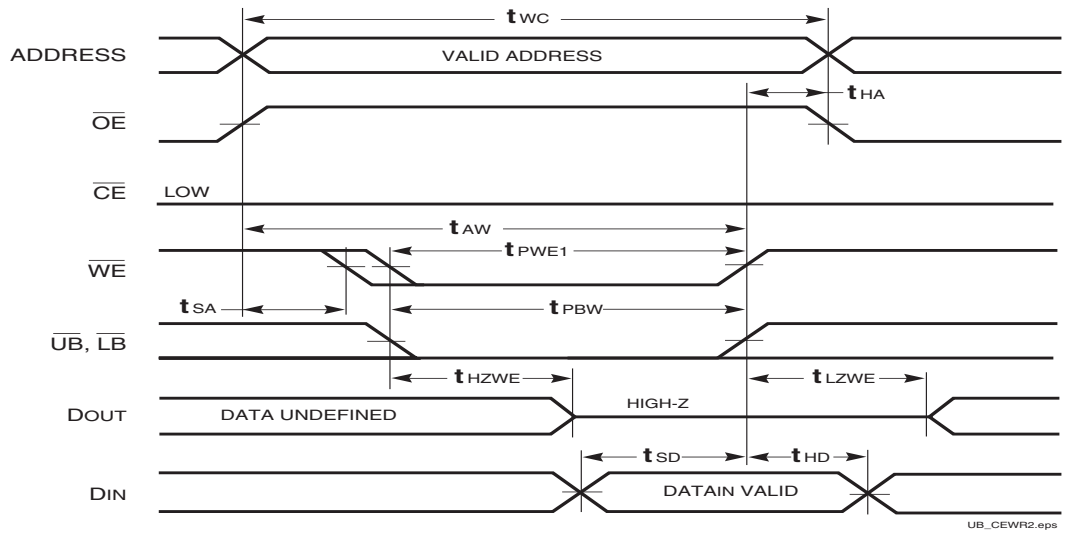
## AC WAVEFORMS

### WRITE CYCLE NO. 1 ($\overline{CE}$ Controlled, $\overline{OE}$ is HIGH or LOW) (1)



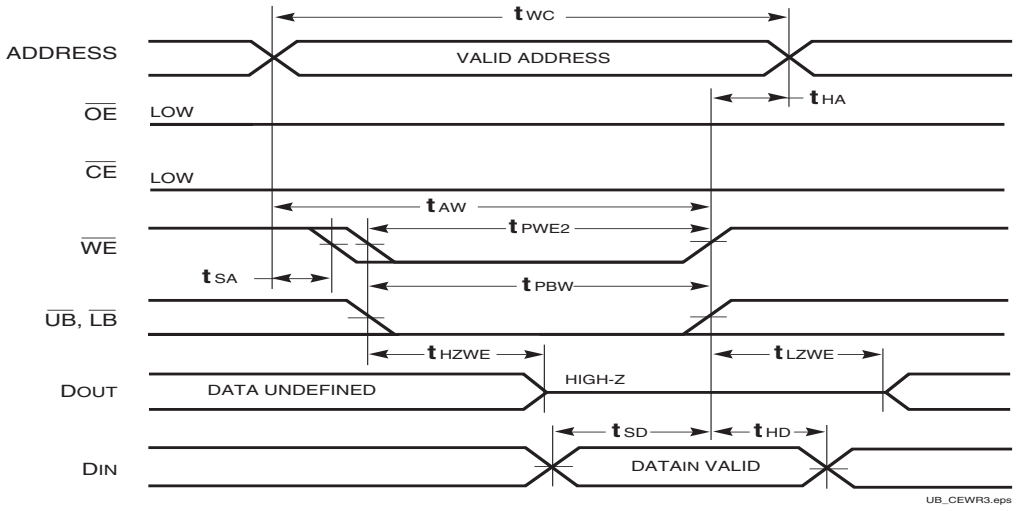

**Notes:**
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [ ($\overline{LB}$) = ($\overline{UB}$) ] ($\overline{WE}$).

### WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled. $\overline{OE}$ is HIGH During Write Cycle) (1,2)

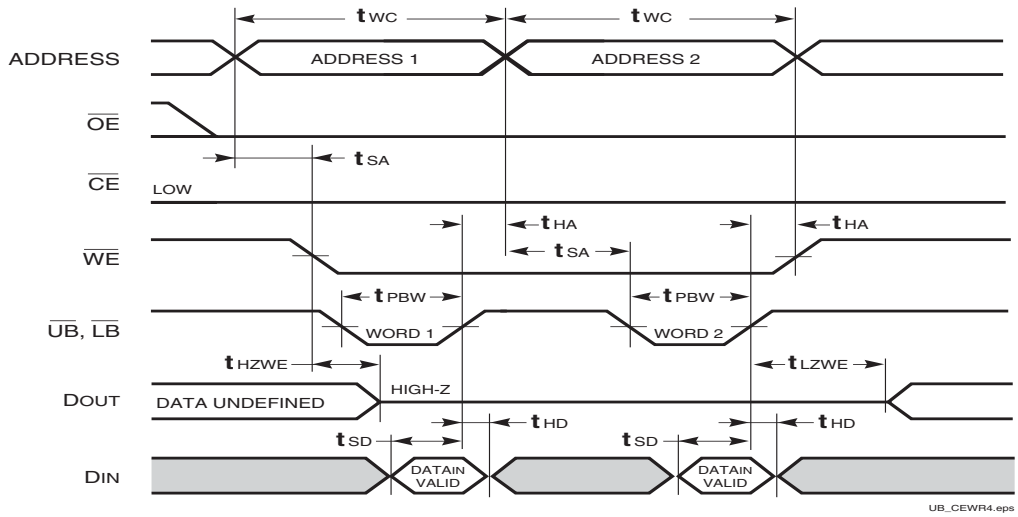


## AC WAVEFORMS

### WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled. $\overline{OE}$ is LOW During Write Cycle) (1)




### WRITE CYCLE NO. 4 ($\overline{LB}$, $\overline{UB}$ Controlled, Back-to-Back Write) (1,3)




**Notes:**

1. The internal Write time is defined by the overlap of $\overline{CE}$ = LOW, $\overline{UB}$ and/or $\overline{LB}$ = LOW, and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The $t_{SA}$, $t_{HA}$, $t_{SD}$, and $t_{HD}$ timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE}$ = LOW to place the I/O in a HIGH-Z state.
3. $\overline{WE}$ may be held LOW across many address cycles and the $\overline{LB}$, $\overline{UB}$ pins can be used to control the Write function.

# HIGH SPEED (IS61WV25616ALL/BLL)

## DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for Data Retention | See Data Retention Waveform | | 2.0 | — | 3.6 | V |
| $I_{DR}$ | Data Retention Current | $V_{DD}$ = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com. | — | 2 | 8 | mA |
| | | | Ind. | — | — | 9 | |
| | | | Auto. | | | 15 | |
| $t_{SDR}$ | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| $t_{RDR}$ | Recovery Time | See Data Retention Waveform | | $t_{RC}$ | — | — | ns |

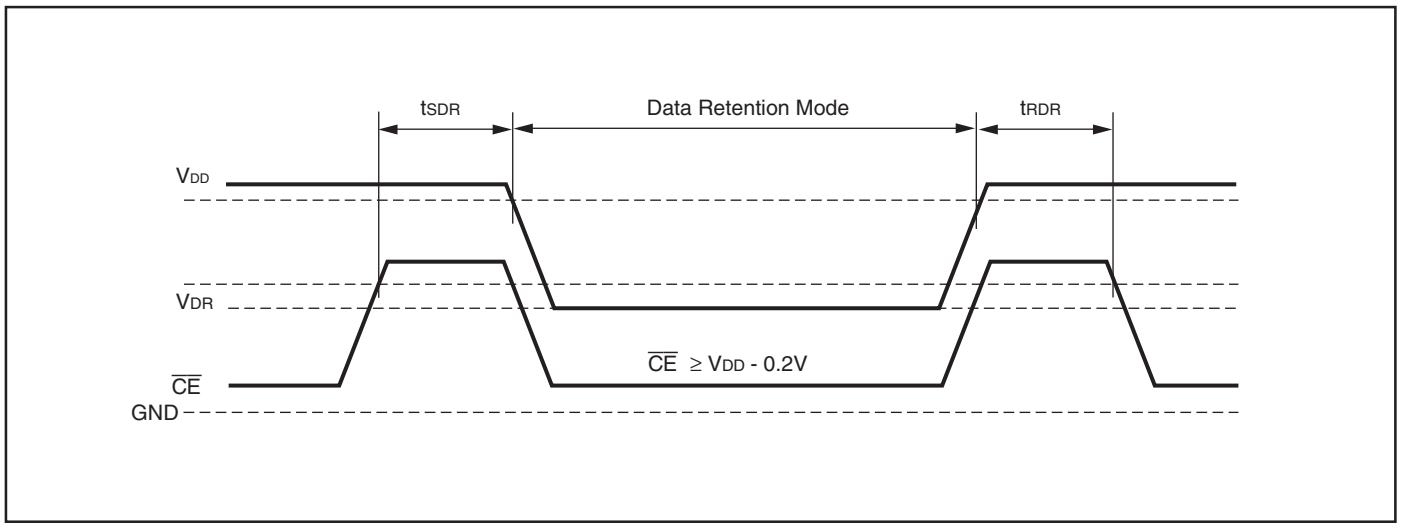
**Note 1**: Typical values are measured at $V_{DD}$ = 3.0V, $T_A$ = 25°C and not 100% tested.

## DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for Data Retention | See Data Retention Waveform | | 1.2 | — | 3.6 | V |
| $I_{DR}$ | Data Retention Current | $V_{DD}$ = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com. | — | 5 | 10 | mA |
| | | | Ind. | — | — | 15 | |
| $t_{SDR}$ | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| $t_{RDR}$ | Recovery Time | See Data Retention Waveform | | $t_{RC}$ | — | — | ns |

**Note 1**: Typical values are measured at $V_{DD}$ = 1.8V, $T_A$ = 25°C and not 100% tested.

## DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



## LOW POWER (IS61WV25616ALS/BLS)

### DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for Data Retention | See Data Retention Waveform | | 2.0 | — | 3.6 | V |
| $I_{DR}$ | Data Retention Current | $V_{DD}$ = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com. | — | 0.2 | 1 | mA |
| | | | Ind. | — | — | 2 | |
| | | | Auto. | | | 10 | |
| $t_{SDR}$ | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| $t_{RDR}$ | Recovery Time | See Data Retention Waveform | | $t_{RC}$ | — | — | ns |

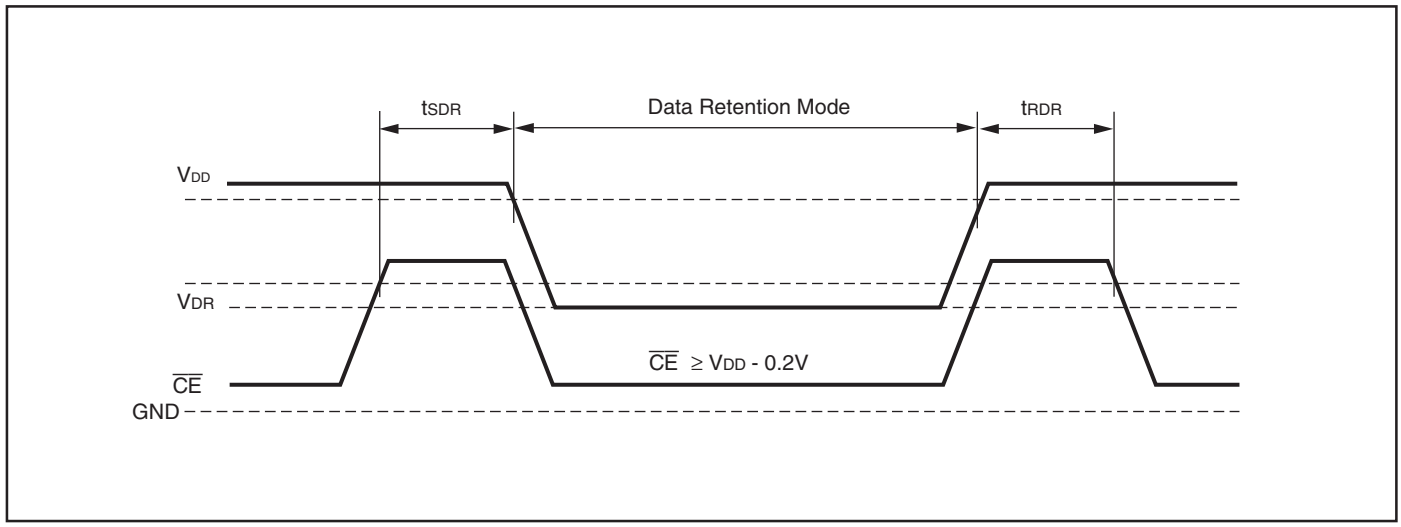
**Note 1**: Typical values are measured at $V_{DD}$ = 3.0V, $T_A$ = 25°C and not 100% tested.

### DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for Data Retention | See Data Retention Waveform | | 1.2 | — | 3.6 | V |
| $I_{DR}$ | Data Retention Current | $V_{DD}$ = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com. | — | 0.2 | 1 | mA |
| | | | Ind. | — | — | 2 | |
| $t_{SDR}$ | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| $t_{RDR}$ | Recovery Time | See Data Retention Waveform | | $t_{RC}$ | — | — | ns |

: Typical values are measured at $V_{DD}$ = 1.8V, $T_A$ = 25°C and not 100% tested.

### DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



## ORDERING INFORMATION (HIGH SPEED)

### Commercial Range: 0°C to +70°C
### Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 10 (8[1]) | IS61WV25616BLL-10TL | TSOP (Type II), Lead-free |

**Note:**
1. Speed = 8ns for $V_{DD}$ = 3.3V ± 5%. Speed = 10ns for $V_{DD}$ = 2.4V to 3.6V.

### Industrial Range: -40°C to +85°C
### Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 10 (8[1]) | IS61WV25616BLL-10BI | 48 mini BGA (6mm x 8mm) |
| | IS61WV25616BLL-10BLI | 48 mini BGA (6mm x 8mm), Lead-free |
| | IS61WV25616BLL-10TI | TSOP (Type II) |
| | IS61WV25616BLL-10TLI | TSOP (Type II), Lead-free |

**Note:**
1. Speed = 8ns for $V_{DD}$ = 3.3V ± 5%. Speed = 10ns for $V_{DD}$ = 2.4V to 3.6V.

### Industrial Range: -40°C to +85°C
### Voltage Range: 1.65V to 2.2V

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 20 | IS61WV25616ALL-20BI | 48 mini BGA (6mm x 8mm) |
| | IS61WV25616ALL-20TI | TSOP (Type II) |
| | IS61WV25616ALL-20TLI | TSOP (Type II), Lead-free |

### Automotive Range: -40°C to +125°C
### Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 10 | IS64WV25616BLL-10BA3 | 48 mini BGA (6mm x 8mm) |
| | IS64WV25616BLL-10BLA3 | 48 mini BGA (6mm x 8mm), Lead-free |
| | IS64WV25616BLL-10CTA3 | TSOP (Type II), Copper Leadframe |
| | IS64WV25616BLL-10CTLA3 | TSOP (Type II), Lead-free, Copper Leadframe |

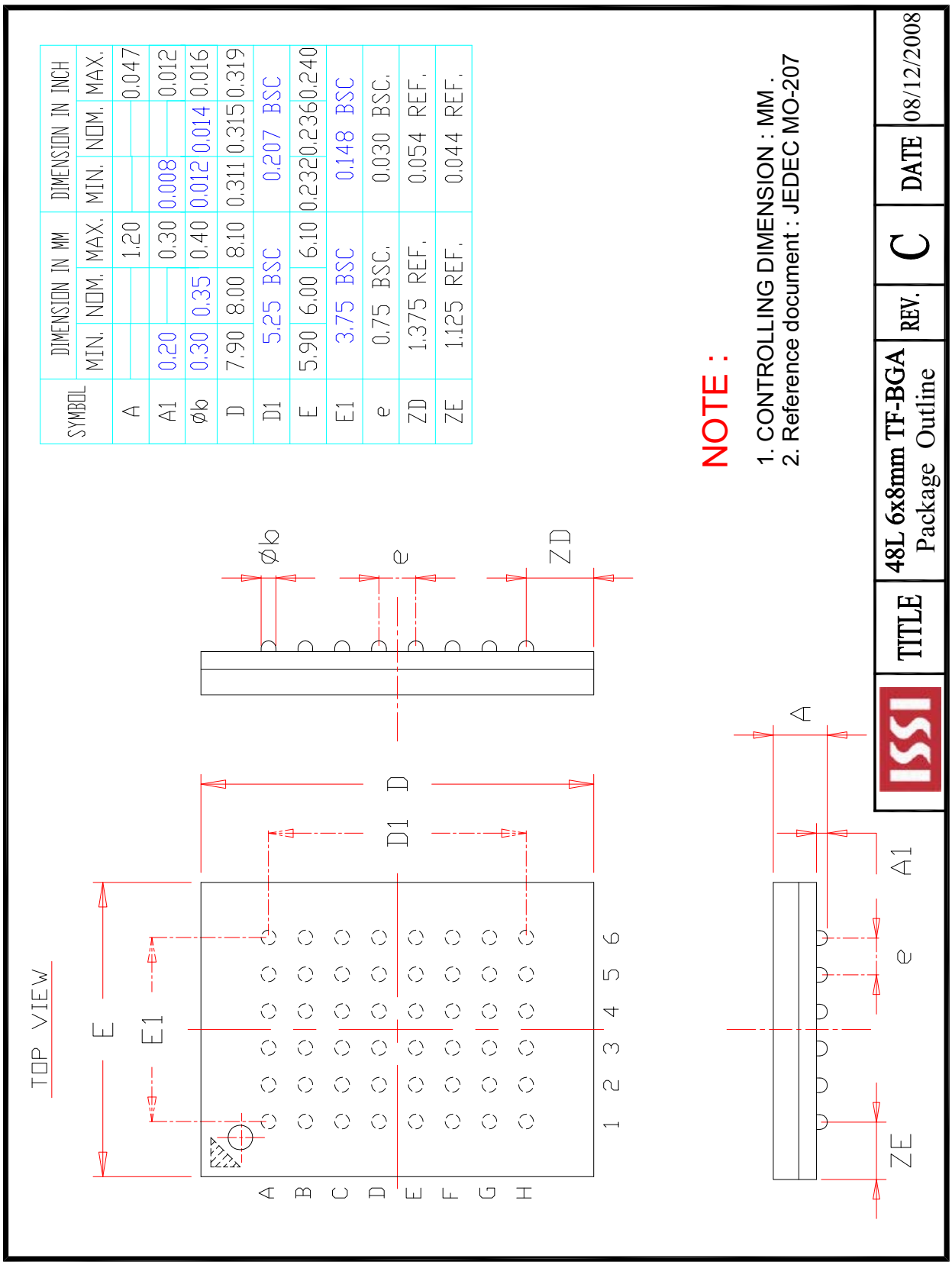
## ORDERING INFORMATION (LOW POWER)

### Industrial Range: -40°C to +85°C
### Voltage Range: 2.4V to 3.6V

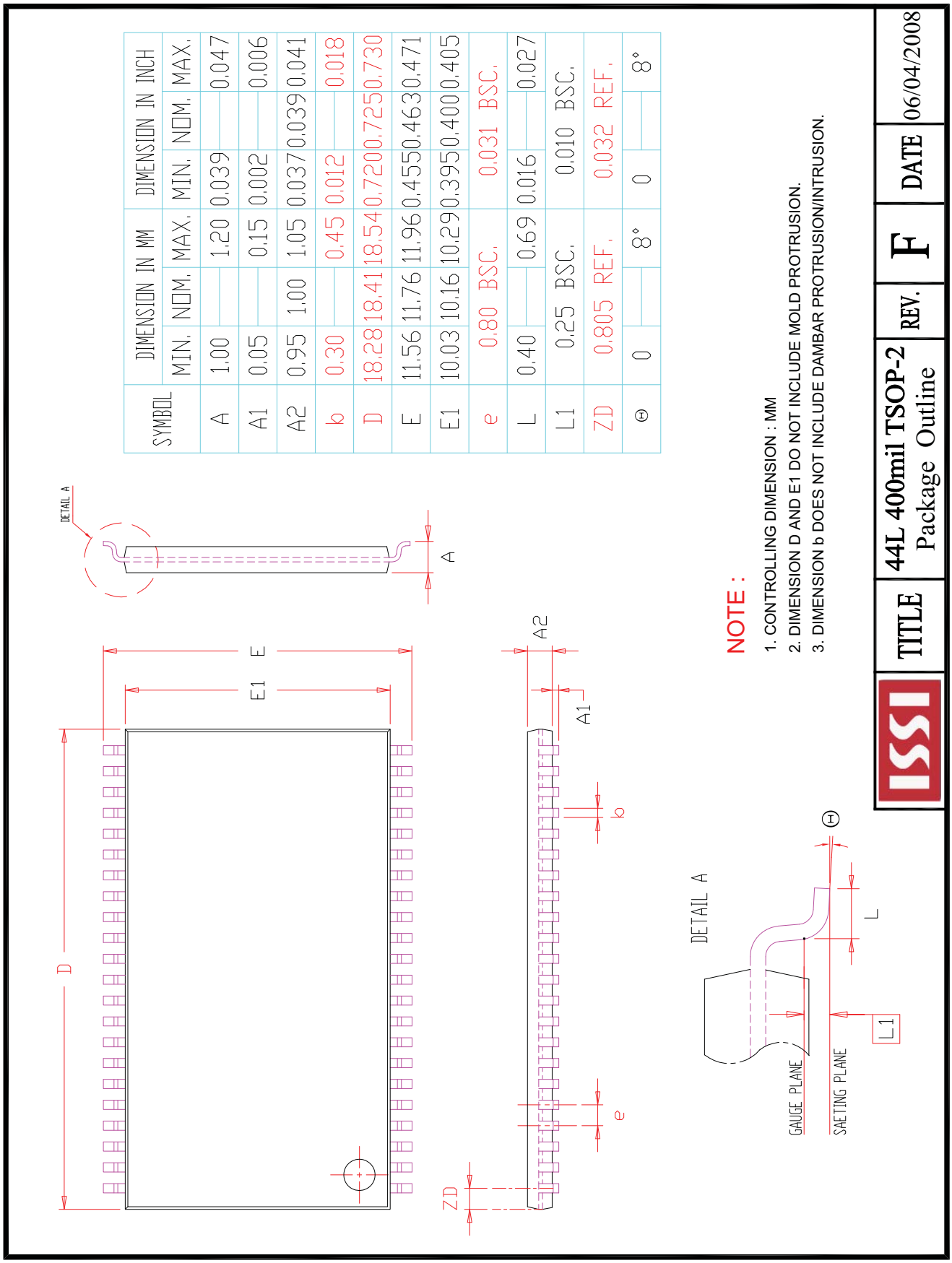
| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 25 | IS61WV25616BLS-25TLI | TSOP (Type II), Lead-free |

### Industrial Range: -40°C to +85°C
### Voltage Range: 1.65V to 2.2V

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 45 | IS61WV25616ALS-45TLI | TSOP (Type II), Lead-free |


SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.20 — 0.30 0.008 — 0.012
øb 0.30 0.35 0.40 0.012 0.014 0.016
D 7.90 8.00 8.10 0.311 0.315 0.319
D1 5.25 BSC 0.207 BSC
E 5.90 6.00 6.10 0.232 0.236 0.240
E1 3.75 BSC 0.148 BSC
e 0.75 BSC. 0.030 BSC.
ZD 1.375 REF. 0.054 REF.
ZE 1.125 REF. 0.044 REF.
NOTE :
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207
TOP VIEW
A B C D E F G H
1 2 3 4 5 6
E
E1
D
D1
øb
e
ZD
A
A1
e
ZE
TITLE
48L 6x8mm TF-BGA
Package Outline
REV.
C
DATE
08/12/2008

| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | — | 1.20 | 0.039 | — | 0.047 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.30 | — | 0.45 | 0.012 | — | 0.018 |
| D | 18.28 | 18.41 | 18.54 | 0.720 | 0.725 | 0.730 |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | 0.80 BSC, | | | 0.031 BSC, | | |
| L | 0.40 | — | 0.69 | 0.016 | — | 0.027 |
| L1 | 0.25 BSC, | | | 0.010 BSC, | | |
| ZD | 0.805 REF, | | | 0.032 REF, | | |
| θ | 0 | — | 8° | 0 | — | 8° |



LifeElectronics
Живое партнерство

**ООО «ЛайфЭлектроникс»** **“LifeElectronics” LLC**

*ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703*

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- *Приемлемые сроки поставки, возможна ускоренная поставка.*
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- *Комплексную поставку.*
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*Тел: +7 (812) 336 43 04 (многоканальный)*
*Email: org@lifeelectronics.ru*

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