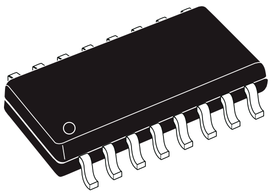
L6599E

Improved high-voltage resonant controller

Datasheet — production data

Features

- 50% duty cycle, variable frequency control of resonant half-bridge
- High-accuracy oscillator
- Up to 500 kHz operating frequency
- Two-level OCP: frequency-shift and latched shutdown
- Interface with PFC controller
- Latched disable input
- Burst-mode operation at light load
- Input for power-ON/OFF sequencing or brownout protection
- Non-linear soft-start for monotonic output voltage rise
- 600 V-rail compatible high-side gate driver with integrated bootstrap diode and high dv/dt immunity
- -300/800 mA high-side and low-side gate drivers with UVLO pull-down
- SO16N package



SO16 Narrow

Application

- LCD and PDP TV
- Desktop PC, entry-level server
- Telecom SMPS
- High efficiency industrial SMPS
- AC-DC adapter, open frame SMPS

Table 1. Device summary

Order codes	Package	Packaging
L6599ED	SO16N	Tube
L6599EDTR	SO16N	Tape and reel

This is information on a product in full production.

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1 Description

The L6599E is an improved revision of the previous L6599. It is a double-ended controller specific for the series-resonant half-bridge topology. It provides 50% complementary duty cycle: the high-side switch and the low-side switch are driven ON/OFF 180° out-of-phase for exactly the same time. Output voltage regulation is obtained by modulating the operating frequency. A fixed dead-time inserted between the turn-off of one switch and the turn-on of the other one guarantees soft-switching and enables high-frequency operation.

To drive the high-side switch with the bootstrap approach, the IC incorporates a high-voltage floating structure able to withstand more than 600 V with a synchronous-driven high-voltage DMOS that replaces the external fast-recovery bootstrap diode.

The IC enables the designer to set the operating frequency range of the converter by means of an externally programmable oscillator.

At start-up, to prevent uncontrolled inrush current, the switching frequency starts from a programmable maximum value and progressively decays until it reaches the steady-state value determined by the control loop. This frequency shift is non linear to minimize output voltage overshoots; its duration is programmable as well.

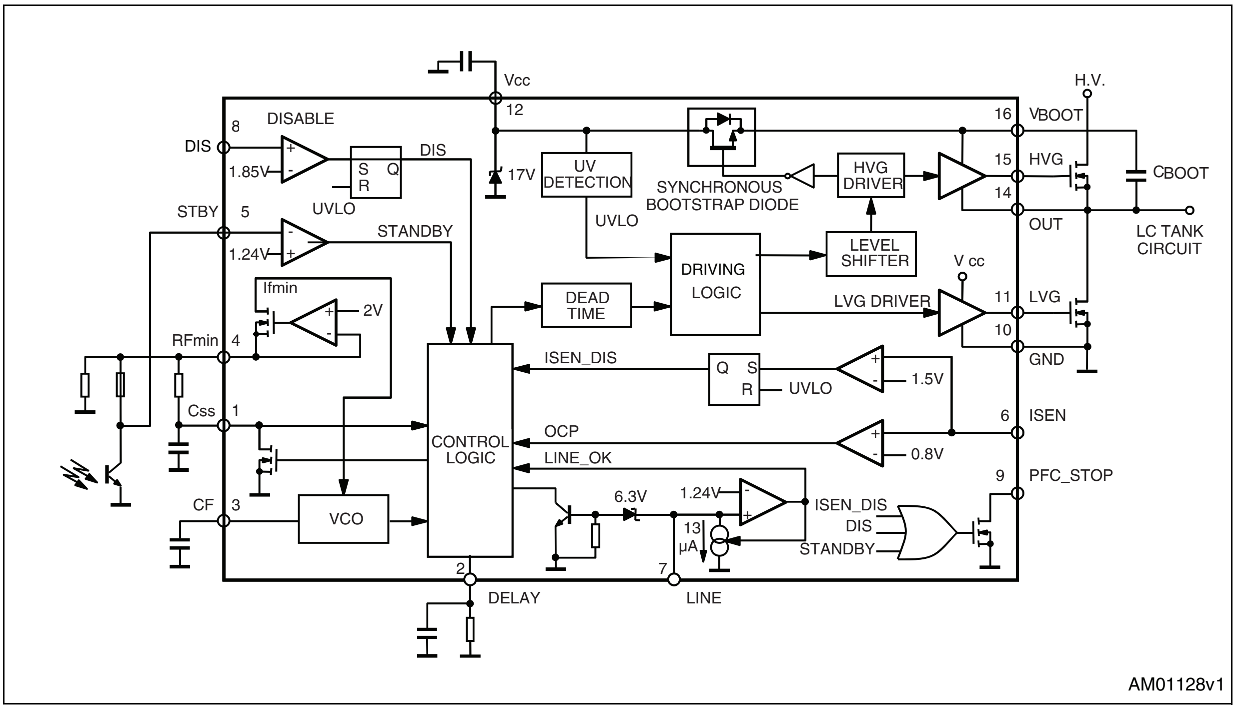
At light load the IC may enter a controlled burst-mode operation that keeps the converter input consumption to a minimum.

IC’s functions include a not-latched active-low disable input with current hysteresis useful for power sequencing or for brownout protection, a current sense input for OCP with frequency shift and delayed shutdown with automatic restart. A higher level OCP latches off the IC if the first-level protection is not sufficient to control the primary current. Their combination offers complete protection against overload and short circuits. An additional latched disable input (DIS) allows easy implementation of OTP and/or OVP.

An interface with the PFC controller is provided that enables to switch off the pre-regulator during fault conditions, such as OCP shutdown and DIS high, or during burst-mode operation.

2 Block diagram

Figure 1. Block diagram



3 Pin connection

Figure 2. Pin connection (top view)

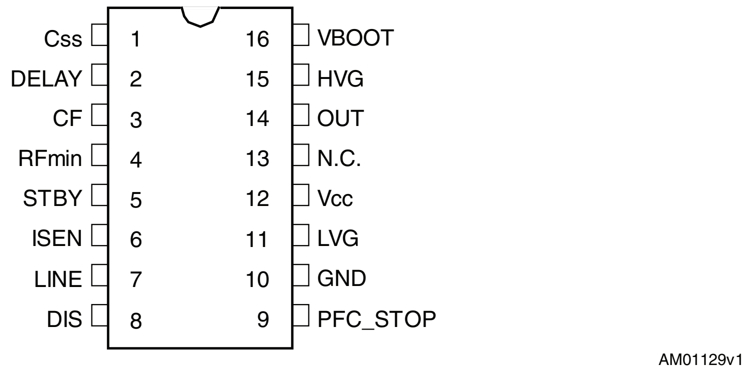


Table 2. Pin description

Pin N#	Type	Function
1	Css	Soft-start. This pin connects an external capacitor to GND and a resistor to RFmin (pin 4) that set both the maximum oscillator frequency and the time constant for the frequency shift that occurs as the chip starts up (soft-start). An internal switch discharges this capacitor every time the chip turns off (Vcc < UVLO, LINE < 1.24 V or > 6 V, DIS > 1.85 V, ISEN > 1.5 V, DELAY > 2 V) to make sure it will be soft-started next, and when the voltage on the current sense pin (ISEN) exceeds 0.8 V, as long as it stays above 0.75 V.
2	DELAY	Delayed shutdown upon overcurrent. A capacitor and a resistor are connected from this pin to GND to set the maximum duration of an overcurrent condition before the IC stops switching and the delay after which the IC restarts switching. Every time the voltage on the ISEN pin exceeds 0.8 V the capacitor is charged by an internal 150 µA current generator and is slowly discharged by the external resistor. If the voltage on the pin reaches 2 V, the soft start capacitor is completely discharged so that the switching frequency is pushed to its maximum value and the 150 µA is kept always on. As the voltage on the pin exceeds 3.5 V the IC stops switching and the internal generator is turned off, so that the voltage on the pin will decay because of the external resistor. The IC will be soft-restarted as the voltage drops below 0.3 V. In this way, under short circuit conditions, the converter will work intermittently with very low input average power.
3	CF	Timing capacitor. A capacitor connected from this pin to GND is charged and discharged by internal current generators programmed by the external network connected to pin 4 (RFmin) and determines the switching frequency of the converter.

Table 2. Pin description (continued)

Pin N#	Type	Function
4	RFmin	Minimum oscillator frequency setting. This pin provides a precise 2 V reference and a resistor connected from this pin to GND defines a current that is used to set the minimum oscillator frequency. To close the feedback loop that regulates the converter output voltage by modulating the oscillator frequency, the phototransistor of an optocoupler will be connected to this pin through a resistor. The value of this resistor will set the maximum operating frequency. An R-C series connected from this pin to GND sets frequency shift at start-up to prevent excessive energy inrush (soft-start).
5	STBY	Burst-mode operation threshold. The pin senses some voltage related to the feedback control, which is compared to an internal reference (1.24 V). If the voltage on the pin is lower than the reference, the IC enters an idle state and its quiescent current is reduced. The chip restarts switching as the voltage exceeds the reference by 50 mV. Soft-start is not invoked. This function realizes burst-mode operation when the load falls below a level that can be programmed by properly choosing the resistor connecting the optocoupler to pin RFmin (see block diagram). Tie the pin to RFmin if burst-mode is not used.
6	ISEN	Current sense input. The pin senses the primary current though a sense resistor or a capacitive divider for lossless sensing. This input is not intended for a cycle-by-cycle control; hence the voltage signal must be filtered to get average current information. As the voltage exceeds a 0.8 V threshold (with 50 mV hysteresis), the soft-start capacitor connected to pin 1 is internally discharged: the frequency increases hence limiting the power throughput. Under output short circuit, this normally results in a nearly constant peak primary current. This condition is allowed for a maximum time set at pin 2. If the current keeps on building up despite this frequency increase, a second comparator referenced at 1.5 V latches the device off and brings its consumption almost to a “before start-up” level. The information is latched and it is necessary to recycle the supply voltage of the IC to enable it to restart: the latch is removed as the voltage on the Vcc pin goes below the UVLO threshold. Tie the pin to GND if the function is not used.
7	LINE	Line sensing input. The pin is to be connected to the high-voltage input bus with a resistor divider to perform either AC or DC (in systems with PFC) brownout protection. A voltage below 1.24 V shuts down (not latched) the IC, lowers its consumption and discharges the soft-start capacitor. IC’s operation is re-enabled (soft-started) as the voltage exceeds 1.24 V. The comparator is provided with current hysteresis: an internal 13 µA current generator is ON as long as the voltage applied at the pin is below 1.24 V and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND to reduce noise pick-up. The voltage on the pin is top-limited by an internal zener. Activating the zener causes the IC to shut down (not latched). Bias the pin between 1.24 and 6 V if the function is not used.
8	DIS	Latched device shutdown. Internally the pin connects a comparator that, when the voltage on the pin exceeds 1.85 V, shuts the IC down and brings its consumption almost to a “before start-up” level. The information is latched and it is necessary to recycle the supply voltage of the IC to enable it to restart: the latch is removed as the voltage on the Vcc pin goes below the UVLO threshold. Tie the pin to GND if the function is not used.

Table 2. Pin description (continued)

Pin N#	Type	Function
9	PFC_STOP	Open-drain ON/OFF control of PFC controller. This pin, normally open, is intended for stopping the PFC controller, for protection purpose or during burst-mode operation. It goes low when the IC is shut down by DIS>1.85 V, ISEN > 1.5 V, LINE > 6 V and STBY < 1.24 V. The pin is pulled low also when the voltage on pin DELAY exceeds 2 V and goes back open as the voltage falls below 0.3 V. During UVLO, it is open. Leave the pin unconnected if not used.
10	GND	Chip ground. Current return for both the low-side gate-drive current and the bias current of the IC. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
11	LVG	Low-side gate-drive output. The driver is capable of 0.3 A min. source and 0.8 A min. sink peak current to drive the lower MOSFET of the half-bridge leg. The pin is actively pulled to GND during UVLO.
12	Vcc	Supply voltage of both the signal part of the IC and the low-side gate driver. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.
13	N.C.	High-voltage spacer. The pin is not internally connected to isolate the high-voltage pin and ease compliance with safety regulations (creepage distance) on the PCB.
14	OUT	High-side gate-drive floating ground. Current return for the high-side gate-drive current. Layout carefully the connection of this pin to avoid too large spikes below ground.
15	HVG	High-side floating gate-drive output. The driver is capable of 0.3 A min. source and 0.8 A min. sink peak current to drive the upper MOSFET of the half-bridge leg. A resistor internally connected to pin 14 (OUT) ensures that the pin is not floating during UVLO.
16	VBOOT	High-side gate-drive floating supply voltage. The bootstrap capacitor connected between this pin and pin 14 (OUT) is fed by an internal synchronous bootstrap diode driven in-phase with the low-side gate-drive. This patented structure replaces the normally used external diode.

4 Electrical data

4.1 Absolute maximum ratings

Table 3. Absolute maximum rating

Symbol	Pin	Parameter	Value	Unit
V_{BOOT}	16	Floating supply voltage	-1 to 618	V
V_{OUT}	14	Floating ground voltage	-3 to V_{BOOT}-18	V
dV_{OUT} /dt	14	Floating ground max. slew rate	50	V/ns
Vcc	12	IC supply voltage (Icc = 25 mA)	Self-limited	V
V_{PFC_STOP}	9	Maximum voltage (pin open)	-0.3 to Vcc	V
I_{PFC_STOP}	9	Maximum sink current (pin low)	Self-limited	A
$V_{LINEmax}$	7	Maximum pin voltage (Ipin ≤1 mA)	Self-limited	V
I_{RFmin}	4	Maximum source current	2	mA
---	1 to 6, 8	Analog inputs and Outputs	-0.3 to 5	V
Ptot		Power dissipation @T_A = 70 °C (DIP16)	1	W
		Power dissipation @T_A = 50 °C (SO16)	0.83	
Tj		Junction temperature operating range	-40 to 150	°C
Tstg		Storage temperature	-55 to 150	°C

Note: ESD immunity for pins 14, 15 and 16 is guaranteed up to 900 V.

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Max. thermal resistance junction to ambient (DIP16)	80	°C/W
	Max. thermal resistance junction to ambient (SO16)	120	°C/W

5 Electrical characteristics

T_J = 0 to 105 °C, Vcc = 15 V, VBOOT = 15 V, C_{HVG} = C_{LVG} = 1 nF; C_F = 470 pF; R_{RFmin} = 12 kΩ; unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IC supply voltage						
Vcc	Operating range	After device turn-on	8.85		16	V
Vcc_{On}	Turn-on threshold	Voltage rising	10	10.7	11.4	V
Vcc_{Off}	Turn-off threshold	Voltage falling	7.45	8.15	8.85	V
Hys	Hysteresis			2.55		V
V_Z	Vcc clamp voltage	Iclamp = 15 mA	16	17	17.9	V
Supply current						
$I_{start-up}$	Start-up current	Before device turn-on Vcc = Vcc_{On}- 0.2 V		200	250	µA
I_q	Quiescent current	Device on, V_{STBY} = 1 V		1.5	2	mA
I_{op}	Operating current	Device on, V_{STBY} = V_{RFmin}		3.5	5	mA
I_q	Residual consumption	V_{DIS} > 1.85 V or V_{DELAY} > 3.5 V or V_{LINE} < 1.24 V or V_{LINE} = V_{clamp}		300	400	µA
High-side floating gate-drive supply						
I_{LKBOOT}	V_{BOOT} pin leakage current	V_{BOOT} = 580 V			5	µA
I_{LKOUT}	OUT pin leakage current	V_{OUT} = 562 V			5	µA
$R_{DS(on)}$	Synchronous bootstrap diode on-resistance	V_{LVG} = HIGH		150		Ω
Overcurrent comparator						
I_{ISEN}	Input bias current	V_{ISEN} = 0 to $V_{ISENdis}$			-1	µA
t_{LEB}	Leading edge blanking	After V_{HVG} and V_{LVG} low-to-high transition		250		ns
V_{ISENx}	Frequency shift threshold	Voltage rising (1)	0.77	0.8	0.83	V
	Hysteresis	Voltage falling		50		mV
$V_{ISENdis}$	Latch off threshold	Voltage rising (1)	1.45	1.5	1.55	V
$td_{(H-L)}$	Delay to output			300	400	ns
Line sensing						
Vth	Threshold voltage	Voltage rising or falling (1)	1.2	1.24	1.28	V
I_{Hys}	Current hysteresis	V_{LINE} = 1.1 V	10	13	16	µA
V_{clamp}	Clamp level	I_{LINE} = 1 mA	6		8	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DIS function						
I_{DIS}	Input bias current	V_{DIS} = 0 to Vth			-1	µA
Vth	Disable threshold	Voltage rising (1)	1.78	1.85	1.92	V
Oscillator						
D	Output duty cycle	Both HVG and LVG	48	50	52	%
f_{osc}	Oscillation frequency		58.2	60	61.8	kHz
		R_{RFmin} = 2.7 kΩ	240	250	260	
T_D	Dead-time	Between HVG and LVG	0.2	0.3	0.4	µs
V_{CFp}	Peak value			3.9		V
V_{CFv}	Valley value			0.9		V
V_{REF}	Voltage reference at pin 4	(1)	1.93	2	2.07	V
		I_{REF} = - 2 mA (1)	1.93	2	2.07	
K_M	Current mirroring ratio			1		A/A
PFC_STOP function						
I_{leak}	High level leakage current	V_{PFC_STOP} =Vcc, V_{DIS} = 0 V			1	µA
R_{PFC_STOP}	ON-state resistance	I_{PFC_STOP} = 1 mA, V_{DIS} = 1.5 V		130	200	Ω
V_L	Low saturation level	I_{PFC_STOP} = 1 mA, V_{DIS} = 1.5 V			0.2	V
Soft-start function						
I_{leak}	Open-state current	V(Css) = 2 V			0.5	µA
R	Discharge resistance	V_{ISEN} > V_{ISENx}		120		Ω
Standby function						
I_{DIS}	Input bias current	V_{DIS} = 0 to Vth			-1	µA
Vth	Disable threshold	Voltage falling (1)	1.2	1.24	1.28	V
Hys	Hysteresis	Voltage rising		50		mV
Delayed shutdown function						
I_{leak}	Open-state current	V(DELAY) = 0			0.5	µA
I_{CHARGE}	Charge current	V_{DELAY} = 1 V, V_{ISEN} = 0.85 V	100	150	200	µA
Vth_1	Threshold for forced operation at max. frequency	Voltage rising (1)	1.98	2.05	2.12	V
Vth_2	Shutdown threshold	Voltage rising (1)	3.35	3.5	3.65	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vth_3	Restart threshold	Voltage falling [1]	0.3	0.33	0.36	V
Low-side gate driver (voltages referred to GND)						
V_{LVGL}	Output low voltage	I_{sink} = 200 mA			1.5	V
V_{LVGH}	Output high voltage	I_{source} = 5 mA	12.8	13.3		V
$I_{sourcepk}$	Peak source current		-0.3			A
I_{sinkpk}	Peak sink current		0.8			A
t_f	Fall time			30		ns
t_r	Rise time			60		ns
	UVLO saturation	Vcc= 0 to Vcc_{On}, I_{sink} = 2 mA			1.1	V
High-side gate driver (voltages referred to OUT)						
V_{LVGL}	Output low voltage	I_{sink} = 200 mA			1.5	V
V_{LVGH}	Output high voltage	I_{source} = 5 mA	12.8	13.3		V
$I_{sourcepk}$	Peak source current		-0.3			A
I_{sinkpk}	Peak sink current		0.8			A
t_f	Fall time			30		ns
t_r	Rise time			60		ns
	HVG-OUT pull-down			25		kΩ

1. Values tracking each other

6 Typical electrical performance

Figure 3. Device consumption vs supply voltage

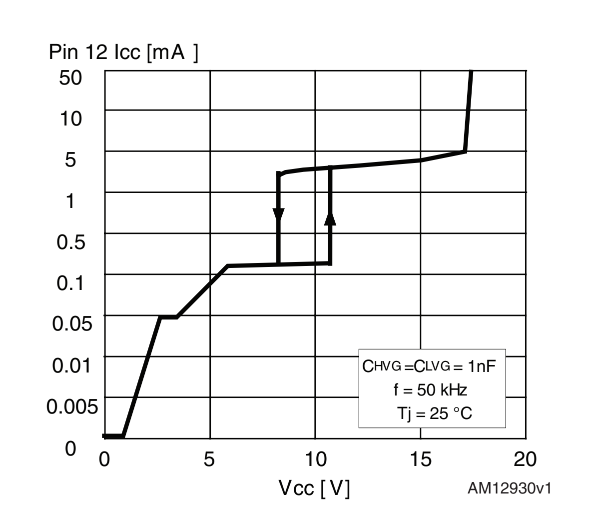


Figure 4. IC consumption vs junction temperature

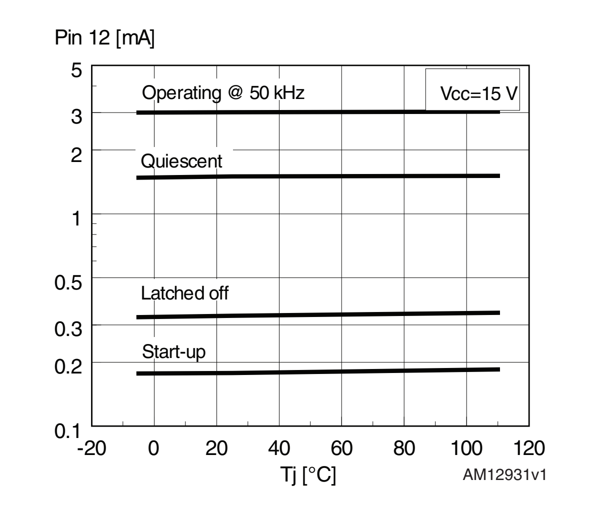


Figure 5. V_{CC} clamp voltage vs junction temperature

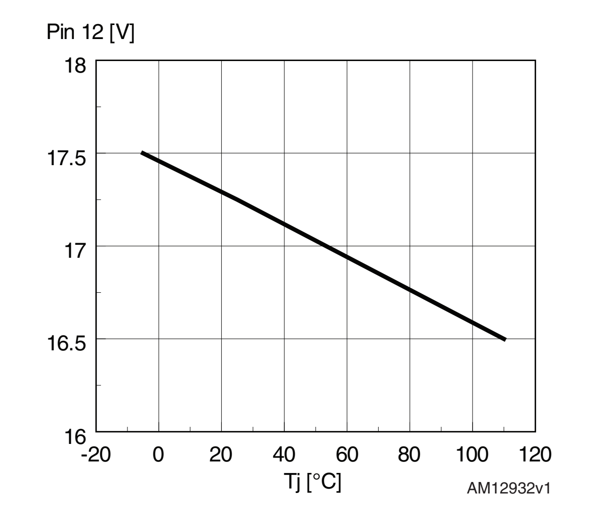


Figure 6. UVLO thresholds vs junction temperature

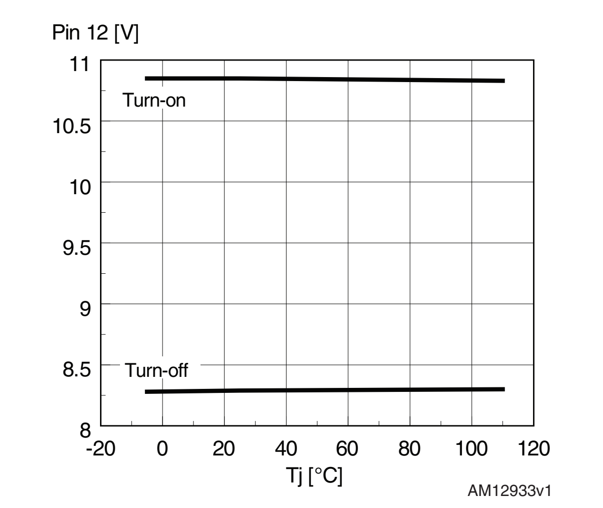


Figure 7. Oscillator frequency vs junction temperature

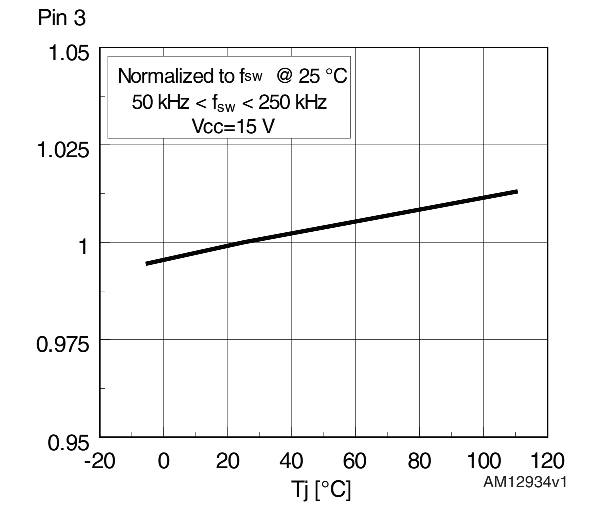


Figure 8. Dead-time vs junction temperature

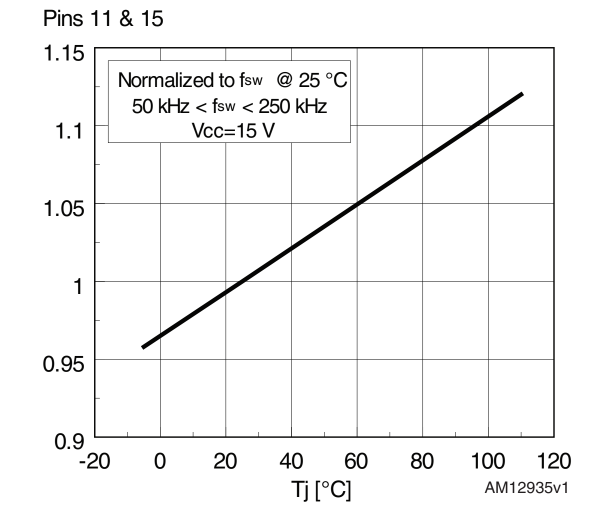


Figure 9. Oscillator frequency vs timing components

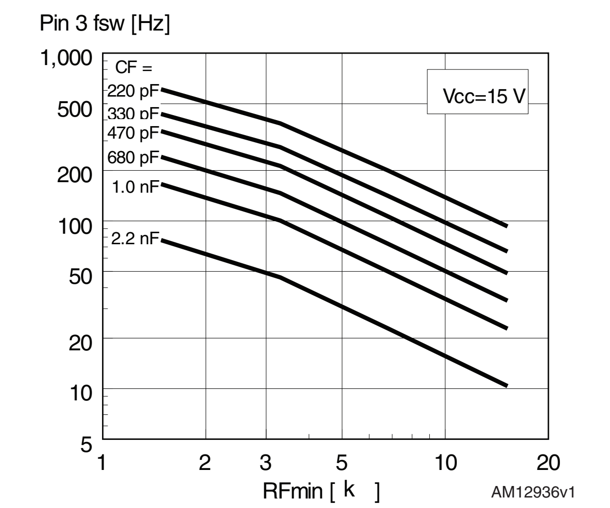


Figure 10. Oscillator ramp vs junction temperature

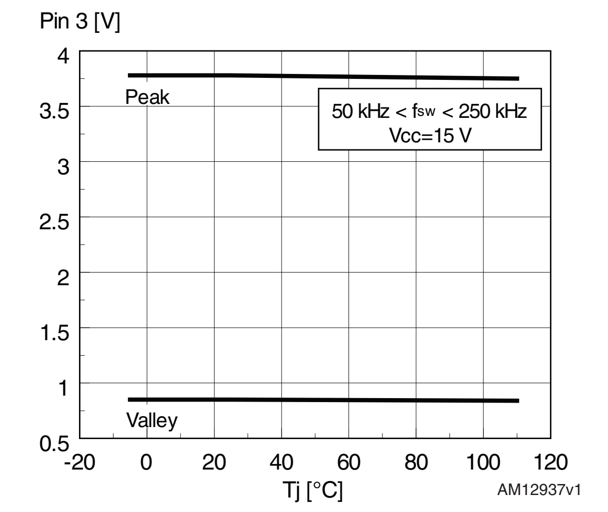


Figure 11. Reference voltage vs junction temperature

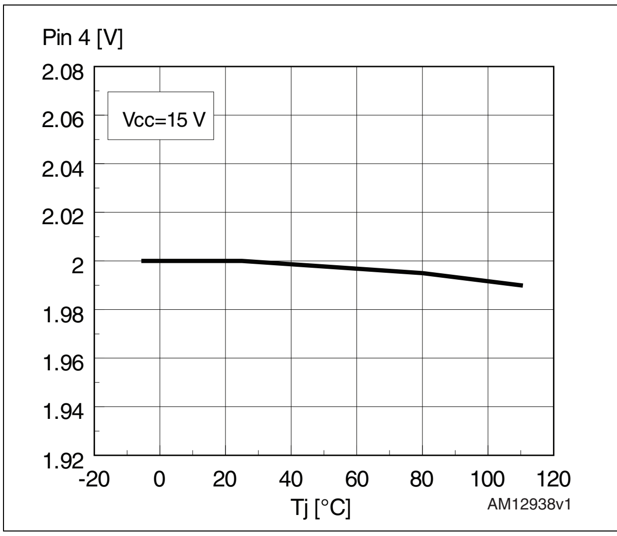


Figure 12. Current mirroring ratio vs junction temperature

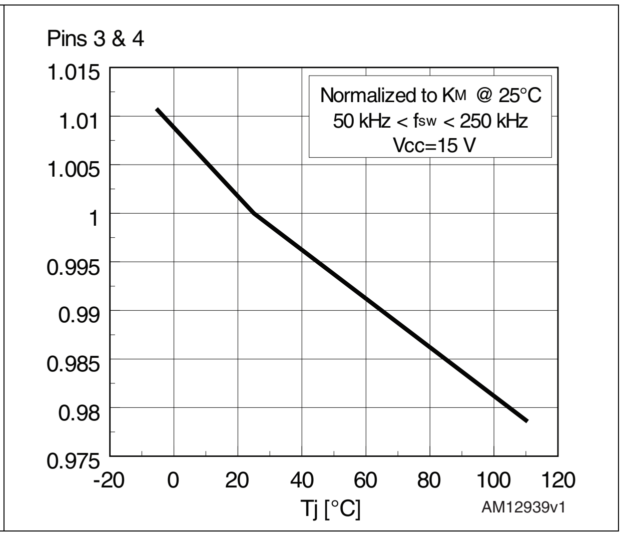


Figure 13. OCP delay source current vs junction temperature

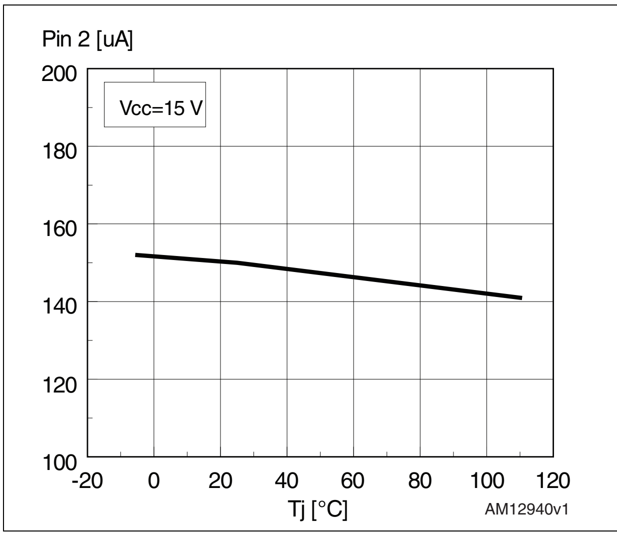


Figure 14. OCP delay thresholds vs junction temperature

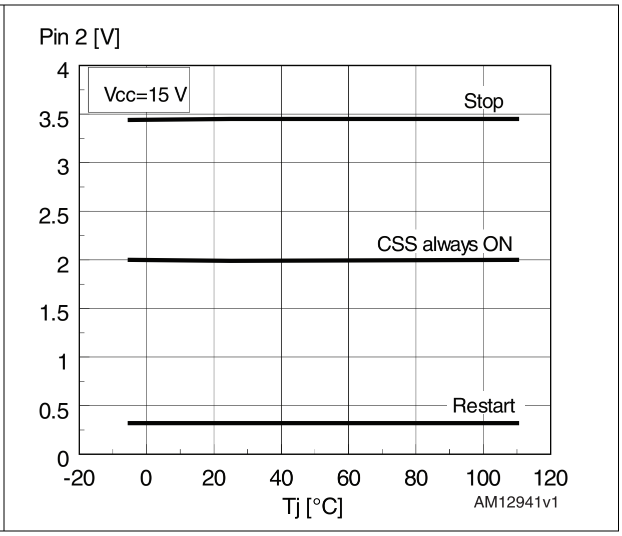


Figure 15. Standby thresholds vs junction temperature

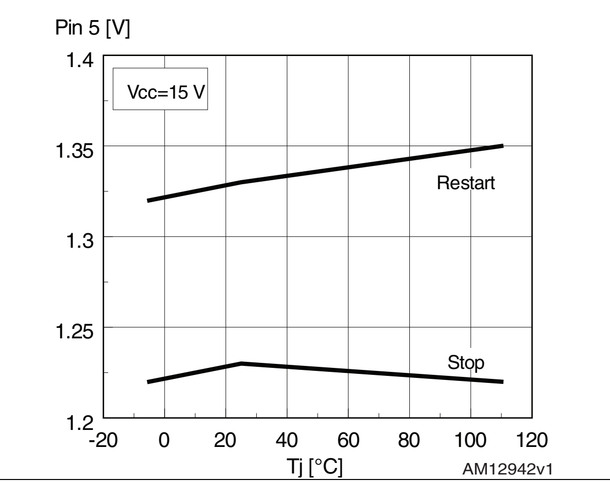


Figure 16. Current sense thresholds vs junction temperature

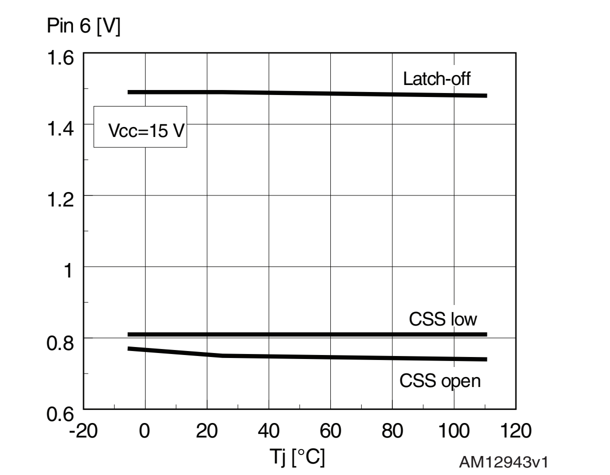


Figure 17. Line thresholds vs junction temperature

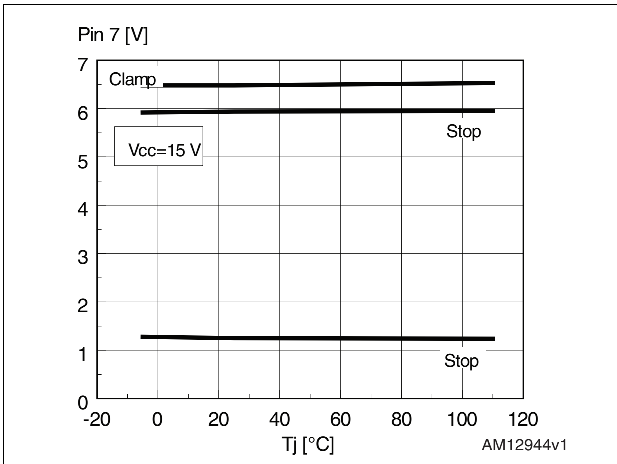


Figure 18. Line source current vs junction temperature

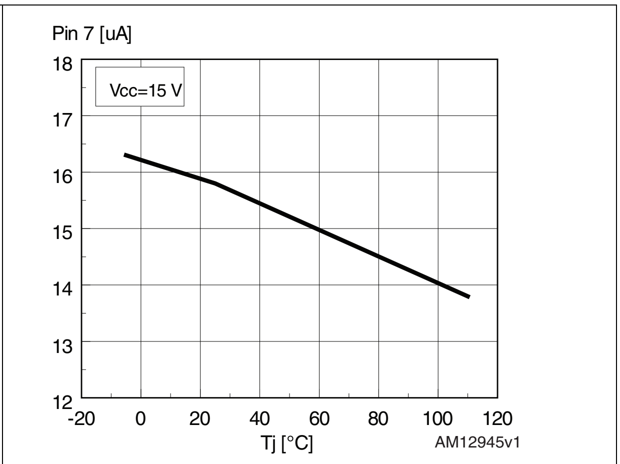
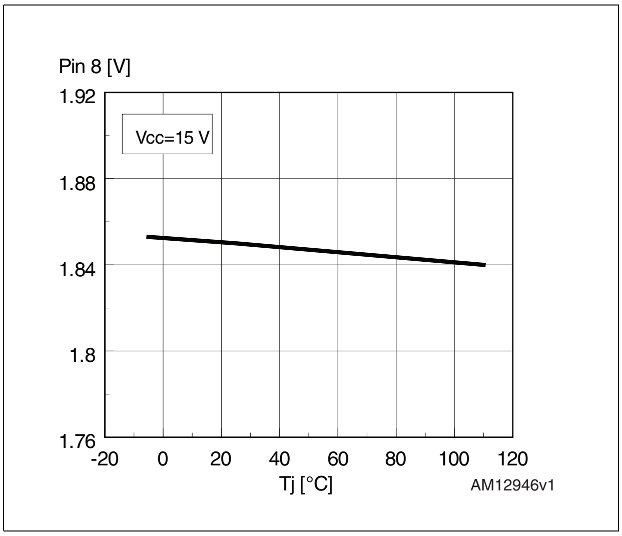


Figure 19. Latched disable threshold vs junction temperature



7 Application information

The L6599E is an advanced double-ended controller specific for resonant half-bridge topology (see *Figure 21.*). In these converters the switches (MOSFETs) of the half-bridge leg are alternately switched on and off (180° out-of-phase) for exactly the same time. This is commonly referred to as operation at “50% duty cycle”, although the real duty cycle, that is the ratio of the on-time of either switch to the switching period, is actually less than 50%. The reason is that there is an internally fixed dead-time T_D inserted between the turn-off of either MOSFET and the turn-on of the other one, where both MOSFETs are off. This dead-time is essential in order for the converter to work correctly: it will ensure soft-switching and enable high-frequency operation with high efficiency and low EMI emissions.

To perform converter's output voltage regulation the device is able to operate in different modes (*Figure 20*), depending on the load conditions:

1. Variable frequency at heavy and medium/light load. A relaxation oscillator (see *Section 7.1: Oscillator* for more details) generates a symmetrical triangular waveform, which MOSFETs' switching is locked to. The frequency of this waveform is related to a current that will be modulated by the feedback circuitry. As a result, the tank circuit driven by the half-bridge will be stimulated at a frequency dictated by the feedback loop to keep the output voltage regulated, thus exploiting its frequency-dependent transfer characteristics.
2. Burst-mode control with no or very light load. When the load falls below a value, the converter will enter a controlled intermittent operation, where a series of a few switching cycles at a nearly fixed frequency are spaced out by long idle periods where both MOSFETs are in OFF-state. A further load decrease will be translated into longer idle periods and then in a reduction of the average switching frequency. When the converter is completely unloaded, the average switching frequency can go down even to few hundred hertz, thus minimizing magnetizing current losses as well as all frequency-related losses and making it easier to comply with energy saving recommendations.

Figure 20. Multi-mode operation of the L6599E

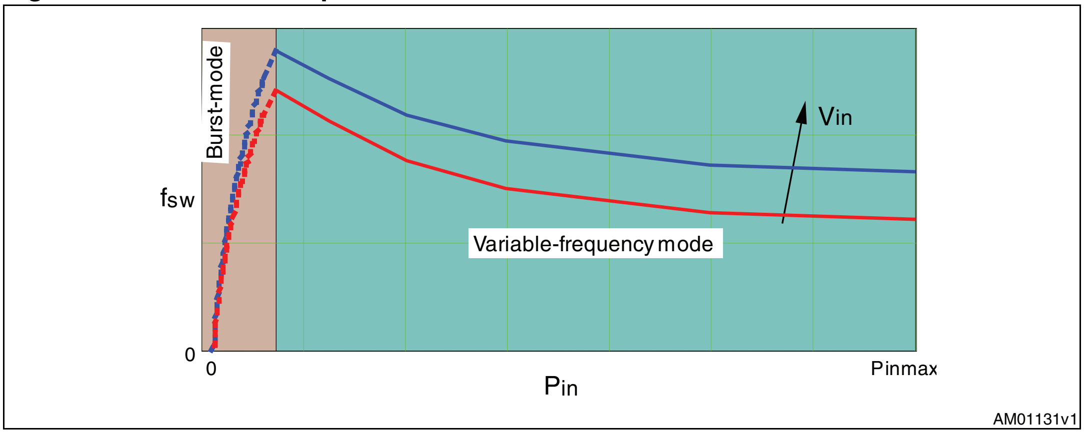
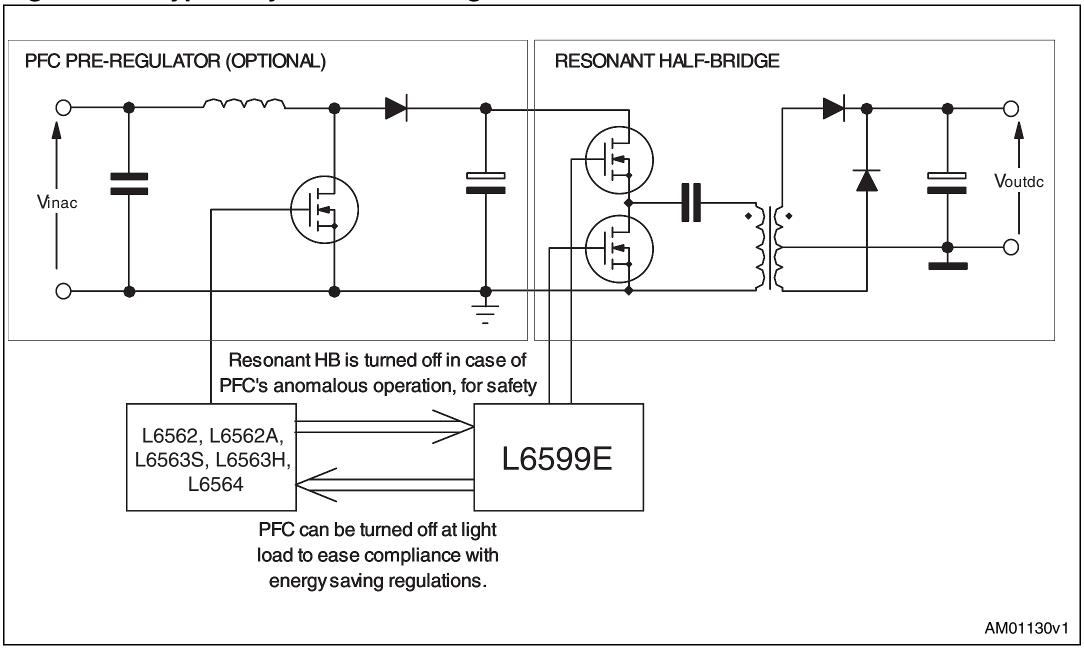


Figure 21. Typical system block diagram



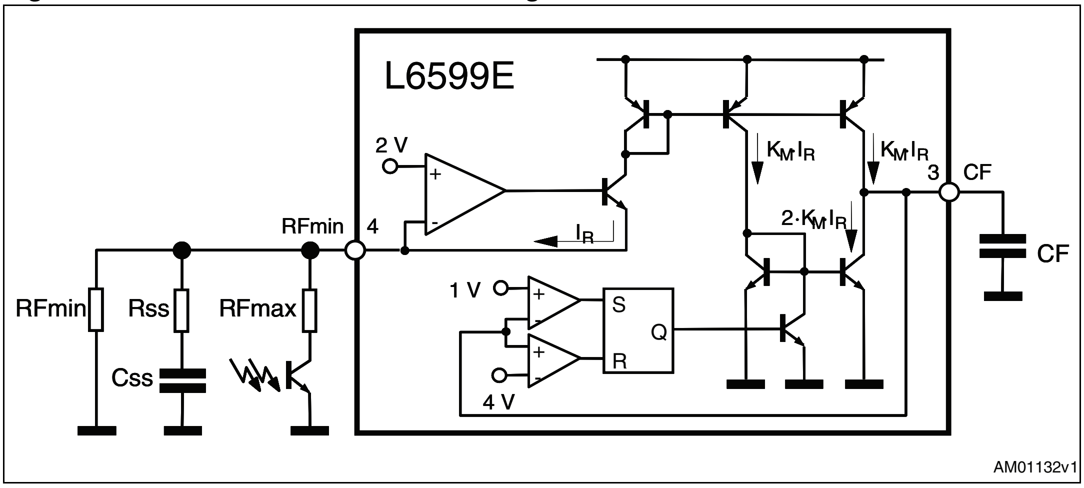
7.1 Oscillator

The oscillator is programmed externally by means of a capacitor (CF), connected from pin 3 (CF) to ground, that will be alternately charged and discharged by the current defined with the network connected to pin 4 (RFmin). The pin provides an accurate 2 V reference with about 2 mA source capability and the higher the current sourced by the pin is, the higher the oscillator frequency will be. The block diagram of *Figure 22* shows a simplified internal circuit that explains the operation.

The network that loads the RFmin pin generally comprises three branches:

1. A resistor RFmin connected between the pin and ground that determines the minimum operating frequency;
2. a resistor RFmax connected between the pin and the collector of the (emitter-grounded) phototransistor that transfers the feedback signal from the secondary side back to the primary side; while in operation, the phototransistor will modulate the current through this branch - hence modulating the oscillator frequency - to perform output voltage regulation; the value of RFmax determines the maximum frequency the half-bridge will be operated at when the phototransistor is fully saturated;
3. an R-C series circuit (CSS+RSS) connected between the pin and ground that enables to set up a frequency shift at start-up (see *Section 7.3: Soft-start*). Note that the contribution of this branch is zero during steady-state operation.

Figure 22. Oscillator's internal block diagram



The following approximate relationships hold for the minimum and the maximum oscillator frequency respectively:

Equation 1

$$f_{min} = \frac{1}{3 \cdot CF \cdot RF_{min}}; \qquad f_{max} = \frac{1}{3 \cdot CF \cdot (RF_{min} // RF_{max})}$$

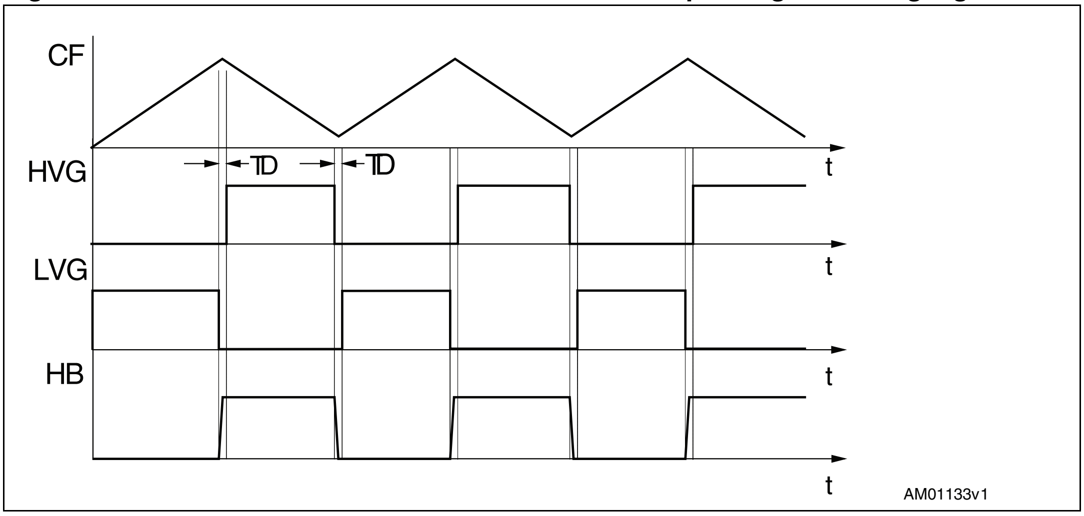
After fixing CF in the hundred pF or in the nF (consistently with the maximum source capability of the RFmin pin and trading this off against the total consumption of the device), the value of RF_{min} and RF_{max} will be selected so that the oscillator frequency is able to cover the entire range needed for regulation, from the minimum value f_{min} (at minimum input voltage and maximum load) to the maximum value f_{max} (at maximum input voltage and minimum load):

Equation 2

$$RF_{min} = \frac{1}{3 \cdot CF \cdot f_{min}}; \qquad RF_{max} = \frac{RF_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

A different selection criterion will be given for R_{Fmax} in case burst-mode operation at no-load will be used (see *Section 7.2: Operation at no load or very light load*).

Figure 23. Oscillator waveforms and their relationship with gate-driving signals



In *Figure 23* the timing relationship between the oscillator waveform and the gate-drive signal, as well as the swinging node of the half-bridge leg (HB) is shown. Note that the low-side gate-drive is turned on while the oscillator's triangle is ramping up and the high-side gate-drive is turned on while the triangle is ramping down. In this way, at start-up, or as the IC resumes switching during burst-mode operation, the low-side MOSFET will be switched on first to charge the bootstrap capacitor. As a result, the bootstrap capacitor will always be charged and ready to supply the high-side floating driver.

7.2 Operation at no load or very light load

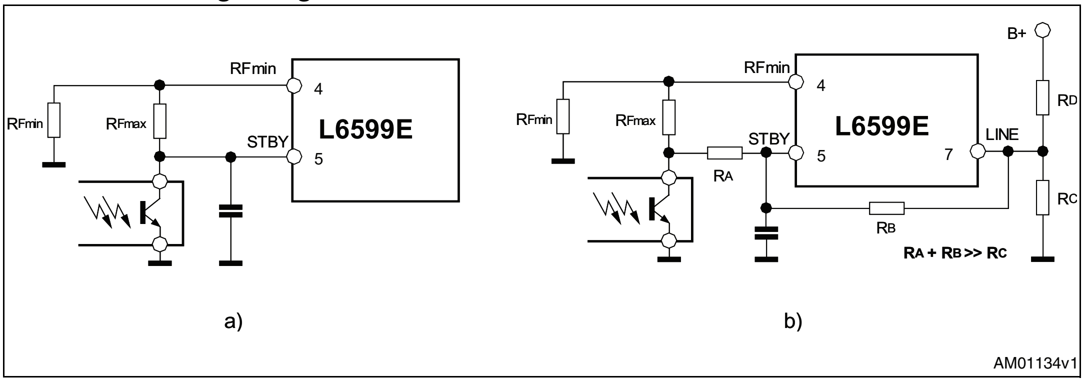
When the resonant half-bridge is lightly loaded or unloaded at all, its switching frequency will be at its maximum value. To keep the output voltage under control in these conditions and to avoid losing soft-switching, there must be some significant residual current flowing through the transformer's magnetizing inductance. This current, however, produces some associated losses that prevent converter's no-load consumption from achieving very low values.

To overcome this issue, the L6599E enables the designer to make the converter operate intermittently (burst-mode operation), with a series of a few switching cycles spaced out by long idle periods where both MOSFETs are in OFF-state, so that the average switching frequency can be substantially reduced. As a result, the average value of the residual magnetizing current and the associated losses will be considerably cut down, thus facilitating the converter to comply with energy saving recommendations.

The L6599E can be operated in burst-mode by using pin 5 (STBY): if the voltage applied to this pin falls below 1.24 V the IC will enter an idle state where both gate-drive outputs are low, the oscillator is stopped, the soft-start capacitor CSS keeps its charge and only the 2 V reference at RFmin pin stays alive to minimize IC's consumption and Vcc capacitor's discharge. The IC will resume normal operation as the voltage on the pin exceeds 1.24 V by 50 mV.

To implement burst-mode operation the voltage applied to the STBY pin needs to be related to the feedback loop. *Figure 24*a shows the simplest implementation, suitable with a narrow input voltage range (e.g. when there is a PFC front-end).

Figure 24. Burst-mode implementation: a) narrow input voltage range; b) wide input voltage range



Essentially, RF_{max} will define the switching frequency fmax above which the L6599E will enter burst-mode operation. Once fixed fmax, RF_{max} will be found from the relationship:

Note that, unlike the f_{max} considered in the previous section (*Section 7.1: Oscillator*), here

$$RF_{max} = \frac{3}{8}\frac{RF_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

f_{max} is associated to some load $Pout_B$ greater than the minimum one. $Pout_B$ will be such that the transformer's peak currents are low enough not to cause audible noise.

Resonant converter's switching frequency, however, depends also on the input voltage; hence, in case there is quite a large input voltage range with the circuit of *Figure 24*a the value of $Pout_B$ would change considerably. In this case it is recommended to use the arrangement shown in *Figure 24*b, where the information on the converter's input voltage is added to the voltage applied to the STBY pin. Due to the strongly non-linear relationship between switching frequency and input voltage, it is more practical to find empirically the right amount of correction R_A / (R_A + R_B) needed to minimize the change of $Pout_B$. Just be careful in choosing the total value R_A + R_B much greater than R_C to minimize the effect on the LINE pin voltage (see *Section 7.6: Line sensing function*).

Whichever circuit is in use, its operation can be described as follows. As the load falls below the value $Pout_B$ the frequency will try to exceed the maximum programmed value fmax and the voltage on the STBY pin (V_{STBY}) will go below 1.24 V. The IC will then stop with both gate-drive outputs low, so that both MOSFETs of the half-bridge leg are in OFF-state. The voltage V_{STBY} will now increase as a result of the feedback reaction to the energy delivery stop and, as it exceeds 1.29 V, the IC will restart switching. After a while, V_{STBY} will go down again in response to the energy burst and stop the IC. In this way the converter will work in a burst-mode fashion with a nearly constant switching frequency. A further load decrease will then cause a frequency reduction, which can go down even to few hundred hertz. The timing diagram of *Figure 25* illustrates this kind of operation, showing the most significant signals. A small capacitor (typically in the hundred pF) from the STBY pin to ground, placed as close to the IC as possible to reduce switching noise pick-up, will help get clean operation.

To help the designer meet energy saving requirements even in power-factor-corrected systems, where a PFC pre-regulator precedes the DC-DC converter, the L6599E allows that the PFC pre-regulator can be turned off during burst-mode operation, hence eliminating the no-load consumption of this stage (0.5 1 W). There is no compliance issue in that because

EMC regulations on low-frequency harmonic emissions refer to nominal load, no limit is envisaged when the converter operates with light or no load.

To do so, the L6599E provides pin 9 (PFC_STOP): it is an open collector output, normally open, that is asserted low when the IC is idle during burst-mode operation. This signal will be externally used for switching off the PFC controller and the pre-regulator as shown in *Figure 26*. When the L6599E is in UVLO the pin is kept open, to let the PFC controller start first

Figure 25. Load-dependent operating modes: timing diagram

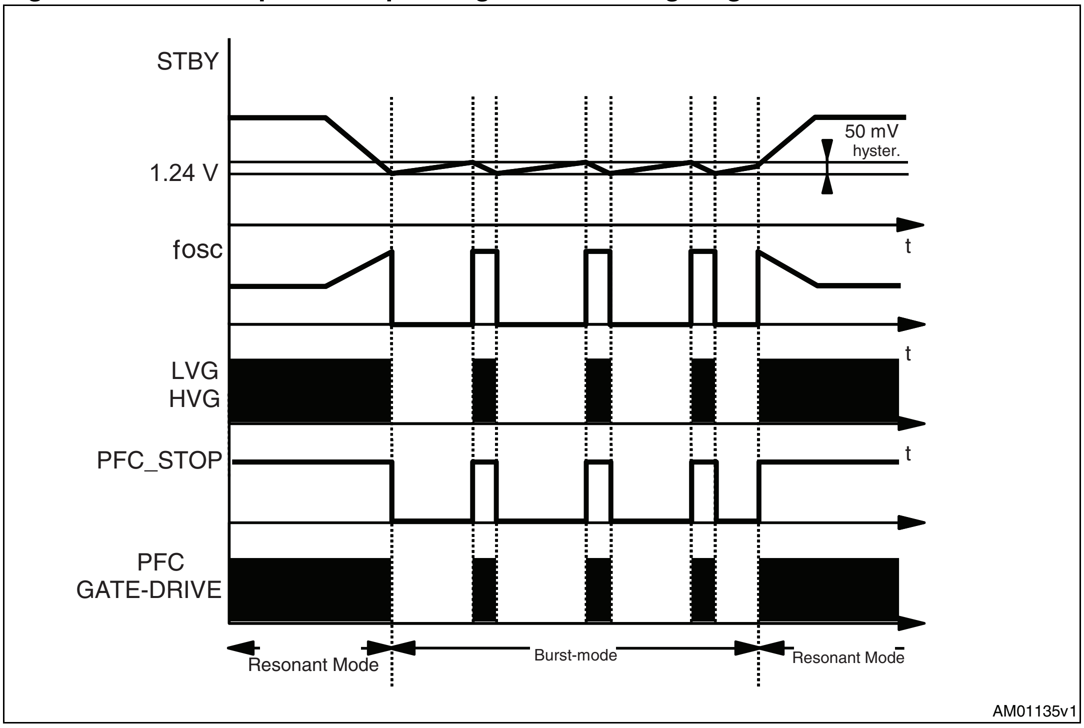
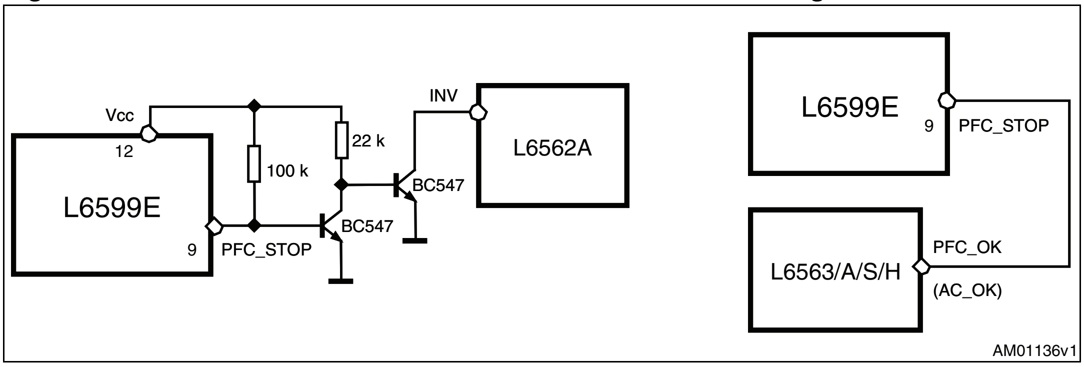


Figure 26. How the L6599E can switch off a PFC controller at light load



7.3 Soft-start

Generally speaking, purpose of soft-start is to progressively increase converter's power capability when it is started up, so as to avoid excessive inrush current. In resonant converters the deliverable power depends inversely on frequency, then soft- start is done by sweeping the operating frequency from an initial high value until the control loop takes over. With the L6599E converter's soft start-up is simply realized with the addition of an R-C series circuit from pin 4 (RFmin) to ground (see *Figure 27*, left).

Initially, the capacitor CSS is totally discharged, so that the series resistor RSS is effectively in parallel to RFmin and the resulting initial frequency is determined by RSS and RFmin only, since the optocoupler's phototransistor is cut off (as long as the output voltage is not too far away from the regulated value):

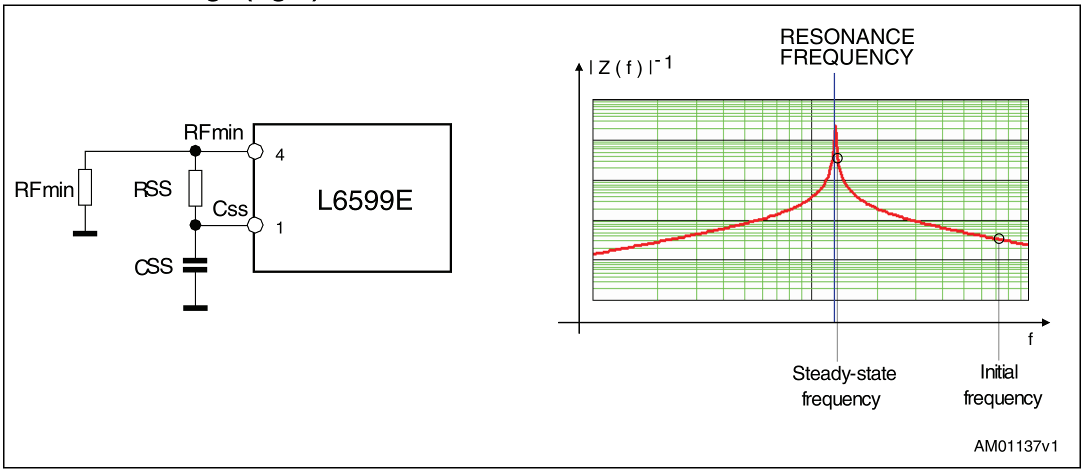
Equation 3

$$f_{start} = \frac{1}{3 \cdot CF \cdot (RF_{min} // R_{ss})}$$

The C_{SS} capacitor is progressively charged until its voltage reaches the reference voltage (2 V) and, consequently, the current through R_{SS} goes to zero. This conventionally takes 5 times constants $R_{SS} \cdot C_{SS}$ but, before that time, the output voltage will have got close to the regulated value and the feedback loop taken over, so that it will be the optocoupler's phototransistor to determine the operating frequency from that moment onwards.

During this frequency sweep phase the operating frequency will decay following the exponential charge of C_{SS}, that is, initially it will change relatively quickly but the rate of change will get slower and slower. This counteract the non-linear frequency dependence of the tank circuit that makes converter's power capability change little as frequency is away from resonance and change very quickly as frequency approaches resonance frequency (see *Figure 27*, right).

Figure 27. Soft-start circuit (left) and power vs. frequency curve in an resonant half-bridge (right)



As a result, the average input current will smoothly increase, without the peaking that occurs with linear frequency sweep, and the output voltage will reach the regulated value with almost no overshoot.

Typically, R_{SS} and C_{SS} will be selected based on the following relationships:

Equation 4

$$R_{ss} = \frac{RF_{min}}{\frac{f_{start}}{f_{min}} - 1}; \qquad C_{ss} = \frac{3 \cdot 10^{-3}}{R_{ss}}$$

where f_{start} is recommended to be at least 4 times f_{min}. The proposed criterion for C_{SS} is quite empirical and is a compromise between an effective soft-start action and an effective OCP (see next section). Please refer to the timing diagram of *Figure 27* to see some significant signals during the soft-start phase.

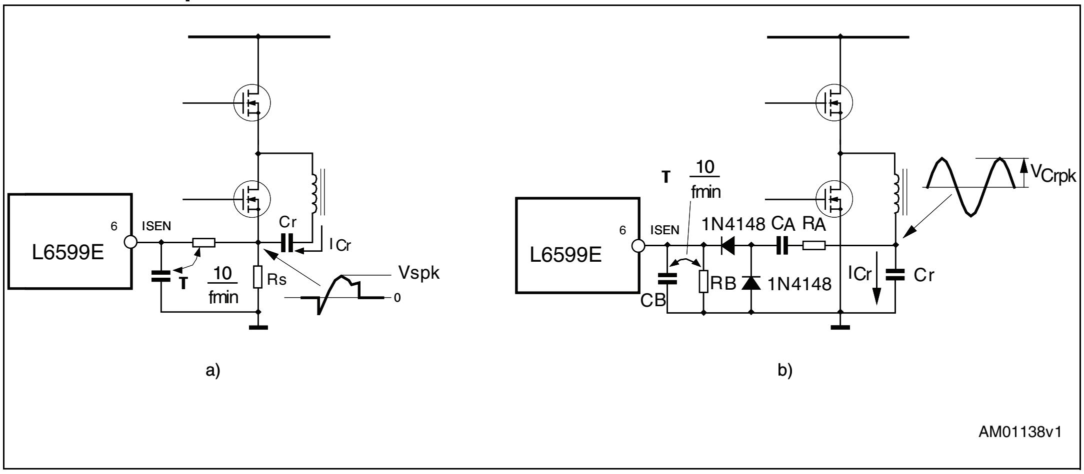
7.4 Current sense, OCP and OLP

The resonant half-bridge is essentially voltage-mode controlled; hence a current sense input will only serve as an overcurrent protection (OCP).

Unlike PWM-controlled converters, where energy flow is controlled by the duty cycle of the primary switch (or switches), in a resonant half-bridge the duty cycle is fixed and energy flow is controlled by its switching frequency. This impacts on the way current limitation can be realized. While in PWM-controlled converters energy flow can be limited simply by terminating switch conduction beforehand when the sensed current exceeds a preset threshold (this is commonly now as cycle-by-cycle limitation), in a resonant half-bridge the switching frequency, that is, its oscillator's frequency must be increased and this cannot be done as quickly as turning off a switch: it takes at least the next oscillator cycle to see the frequency change. This implies that to have an effective increase, able to change the energy flow significantly, the rate of change of the frequency must be slower than the frequency itself. This, in turn, implies that cycle-by-cycle limitation is not feasible and that, therefore, the information on the primary current fed to the current sensing input must be somehow averaged. Of course, the averaging time must not be too long to prevent the primary current from reaching too high values.

In *Figure 28* a couple of current sensing methods are illustrated that will be described in the following. The circuit of *Figure 28*a is simpler but the dissipation on the sense resistor Rs might not be negligible, hurting efficiency; the circuit of *Figure 28*b is more complex but virtually lossless and recommended when the efficiency target is very high.

Figure 28. Current sensing techniques: a) with sense resistor, b) “lossless”,with capacitive shunt



The L6599E is equipped with a current sensing input (pin 6, ISEN) and a sophisticated overcurrent management system. The ISEN pin is internally connected to the input of a first comparator, referenced to 0.8 V, and to that of a second comparator referenced to 1.5 V. If the voltage externally applied to the pin by either circuit in *Figure 28* exceeds 0.8 V the first comparator is tripped and this causes an internal switch to be turned on and discharge the soft-start capacitor C_{SS} (see *Section 7.3: Soft-start*). This will quickly increase the oscillator frequency and thereby limit energy transfer. The discharge will go on until the voltage on the ISEN pin has dropped by 50 mV; this, with an averaging time in the range of $10/f_{min}$, ensures an effective frequency rise. Under output short circuit, this operation results in a nearly constant peak primary current.

It is normal that the voltage on the ISEN pin may overshoot above 0.8 V; however, if the voltage on the ISEN pin reaches 1.5 V, the second comparator will be triggered, the L6599E will shutdown and latch off with both the gate-drive outputs and the PFC_STOP pin low, hence turning off the entire unit. The supply voltage of the IC must be pulled below the UVLO threshold and then again above the start-up level in order to restart. Such an event may occur if the soft-start capacitor C_{SS} is too large, so that its discharge is not fast enough or in case of transformer’s magnetizing inductance saturation or a shorted secondary rectifier.

In the circuit shown in *Figure 28*a, where a sense resistor Rs in series to the source of the low-side MOSFET is used, note the particular connection of the resonant capacitor. In this way the voltage across Rs is related to the current flowing through the high-side MOSFET and is positive most of the switching period, except for the time needed for the resonant current to reverse after the low-side MOSFET has been switched off. Assuming that the time constant of the RC filter is at least ten times the minimum switching frequency f_{min}, the approximate value of Rs can be found using the empirical equation:

Equation 5

$$\frac{V_{Spkx}}{I_{Crpkx}} \approx \frac{5 \cdot 0.8}{I_{Crpkx}} \approx \frac{4}{I_{Crpkx}}$$

where I_{Crpkx} is the maximum desired peak current flowing through the resonant capacitor and the primary winding of the transformer, which is related to the maximum load and the minimum input voltage.

The circuit shown in *Figure 28*b can be operated in two different ways. If the resistor R_A in series to C_A is small (not above some hundred Ω, just to limit current spiking) the circuit operates like a capacitive current divider; C_A will be typically selected equal to Cr/100 or less and will be a low-loss type, the sense resistor R_B will be selected as:

Equation 6

$$R_B = \frac{0.8\pi}{I_{Crpkx}} \left(1 + \frac{C_r}{C_A}\right)$$

and C_B will be such that $R_B \cdot C_B$ is in the range of 10 /f_{min}.

If the resistor R_A in series to C_A is not small (in this case it will be typically selected in the ten kΩ), the circuit operates like a divider of the ripple voltage across the resonant capacitor Cr, which, in turn, is related to its current through the reactance of Cr. Again, C_A will be typically selected equal to Cr/100 or less, this time not necessarily a low-loss type, while R_B (provided it is << R_A) according to:

Equation 7

$$R_B = \frac{0.8\pi}{I_{Crpkx}} \frac{\sqrt{R^2{}_A + X^2{}_{C_A}}}{X_{Cr}}$$

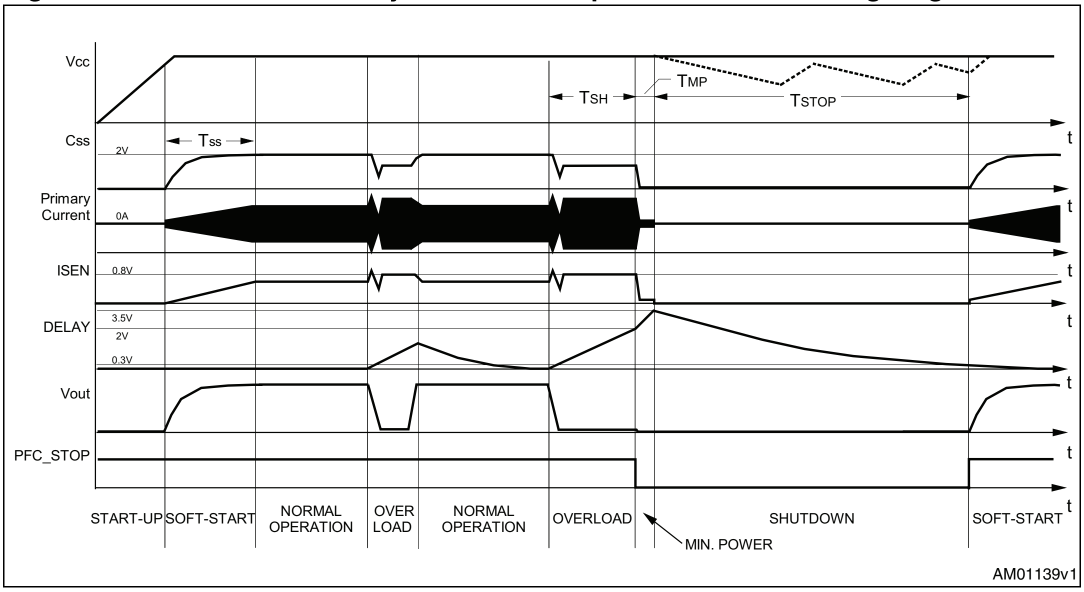
where the reactance of C_A (X_{CA}) and Cr (X_{Cr}) should be calculated at the frequency where $I_{Crpk} = I_{Crpkx}$. Again, C_B will be such that $R_B \cdot C_B$ is in the range of 10 /f_{min}.

Whichever circuit one is going to use, the calculated values of Rs or R_B should be considered just a first cut value that needs to be adjusted after experimental verification.

OCP is effective in limiting primary-to-secondary energy flow in case of an overload or an output short circuit, but the output current through the secondary winding and rectifiers under these conditions might be so high to endanger converter's safety if continuously flowing. To prevent any damage during these conditions it is customary to force converter's intermittent operation, in order to bring the average output current to values such that the thermal stress for the transformer and the rectifiers can be easily handled.

With the L6599E the designer can program externally the maximum time T_{SH} that the converter is allowed to run overloaded or under short circuit conditions. Overloads or short circuits lasting less than T_{SH} will not cause any other action, hence providing the system with immunity to short duration phenomena. If, instead, T_{SH} is exceeded an overload protection (OLP) procedure is activated that shuts down the L6599E and, in case of continuous overload/short circuit, results in continuous intermittent operation with a user-defined duty cycle.

Figure 29. Soft-start and delayed shutdown upon overcurrent timing diagram



This function is realized with pin 2 (DELAY), by means of a capacitor C_{Delay} and a parallel resistor R_{Delay} connected to ground. As the voltage on the ISEN pin exceeds 0.8 V the first OCP comparator, in addition to discharging C_{SS}, turns on an internal current generator that sources 150 µA from the DELAY pin and charges C_{Delay}. During an overload/short-circuit the OCP comparator and the internal current source will be repeatedly activated and C_{Delay} will be charged with an average current that depends essentially on the time constant of the current sense filtering circuit, on C_{SS} and the characteristics of the resonant circuit; the discharge due to R_{Delay} can be neglected, considering that the associated time constant is typically much longer.

This operation will go on until the voltage on C_{Delay} reaches 2 V, which defines the time T_{SH}. There is not a simple relationship that links T_{SH} to C_{Delay}, thus it is more practical to determine C_{Delay} experimentally. As a rough indication, with C_{Delay} = 1 µF T_{SH} will be in the order of 100 ms.

Once C_{Delay} is charged at 2 V the internal switch that discharges C_{SS} is forced low continuously regardless of the OCP comparator's output, and the 150 µA current source is continuously on, until the voltage on C_{Delay} reaches 3.5 V. This phase lasts:

Equation 8

$$T_{MP} = 10 \cdot C_{Delay}$$

with T_{MP} is expressed in ms and C_{Delay} in µF. During this time the L6599E runs at a frequency close to f_{start} (see *Section 7.3: Soft-start*) to minimize the energy inside the resonant circuit. As the voltage on C_{Delay} is 3.5 V, the L6599E stops switching and the PFC_STOP pin is pulled low. Also the internal generator is turned off, so that C_{Delay} will now be slowly discharged by R_{Delay}. The IC will restart when the voltage on C_{Delay} will be less than 0.3 V, which will take:

Equation 9

$$T_{STOP} = R_{Delay} C_{Delay} \ln\frac{3.5}{0.3} \approx 2.5 R_{Delay} C_{Delay}$$

The timing diagram of *Figure 29* shows this operation. Note that if during T_{STOP} the supply voltage of the L6599E (Vcc) falls below the UVLO threshold the IC keeps memory of the event and will not restart immediately after Vcc exceeds the start-up threshold if V(DELAY) is still higher than 0.3 V. Also the PFC_STOP pin will stay low as long as V(DELAY) is greater than 0.3 V. Note also that in case there is an overload lasting less than T_{SH}, the value of T_{SH} for the next overload will be lower if they are close to one another.

7.5 Latched shutdown

The L6599E is equipped with a comparator having the non-inverting input externally available at pin 8 (DIS) and with the inverting input internally referenced to 1.85V. As the voltage on the pin exceeds the internal threshold, the IC is immediately shut down and its consumption reduced at a low value. The information is latched and it is necessary to let the voltage on the Vcc pin go below the UVLO threshold to reset the latch and restart the IC.

This function is useful to implement a latched overtemperature protection very easily by biasing the pin with a divider from an external reference voltage (e.g. pin 4, RFmin), where the upper resistor is an NTC physically located close to a heating element like the MOSFET, or the secondary diode or the transformer.

An OVP can be implemented as well, e.g. by sensing the output voltage and transferring an overvoltage condition via an optocoupler.

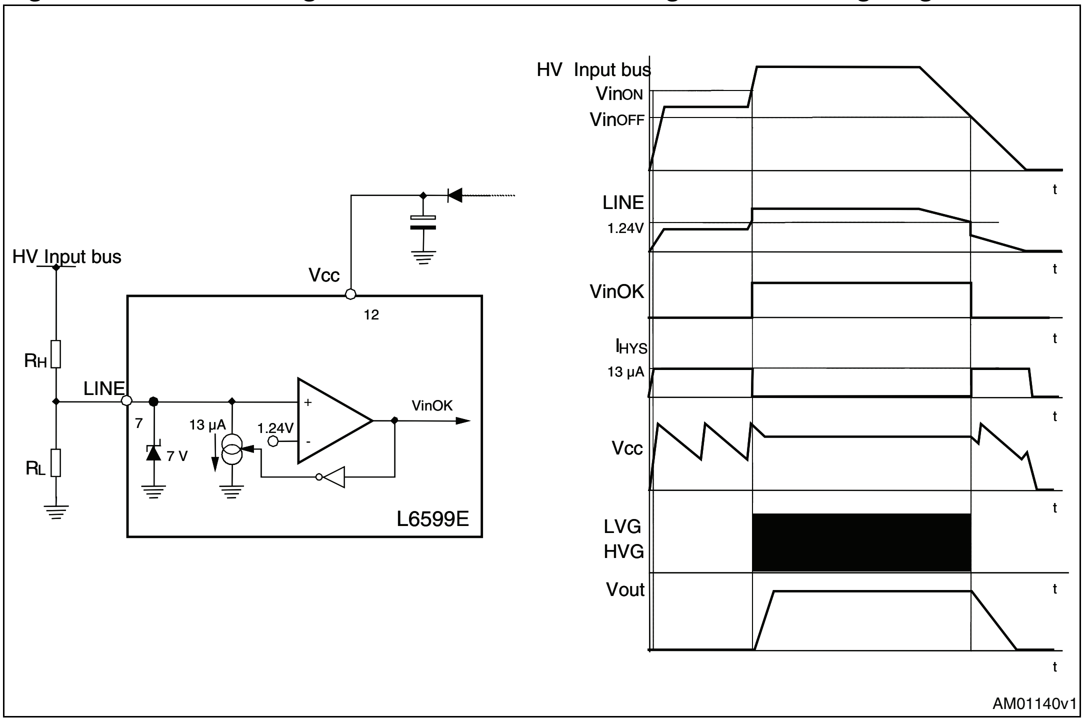
7.6 Line sensing function

This function basically stops the IC as the input voltage to the converter falls below the specified range and lets it restart as the voltage goes back within the range. The sensed voltage can be either the rectified and filtered mains voltage, in which case the function will act as a brownout protection, or, in systems with a PFC pre-regulator front-end, the output voltage of the PFC stage, in which case the function will serve as a power-on and power-off sequencing.

L6599E shutdown upon input undervoltage is accomplished by means of an internal comparator, as shown in the block diagram of *Figure 30*, whose non-inverting input is available at pin 7 (LINE). The comparator is internally referenced to 1.24 V and disables the IC if the voltage applied at the LINE pin is below the internal reference. Under these conditions the soft-start is discharged, the PFC_STOP pin is open and the consumption of the IC is reduced. PWM operation is re-enabled as the voltage on the pin is above the reference. The comparator is provided with current hysteresis instead of a more usual voltage hysteresis: an internal 13 µA current sink is ON as long as the voltage applied at the LINE pin is below the reference and is OFF if the voltage is above the reference.

This approach provides an additional degree of freedom: it is possible to set the ON threshold and the OFF threshold separately by properly choosing the resistors of the external divider (see below). With voltage hysteresis, instead, fixing one threshold automatically fixes the other one depending on the built-in hysteresis of the comparator.

Figure 30. Line sensing function: internal block diagram and timing diagram



With reference to *Figure 28*, the following relationships can be established for the ON (Vin_{ON}) and OFF (Vin_{OFF}) thresholds of the input voltage:

Equation 10

$$\frac{V_{in_{ON}} - 1.24}{R_H} = 13 \cdot 10^{-6} + \frac{1.24}{R_L} \qquad \frac{V_{in_{OFF}} - 1.24}{R_H} = \frac{1.24}{R_L}$$

which, solved for R_H and R_L, yield:

Equation 11

$$R_H = \frac{V_{in_{ON}} - V_{in_{OFF}}}{13 \cdot 10^{-6}} ; \qquad R_L = R_H \frac{1.24}{V_{in_{OFF}} - 1.24}$$

While the line undervoltage is active the start-up generator keeps on working but there is no PWM activity, thus the Vcc voltage (if not supplied by another source) continuously oscillates between the start-up and the UVLO thresholds, as shown in the timing diagram of *Figure 30*.

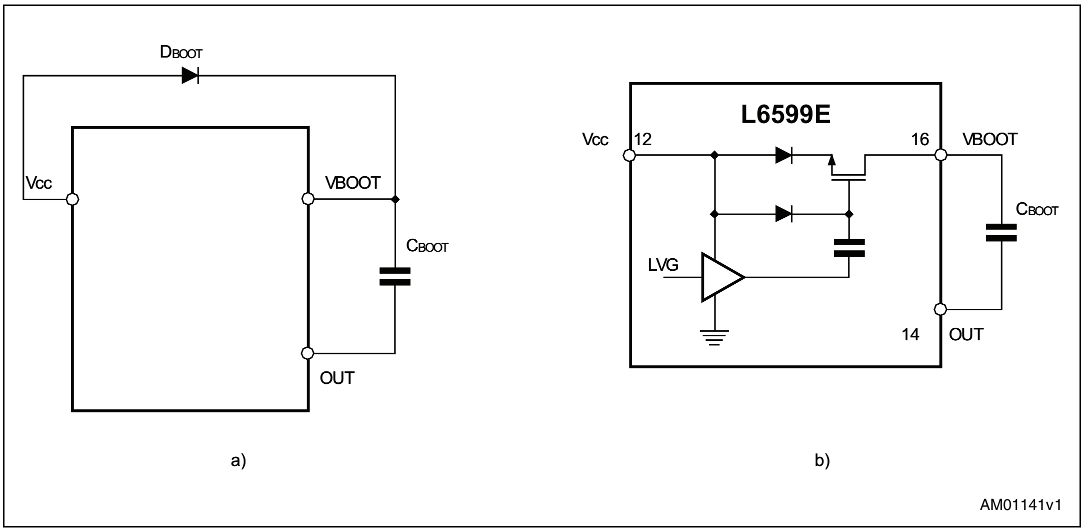
As an additional measure of safety (e.g. in case the low-side resistor is open or missing, or in non-power factor corrected systems in case of abnormally high input voltage) if the voltage on the pin exceeds 7 V the L6599E is shutdown. If its supply voltage is always above the UVLO threshold, the IC will restart as the voltage falls below 7 V.

The LINE pin, while the device is operating, is a high impedance input connected to high value resistors, thus it is prone to pick up noise, which might alter the OFF threshold or give origin to undesired switch-off of the IC during ESD tests. It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind. If the function is not used the pin has to be connected to a voltage greater than 1.24 V but lower than 6V (worst-case value of the 7 V threshold).

7.7 Bootstrap section

The supply of the floating high-side section is obtained by means of a bootstrap circuitry. This solution normally requires a high voltage fast recovery diode (D_{BOOT}, *Figure 31*a) to charge the bootstrap capacitor C_{BOOT}. In the L6599E a patented integrated structure, replaces this external diode. It is realized by means of a high voltage DMOS, working in the third quadrant and driven synchronously with the low side driver (LVG), with a diode in series to the source, as shown in *Figure 31*b.

Figure 31. Bootstrap supply: a) standard circuit; b) internal bootstrap synchronous diode



The diode prevents any current can flow from the VBOOT pin back to Vcc in case that the supply is quickly turned off when the internal capacitor of the pump is not fully discharged. To drive the synchronous DMOS it is necessary a voltage higher than the supply voltage Vcc. This voltage is obtained by means of an internal charge pump (*Figure 31*b).

The bootstrap structure introduces a voltage drop while recharging CBOOT (i.e. when the low side driver is on), which increases with the operating frequency and with the size of the external power MOS. It is the sum of the drop across the $R_{(DS)ON}$ and the forward drop across the series diode. At low frequency this drop is very small and can be neglected but, as the operating frequency increases, it must be taken into account. In fact, the drop reduces the amplitude of the driving signal and can significantly increase the $R_{(DS)ON}$ of the external high-side MOSFET and then its conductive loss.

This concern applies to converters designed with a high resonance frequency (indicatively, > 150 kHz), so that they run at high frequency also at full load. Otherwise, the converter will run at high frequency at light load, where the current flowing in the MOSFETs of the half-bridge leg is low, so that, generally, an $R_{(DS)ON}$ rise is not an issue. However, it is wise to check this point anyway and the following equation is useful to compute the drop on the bootstrap driver:

Equation 12

$$V_{Drop} = I_{charge} R_{(DS)on} + V_F = \frac{Q_g}{T_{charge}} R_{(DS)on} + V_F$$

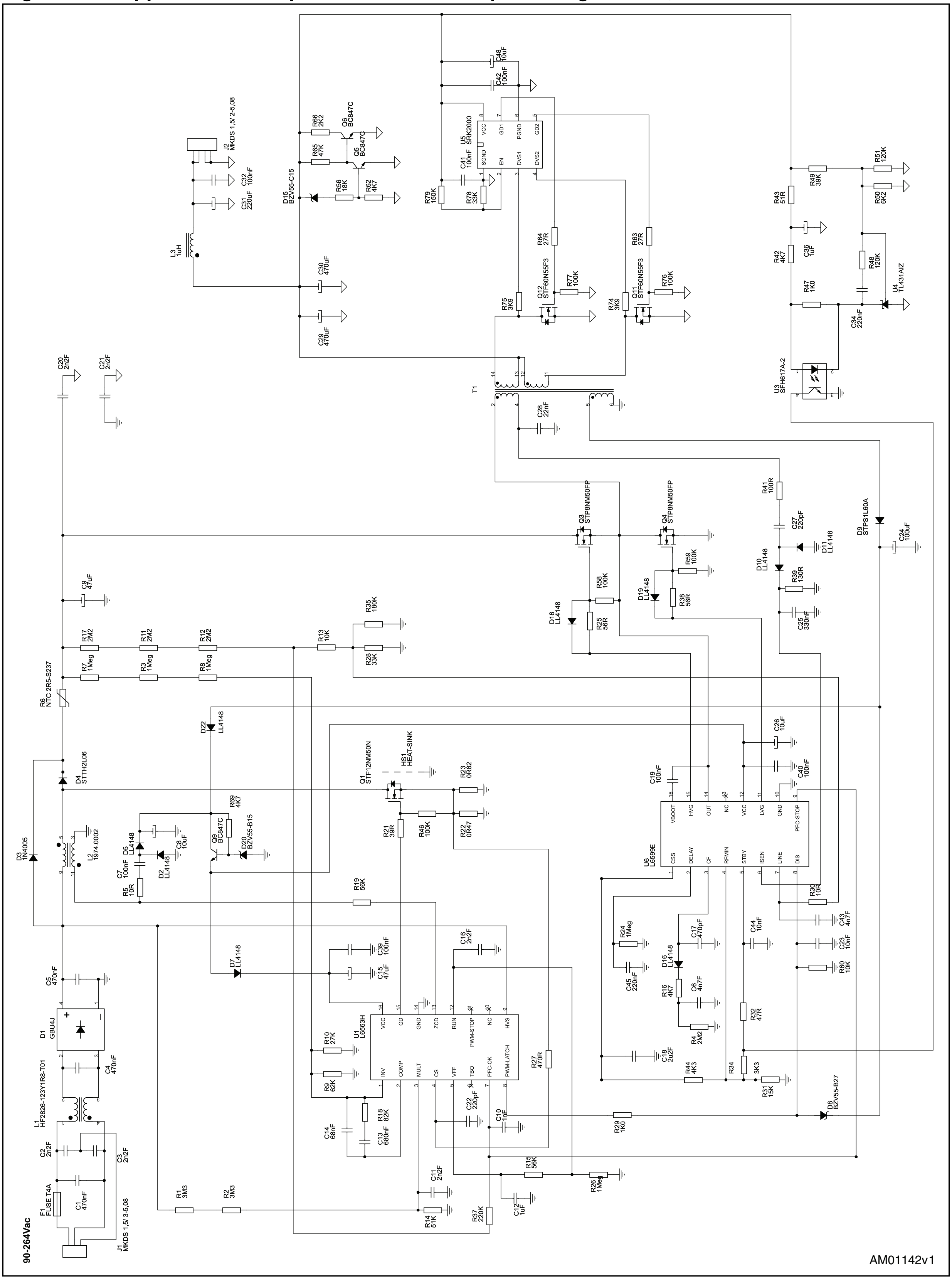
where Qg is the gate charge of the external power MOS, $R_{(DS)ON}$ is the on-resistance of the bootstrap DMOS (150 W, typ.) and T_{charge} is the ON-time of the bootstrap driver, which equals about half the switching period minus the dead time T_D. For example, using a MOSFET with a total gate charge of 30nC, the drop on the bootstrap driver is about 3 V at a switching frequency of 200 kHz:

Equation 13

$$V_{Drop} = \frac{30 \cdot 10^{-9}}{2.5 \cdot 10^{-6} - 0.27 \cdot 10^{-6}} \quad 150+0.6=2.7\ \mathrm{V}$$

If a significant drop on the bootstrap driver is an issue, an external ultra-fast diode can be used, thus saving the drop on the $R_{(DS)ON}$ of the internal DMOS.

Figure 32. Application example: 90 W AC/DC adapter using L6563H, L6599E and SRK2000



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 6. SO16N dimentions

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0		8°
ccc			0.10

Figure 33. SO16N drawing

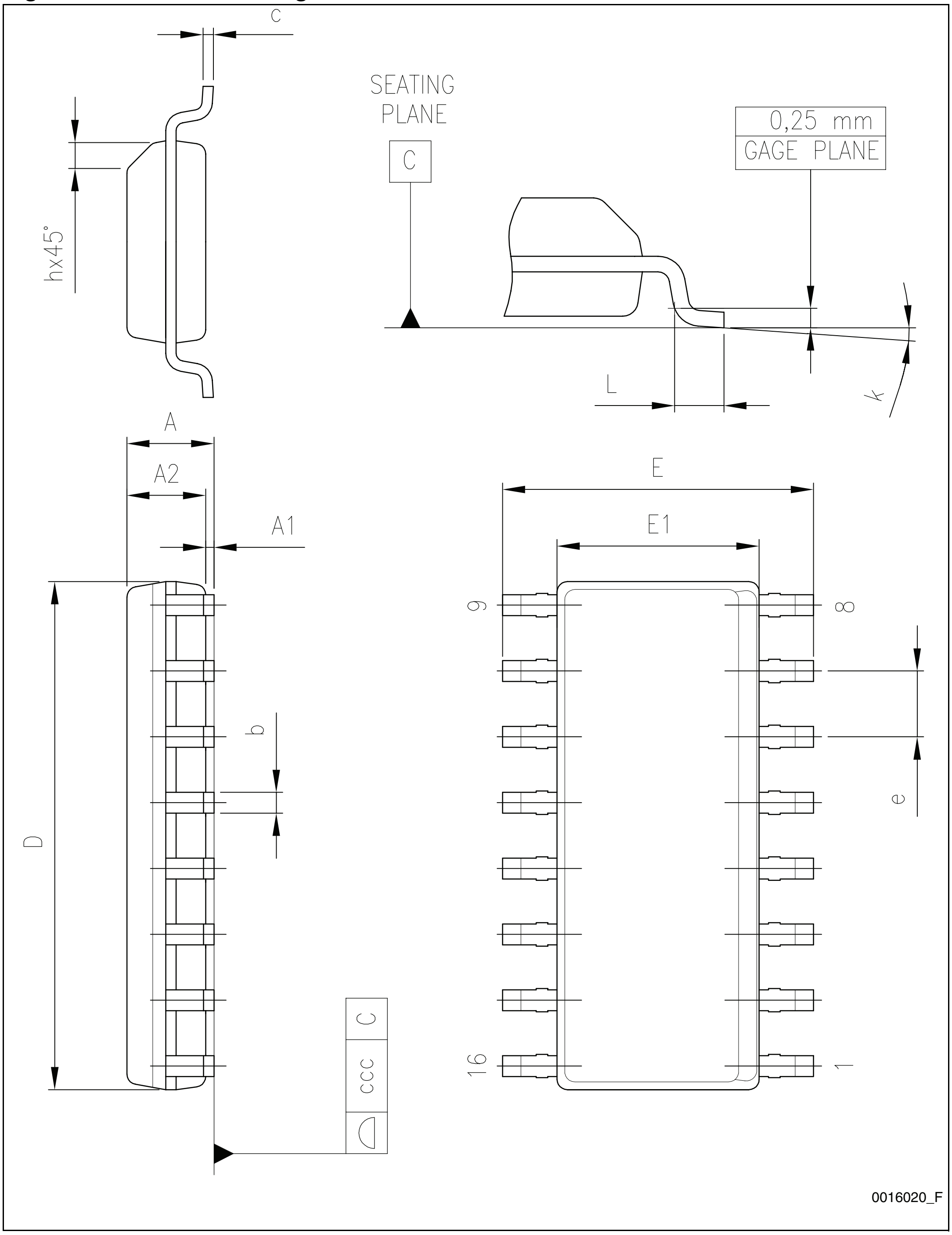
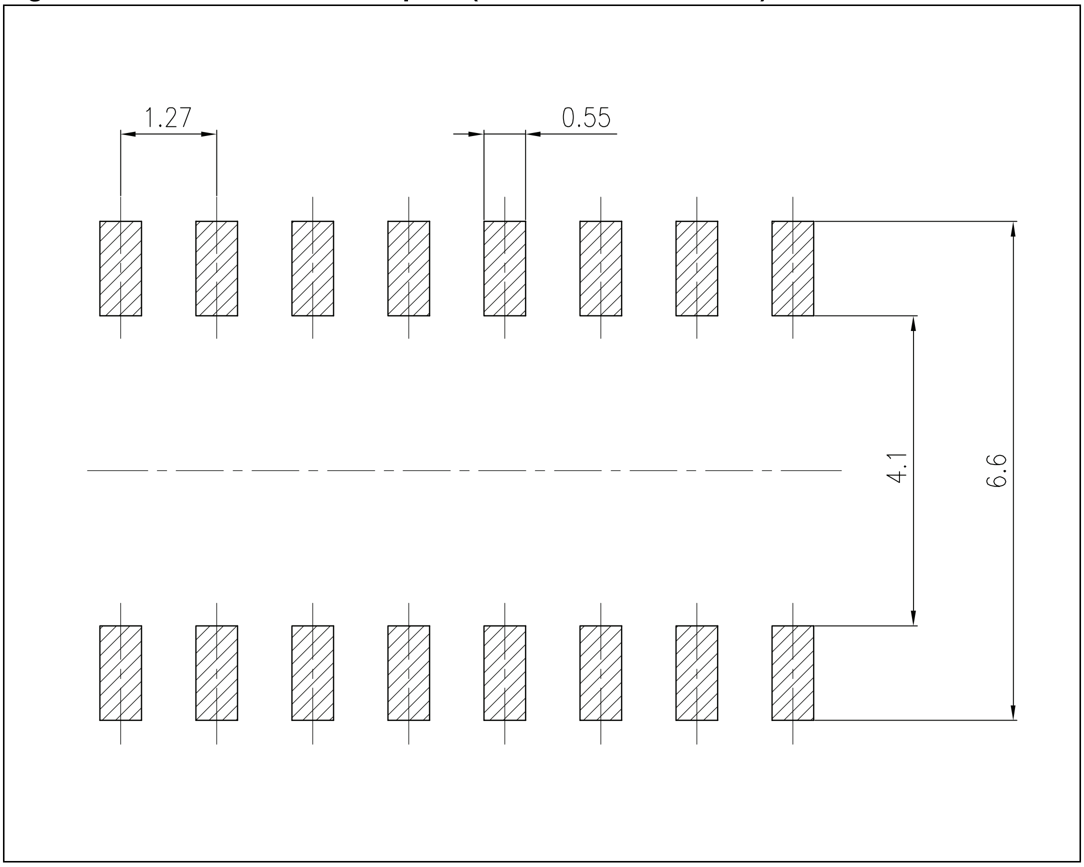


Figure 34. Recommended footprint (dimensions are in mm)



9 Revision history

Table 7. Document revision history

Date	Revision	Changes
29-May-2012	1	Initial release

Please Read Carefully:

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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