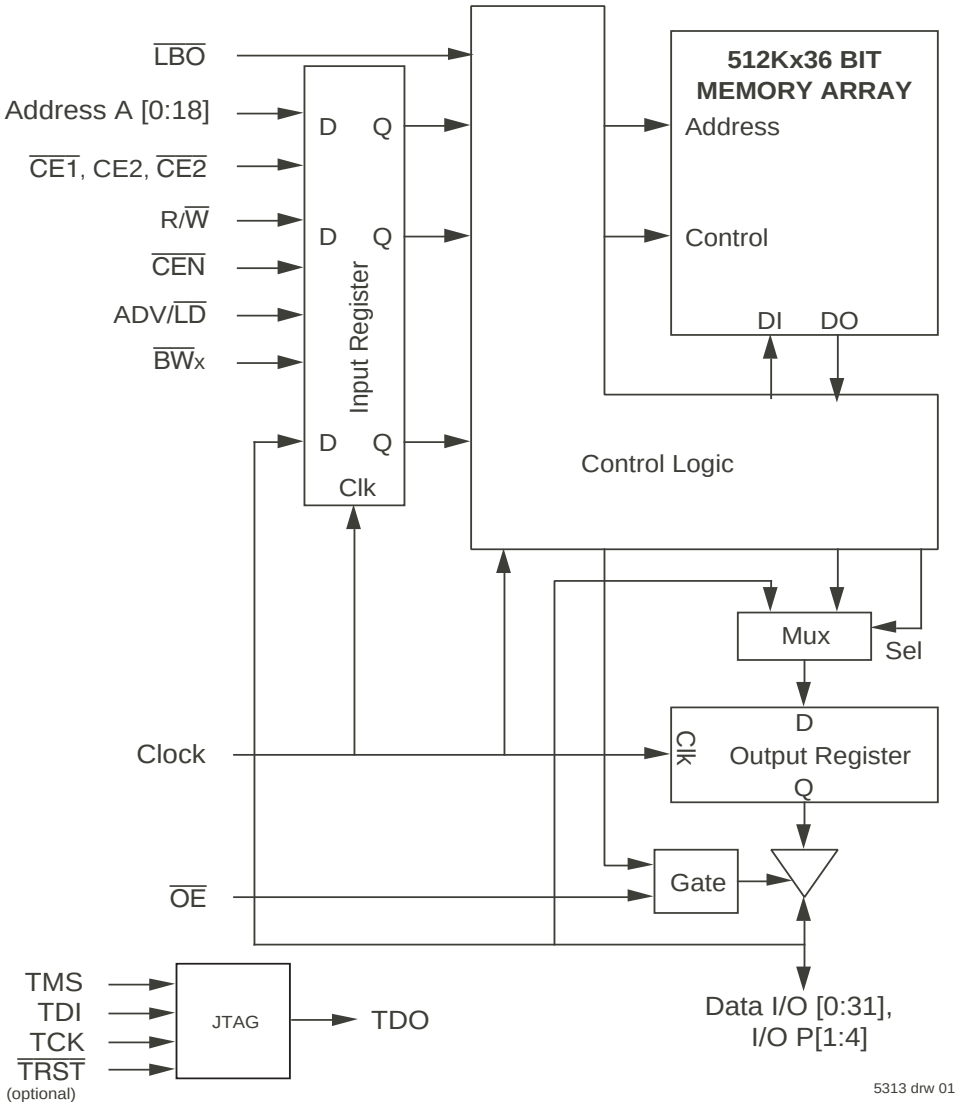
# 512K x 36, 1M x 18
# 2.5V Synchronous ZBT™ SRAMs
# 2.5V I/O, Burst Counter
# Pipelined Outputs

***IDT71T75602***
***IDT71T75802***

## Features

- 512K x 36, 1M x 18 memory configurations
- Supports high performance system speed - 200 MHz (3.2 ns Clock-to-Data Access)
- ZBT™ Feature - No dead cycles between write and read cycles
- Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$
- Single R/$\overline{W}$ (READ/WRITE) control pin
- Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- 4-word burst capability (interleaved or linear)
- Individual byte write ($\overline{BW}_1$ - $\overline{BW}_4$) control (May tie active)
- Three chip enables for simple depth expansion
- 2.5V power supply (±5%)
- 2.5V I/O Supply ($V_{DDQ}$)
- Power down controlled by ZZ input
- Boundary Scan JTAG Interface (IEEE 1149.1 Compliant)
- Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA)
- Green parts available, see Ordering Information

## Functional Block Diagram - 512K x 36

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## Description

The IDT71T75602/802 are 2.5V high-speed 18,874,368-bit (18 Mega-bit) synchronous SRAMs. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71T75602/802 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable $\overline{CEN}$ pin allows operation of the IDT71T75602/802 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CEN}$) is high and the internal device registers will hold their previous values.

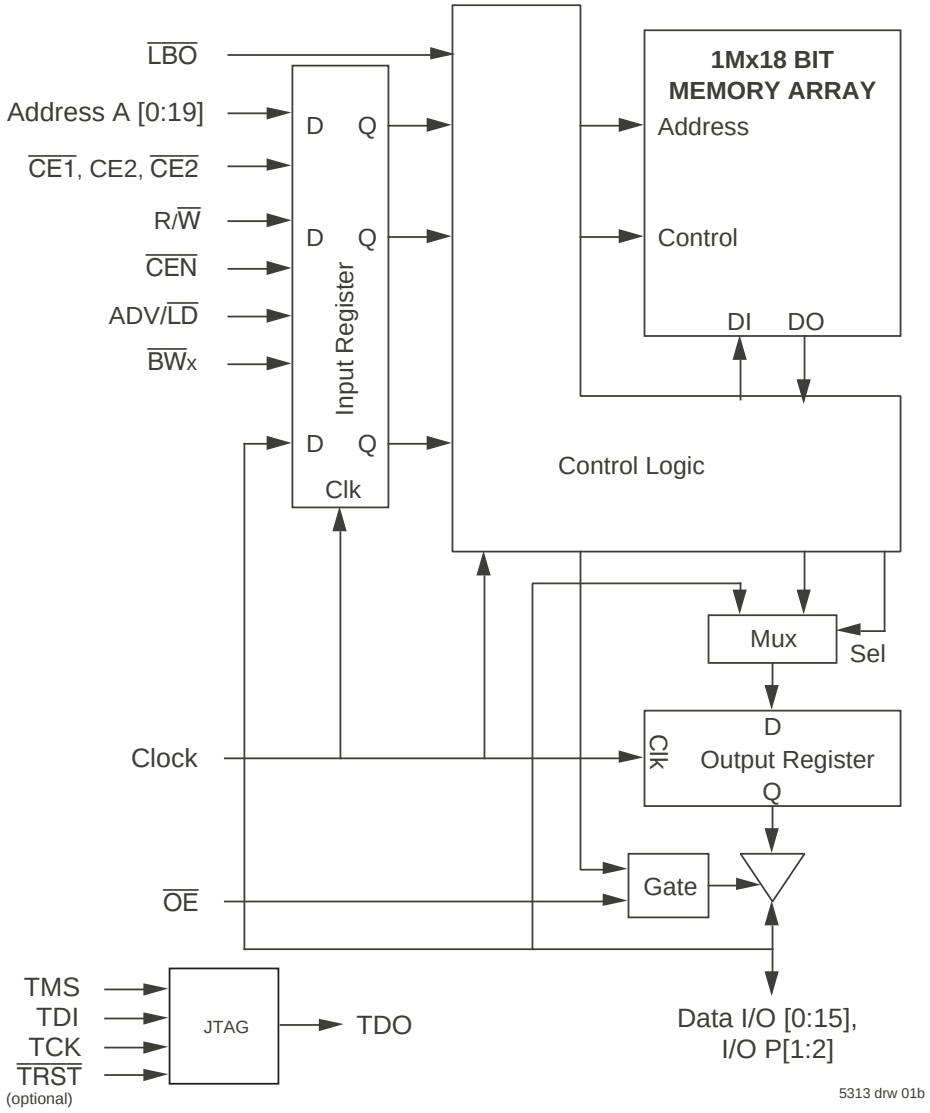
There are three chip enable pins ($\overline{CE}_1$, $CE_2$, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three is not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated.

However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after the chip is deselected or a write is initiated.

The IDT71T75602/802 have an on-chip burst counter. In the burst mode, the IDT71T75602/802 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71T75602/802 SRAMs utilize a high-performance 2.5V CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA).

## Functional Block Diagram - 1M x 18



## Pin Description Summary

| | | | |
|---|---|---|---|
| $A_0$-$A_{19}$ | Address Inputs | Input | Synchronous |
| $\overline{CE}_1$, $CE_2$, $\overline{CE}_2$ | Chip Enables | Input | Synchronous |
| $\overline{OE}$ | Output Enable | Input | Asynchronous |
| R/$\overline{W}$ | Read/Write Signal | Input | Synchronous |
| $\overline{CEN}$ | Clock Enable | Input | Synchronous |
| $\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$ | Individual Byte Write Selects | Input | Synchronous |
| CLK | Clock | Input | N/A |
| ADV/$\overline{LD}$ | Advance burst address / Load new address | Input | Synchronous |
| $\overline{LBO}$ | Linear / Interleaved Burst Order | Input | Static |
| TMS | Test Mode Select | Input | N/A |
| TDI | Test Data Input | Input | N/A |
| TCK | Test Clock | Input | N/A |
| TDO | Test Data Input | Output | N/A |
| $\overline{TRST}$ | JTAG Reset (Optional) | Input | Asynchronous |
| ZZ | Sleep Mode | Input | Synchronous |
| $I/O_0$-$I/O_{31}$, $I/O_{P1}$-$I/O_{P4}$ | Data Input / Output | I/O | Synchronous |
| $V_{DD}$, $V_{DDQ}$ | Core Power, I/O Power | Supply | Static |
| $V_{SS}$ | Ground | Supply | Static |

5313 tbl 01

# Pin Definitions(1)

| Symbol | Pin Function | I/O | Active | Description |
|---|---|---|---|---|
| $A_0$-$A_{19}$ | Address Inputs | I | N/A | Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ low, $\overline{CEN}$ low, and true chip enables. |
| ADV/$\overline{LD}$ | Advance / Load | I | N/A | ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high. |
| R/$\overline{W}$ | Read / Write | I | N/A | R/$\overline{W}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later. |
| $\overline{CEN}$ | Clock Enable | I | LOW | Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock. |
| $\overline{BW}_1$-$\overline{BW}_4$ | Individual Byte Write Enables | I | LOW | Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (when R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW}_1$-$\overline{BW}_4$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device two cycles later. $\overline{BW}_1$-$\overline{BW}_4$ can all be tied low if always doing write to the entire 36-bit word. |
| $\overline{CE}_1$, $\overline{CE}_2$ | Chip Enables | I | LOW | Synchronous active low chip enable. $\overline{CE}_1$ and $\overline{CE}_2$ are used with $CE_2$ to enable the IDT71T75602/802 ($\overline{CE}_1$ or $\overline{CE}_2$ sampled high or $CE_2$ sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated. |
| $CE_2$ | Chip Enable | I | HIGH | Synchronous active high chip enable. $CE_2$ is used with $\overline{CE}_1$ and $\overline{CE}_2$ to enable the chip. $CE_2$ has inverted polarity but otherwise identical to $\overline{CE}_1$ and $\overline{CE}_2$. |
| CLK | Clock | I | N/A | This is the clock input to the IDT71T75602/802. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK. |
| $I/O_0$-$I/O_{31}$ $I/O_{P1}$-$I/O_{P4}$ | Data Input/Output | I/O | N/A | Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK. |
| $\overline{LBO}$ | Linear Burst Order | I | LOW | Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static input and it must not change during device operation. |
| $\overline{OE}$ | Output Enable | I | LOW | Asynchronous output enable. $\overline{OE}$ must be low to read data from the 71T75602/802. When $\overline{OE}$ is high the I/O pins are in a high-impedance state.$\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low. |
| TMS | Test Mode Select | I | N/A | Gives input command for TAP controller. Sampled on rising edge of TDK. This pin has an internal pullup. |
| TDI | Test Data Input | I | N/A | Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK. This pin has an internal pullup. |
| TCK | Test Clock | I | N/A | Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from the falling edge of TCK. This pin has an internal pullup. |
| TDO | Test Data Output | O | N/A | Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller. |
| $\overline{TRST}$ | JTAG Reset (Optional) | I | LOW | Optional asynchronous JTAG reset. Can be used to reset the TAP controller, but not required. JTAG reset occurs automatically at power up and also resets using TMS and TCK per IEEE 1149.1. If not used $\overline{TRST}$ can be left floating. This pin has an internal pullup. Only available in BGA package. |
| ZZ | Sleep Mode | I | HIGH | Synchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71T75602/802 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. This pin has an internal pulldown. |
| $V_{DD}$ | Power Supply | N/A | N/A | 2.5V core power supply. |
| $V_{DDQ}$ | Power Supply | N/A | N/A | 2.5V I/O Supply. |
| $V_{SS}$ | Ground | N/A | N/A | Ground. |

5313 tbl 02

**NOTE:**

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| $V_{DDQ}$ | I/O Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| $V_{SS}$ | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage - Inputs | 1.7 | — | $V_{DD}$ +0.3 | V |
| $V_{IH}$ | Input High Voltage - I/O | 1.7 | — | $V_{DDQ}$+0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.3[1] | — | 0.7 | V |

5313 tbl 03

**NOTE:**
1. $V_{IL}$ (min.) = –0.8V for pulse width less than $t_{CYC}$/2, once per cycle.

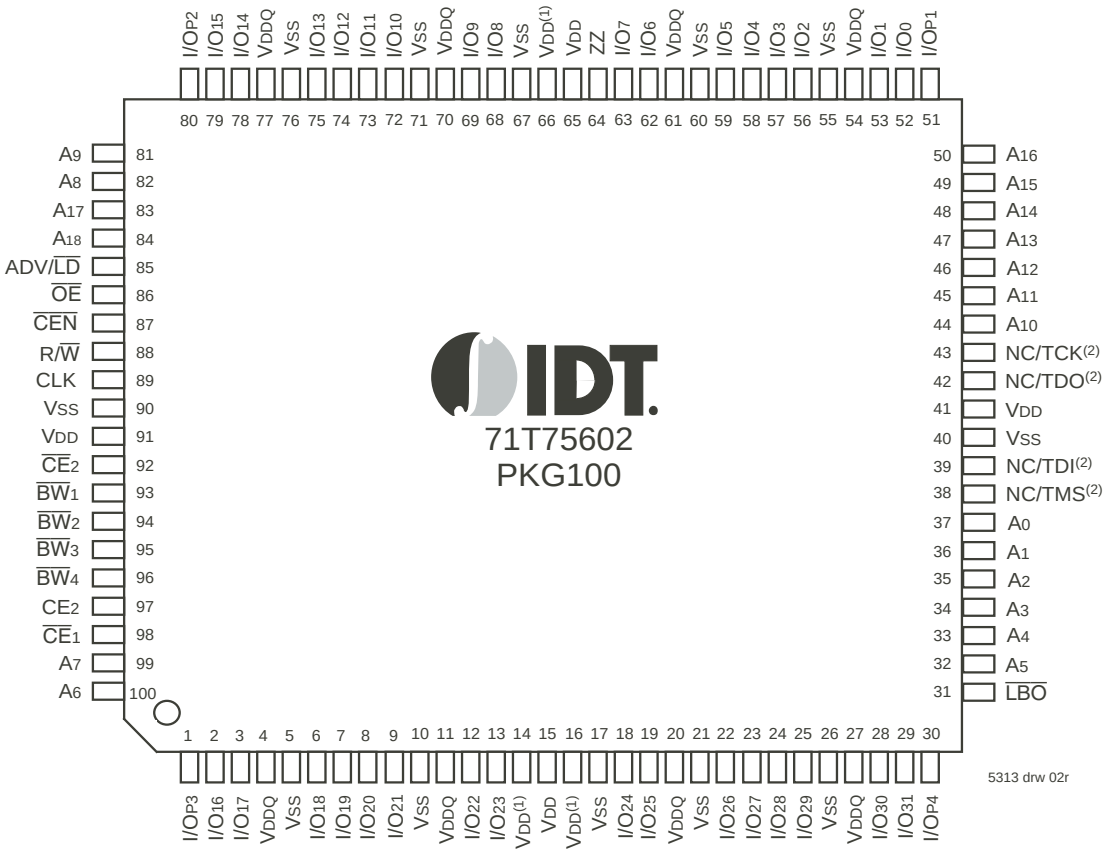
## Recommended Operating Temperature and Supply Voltage

| Grade | Ambient Temperature[1] | VSS | VDD | VDDQ |
|---|---|---|---|---|
| Commercial | 0° C to +70° C | OV | 2.5V ± 5% | 2.5V ± 5% |
| Industrial | -40° C to +85° C | OV | 2.5V ± 5% | 2.5V ± 5% |

5313 tbl 05

**NOTE:**
1. During production testing, the case temperature equals the ambient temperature.

## Pin Configuration — 512K x 36




Top View
100 TQFP

**NOTES:**
1. Pins 14, 16, and 66 do not have to be connected directly to $V_{DD}$ as long as the input voltage is $\geq V_{IH}$.
2. Pins 38, 39 and 43 will be pulled internally to $V_{DD}$ if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. Pins 38, 39 and 43 could be tied to $V_{DD}$ or $V_{SS}$ and pin 42 should be left unconnected. Or all JTAG inputs (TMS, TDI and TCK) pins 38, 39 and 43 could be left unconnected "NC" and the JTAG circuit will remain disabled from power up.

## Pin Configuration — 1Mx 18

Top View
100 TQFP

**NOTES:**

1. Pins 14, 16, and 66 do not have to be connected directly to $V_{DD}$ as long as the input voltage is $\geq V_{IH}$.
2. Pins 38, 39 and 43 will be pulled internally to $V_{DD}$ if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. Pins 38, 39 and 43 could be tied to $V_{DD}$ or $V_{SS}$ and pin 42 should be left unconnected. Or all JTAG inputs (TMS, TDI and TCK) pins 38, 39 and 43 could be left unconnected "NC" and the JTAG circuit will remain disabled from power up.

## Pin Configuration — 512K X 36, 119 BGA(1,2)
## Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | $A_6$ | $A_4$ | $A_{18}$ | $A_8$ | $A_{16}$ | $V_{DDQ}$ |
| B | NC | $CE_2$ | $A_3$ | ADV/$\overline{LD}$ | $A_9$ | $\overline{CE}_2$ | NC |
| C | NC | $A_7$ | $A_2$ | $V_{DD}$ | $A_{12}$ | $A_{15}$ | NC |
| D | $I/O_{16}$ | $I/O_{P3}$ | $V_{SS}$ | NC | $V_{SS}$ | $I/O_{P2}$ | $I/O_{15}$ |
| E | $I/O_{17}$ | $I/O_{18}$ | $V_{SS}$ | $\overline{CE}_1$ | $V_{SS}$ | $I/O_{13}$ | $I/O_{14}$ |
| F | $V_{DDQ}$ | $I/O_{19}$ | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | $I/O_{12}$ | $V_{DDQ}$ |
| G | $I/O_{20}$ | $I/O_{21}$ | $\overline{BW}_3$ | $A_{17}$ | $\overline{BW}_2$ | $I/O_{11}$ | $I/O_{10}$ |
| H | $I/O_{22}$ | $I/O_{23}$ | $V_{SS}$ | R/$\overline{W}$ | $V_{SS}$ | $I/O_9$ | $I/O_8$ |
| J | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$(1) | $V_{DD}$ | $V_{DD}$(1) | $V_{DD}$ | $V_{DDQ}$ |
| K | $I/O_{24}$ | $I/O_{26}$ | $V_{SS}$ | CLK | $V_{SS}$ | $I/O_6$ | $I/O_7$ |
| L | $I/O_{25}$ | $I/O_{27}$ | $\overline{BW}_4$ | NC | $\overline{BW}_1$ | $I/O_4$ | $I/O_5$ |
| M | $V_{DDQ}$ | $I/O_{28}$ | $V_{SS}$ | $\overline{CEN}$ | $V_{SS}$ | $I/O_3$ | $V_{DDQ}$ |
| N | $I/O_{29}$ | $I/O_{30}$ | $V_{SS}$ | $A_1$ | $V_{SS}$ | $I/O_2$ | $I/O_1$ |
| P | $I/O_{31}$ | $I/O_{P4}$ | $V_{SS}$ | $A_0$ | $V_{SS}$ | $I/O_{P1}$ | $I/O_0$ |
| R | NC | $A_5$ | $\overline{LBO}$ | $V_{DD}$ | $V_{DD}$(1) | $A_{13}$ | NC |
| T | NC | NC | $A_{10}$ | $A_{11}$ | $A_{14}$ | NC | ZZ |
| U | $V_{DDQ}$ | NC/TMS(2) | NC/TDI(2) | NC/TCK(2) | NC/TDO(2) | NC/$\overline{TRST}$(2,3) | $V_{DDQ}$ |

5313 tbl 25b

## Pin Configuration — 1M X 18, 119 BGA(1,2)
## Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | $A_6$ | $A_4$ | $A_{19}$ | $A_8$ | $A_{16}$ | $V_{DDQ}$ |
| B | NC | $CE_2$ | $A_3$ | ADV/$\overline{LD}$ | $A_9$ | $\overline{CE}_2$ | NC |
| C | NC | $A_7$ | $A_2$ | $V_{DD}$ | $A_{13}$ | $A_{17}$ | NC |
| D | $I/O_8$ | NC | $V_{SS}$ | NC | $V_{SS}$ | $I/O_{P1}$ | NC |
| E | NC | $I/O_9$ | $V_{SS}$ | $\overline{CE}_1$ | $V_{SS}$ | NC | $I/O_7$ |
| F | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | $I/O_6$ | $V_{DDQ}$ |
| G | NC | $I/O_{10}$ | $\overline{BW}_2$ | $A_{18}$ | $V_{SS}$ | NC | $I/O_5$ |
| H | $I/O_{11}$ | NC | $V_{SS}$ | R/$\overline{W}$ | $V_{SS}$ | $I/O_4$ | NC |
| J | $V_{DDQ}$ | $V_{DD}$ | $V_{DD}$(1) | $V_{DD}$ | $V_{DD}$(1) | $V_{DD}$ | $V_{DDQ}$ |
| K | NC | $I/O_{12}$ | $V_{SS}$ | CLK | $V_{SS}$ | NC | $I/O_3$ |
| L | $I/O_{13}$ | NC | $V_{SS}$ | NC | $\overline{BW}_1$ | $I/O_2$ | NC |
| M | $V_{DDQ}$ | $I/O_{14}$ | $V_{SS}$ | $\overline{CEN}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| N | $I/O_{15}$ | NC | $V_{SS}$ | $A_1$ | $V_{SS}$ | $I/O_1$ | NC |
| P | NC | $I/O_{P2}$ | $V_{SS}$ | $A_0$ | $V_{SS}$ | NC | $I/O_0$ |
| R | NC | $A_5$ | $\overline{LBO}$ | $V_{DD}$ | $V_{DD}$(1) | $A_{12}$ | NC |
| T | NC | $A_{10}$ | $A_{15}$ | NC | $A_{14}$ | $A_{11}$ | ZZ |
| U | $V_{DDQ}$ | NC/TMS(2) | NC/TDI(2) | NC/TCK(2) | NC/TDO(2) | NC/$\overline{TRST}$(2,3) | $V_{DDQ}$ |

5313 tbl 25c

**NOTES:**

1. J3, R5, and J5 do not have to be directly connected to $V_{DD}$ as long as the input voltage is $\geq V_{IH}$.
2. U2, U3, U4 and U6 will be pulled internally to $V_{DD}$ if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. U2, U3, U4 and U6 could be tied to VDD or VSS and U5 should be left unconnected. Or all JTAG inputs(TMS, TDI, and TCK and $\overline{TRST}$) U2, U3, U4 and U6 could be left unconnected "NC" and the JTAG circuit will remain disabled from power up.
3. $\overline{TRST}$ is offered as an optional JTAG reset if required in the application. If not needed, can be left floating and will internally be pulled to $V_{DD}$.

## Absolute Maximum Ratings(1)

| Symbol | Rating | Commercial | Industrial | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | -0.5 to +3.6 | -0.5 to +3.6 | V |
| $V_{TERM}$(3,6) | Terminal Voltage with Respect to GND | -0.5 to $V_{DD}$ | -0.5 to $V_{DD}$ | V |
| $V_{TERM}$(4,6) | Terminal Voltage with Respect to GND | -0.5 to $V_{DD}$ +0.5 | -0.5 to $V_{DD}$ +0.5 | V |
| $V_{TERM}$(5,6) | Terminal Voltage with Respect to GND | -0.5 to $V_{DDQ}$ +0.5 | -0.5 to $V_{DDQ}$ +0.5 | V |
| $T_A$(7) | Operating Ambient Temperature | 0 to +70 | -40 to +85 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +125 | -55 to +125 | °C |
| $P_T$ | Power Dissipation | 2.0 | 2.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | 50 | mA |

5313 tbl 06

**NOTES:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{DD}$ terminals only.
3. $V_{DDQ}$ terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed $V_{DDQ}$ during power supply ramp up.
7. During production testing, the case temperature equals $T_A$.

## 100-Pin TQFP Capacitance

($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 5 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 7 | pF |

5313 tbl 07

## 119 BGA Capacitance

($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 7 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 7 | pF |

5313 tbl 07a

**NOTE:**

1. This parameter is guaranteed by device characterization, but not production tested.

## Synchronous Truth Table(1)

| $\overline{CEN}$ | R/$\overline{W}$ | Chip(5) Enable | ADV/$\overline{LD}$ | $\overline{BW}$x | ADDRESS USED | PREVIOUS CYCLE | CURRENT CYCLE | I/O (2 cycles later) |
|---|---|---|---|---|---|---|---|---|
| L | L | Select | L | Valid | External | X | LOAD WRITE | D(7) |
| L | H | Select | L | X | External | X | LOAD READ | Q(7) |
| L | X | X | H | Valid | Internal | LOAD WRITE / BURST WRITE | BURST WRITE (Advance burst counter)(2) | D(7) |
| L | X | X | H | X | Internal | LOAD READ / BURST READ | BURST READ (Advance burst counter)(2) | Q(7) |
| L | X | Deselect | L | X | X | X | DESELECT or STOP(3) | HiZ |
| L | X | X | H | X | X | DESELECT / NOOP | NOOP | HiZ |
| H | X | X | X | X | X | X | SUSPEND(4) | Previous Value |

5313 tbl 08

**NOTES:**
1. L = $V_{IL}$, H = $V_{IH}$, X = Don't Care.
2. When ADV/$\overline{LD}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{CE}_1$, or $\overline{CE}_2$ is sampled high or $CE_2$ is sampled low) and ADV/$\overline{LD}$ is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE}_1$ = L, $\overline{CE}_2$ = L, $CE_2$ = H on these chip enables. Chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
7. Q - Data read from the device, D - data written to the device.

## Partial Truth Table for Writes(1)

| OPERATION | R/$\overline{W}$ | $\overline{BW}_1$ | $\overline{BW}_2$ | $\overline{BW}_3$(3) | $\overline{BW}_4$(3) |
|---|---|---|---|---|---|
| READ | H | X | X | X | X |
| WRITE ALL BYTES | L | L | L | L | L |
| WRITE BYTE 1 (I/O[0:7], $I/O_{P1}$)(2) | L | L | H | H | H |
| WRITE BYTE 2 (I/O[8:15], $I/O_{P2}$)(2) | L | H | L | H | H |
| WRITE BYTE 3 (I/O[16:23], $I/O_{P3}$)(2,3) | L | H | H | L | H |
| WRITE BYTE 4 (I/O[24:31], $I/O_{P4}$)(2,3) | L | H | H | H | L |
| NO WRITE | L | H | H | H | H |

5313 tbl 09

**NOTES:**
1. L = $V_{IL}$, H = $V_{IH}$, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.
3. N/A for X18 configuration.

## Interleaved Burst Sequence Table ($\overline{LBO}$=VDD)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|---|---|---|---|---|---|---|---|---|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address(1) | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

5313 tbl 10

**NOTE:**
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

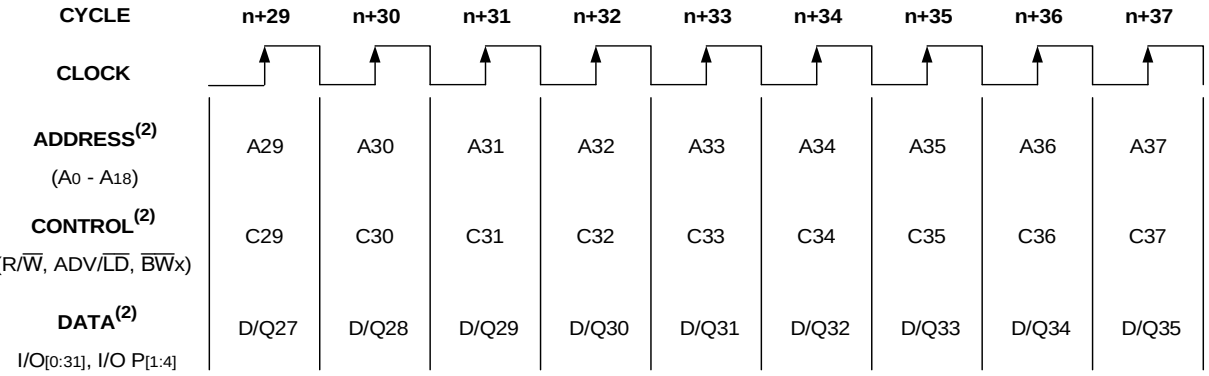
## Linear Burst Sequence Table ($\overline{LBO}$=VSS)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|---|---|---|---|---|---|---|---|---|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address(1) | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

5313 tbl 11

**NOTE:**
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

## Functional Timing Diagram(1)




5313drw 03

**NOTES:**
1. This assumes $\overline{CEN}$, $\overline{CE}_1$, $CE_2$, $\overline{CE}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

## Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles(2)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(1) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | H | L | L | L | X | X | X | Load read |
| n+1 | X | X | H | X | L | X | X | X | Burst read |
| n+2 | $A_1$ | H | L | L | L | X | L | $Q_0$ | Load read |
| n+3 | X | X | L | H | L | X | L | $Q_{0+1}$ | Deselect or STOP |
| n+4 | X | X | H | X | L | X | L | $Q_1$ | NOOP |
| n+5 | $A_2$ | H | L | L | L | X | X | Z | Load read |
| n+6 | X | X | H | X | L | X | X | Z | Burst read |
| n+7 | X | X | L | H | L | X | L | $Q_2$ | Deselect or STOP |
| n+8 | $A_3$ | L | L | L | L | L | L | $Q_{2+1}$ | Load write |
| n+9 | X | X | H | X | L | L | X | Z | Burst write |
| n+10 | $A_4$ | L | L | L | L | L | X | $D_3$ | Load write |
| n+11 | X | X | L | H | L | X | X | $D_{3+1}$ | Deselect or STOP |
| n+12 | X | X | H | X | L | X | X | $D_4$ | NOOP |
| n+13 | $A_5$ | L | L | L | L | L | X | Z | Load write |
| n+14 | $A_6$ | H | L | L | L | X | X | Z | Load read |
| n+15 | $A_7$ | L | L | L | L | L | X | $D_5$ | Load write |
| n+16 | X | X | H | X | L | L | L | $Q_6$ | Burst write |
| n+17 | $A_8$ | H | L | L | L | X | X | $D_7$ | Load read |
| n+18 | X | X | H | X | L | X | X | $D_{7+1}$ | Burst read |
| n+19 | $A_9$ | L | L | L | L | L | L | $Q_8$ | Load write |

5313 tbl 12

**NOTES:**
1. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and $CE_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or $CE_2$ = L.
2. H = High; L = Low; X = Don't Care; Z = High Impedance.

## Read Operation(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | H | L | L | L | X | X | X | Address and Control meet setup |
| n+1 | X | X | X | X | L | X | X | X | Clock Setup Valid |
| n+2 | X | X | X | X | X | X | L | $Q_0$ | Contents of Address $A_0$ Read Out |

5313 tbl 13

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and $CE_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or $CE_2$ = L.

## Burst Read Operation(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | H | L | L | L | X | X | X | Address and Control meet setup |
| n+1 | X | X | H | X | L | X | X | X | Clock Setup Valid, Advance Counter |
| n+2 | X | X | H | X | L | X | L | $Q_0$ | Address $A_0$ Read Out, Inc. Count |
| n+3 | X | X | H | X | L | X | L | $Q_{0+1}$ | Address $A_{0+1}$ Read Out, Inc. Count |
| n+4 | X | X | H | X | L | X | L | $Q_{0+2}$ | Address $A_{0+2}$ Read Out, Inc. Count |
| n+5 | $A_1$ | H | L | L | L | X | L | $Q_{0+3}$ | Address $A_{0+3}$ Read Out, Load $A_1$ |
| n+6 | X | X | H | X | L | X | L | $Q_0$ | Address $A_0$ Read Out, Inc. Count |
| n+7 | X | X | H | X | L | X | L | $Q_1$ | Address $A_1$ Read Out, Inc. Count |
| n+8 | $A_2$ | H | L | L | L | X | L | $Q_{1+1}$ | Address $A_{1+1}$ Read Out, Load $A_2$ |

5313 tbl 14

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and $CE_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or $CE_2$ = L.

## Write Operation(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | L | L | L | L | L | X | X | Address and Control meet setup |
| n+1 | X | X | X | X | L | X | X | X | Clock Setup Valid |
| n+2 | X | X | X | X | L | X | X | $D_0$ | Write to Address $A_0$ |

5313 tbl 15

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and $CE_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or $CE_2$ = L.

## Burst Write Operation(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(2) | $\overline{CEN}$ | $\overline{BW}$x | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | L | L | L | L | L | X | X | Address and Control meet setup |
| n+1 | X | X | H | X | L | L | X | X | Clock Setup Valid, Inc. Count |
| n+2 | X | X | H | X | L | L | X | $D_0$ | Address $A_0$ Write, Inc. Count |
| n+3 | X | X | H | X | L | L | X | $D_{0+1}$ | Address $A_{0+1}$ Write, Inc. Count |
| n+4 | X | X | H | X | L | L | X | $D_{0+2}$ | Address $A_{0+2}$ Write, Inc. Count |
| n+5 | $A_1$ | L | L | L | L | L | X | $D_{0+3}$ | Address $A_{0+3}$ Write, Load $A_1$ |
| n+6 | X | X | H | X | L | L | X | $D_0$ | Address $A_0$ Write, Inc. Count |
| n+7 | X | X | H | X | L | L | X | $D_1$ | Address $A_1$ Write, Inc. Count |
| n+8 | $A_2$ | L | L | L | L | L | X | $D_{1+1}$ | Address $A_{1+1}$ Write, Load $A_2$ |

5313 tbl 16

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and $CE_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or $CE_2$ = L.

## Read Operation with Clock Enable Used(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(2) | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | H | L | L | L | X | X | X | Address and Control meet setup |
| n+1 | X | X | X | X | H | X | X | X | Clock n+1 Ignored |
| n+2 | $A_1$ | H | L | L | L | X | X | X | Clock Valid |
| n+3 | X | X | X | X | H | X | L | $Q_0$ | Clock Ignored. Data $Q_0$ is on the bus. |
| n+4 | X | X | X | X | H | X | L | $Q_0$ | Clock Ignored. Data $Q_0$ is on the bus. |
| n+5 | $A_2$ | H | L | L | L | X | L | $Q_0$ | Address $A_0$ Read out (bus trans.) |
| n+6 | $A_3$ | H | L | L | L | X | L | $Q_1$ | Address $A_1$ Read out (bus trans.) |
| n+7 | $A_4$ | H | L | L | L | X | L | $Q_2$ | Address $A_2$ Read out (bus trans.) |

5313 tbl 17

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and $CE_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or $CE_2$ = L.

## Write Operation with Clock Enable Used(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(2) | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | $A_0$ | L | L | L | L | L | X | X | Address and Control meet setup. |
| n+1 | X | X | X | X | H | X | X | X | Clock n+1 Ignored. |
| n+2 | $A_1$ | L | L | L | L | L | X | X | Clock Valid. |
| n+3 | X | X | X | X | H | X | X | X | Clock Ignored. |
| n+4 | X | X | X | X | H | X | X | X | Clock Ignored. |
| n+5 | $A_2$ | L | L | L | L | L | X | $D_0$ | Write Data $D_0$ |
| n+6 | $A_3$ | L | L | L | L | L | X | $D_1$ | Write Data $D_1$ |
| n+7 | $A_4$ | L | L | L | L | L | X | $D_2$ | Write Data $D_2$ |

5313 tbl 18

**NOTES:**
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and $CE_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or $CE_2$ = L.

## Read Operation with Chip Enable Used(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(2) | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O(3) | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | X | X | L | H | L | X | X | ? | Deselected. |
| n+1 | X | X | L | H | L | X | X | ? | Deselected. |
| n+2 | $A_0$ | H | L | L | L | X | X | Z | Address and Control meet setup. |
| n+3 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+4 | $A_1$ | H | L | L | L | X | L | $Q_0$ | Address $A_0$ Read out. Load $A_1$. |
| n+5 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+6 | X | X | L | H | L | X | L | $Q_1$ | Address $A_1$ Read out. Deselected. |
| n+7 | $A_2$ | H | L | L | L | X | X | Z | Address and control meet setup. |
| n+8 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+9 | X | X | L | H | L | X | L | $Q_2$ | Address $A_2$ Read out. Deselected. |

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**NOTES:**
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE_1}$ = L, $\overline{CE_2}$ = L and $CE_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE_1}$ = H, $\overline{CE_2}$ = H or $CE_2$ = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

## Write Operation with Chip Enable Used(1)

| Cycle | Address | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$(2) | $\overline{CEN}$ | $\overline{BWx}$ | $\overline{OE}$ | I/O | Comments |
|---|---|---|---|---|---|---|---|---|---|
| n | X | X | L | H | L | X | X | ? | Deselected. |
| n+1 | X | X | L | H | L | X | X | ? | Deselected. |
| n+2 | $A_0$ | L | L | L | L | L | X | Z | Address and Control meet setup. |
| n+3 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+4 | $A_1$ | L | L | L | L | L | X | $D_0$ | Address $D_0$ Write in. Load $A_1$. |
| n+5 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+6 | X | X | L | H | L | X | X | $D_1$ | Address $D_1$ Write in. Deselected. |
| n+7 | $A_2$ | L | L | L | L | L | X | Z | Address and control meet setup. |
| n+8 | X | X | L | H | L | X | X | Z | Deselected or STOP. |
| n+9 | X | X | L | H | L | X | X | $D_2$ | Address $D_2$ Write in. Deselected. |

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**NOTES:**
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE_1}$ = L, $\overline{CE_2}$ = L and $CE_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE_1}$ = H, $\overline{CE_2}$ = H or $CE_2$ = L.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD}$ = 2.5V±5%)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 5 | µA |
| $\|I_{LI}\|$ | $\overline{LBO}$, JTAG and ZZ Input Leakage Current (1) | $V_{DD}$ = Max., $V_{IN}$ = 0V to $V_{DD}$ | — | 30 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{DDQ}$, Device Deselected | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = +6mA, $V_{DD}$ = Min. | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -6mA, $V_{DD}$ = Min. | 2.0 | — | V |

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**NOTE:**
1. The $\overline{LBO}$, TMS, TDI, TCK and $\overline{TRST}$ pins will be internally pulled to $V_{DD}$, and the ZZ pin will be internally pulled to $V_{SS}$ if they are not actively driven in the application.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1) ($V_{DD}$ = 2.5V±5%)

| Symbol | Parameter | Test Conditions | 200MHz(4) | | 166MHz | | 150MHz | | 133MHz | | 100MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l | Ind | Com'l | Ind | Com'l | Ind | Com'l | Ind | Com'l | Ind | |
| $I_{DD}$ | Operating Power Supply Current | Device Selected, Outputs Open, ADV/$\overline{LD}$ = X, $V_{DD}$ = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = $f_{MAX}$(2) | 275 | 295 | 245 | 265 | 215 | 235 | 195 | 215 | 175 | 195 | mA |
| $I_{SB1}$ | CMOS Standby Power Supply Current | Device Deselected, Outputs Open, $V_{DD}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2,3) | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | mA |
| $I_{SB2}$ | Clock Running Power Supply Current | Device Deselected, Outputs Open, $V_{DD}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = $f_{MAX}$(2,3) | 80 | 100 | 70 | 90 | 60 | 80 | 50 | 70 | 45 | 65 | mA |
| $I_{SB3}$ | Idle Power Supply Current | Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}$, $V_{DD}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = $f_{MAX}$(2,3) | 60 | 80 | 60 | 80 | 60 | 80 | 60 | 80 | 60 | 80 | mA |
| $I_{ZZ}$ | Full Sleep Mode Supply Current | Device Selected, Outputs Open, $\overline{CEN} \leq V_{IH}$, $V_{DD}$ = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = $f_{MAX}$(2,3), ZZ $\geq V_{HD}$ | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | mA |

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**NOTES:**
1. All values are maximum guaranteed values.
2. At f = $f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of 1/$t_{CYC}$; f=0 means no input lines are changing.
3. For I/Os $V_{HD}$ = $V_{DDQ}$ – 0.2V, $V_{LD}$ = 0.2V. For other inputs $V_{HD}$ = $V_{DD}$ – 0.2V, $V_{LD}$ = 0.2V.
4. 200MHz is for 71T75802 only.

## AC Test Load

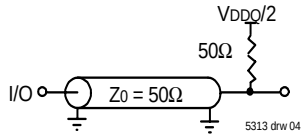



**Figure 1. AC Test Load**

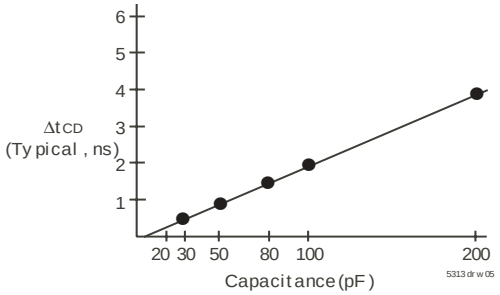



**Figure 2. Lumped Capacitive Load, Typical Derating**

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | 0 to 2.5V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | ($V_{DDQ}$/2) |
| Output Timing Reference Levels | ($V_{DDQ}$/2) |
| AC Test Load | See Figure 1 |

5313 tbl 23

## AC Electrical Characteristics

(VDD = 2.5V +/-5%, Commercial and Industrial Temperature Ranges)

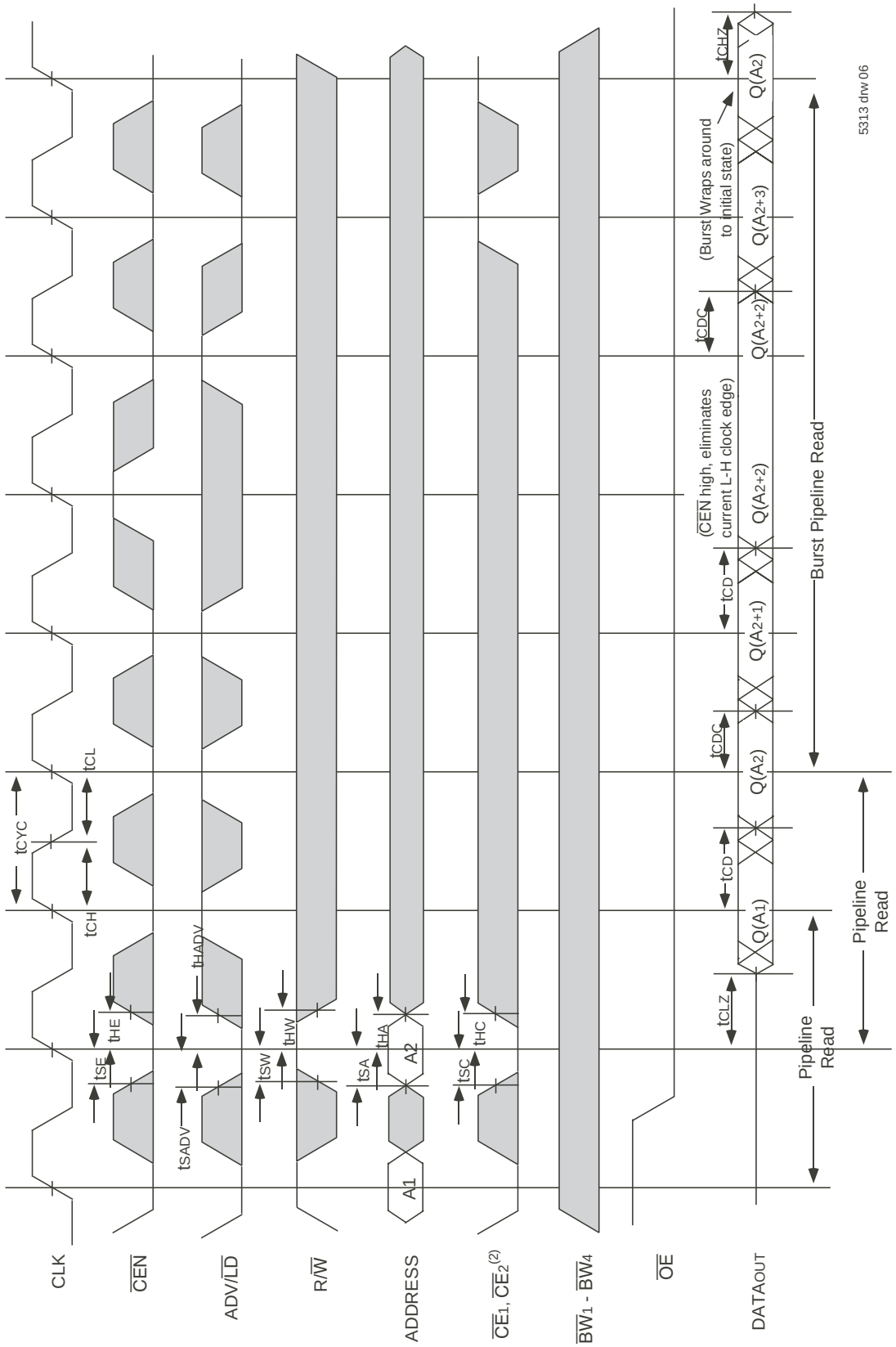
| Symbol | Parameter | 200MHz(6) | | 166MHz | | 150MHz | | 133MHz | | 100MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| | | | | | | | | | | | | |
| $t_{CYC}$ | Clock Cycle Time | 5 | — | 6 | — | 6.7 | — | 7.5 | — | 10 | — | ns |
| $t_F$(1) | Clock Frequency | — | 200 | — | 166 | — | 150 | — | 133 | — | 100 | MHz |
| $t_{CH}$(2) | Clock High Pulse Width | 1.8 | — | 1.8 | — | 2.0 | — | 2.2 | — | 3.2 | — | ns |
| $t_{CL}$(2) | Clock Low Pulse Width | 1.8 | — | 1.8 | — | 2.0 | — | 2.2 | — | 3.2 | — | ns |
| **Output Parameters** | | | | | | | | | | | | |
| $t_{CD}$ | Clock High to Valid Data | — | 3.2 | — | 3.5 | — | 3.8 | — | 4.2 | — | 5 | ns |
| $t_{CDC}$ | Clock High to Data Change | 1.0 | — | 1.0 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_{CLZ}$(3,4,5) | Clock High to Output Active | 1.0 | — | 1.0 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_{CHZ}$(3,4,5) | Clock High to Data High-Z | 1.0 | 3 | 1.0 | 3 | 1.5 | 3 | 1.5 | 3 | 1.5 | 3.3 | ns |
| $t_{OE}$ | Output Enable Access Time | — | 3.2 | — | 3.5 | — | 3.8 | — | 4.2 | — | 5 | ns |
| $t_{OLZ}$(3,4) | Output Enable Low to Data Active | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OHZ}$(3,4) | Output Enable High to Data High-Z | — | 3.2 | — | 3.5 | — | 3.8 | — | 4.2 | — | 5 | ns |
| **Set Up Times** | | | | | | | | | | | | |
| $t_{SE}$ | Clock Enable Setup Time | 1.4 | — | 1.5 | — | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{SA}$ | Address Setup Time | 1.4 | — | 1.5 | — | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{SD}$ | Data In Setup Time | 1.4 | — | 1.5 | — | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{SW}$ | Read/Write (R/$\overline{W}$) Setup Time | 1.4 | — | 1.5 | — | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{SADV}$ | Advance/Load (ADV/$\overline{LD}$) Setup Time | 1.4 | — | 1.5 | — | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{SC}$ | Chip Enable/Select Setup Time | 1.4 | — | 1.5 | — | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{SB}$ | Byte Write Enable ($\overline{BW}$x) Setup Time | 1.4 | — | 1.5 | — | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| **Hold Times** | | | | | | | | | | | | |
| $t_{HE}$ | Clock Enable Hold Time | 0.4 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HA}$ | Address Hold Time | 0.4 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HD}$ | Data In Hold Time | 0.4 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HW}$ | Read/Write (R/$\overline{W}$) Hold Time | 0.4 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HADV}$ | Advance/Load (ADV/$\overline{LD}$) Hold Time | 0.4 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HC}$ | Chip Enable/Select Hold Time | 0.4 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| $t_{HB}$ | Byte Write Enable ($\overline{BW}$x) Hold Time | 0.4 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |

5313 tbl 24

**NOTES:**

1. tF = 1/tCYC.
2. Measured as HIGH above 0.6VDDQ and LOW below 0.4VDDQ.
3. Transition is measured ±200mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that tCHZ (device turn-off) is faster than tCLZ (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because tCLZ is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 2.625V) than tCHZ, which is a Max. parameter (worse case at 70 deg. C, 2.375V)
6. 200MHz is for 71T75802 only.

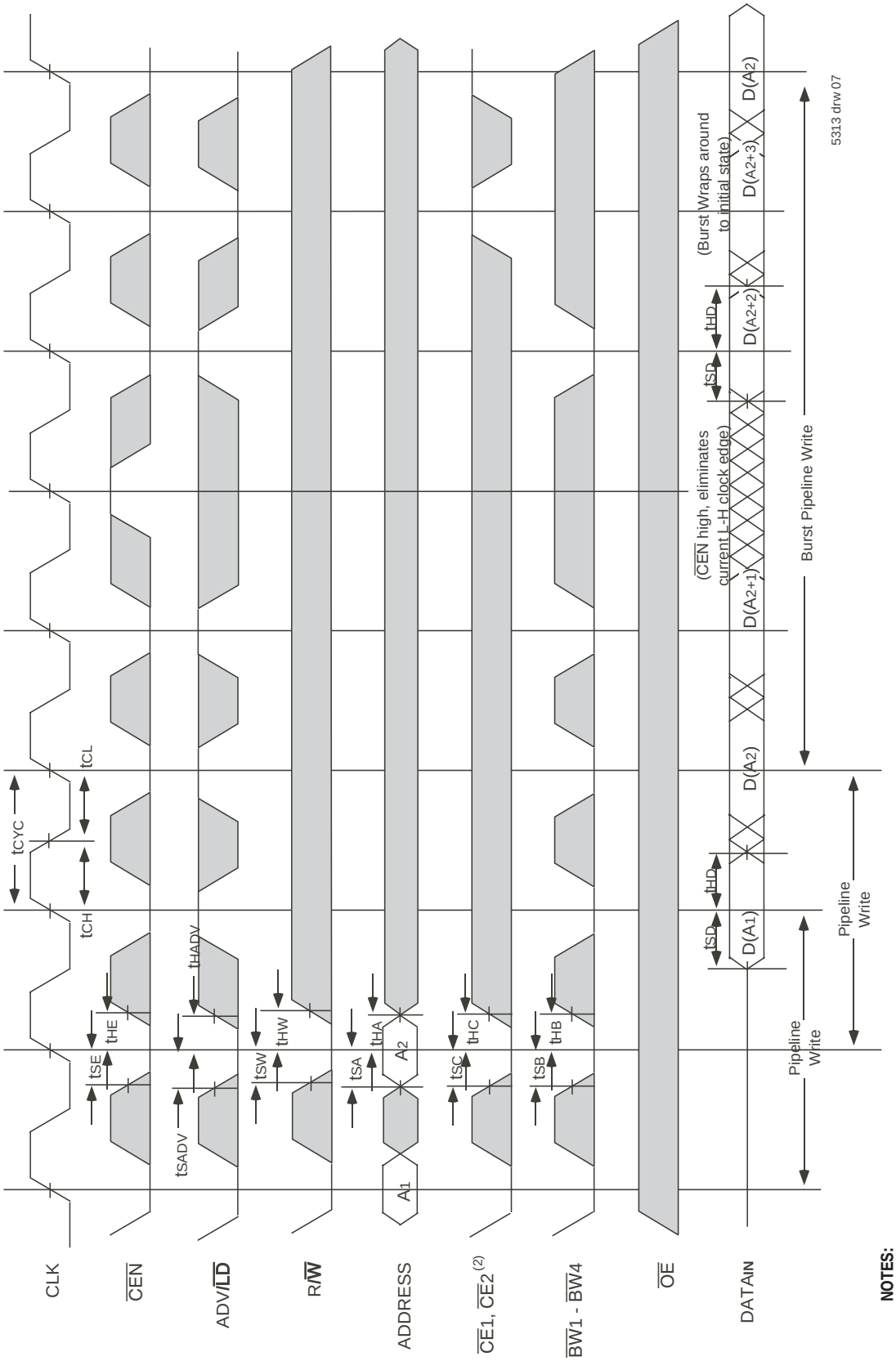
# Timing Waveform of Read Cycle(1,2,3,4)




**NOTES:**

1. Q ($A_1$) represents the first output from the external address $A_1$. Q ($A_2$) represents the first output from the external address $A_2$; Q ($A_{2+1}$) represents the next output data in the burst sequence of the base address $A_2$, etc. where address bits $A_0$ and $A_1$ are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. $CE_2$ timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, $CE_2$ is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.

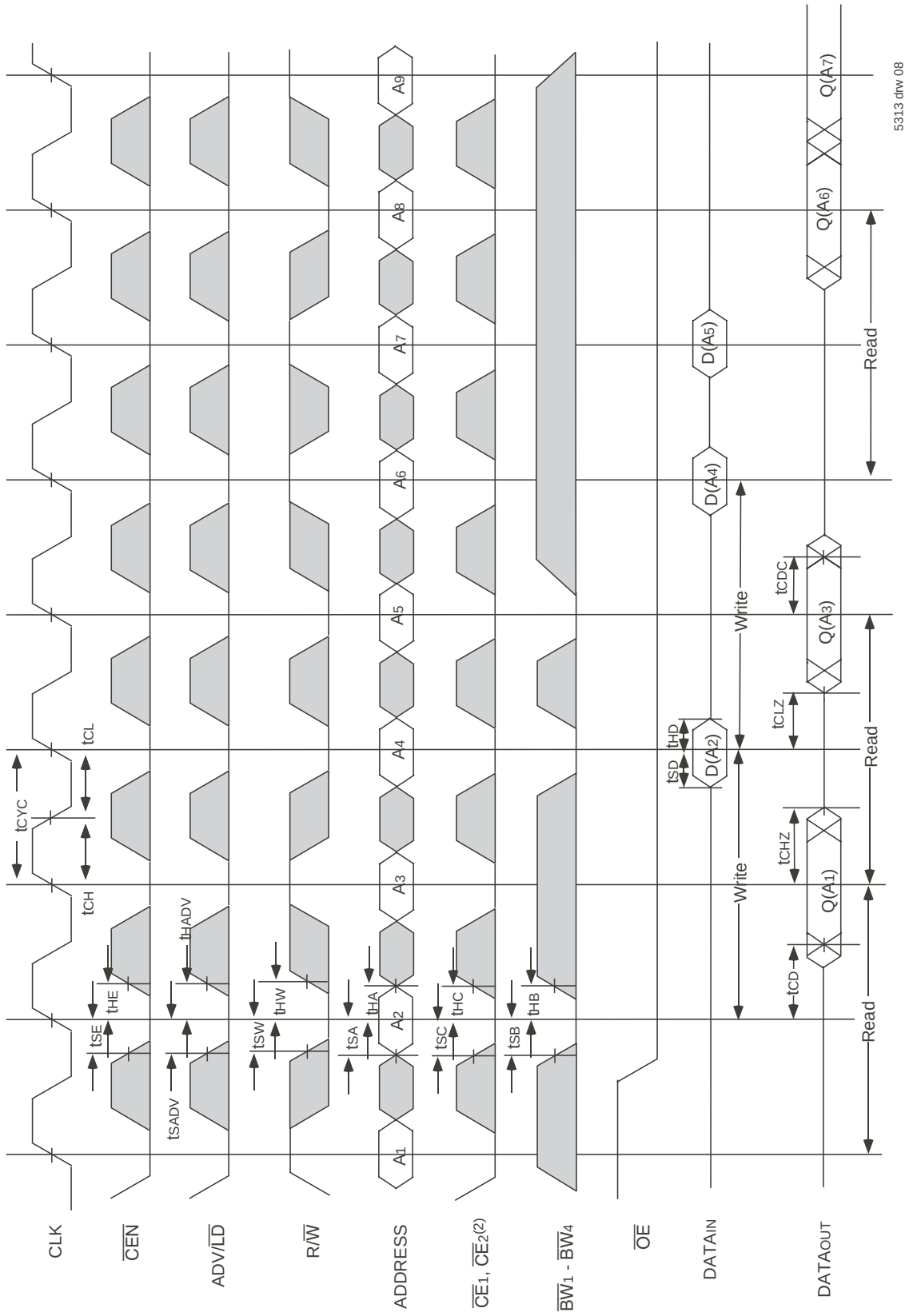
## Timing Waveform of Write Cycles(1,2,3,4,5)




**NOTES:**

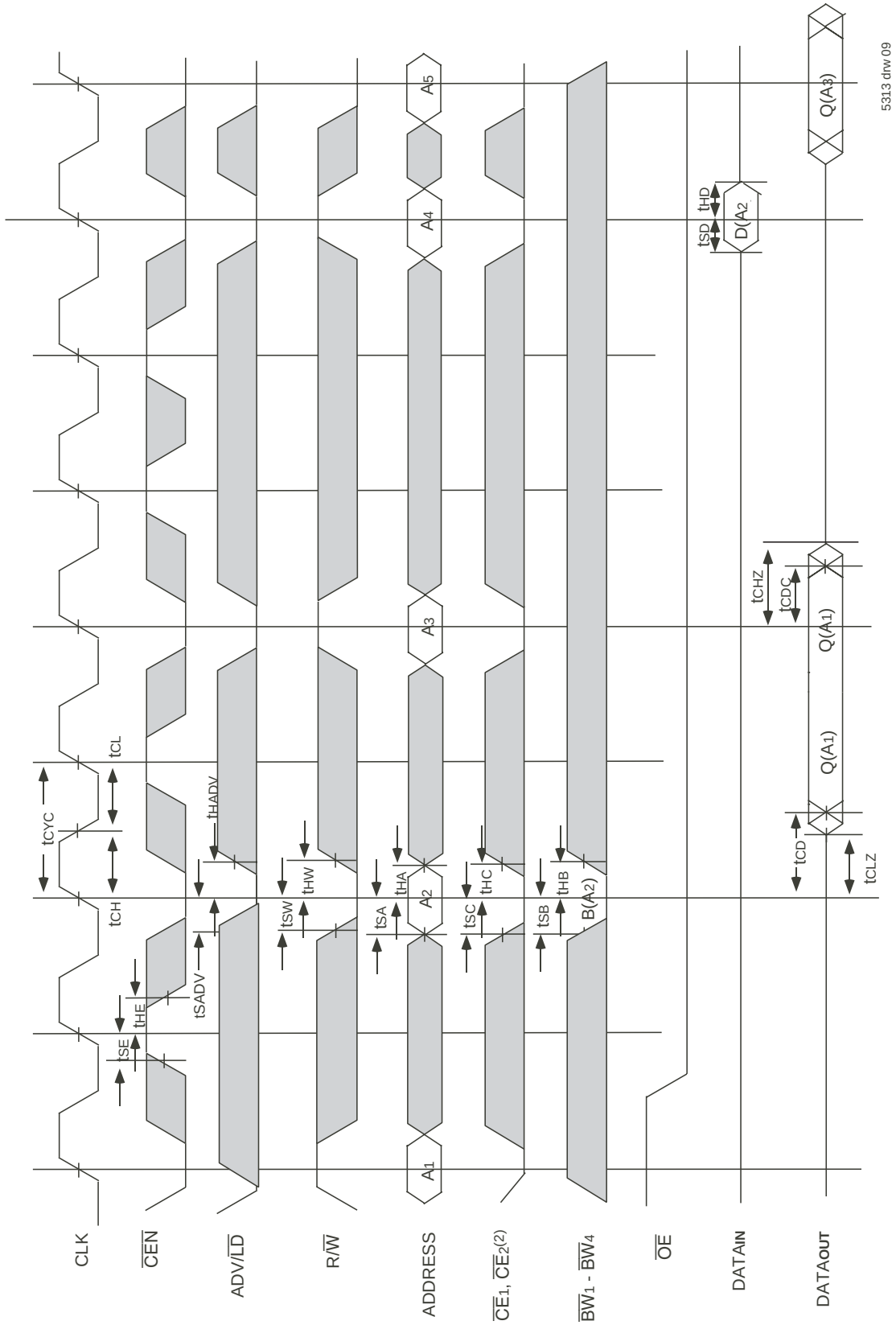
1. D ($A_1$) represents the first input to the external address $A_1$. D ($A_2$) represents the first input to the external address $A_2$; D ($A_{2+1}$) represents the next input data in the burst sequence of the base address $A_2$, etc. where address bits $A_0$ and $A_1$ are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. $CE_2$ timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, $CE_2$ is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals ($\overline{BW}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

# Timing Waveform of Combined Read and Write Cycles(1,2,3)



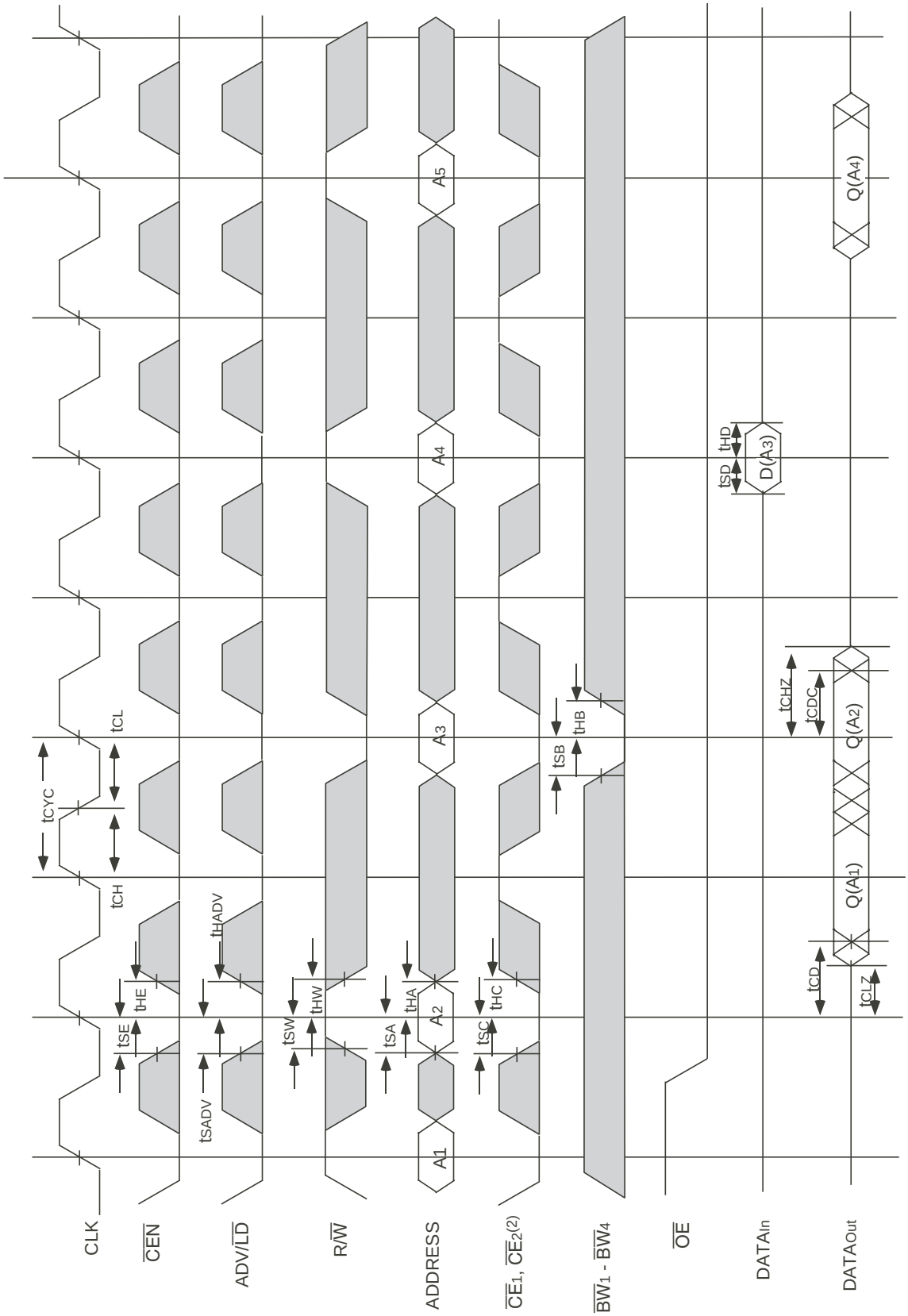

**NOTES:**
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

## Timing Waveform of $\overline{CEN}$ Operation(1,2,3,4)




**NOTES:**
1. Q ($A_1$) represents the first output from the external address $A_1$. D ($A_2$) represents the input data to the SRAM corresponding to address $A_2$.
2. $CE_2$ timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, $CE_2$ is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BWx}$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

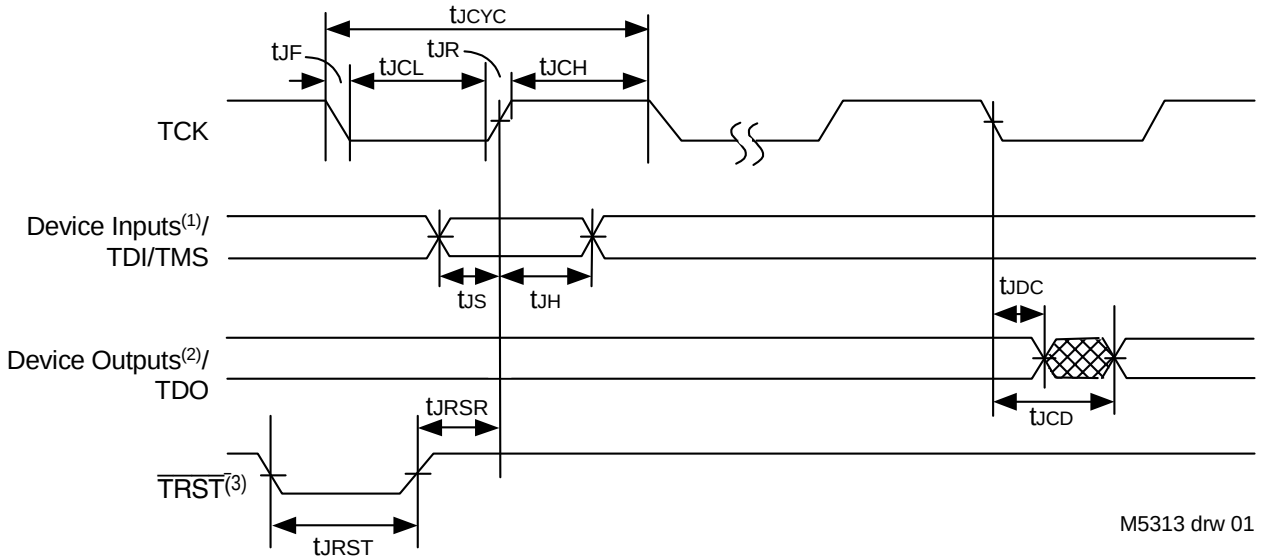
## Timing Waveform of $\overline{CS}$ Operation(1,2,3,4)




**NOTES:**

1. Q ($A_1$) represents the first output from the external address $A_1$. D ($A_3$) represents the input data to the SRAM corresponding to address $A_3$.
2. $CE_2$ timing transitions are identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals. For example, when $\overline{CE_1}$ and $\overline{CE_2}$ are LOW on this waveform, $CE_2$ is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BW}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

## JTAG Interface Specification




**NOTES:**
1. Device inputs = All device inputs except TDI, TMS and $\overline{TRST}$.
2. Device outputs = All device outputs except TDO.
3. During power up, $\overline{TRST}$ could be driven low or not be used since the JTAG circuit resets automatically. $\overline{TRST}$ is an optional JTAG reset.

## JTAG AC Electrical Characteristics(1,2,3,4)

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{JCYC}$ | JTAG Clock Input Period | 100 | — | ns |
| $t_{JCH}$ | JTAG Clock HIGH | 40 | — | ns |
| $t_{JCL}$ | JTAG Clock Low | 40 | — | ns |
| $t_{JR}$ | JTAG Clock Rise Time | — | 5(1) | ns |
| $t_{JF}$ | JTAG Clock Fall Time | — | 5(1) | ns |
| $t_{JRST}$ | JTAG Reset | 50 | — | ns |
| $t_{JRSR}$ | JTAG Reset Recovery | 50 | — | ns |
| $t_{JCD}$ | JTAG Data Output | — | 20 | ns |
| $t_{JDC}$ | JTAG Data Output Hold | 0 | — | ns |
| $t_{JS}$ | JTAG Setup | 25 | — | ns |
| $t_{JH}$ | JTAG Hold | 25 | — | ns |

I5313 tbl 01

**NOTES:**

1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

## Scan Register Sizes

| Register Name | Bit Size |
|---|---|
| Instruction (IR) | 4 |
| Bypass (BYR) | 1 |
| JTAG Identification (JIDR) | 32 |
| Boundary Scan (BSR) | Note (1) |

I5313 tbl 03

**NOTE:**
1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

## JTAG Identification Register Definitions

| Instruction Field | Value | Description |
|---|---|---|
| Revision Number (31:28) | 0x2 | Reserved for version number. |
| IDT Device ID (27:12) | 0x220, 0x222 | Defines IDT part number 71T75602 and 71T75802, respectively. |
| IDT JEDEC ID (11:1) | 0x33 | Allows unique identification of device vendor as IDT. |
| ID Register Indicator Bit (Bit 0) | 1 | Indicates the presence of an ID register. |

I5313 tbl 02

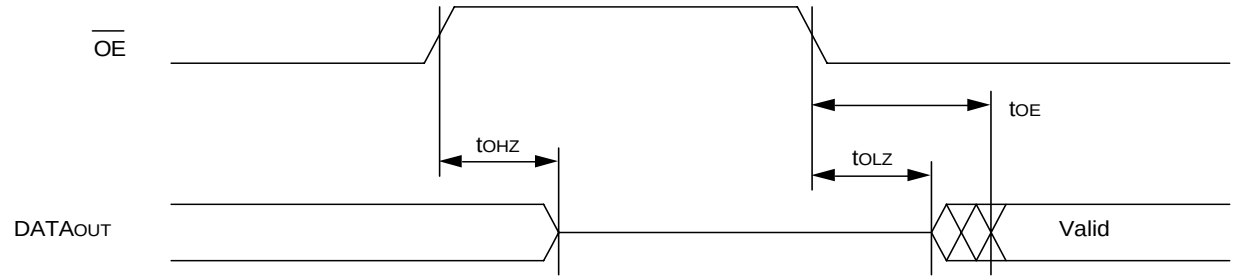
## Available JTAG Instructions

| Instruction | Description | OPCODE |
|---|---|---|
| EXTEST | Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO. | 0000 |
| SAMPLE/PRELOAD | Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(2) and outputs(1) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI. | 0001 |
| DEVICE_ID | Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO. | 0010 |
| HIGHZ | Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state. | 0011 |
| RESERVED | Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions. | 0100 |
| RESERVED | | 0101 |
| RESERVED | | 0110 |
| RESERVED | | 0111 |
| CLAMP | Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO. | 1000 |
| RESERVED | Same as above. | 1001 |
| RESERVED | | 1010 |
| RESERVED | | 1011 |
| RESERVED | | 1100 |
| VALIDATE | Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE std. 1149.1 specification. | 1101 |
| RESERVED | Same as above. | 1110 |
| BYPASS | The BYPASS instruction is used to truncate the boundary scan register as a single bit in length. | 1111 |

I5313 tbl 04

**NOTES:**
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{TRST}$.

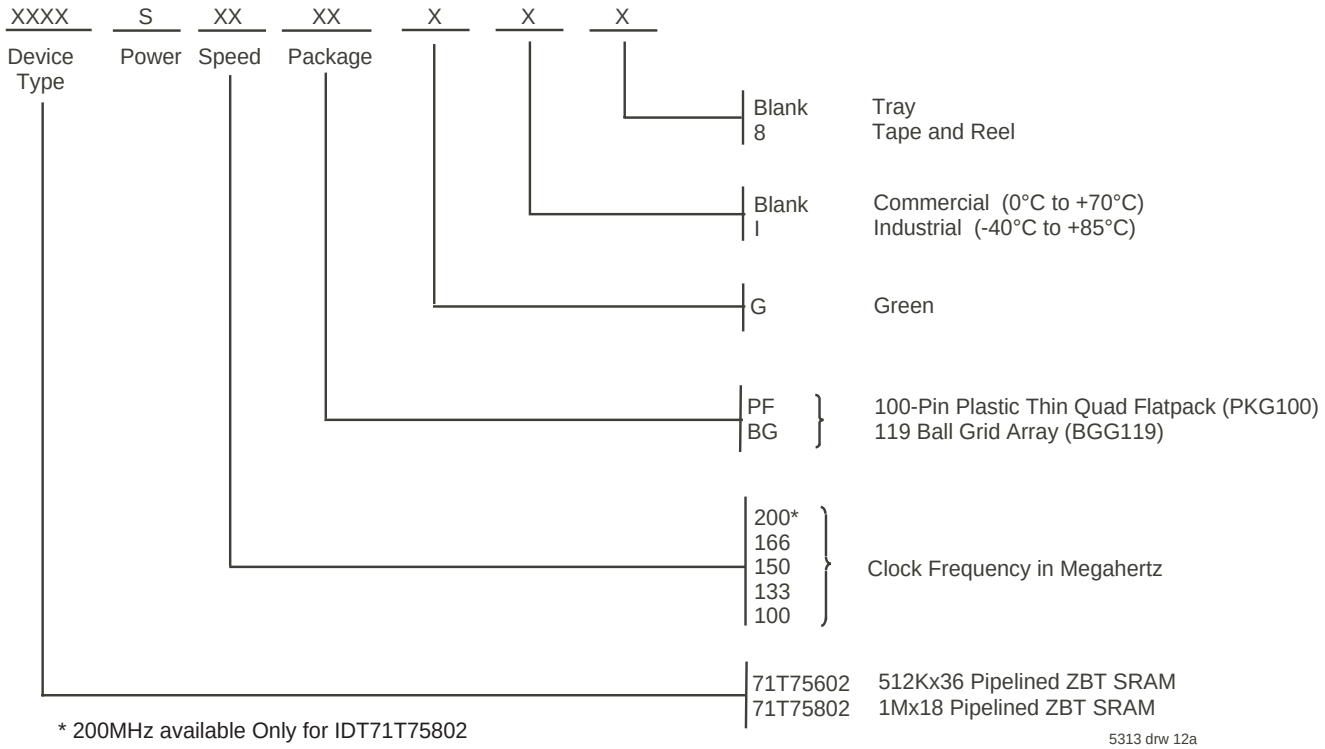
## Timing Waveform of $\overline{OE}$ Operation(1)




**NOTE:**
1. A read operation is assumed to be in progress.

5313 drw 11

## Ordering Information




* 200MHz available Only for IDT71T75802

5313 drw 12a

## Orderable Part Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 100 | 71T75602S100BG | BG119 | PBGA | C |
| | 71T75602S100BG8 | BG119 | PBGA | C |
| | 71T75602S100BGG | BGG119 | PBGA | C |
| | 71T75602S100BGG8 | BGG119 | PBGA | C |
| | 71T75602S100BGGI | BGG119 | PBGA | I |
| | 71T75602S100BGGI8 | BGG119 | PBGA | I |
| | 71T75602S100BGI | BG119 | PBGA | I |
| | 71T75602S100BGI8 | BG119 | PBGA | I |

5313 tbl 27

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 100 | 71T75802S100BG | BG119 | PBGA | C |
| | 71T75802S100BG8 | BG119 | PBGA | C |
| | 71T75802S100BGGI | BGG119 | PBGA | I |
| | 71T75802S100BGGI8 | BGG119 | PBGA | I |
| | 71T75802S100BGI | BG119 | PBGA | I |
| | 71T75802S100BGI8 | BG119 | PBGA | I |

5313 tbl 28

## Orderable Part Information (con't)

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 133 | 71T75602S133BG | BG119 | PBGA | C |
| | 71T75602S133BG8 | BG119 | PBGA | C |
| | 71T75602S133BGG | BGG119 | PBGA | C |
| | 71T75602S133BGG8 | BGG119 | PBGA | C |
| | 71T75602S133BGGI | BGG119 | PBGA | I |
| | 71T75602S133BGGI8 | BGG119 | PBGA | I |
| | 71T75602S133BGI | BG119 | PBGA | I |
| | 71T75602S133BGI8 | BG119 | PBGA | I |
| | 71T75602S133PFG | PKG100 | TQFP | C |
| | 71T75602S133PFG8 | PKG100 | TQFP | C |
| | 71T75602S133PFGI | PKG100 | TQFP | I |
| | 71T75602S133PFGI8 | PKG100 | TQFP | I |
| 150 | 71T75602S150BG | BG119 | PBGA | C |
| | 71T75602S150BG8 | BG119 | PBGA | C |
| | 71T75602S150BGG | BGG119 | PBGA | C |
| | 71T75602S150BGG8 | BGG119 | PBGA | C |
| | 71T75602S150BGGI | BGG119 | PBGA | I |
| | 71T75602S150BGGI8 | BGG119 | PBGA | I |
| | 71T75602S150BGI | BG119 | PBGA | I |
| | 71T75602S150BGI8 | BG119 | PBGA | I |
| | 71T75602S150PFG | PKG100 | TQFP | C |
| | 71T75602S150PFG8 | PKG100 | TQFP | C |
| | 71T75602S150PFGI | PKG100 | TQFP | I |
| | 71T75602S150PFGI8 | PKG100 | TQFP | I |
| 166 | 71T75602S166BG | BG119 | PBGA | C |
| | 71T75602S166BG8 | BG119 | PBGA | C |
| | 71T75602S166BGG | BGG119 | PBGA | C |
| | 71T75602S166BGG8 | BGG119 | PBGA | C |
| | 71T75602S166BGGI | BGG119 | PBGA | I |
| | 71T75602S166BGGI8 | BGG119 | PBGA | I |
| | 71T75602S166BGI | BG119 | PBGA | I |
| | 71T75602S166BGI8 | BG119 | PBGA | I |
| | 71T75602S166PFG | PKG100 | TQFP | C |
| | 71T75602S166PFG8 | PKG100 | TQFP | C |
| | 71T75602S166PFGI | PKG100 | TQFP | I |
| | 71T75602S166PFGI8 | PKG100 | TQFP | I |

5313 tbl 27a

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| 133 | 71T75802S133BG | BG119 | PBGA | C |
| | 71T75802S133BG8 | BG119 | PBGA | C |
| | 71T75802S133BGG | BGG119 | PBGA | C |
| | 71T75802S133BGG8 | BGG119 | PBGA | C |
| | 71T75802S133BGGI | BGG119 | PBGA | I |
| | 71T75802S133BGGI8 | BGG119 | PBGA | I |
| | 71T75802S133BGI | BG119 | PBGA | I |
| | 71T75802S133BGI8 | BG119 | PBGA | I |
| | 71T75802S133PFG | PKG100 | TQFP | C |
| | 71T75802S133PFG8 | PKG100 | TQFP | C |
| | 71T75802S133PFGI | PKG100 | TQFP | I |
| | 71T75802S133PFGI8 | PKG100 | TQFP | I |
| 150 | 71T75802S150BG | BG119 | PBGA | C |
| | 71T75802S150BG8 | BG119 | PBGA | C |
| | 71T75802S150BGG | BGG119 | PBGA | C |
| | 71T75802S150BGG8 | BGG119 | PBGA | C |
| | 71T75802S150BGGI | BGG119 | PBGA | I |
| | 71T75802S150BGGI8 | BGG119 | PBGA | I |
| | 71T75802S150BGI | BG119 | PBGA | I |
| | 71T75802S150BGI8 | BG119 | PBGA | I |
| | 71T75802S150PFG | PKG100 | TQFP | C |
| | 71T75802S150PFG8 | PKG100 | TQFP | C |
| 166 | 71T75802S166BG | BG119 | PBGA | C |
| | 71T75802S166BG8 | BG119 | PBGA | C |
| | 71T75802S166BGG | BGG119 | PBGA | C |
| | 71T75802S166BGG8 | BGG119 | PBGA | C |
| | 71T75802S166BGGI | BGG119 | PBGA | I |
| | 71T75802S166BGGI8 | BGG119 | PBGA | I |
| | 71T75802S166BGI | BG119 | PBGA | I |
| | 71T75802S166BGI8 | BG119 | PBGA | I |
| | 71T75802S166PFG | PKG100 | TQFP | C |
| | 71T75802S166PFG8 | PKG100 | TQFP | C |
| | 71T75802S166PFGI | PKG100 | TQFP | I |
| | 71T75802S166PFGI8 | PKG100 | TQFP | I |
| 200 | 71T75802S200BG | BG119 | PBGA | C |
| | 71T75802S200BG8 | BG119 | PBGA | C |
| | 71T75802S200BGG | BGG119 | PBGA | C |
| | 71T75802S200BGG8 | BGG119 | PBGA | C |
| | 71T75802S200BGI | BG119 | PBGA | I |
| | 71T75802S200BGI8 | BG119 | PBGA | I |
| | 71T75802S200PFG | PKG100 | TQFP | C |
| | 71T75802S200PFG8 | PKG100 | TQFP | C |
| | 71T75802S200PFGI | PKG100 | TQFP | I |
| | 71T75802S200PFGI8 | PKG100 | TQFP | I |

5313 tbl 28a

# Datasheet Document History

| Rev | Date | Pages | Description |
|---|---|---|---|
| 0 | 04/20/00 | | Created New Datasheet |
| 1 | 05/25/00 | Pg.1,14,15,25 | Added 166MHz speed grade offering |
| | | Pg. 1,2,14 | Corrected error in ZZ Sleep Mode |
| | | Pg. 23 | AddBQ165 Package Diagram Outline |
| | | Pg. 24 | Corrected 119BGA Package Diagram Outline. |
| | | Pg. 25 | Corrected topmark on ordering information |
| 2 | 08/23/01 | Pg. 1,2,24 | Removed reference of BQ165 Package |
| | | Pg. 7 | Removed page of the 165 BGA pin configuration |
| | | Pg. 23 | Removed page of the 165 BGA package diagram outline |
| 3 | 10/16/01 | Pg. 6 | Corrected 3.3V to 2.5V in Note 2 |
| | 10/29/01 | Pg. 13 | Improved DC Electrical characteristics-parameters improved: Icc, ISB2, ISB3, IZZ. |
| 4 | 12/21/01 | Pg. 4-6 | Added clarification to JTAG pins, allow for NC. Added 36M address pin locations. |
| | | Pg. 14 | Revised 166MHz $t_{CDC}$(min), $t_{CLZ}$(min) and $t_{CHZ}$(min) to 1.0ns |
| 5 | 06/07/02 | Pg. 1-3,6,13,20,21 | Added complete JTAG functionality. |
| | | Pg. 2,13 | Added notes for ZZ pin internal pulldown and ZZ leakage current. |
| | | Pg. 13,14,24 | Added 200MHz and 225MHz to DC and AC Electrical Characteristics. Updated supply current for Idd, ISB1, ISB3 and Izz. |
| 6 | 11/19/02 | Pg.1-24 | Changed datasheet from Advanced Information to final release. |
| | | Pg.13 | Updated DC Electrical characteristics temperature and voltage range table. |
| 7 | 05/23/03 | Pg.4,5,13,14,24 | Added I-temp to the datasheet. |
| | | Pg.5 | Updated 165 BGA Capacitance table. |
| 8 | 04/01/04 | Pg. 1 | Updated logo with new design. |
| | | Pg. 4,5 | Clarified ambient and case operating temperatures. |
| | | Pg. 6 | Updated pin I/O number order for the 119 BGA. |
| | | Pg. 23 | Updated 119BGA Package Diagram Drawing. |
| 9 | 10/01/08 | Pg. 1,13,14,24 | Deleted 225MHz part, added 200MHz Industrial grade and added green packages. Updated the ordering information by removing the "IDT" notation. |
| 10 | 04/04/12 | Pg. 2,22 | Updated text on Page 2 last paragraph. Added Note to ordering information and updated to include tube or tray and tape & reel. |
| 11 | 10/04/17 | Pg. 1 & 26 | Updated IDT logo from Trademark to Registered |
| | | Pg. 1- 4 | In Features: Added text: "Green parts available, see Ordering Information"<br>Moved the 512Kx36 FBD from page 3 to page 1, moved the 1Mx18 FBD from page 3 to page 2, moved the Pin Description Summary from page 1 to page 3 and moved the Pin Definitions from page 2 to page 4 in accordance with our standard datasheet format |
| | | Pg. 5 & 6 | Updated the TQFP pin configurations for the 512kx36 and 1Mx18 by rotating package pin labels and pin numbers 90 degrees counter clockwise, added IDT logo & in accordance with the packaging code, changed the PK100 designation to PKG100 , changed the text to be in alignment with new diagram marking specs |
| | | Pg. 6 | Removed fBGA capacitance table as this package is no longer offered for this device |
| | | Pg. 12 | Removed "? = don't know" from Burst Write Operation footnote 1 as it does not apply to this table |
| | | Pg. 15 | Updated DC Chars table added footnote 4 & reference 4 for the 512K x 36, 119 BGA 200Mhz speed offered only for the 71T75802 device |
| | | Pg. 16 | Updated AC Chars table added footnote 6 & reference 6 for the 1M x 18, 119 BGA 200Mhz speed offered only for the 71T75802 device |
| | | Pg. 24 | Ordering Information updated to Tray and Green indicator<br>Updated package codes TQFP to PKG100 and BGA to BGG119 |
| | | Pg. 24-25 | Added Orderable Part Information from idt.com |

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71T75802S200BGG8 71T75802S166BGGI8 71T75802S166BG8 71T75802S100BGGI 71T75802S133PFG8 71T75802S166BGGI 71T75602S150BG 71T75802S150BG 71T75602S150PFG8 71T75802S133PFGI8 71T75602S166PFG8 71T75802S200PFG8 71T75802S150BGGI 71T75802S133BGGI 71T75602S133BGGI8 71T75802S150BG8 71T75602S150PFG 71T75602S150BGI 71T75602S133BGGI 71T75602S150BGG 71T75602S150BG8 71T75802S166BG 71T75602S166BG 71T75602S100BGG8 71T75602S100BGI8 71T75602S150BGG8 71T75602S150BGI8 71T75802S133PFG 71T75802S133BGG 71T75802S133BGI 71T75802S133PFGI 71T75802S200PFGI8 71T75802S133BGI8 71T75802S133BGG8 71T75602S133BGI 71T75602S133BGG 71T75602S133PFG 71T75802S200PFGI 71T75802S166BGI 71T75802S166BGG 71T75602S166BGG8 71T75602S166BGI8 71T75602S100BGGI8 71T75602S150BGGI8 71T75602S133BG 71T75802S166PFGI 71T75802S133BG 71T75602S166PFG 71T75602S166BGG 71T75602S166BGI 71T75802S200BGG 71T75802S200BGI 71T75802S200PFG 71T75602S166BG8 71T75802S200BGI8 71T75802S166PFG 71T75802S100BGI8 71T75802S100BG 71T75602S100BG 71T75802S166BGI8 71T75802S166BGG8 71T75602S100BGGI 71T75602S166PFGI8 71T75802S150PFG8 71T75802S166PFGI8 71T75602S133BGG8 71T75602S133BGI8 71T75602S166BGGI 71T75602S133PFG8 71T75802S150BGGI8 71T75802S100BGGI8 71T75602S133PFGI 71T75602S150PFGI8 71T75802S100BGI 71T75802S200BG 71T75602S100BGI 71T75602S100BGG 71T75602S150PFGI 71T75602S166PFGI 71T75602S166BGGI8 71T75802S166PFG8 71T75802S200BG8 71T75802S133BGGI8 71T75602S150BGGI 71T75802S150PFG 71T75802S100BG8 71T75802S133BG8 71T75602S100BG8 71T75602S133PFGI8 71T75802S150BGG 71T75802S150BGI 71T75602S133BG8 71T75802S150BGI8 71T75802S150BGG8 71T75802S200BGGI8

ООО «ЛайфЭлектроникс» “LifeElectronics” LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

*Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.*

*С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров*

*Мы предлагаем:*

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

*В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.*

*Конструкторский отдел помогает осуществить:*

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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*Email: org@lifeelectronics.ru*

***www.lifeelectronics.ru***