

MCP2210

USB-to-SPI Protocol Converter with GPIO (Master Mode)

Features:

Universal Serial Bus (USB)

- Supports Full-Speed USB (12 Mb/s)
- Human Interface Device (HID) device
- 128-Byte Buffer to Handle Data Throughput:
 - 64-byte transmit
 - 64-byte receive
- Fully Configurable VID, PID Assignments and String Descriptor (factory programming also available)
- Bus Powered (factory default) or Self-Powered (can be selected through special USB commands)
- USB 2.0 Compliant

USB Driver and Software Support

- Uses Standard HID Drivers (built-in support on Windows[®] XP, Vista, 7, Linux and Mac OS[®])
- Configuration Utility for Device's Power-up Configuration
- Utility for USB-SPI Communication, GPIO Manipulation and Miscellaneous Features Usage

SPI Master Peripheral

- Supports all Four SPI modes (Mode 0, 1, 2, 3)
- · Bit Rates from 1500 bps up to 12 Mbps
- · Configurable Delays for SPI Transactions:
 - Chip Select (assert) to 1st byte of data delay
 - Data to data delay
 - Data to Chip Select (de-assert) delay
- SPI Transactions Lengths of up to 65535 Bytes Long
- Up to 9 Chip Select lines to be used in any combination for a given SPI transaction (the Chip Select lines are shared between GPIOs and alternate function pins; certain GPs – up to 9 of them – can be assigned with the Chip Select functionality)

General Purpose Input/Output (GPIO) Pins

• Nine General Purpose I/O Pins

EEPROM

• 256 Bytes of User EEPROM (accessible through certain USB commands)

Package Types:

The device will be offered in the following packages:

- 20-lead QFN (5 x 5 mm)
- 20-lead SOIC
- 20-lead SSOP



Other

- USB Activity LED Output
- SSPND Output Pin (to signal USB Suspend state)
- USBCFG Output Pin (indicates when the enumeration is completed)
- Operating Voltage: 3.3-5.5V
- Oscillator Input: 12 MHz
- Industrial Operating Temperature: -40°C to +85°C

Block Diagram



1.0 FUNCTIONAL DESCRIPTION

The MCP2210 device is a USB-to-SPI Master converter which enables USB connectivity in applications that have an SPI interface. The device reduces external components by integrating the USB termination resistors.

The MCP2210 also has 256 bytes of integrated user EEPROM.

The MCP2210 has nine general purpose input/output pins. Seven pins have alternate functions to indicate USB and communication status. See Table 1-1 and **Section 1.6 "GP Module"** for details about the pin functions.

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QFN	SOIC, SSOP	Symbol	Туре	Standard Functic (GPIO)	Alternate Functio (Chip Selects)	Alternate Functio (dedicated functio	Description
1	4	RST	I	_	_	—	Reset input
2	5	GP0	I/O	GPIO0	CS0	—	General Purpose I/O
3	6	GP1	I/O	GPIO1	CS1	—	General Purpose I/O
4	7	GP2	I/O	GPIO2	CS2	USB Suspend	General Purpose I/O
5	8	GP3	I/O	GPIO3	CS3	SPI Transfer Traffic LED	General Purpose I/O
6	9	MOSI	0	—	—	—	SPI Master output
7	10	GP4	I/O	GPIO4	CS4	USB Low Power	General Purpose I/O
8	11	SCK	0	—	—	—	SPI Clock output
9	12	GP5	I/O	GPIO5	CS5	USB Configured	General Purpose I/O
10	13	MISO	I	_	_	—	SPI Master input
11	14	GP6	I/O	GPIO6	CS6	External Interrupt	General Purpose I/O
12	15	GP7	I/O	GPIO7	CS7	SPI Bus Release ACK	General Purpose I/O
13	16	GP8	I/O	GPIO8	CS8	SPI Bus Release REQ	General Purpose I/O
14	17	Vusb	USB	—	—	—	USB Regulator output
15	18	D-	USB	—	—	—	USB D-
16	19	D+	USB	—	—	—	USB D+
17	20	Vss	GND	_	_		Ground
18	1	VDD	Р	—	—		Power
19	2	OSC1	I	_			Oscillator input
20	3	OSC2	0	_	_	—	Oscillator output

1.1 Supported Operating Systems

The following operating systems are supported:

- Windows XP/Vista/7
- Linux
- Mac OS

1.1.1 ENUMERATION

The MCP2210 will enumerate as a USB device after Power-on Reset (POR). The device enumerates as a Human Interface Device (HID) only.

1.1.1.1 Human Interface Device (HID)

The MCP2210 enumerates as an HID, so the device can be configured and all the other functionalities can be controlled. A DLL package that facilitates I/O control through a custom interface is supplied by Microchip and is available on the product landing page.

1.2 Control Module

The control module is the heart of the MCP2210. All other modules are tied together and controlled via the control module. The control module manages the data transfers between the USB and the SPI, as well as command requests generated by the USB host controller, and commands for controlling the function of the SPI and I/O.

1.2.1 SPI INTERFACE

The control module interfaces to the SPI and USB modules.

1.2.2 INTERFACING TO THE DEVICE

The MCP2210 can be accessed for reading and writing via USB host commands. The device cannot be accessed and controlled via the SPI interface.

1.3 SPI Module

The MCP2210 SPI module provides the MOSI, MISO and SCK signals to the outside world. The module has the ability to control the GP pins (as Chip Select) only if these pins are configured for Chip Select operation.

1.3.1 SPI MODULE FEATURES

The SPI module has the following configurable features:

- Bit rates
- Delays
- Chip Select pin assignments (up to 9 Chip Select lines)

All the above features are available for customization using certain USB commands.

1.3.2 SPI MODULE POWER-UP CONFIGURATION

Default parameters:

- 1 Mbit
- 4 bytes to transfer per SPI transaction
- · GP1 as Chip Select line

1.4 USB Protocol Controller

The USB controller in the MCP2210 is full-speed USB 2.0 compliant.

- HID only device used for:
 - SPI transfers
 - I/O control
 - EEPROM access
 - Chip configuration manipulation
- 128-byte buffer to handle data for SPI transfers
 - 64-byte transmit
 - 64-byte receive
- Fully configurable VID, PID assignments, string descriptors (stored on-chip) and chip power-up settings (default chip settings and SPI transfer parameters)
- · Bus powered or self-powered

1.4.1 DESCRIPTORS

The string descriptors are stored internally in the MCP2210 and they can be changed so when the chip enumerates, the host gets the customer's own product and manufacturer names. They can be customized to the user's needs by using the Microchip provided configuration utility or a custom built application that will send the proper USB commands for storing the new descriptors into the chip.

1.4.2 USB EVENTS

The MCP2210 provides support for signaling important USB-related events such as:

- USB Suspend and Resume these states are signaled on the GP2, if the pin is configured for its dedicated function
 - USB Suspend mode is entered when a suspend signaling event is detected on the USB bus
 - USB Resume is signaled when one of the following events is occurring:
 - a) Resume signaling is detected or generated
 - b) A USB Reset signal is detected
 - c) A device Reset occurs
- USB device enumerated successfully (this state is signaled if the GP4 is configured for its dedicated function)
- USB Low-Power mode

1.5 USB Transceiver

The MCP2210 has a built-in, USB 2.0, full-speed transceiver internally connected to the USB module.

The USB transceiver obtains power from the VUSB pin, which is internally connected to a 3.3V internal regulator. The best electrical signal quality is obtained when VUSB is locally bypassed with a high-quality ceramic capacitor.

The internal 3.3V regulator draws power from the VDD pin. In certain scenarios, where VDD is lower than 3.3V+ internal LDO dropout, the VUSB pin must be tied to an external regulated 3.3V. This will allow the USB transceiver to work correctly, while the I/O voltage in the rest of the system can be lower than 3.3V. As an example, in a system where the MCP2210 is used and the I/O required is of 2.2V, the VDD of the chip will be tied to the 2.2V digital power rail, while the VUSB pin must be connected to a regulated 3.3V power supply.

1.5.1 INTERNAL PULL-UP RESISTORS

The MCP2210 device has built-in pull-up resistors designed to meet the requirements for full-speed USB.

1.5.2 MCP2210 POWER OPTIONS

The following are the main power options for the MCP2210:

- USB Bus Powered (5V)
- Self Powered (from 3.3V to 5V), while the VUSB pin is supplied with 3.3V (regulated). If the VDD is powered with 5V, then the VUSB will be powered by the internal regulator and the VUSB pin will need only a decoupling capacitor

1.5.2.1 Internal Power Supply Details

MCP2210 offers various options for power supply. To meet the required USB signaling levels, MCP2210 device incorporates an internal LDO used solely by the USB transceiver, in order to present the correct D+/D voltage levels.

Figure 1-1 shows the internal connections of the USB transceiver LDO in relation with the VDD power supply rail. The output of the USB transceiver LDO is tied to the VUSB line.

A capacitor connected to the VUSB pin is required if the USB transceiver LDO provides the 3.3V supply to the transceiver.

FIGURE 1-1: N

MCP2210 INTERNAL POWER SUPPLY DETAILS



The provided VDD voltage has a direct influence on the voltage levels present on the GPIO and SPI module pins (GP8-GP0, MOSI, MISO and SCK). When VDD is 5V, all of these pins will have a logical '1' around 5V with the variations specified in Section 4.1 "DC Characteristics".

For applications that require a 3.3V logical '1' level, VDD must be connected to a power supply providing the 3.3V voltage. In this case, the internal USB transceiver LDO cannot provide the required 3.3V power. It is necessary to also connect the VUSB pin of the MCP2210 to the 3.3V power supply rail. This way, the USB transceiver is powered up directly from the 3.3V power supply.

1.5.2.2 USB Bus Powered (5V)

In Bus Power Only mode, the entire power for the application is drawn from the USB (see Figure 1-2). This is effectively the simplest power method for the device.

FIGURE 1-2: BUS POWER ONLY



In order to meet the inrush current requirements of the USB 2.0 specifications, the total effective capacitance appearing across VBUS and ground must be no more than 10 μ F. If it is more than 10 μ F, some kind of inrush limiting is required. For more details on Inrush Current Limiting, see the current *Universal Serial Bus Specification*.

According to the USB 2.0 specification, all USB devices must also support a Low-Power Suspend mode. In the USB Suspend mode, devices must consume no more than 500 μA (or 2.5 mA for high powered devices that are remote wake-up capable) from the 5V VBUS line of the USB cable.

The host signals the USB device to enter Suspend mode by stopping all USB traffic to that device for more than 3 ms.

The USB bus provides a 5V voltage. However, the USB transceiver requires 3.3V for the signaling (on D+ and D- lines).

During USB Suspend mode, the D+ or D- pull-up resistor must remain active, which will consume some of the allowed suspend current budget (500 μ A/2.5 mA).

The VUSB pin is required to have an external bypass capacitor. It is recommended that the capacitor be a ceramic cap, between 0.22 and 0.47 $\mu F.$

Figure 1-3 shows a circuit where the MCP2210 internal LDO is used to provide 3.3V to the USB transceiver.

The voltage on the VDD affects the voltage levels onto the GP and SPI module pins (GP8-GP0, MOSI, MISO and SCK). With VDD at 5V, these pins will have a logic '1' of 5V with the variations specified in **Section 4.1 "DC Characteristics"**.

FIGURE 1-3: TYPICAL POWER SUPPLY OPTION USING THE 5V PROVIDED BY THE USB



1.5.2.3 3.3V – Self Powered

Typically, many embedded applications are using 3.3V or lower power supplies. When such an option is available in the target system, MCP2210 can be powered up (VDD) from the existing power supply rail. The typical connections for MCP2210 powered from 3.3V rail are shown in Figure 1-4.

In this example MCP2210 has both VDD and VUSB lines tied to the 3.3V rail. These tied connections disable the internal USB transceiver LDO of the MCP2210 to regulate the power supply on VUSB pin. Another consequence is that the '1' logical level on the GP and SPI pins will be at the 3.3V level, in accordance with the variations specified in Section 4.1 "DC Characteristics".



USING AN EXTERNALLY PROVIDED 3.3V POWER SUPPLY



1.6 GP Module

The GP module features nine I/O lines.

1.6.1 CONFIGURABLE PIN FUNCTIONS

The pins can be configured as:

- GPIO individually configurable, general purpose input or output
- Chip Select pins used by the SPI module
- Alternate function pins used for miscellaneous features such as:
 - SSPND USB Suspend and Resume states
 - USBCFG indicates USB configuration status
 - LOWPWR signals when the host does not accept the requirements (presented during enumeration) and the chip is not configured. In this mode, the whole system powered from the USB host should draw up to 100 mA.
 - External Interrupt Input used to count external events
 - SPI bus Release Request used to request SPI bus access from the MCP2210
 - SPI bus Release Acknowledge used to acknowledge when the MCP2210 has released the SPI bus
 - LED indicates SPI traffic led

1.6.1.1 GPIO Pins Function

The GP pins (if enabled for GPIO functionality) can be used as digital inputs/outputs.

These pins can be read (both inputs and outputs) and written (only the outputs).

1.6.1.2 Chip Select Pins Function

The GP pins (if enabled for the Chip Select functionality) are controlled by the SPI module. Their Idle/Active value is determined by the SPI transfer parameters.

1.6.1.3 SSPND Pin Function

The GP2 pin (if enabled for this functionality) reflects the USB state (Suspend/Resume). The pin is active 'low' when the Suspend state has been issued by the USB host.

Likewise, the pin drives 'high' after the Resume state is achieved.

This pin allows the application to go into Low-Power mode when USB communication is suspended, and switches to a full active state when USB activity is resumed.

1.6.1.4 USBCFG Pin Function

The GP5 pin (if enabled for this functionality) starts out 'high' during power-up or after Reset, and goes 'low' after the device successfully configures to the USB. The pin will go 'high' when in Suspend mode and 'low' when the USB resumes.

1.6.1.5 LOWPWR Pin Function

The GP4 pin (if enabled for this functionality) starts out 'low' during power-up or after Reset, and goes 'high' after the device successfully configures to the USB. The pin will go 'low' when in Suspend mode and 'high' when the USB resumes.

1.6.1.6 External Interrupt Input Pin Function

The GP4 pin (if enabled for this functionality) is used as an interrupt input pin and it will count interrupt events such as:

- Falling edges
- Rising edges
- Low-logic pulses
- High-logic pulses

1.6.1.7 SPI Bus Release Request Pin Function

The GP8 pin (if enabled for this functionality) is used by an external device to request the MCP2210 to release the SPI bus. This way, more than one SPI master can have access to the SPI slave chips on the bus. When this pin is driven 'low', the MCP2210 will examine the request and, based on the conditions and internal logic, it might release the SPI bus. If there is an ongoing SPI transfer taking place at the moment when an external device requests the bus, MCP2210 will release it after the transfer is completed or if the USB host cancels the current SPI transfer.

1.6.1.8 SPI Bus Release Acknowledge Pin Function

The GP7 pin (if enabled for this functionality) is used by the MCP2210 to signal back if the SPI bus was released. When a SPI bus release request is registered by the MCP2210, based on the condition and internal logic, the chip might release the bus. The bus is released immediately if there is no SPI transfer taking place, or it will do so after the current SPI transfer is finished or cancelled by the USB host.

1.6.1.9 LED Pin Function

The GP3 pin (if enabled for this functionality) is used as an SPI traffic indication. When an SPI transfer is taking place (active state for this pin), this pin will be driven 'low'. When there is no SPI traffic taking place, the pin is in its inactive state or logic 'high'.

1.7 EEPROM Module

The EEPROM module is a 256-byte array of nonvolatile memory. The memory locations are accessed for read/write operations solely via USB host commands. The memory cells for data EEPROM are rated to endure thousands of erase/write cycles, up to 100K for EEPROM.

Data retention without refresh is conservatively estimated to be greater than 40 years.

1.8 Reset/POR

1.8.1 RESET PIN

The $\overline{\text{RST}}$ pin provides a method for triggering an external Reset of the device. A Reset is generated by holding the pin low. MCP2210 has a noise filter in the Reset path which detects and ignores small pulses.

1.8.2 POR

A POR pulse is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the $\overline{\text{RST}}$ pin through a resistor (1 k Ω to 10 k Ω) to VDD. This will eliminate external RC components usually needed to create a POR delay.

When the device starts normal operation (i.e., exits the Reset condition), the device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not achieved, the device must be held in Reset until the operating conditions are met.

1.9 Oscillator

The input clock must be 12 MHz to provide the proper frequency for the USB module. USB full-speed is nominally 12 Mb/s. The clock input accuracy is $\pm 0.25\%$ (2,500 ppm maximum).

FIGURE 1-5: QUARTZ CRYSTAL OPERATION







2.0 MCP2210 FUNCTIONAL DESCRIPTION

The MCP2210 uses NVRAM to store relevant chip settings. These settings are loaded by the chip during the power-up process and they are used for GP designation and SPI transfers.

The NVRAM settings at power-up (or Reset) are loaded into the RAM portion of the chip and they can be altered through certain USB commands. This is very useful since it allows dynamic reconfiguring of the GPs or SPI transfer parameters. A practical example to illustrate this mechanism is a system which uses at least two SPI slave chips and the GPs in the MCP2210 for various GPIO purposes. The default SPI settings might be ok for one of the SPI slave chips, but not for the 2nd. At first, the PC application will make an SPI transfer to the first chip, using the NVRAM copy of the SPI settings. Then, by sending a certain USB command, the SPI transfer settings residing in RAM will be altered in order to fit the SPI transfer requirements of the second chip.

Also, if the altered SPI transfer settings are needed to be the default power-up (or Reset) settings for SPI, the user can send a series of USB commands in order to store the current (RAM) SPI settings into NVRAM. In this way, these new settings will be the power-up default SPI settings.

The NVRAM settings and EEPROM contents can be protected by password access means, or they can be permanently locked without any possible further modification.

2.1 MCP2210 NVRAM Settings

The chip settings that can be stored in the NVRAM area are as follows:

- SPI transfer parameters:
 - SPI bit rate
 - SPI mode
 - Idle Chip Select values
 - Active Chip Select values
 - SPI transfer configurable delays
 - Number of bytes to read/write for the given SPI transfer
- GP designation:
 - GPIO
 - Chip Select
 - Dedicated function
- GPIO default direction (applies only to those GPs designated as GPIOs)
- GPIO default output value (applies only to those GPs designated as output GPIOs)

- · Chip mode flags:
 - Remote wake-up capability
 - External Interrupt Pin mode (applies only when GP6 is designated for this function)
 - SPI bus release enable/disable enable/ disable the release of the SPI bus when there is no SPI transfer (useful when more than one SPI master on the bus)
- NVRAM Access mode:
 - Full access (no protection factory default)
 - Password protection
 - Permanently locked
- Password (relevant when password protection mechanism is active)

The specified settings are loaded at power-up or Reset moments, and they can be altered through certain USB commands.

When a NVRAM conditional access method is already in place, such as password protection, the NVRAM settings modification is permitted only when the user has supplied the correct password for the chip. The RAM settings can be altered even when a password protection or permanent lock mechanism are in place. This allows the user to communicate with various SPI slave chips without knowing the password, but it will not allow the modification of the power-up default settings in NVRAM.

2.2 SPI Transfers

The MCP2210 device provides advanced SPI communication features such as configurable delays and multiple Chip Select support.

The configurable delays are related to certain aspects of the SPI transfer:

• The delay between the assertion of Chip Select(s) and the first data byte (Figure 2-1)

FIGURE 2-1: CHIP SELECT TO DATA DELAY



• The delay between subsequent data bytes (Figure 2-2)

FIGURE 2-2: DATA-TO-DATA DELAY



• The delay between the end of the last byte (of the SPI transfer) and the de-assertion of the Chip Select(s)





For a particular SPI transfer, the user can choose any number (out of the available ones) of Chip Select pins. The SPI transfer parameters contain two fields where the user will specify the Chip Select values when the SPI transfer is active/idle. This mechanism allows the user to specify any combination of Chip Select values for the Idle mode and some other combination for the Active mode (SPI transfer active).

3.0 USB COMMANDS/RESPONSES DESCRIPTION

MCP2210 implements the HID interface for all the device-provided functionalities. The chip uses a command/response mechanism for the USB engine. This means that for every USB command sent (by the USB host) to the MCP2210, it will always reply with a response packet.

The MCP2210 USB commands can be grouped by their provided features as follows:

NVRAM Settings

- Read/Write NVRAM related parameters
- Send access password

- Read/Write RAM Settings (copied from NVRAM at power-up or Reset):
 - Read/Write (volatile RAM stored settings) SPI transfer settings
 - Read/Write (volatile RAM stored settings) chip settings
 - Read/Write (volatile RAM stored settings) GPIO direction
 - Read/Write (volatile RAM stored settings) GPIO output values
- Read/Write EEPROM Memory
- External Interrupt Pin (GP6) Event Status
- SPI Data Transfer:
 - Read/Write SPI transfer data
 - Cancels the ongoing SPI transfer
 - SPI bus release manipulation
- Chip Status and Unsupported commands

3.1 NVRAM Settings

The commands in this category are related to the NVRAM settings manipulation.

3.1.1 SET CHIP SETTINGS POWER-UP DEFAULT

TABLE 3-1:COMMAND STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – command code
1	0x20 – Set Chip Settings Power-up Default – sub-command code
2	0x00 – Reserved
3	0x00 – Reserved
4	GP0 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	 Dedicated Function pin = 0x02
5	GP1 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	 Dedicated Function pin = 0x02
6	GP2 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	 Dedicated Function pin = 0x02
7	GP3 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	 Dedicated Function pin = 0x02
8	GP4 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	 Dedicated Function pin = 0x02

Byte Index	Meaning			
9	GP5 Pin Designation			
	• GPIO = 0x00			
	Chip Selects = 0x01			
	 Dedicated Function pin = 0x02 			
10	GP6 Pin Designation			
	• GPIO = 0x00			
	Chip Selects = 0x01			
	Dedicated Function pin = 0x02			
11	GP7 Pin Designation			
	• GPIO = 0x00			
	Chip Selects = 0x01			
	Dedicated Function pin = 0x02			
12	GP8 Pin Designation			
	• GPIO = 0x00			
	Chip Selects = 0x01			
	Dedicated Function pin = 0x02			
13	Default GPIO Output – 16-bit value (low byte):			
	• MSB – – – – – LSB			
	GP7VAL GP6VAL GP5VAL GP4VAL GP3VAL GP2VAL GP1VAL GP0VAL			
14	Default GPIO Output – 16-bit value (high byte):			
	• MSB – – – – – LSB			
	X X X X X X X GPOVAL			
45	where x = Don't Cale			
15	Default GPIO Direction – To-bit value (low byte):			
	GP7DIR GP6DIR GP5DIR GP4DIR GP3DIR GP2DIR GP1DIR GP0DIR			
16	Default GPIO Direction – 16-bit value (high byte):			
	• MSB LSB			
	x x x x x x x GP8DIR			

TABLE 3-1: COMMAND STRUCTURE (CONTINUED)

Byte Index	Meaning
17	Other Chip Settings – Enable/Disable Wake-up, Interrupt Counting, SPI Bus Release Options
	• Bit 7 – Don't Care
	• Bit 6 – Don't Care
	Bit 5 – Don't Care
	 Bit 4 – Remote Wake-up Enabled/Disabled
	- 0 – Remote Wake-up Disabled
	- 1 – Remote Wake-up Enabled
	Bit 3 – Dedicated Function – Interrupt Pin mode
	Bit 2 – Dedicated Function – Interrupt Pin mode
	Bit 1 – Dedicated Function – Interrupt Pin mode
	- b111 - Reserved
	- b110 - Reserved
	- b101 - Reserved
	- b100 – Count High Pulses
	- b011 – Count Low Pulses
	- b010 – Count Rising Edges
	- b001 – Count Falling Edges
	- b000 – No Interrupt Counting
	 Bit 0 – SPI Bus Release Enable
	 0 = SPI Bus is Released Between Transfer
	 1 = SPI Bus is Not Released by the MCP2210 between transfers
18	NVRAM Chip Parameters Access Control
	0x00 – Chip settings not protected
	 0x40 – Chip settings protected by password access
	0x80 – Chip settings permanently locked
19	New Password Character 0 (Note 1)
20	New Password Character 1 (Note 1)
21	New Password Character 2 (Note 1)
22	New Password Character 3 (Note 1)
23	New Password Character 4 (Note 1)
24	New Password Character 5 (Note 1)
25	New Password Character 6 (Note 1)
26	New Password Character 7 (Note 1)
27-63	Reserved (fill with 0x00)
Note 1: Wh	en the password does not need to change, this field must be filled with 0 (it applies to (byte index 19 to 26).

TABLE 3-1: COMMAND STRUCTURE (CONTINUED)

3.1.1.1 Responses

TABLE 3-2: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x60 - Set Chip NVRAM Parameters - echos back the given command code
1	0xFB – Blocked Access – The provided password is not matching the one stored in the chip, or the settings are permanently locked.
2-63	Don't Care

TABLE 3-3: RESPONSE 2 STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – echos back the given command code
1	0x00 – Command Completed Successfully – settings written
2	0x20 – Sub-command Echoed Back for Set Chip Settings Power-up Default code
3-63	Don't Care

FIGURE 3-1: SET CHIP SETTINGS POWER-UP DEFAULT LOGIC FLOW



3.1.2 SET SPI POWER-UP TRANSFER SETTINGS

TABLE 3-4: COMMAND STRUCTURE

Byte Index	Meaning			
0	0x60 – Set Chip NVRAM Parameters – command code			
1	0x10 – Set SPI Power-up Transfer Settings – sub-command code			
2	0x00 – Reserved			
3	0x00 – Reserved			
4	Bit Rate (Byte 3) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte = 0x00			
5	Bit Rate (Byte 2) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte = 0x1B			
6	Bit Rate (Byte 1) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte = 0xB7			
7	Bit Rate (Byte 0) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte = 0x00			
8	Idle Chip Select Value – 16-bit value (low byte): • MSB – – – – LSB CS7 CS6 CS5 CS4 CS3 CS2 CS1 CS0			
9	Idle Chip Select Value – 16-bit value (high byte): • MSB – – – – LSB x x x x CS8			
10	Active Chip Select Value – 16-bit value (low byte): • MSB – – – – LSB CS7 CS6 CS5 CS4 CS3 CS2 CS1 CS0			
11	Active Chip Select Value – 16-bit value (high byte): • MSB – – – – LSB x x x x x x x CS8			
12	 Chip Select to Data Delay (quanta of 100 μs) – 16-bit value (low byte) <u>Example</u>: If a 500 μs delay between the CS being asserted and the first byte of data is required, the value will be 0x0005. Fill this byte position with: 0x05 			
13	 Chip Select to Data Delay (quanta of 100 μs) – 16-bit value (high byte) Example: If a 500 μs delay between the CS being asserted and the first byte of data is required, the value will be 0x0005. Fill this byte position with 0x00 			
14	 Last Data Byte to CS (de-asserted) delay (quanta of 100 µs) – 16-bit value (low byte) Example: If a 500 µs delay between the last data byte sent and the CS being de-asserted is required, the value will be 0x0005. Fill this byte position with: 0x05 			
15	 Last Data Byte to CS (de-asserted) delay (quanta of 100 μs) – 16-bit value (high byte) Example: If a 500 μs delay between the last data byte sent and the CS being de-asserted is required, the value will be 0x0005. Fill this byte position with: 0x00 			
16	Delay Between Subsequent Data Bytes (quanta of 100 μs) – 16-bit value (low byte) Example: If a 500 μs delay between two consecutive data bytes is required, the value will be 0x0005. - Fill this byte position with: 0x05			

IADLE 3-4	COMMAND STRUCTURE (CONTINUED)
Byte Index	Meaning
17	Delay Between Subsequent Data Bytes (quanta of 100 μs) – 16-bit value (high byte) <u>Example</u> : If 500 μs delay between two consecutive data bytes is required, the value will be 0x0005.
18	Bytes to Transfer per SPI Transaction – 16-bit value (low byte) <u>Example</u> : If an SPI transaction of 1250 bytes long is required, the corresponding hex value will be 0x04E2.
	- Fill this byte position with: 0xE2
19	Bytes to Transfer per SPI Transaction – 16-bit value (high byte) <u>Example</u> : If an SPI transaction of 1250 bytes long is required, the corresponding hex value will be 0x04E2.
	- Fill this byte position with: 0x04
20	SPI Mode • 0x00 – SPI mode 0 • 0x01 – SPI mode 1 • 0x02 – SPI mode 2 • 0x03 – SPI mode 3
21 - 63	Reserved – fill with 0x00

TABLE 3-4: COMMAND STRUCTURE (CONTINUED)

3.1.2.1 Responses

TABLE 3-5: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – echos back the given command code
1	0xFB – Blocked Access – Access password has not been provided or the settings are permanently locked.
2-63	Don't Care

TABLE 3-6: RESPONSE 2 STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – echos back the given command code
1	0xF8 – USB Transfer in Progress – settings not written
2	0x10 – Sub-command Echoed Back – set SPI power-up transfer settings
3-63	Don't Care

TABLE 3-7: RESPONSE 3 STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – echos back the given command code
1	0x00 – Command Completed Successfully – settings written
2	0x10 – Sub-command Echoed Back for Set SPI Power-up Transfer Settings code
3-63	Don't Care



3.1.3 SET USB POWER-UP KEY PARAMETERS

TABLE 3-8: COMMAND STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – command code
1	0x30 – Set USB Power-up Key Parameters – sub-command code
2	0x00 – Reserved
3	0x00 – Reserved
4	VID – 16-bit value (low byte)
5	VID – 16-bit value (high byte)
6	PID – 16-bit value (low byte)
7	VID – 16-bit value (high byte)
8	Chip Power Option (as per USB specs – Chapter 9)
	 Bit 7 – Host Powered (1 = yes; 0 = no)
	 Bit 6 – Self Powered (1 = yes; 0 = no)
	Bit 5 – Remote Wake-up Capable
	Bit 4 – Reserved – fill with 0
	• Bit 3 – Reserved – fill with 0
	• Bit 2 – Reserved – fill with 0
	• Bit 1 – Reserved – fill with 0
	• Bit 0 – Reserved – fill with 0
	Note: Only bit 6 or bit 7 should be set, not both.
9	Requested Current Amount from USB Host (quanta of 2 mA)
	Example: For 100 mA fill this byte index with 50 (in decimal) or 0x32.
10-63	Reserved – fill with 0x00

3.1.3.1 Responses

TABLE 3-9: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – echo back the given command code
1	0xFB – Blocked Access – The provided password is not matching the one stored in the chip or the settings are permanently locked.
2-63	Don't Care

TABLE 3-10: RESPONSE 2 STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – echo back the given command code
1	0x00 – Command Completed Successfully – Settings written
2	0x30 – Sub-command Echoed Back for Set USB Power-up Key Parameters code
3-63	Don't Care



3.1.4 SET USB MANUFACTURER NAME

TABLE 3-11: COMMAND STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – command code
1	0x50 – Set USB Manufacturer Name – sub-command code
2	0x00 – Reserved
3	0x00 – Reserved
4	Total USB String Descriptor Length (this is the length of the Manufacturer string, multiplied by 2 + 2) <u>Example</u> : "Microchip Technology Inc." has 25 Unicode characters.
	- The value to be filled in is: (25 x 2) + 2 = 52 (decimal) = 0x34
5	USB String Descriptor ID – always fill with 0x03
6	 Unicode Character Low Byte <u>Example</u>: For the "Microchip Technology Inc." Unicode string, place here the low byte of the Unicode for character "M". Fill this index with 0x4D
7	 Unicode Character High Byte <u>Example</u>: For the "Microchip Technology Inc." Unicode string, place here the high byte of the Unicode for character "M". Fill this index with 0x00
8-63	Fill in the remaining Unicode characters in the string

3.1.4.1 Responses

TABLE 3-12: RESPONSE 1 STRUCTURE

B	yte dex	Meaning
	0	0x60 – Set Chip NVRAM Parameters – echos back the given command code
	1	0xFB – Blocked Access – The provided password is not matching the one stored in the chip or the settings are permanently locked.
2.	-63	Don't Care

TABLE 3-13: RESPONSE 2 STRUCTURE

Byte Index	Meaning
0	0x60 - Set Chip NVRAM Parameters - echos back the given command code
1	0x00 – Command Completed Successfully – settings written
2	0x50 – Sub-command Echoed Back for Set USB Manufacturer Name code
3-63	Don't Care





3.1.5 SET USB PRODUCT NAME

TABLE 3-14: COMMAND STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – command code
1	0x40 – Set USB Product Name – sub-command code
2	0x00 – Reserved
3	0x00 – Reserved
4	Total USB String Descriptor Length (this is the length of the Product string multiplied by 2 + 2) <u>Example</u> : "MCP2210 USB to SPI Master" has 25 Unicode characters.
	- The value to be filled in is: (25 * 2) + 2 = 52 (decimal) = 0x34
5	USB String Descriptor ID – always fill with 0x03
6	 Unicode Character Low Byte <u>Example</u>: For the "MCP2210 USB to SPI Master" Unicode string, place here the low byte of the Unicode for character "M". Fill this index with 0x4D
7	 Unicode Character High Byte <u>Example</u>: For the "MCP2210 USB to SPI Master" Unicode string, place here the high byte of the Unicode for character "M". Fill this index with 0x00
8-63	Fill in the remaining Unicode characters in the string

3.1.5.1 Responses

TABLE 3-15: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – echos back the given command code
1	0xFB – Blocked Access – The provided password is not matching the one stored in the chip or the settings are permanently locked.
2-63	Don't Care

TABLE 3-16: RESPONSE 2 STRUCTURE

Byte Index	Meaning
0	0x60 – Set Chip NVRAM Parameters – echos back the given command code
1	0x00 – Command Completed Successfully – settings written
2	0x40 – Sub-command Echoed Back for Set USB Product Name code
3-63	Don't Care





3.1.6 GET SPI POWER-UP TRANSFER SETTINGS

TABLE 3-17: COMMAND STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – command code
1	0x10 – Get SPI Power-up Transfer Settings – sub-command code
2	0x00 – Reserved
3-63	0x00 – Reserved

3.1.6.1 Responses

TABLE 3-18: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – echos back the given command code
1	0x00 – Command Completed Successfully
2	0x10 – Sub-command Echoed Back for Get SPI Power-up Transfer Settings code
3	Don't Care
4	Bit Rate (Byte 3) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3)Example: Bit rate = 12,000,000 bps = 00B7 1B00- This byte position will have a value of = 0x00
5	Bit Rate (Byte 2) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte position will have a value of = 0x1B
6	Bit Rate (Byte 1) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3)Example: Bit rate = 12,000,000 bps = 00B7 1B00- This byte position will have a value of = 0xB7
7	Bit Rate (Byte 0) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte position will have a value of = 0x00
8	Idle Chip Select Value – 16-bit value (low byte): • MSB – – – – LSB CS7 CS6 CS5 CS4 CS3 CS2 CS1 CS0
9	Idle Chip Select Value – 16-bit value (high byte):
	• MSB – – – – – LSB
	x x x x x x CS8
10	Active Chip Select Value – 16-bit value (low byte):
	• MSB LSB
11	Active Chip Select Value – 16-bit value (high byte):
	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
12	 Chip Select to Data Delay (quanta of 100 µs) – 16-bit value (low byte) <u>Example</u>: If a 500 µs delay between the CS being asserted and the first byte of data is required, the value will be 0x0005. This byte position will have a value of: 0x05
13	 Chip Select to Data Delay (quanta of 100 µs) – 16-bit value (high byte) <u>Example</u>: If a 500 µs delay between the CS being asserted and the first byte of data is required, the value will be 0x0005. This byte position will have a value of: 0x00

Byte Index	Meaning
14	Last Data Byte to CS (De-asserted) Delay (quanta of 100 μs) – 16-bit value (low byte) <u>Example</u> : If a 500 μs delay between the last data byte sent and the CS being de-asserted is required, the value will be 0x0005.
15	Last Data Byte to CS (De-asserted) Delay (quanta of 100 μs) – 16-bit value (high byte) <u>Example</u> : If a 500 μs delay between the last data byte sent and the CS being de-asserted is required, the value will be 0x0005.
	- This byte position will have a value of: 0x00
16	Delay Between Subsequent Data Bytes (quanta of 100 μ s) – 16-bit value (low byte) <u>Example</u> : If a 500 μ s delay between two consecutive data bytes is required, the value will be 0x0005.
	- This byte position will have a value of: 0x05
17	Delay Between Subsequent Data Bytes (quanta of 100 μs) – 16-bit value (high byte) <u>Example</u> : If a 500 μs delay between two consecutive data bytes is required, the value will be 0x0005.
	- This byte position will have a value of: 0x00
18	Bytes to Transfer per SPI Transaction – 16-bit value (low byte) <u>Example</u> : If an SPI transaction of 1250 bytes long is required, the corresponding hex value will be 0x04E2.
	- This byte position will have a value of: 0xE2
19	Bytes to Transfer per SPI Transaction – 16-bit value (high byte) <u>Example</u> : If an SPI transaction of 1250 bytes long is required, the corresponding hex value will be 0x04E2 This byte position will have a value of: 0x04
20	SPI Mode
	• UXU2 – SPI mode 2
21 - 63	Don't care

TABLE 3-18: RESPONSE 1 STRUCTURE (CONTINUED)

FIGURE 3-6: GET SPI POWER-UP TRANSFER SETTINGS LOGIC FLOW



3.1.7 GET POWER-UP CHIP SETTINGS

TABLE 3-19: COMMAND STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – command code
1	0x20 – Get Power-up Chip Settings – sub-command code
2	0x00 – Reserved
3-63	0x00 – Reserved

3.1.7.1 Responses

TABLE 3-20: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – echos back the given command code
1	0x00 – Command Completed Successfully
2	0x20 – Sub-command Echoed Back for Get Power-up Chip Settings code
3	Don't Care
4	GP0 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
5	GP1 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
6	GP2 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
7	GP3 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
8	GP4 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
9	GP5 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
10	GP6 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02

Byte Index	Meaning
11	GP7 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
12	GP8 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
13	Default GPIO Output – 16-bit value (low byte):
	• MSB – – – – – LSB
	GP7 GP6 GP5 GP4 GP3 GP2 GP1 GP0
14	Default GPIO Output – 16-bit value (high byte):
	• MSB LSB
	x x x x x x x GP8
	where x = Don't Care
15	Default GPIO Direction – 16-bit value (low byte):
	GP7DIR GP6DIR GP5DIR GP4DIR GP3DIR GP2DIR GP1DIR GP0DIR
16	Default GPIO Direction – 16-bit value (high byte):
17	X X X X X X X GFODIR
17	Pit 7 Don't Caro
	Pit 6 Don't Care
	 Bit 5 — Don't Care Pit 5 — Don't Care
	Bit 4 – Remote Wake up Enabled/Disabled
	- 0 - Pemote Wake-up Litabled
	- 1 - Remote Wake-up Enabled
	Bit 3 – Dedicated Function – Interrunt Pin mode
	Bit 2 – Dedicated Function – Interrupt Pin mode
	Bit 1 – Dedicated Function – Interrupt Pin mode
	- b111 - Reserved
	- b110 - Reserved
	- b101 - Reserved
	- b100 – Count High Pulses
	- b011 – Count Low Pulses
	- b010 - Count Rising Edges
	- b001 – Count Falling Edges
	- b000 – No Interrupt Counting
	Bit 0 – SPI Bus Release Enable
	- 0 = SPI Bus is Released Between Transfer
	- 1 = SPI Bus is not released by the MCP2210 between transfers
18	NVRAM Chip Parameters Access Control
	0x00 – Chip Settings Not Protected
	0x40 – Chip Settings Protected By Password Access
	0x80 – Chip Settings Permanently Locked
19 - 63	Don't Care

TABLE 3-20:	RESPONSE 1 STRUCTURE	(CONTINUED))
		/	

FIGURE 3-7: GET POWER-UP CHIP SETTINGS LOGIC FLOW



3.1.8 GET USB KEY PARAMETERS

TABLE 3-21: COMMAND STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – command code
1	0x30 – Get USB Key Parameters – sub-command code
2	0x00 – Reserved
3-63	0x00 – Reserved

3.1.8.1 Responses

TABLE 3-22: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – echos back the given command code
1	0x00 – Command Completed Successfully
2	0x30 – Sub-command Echoed Back for Get USB Key Parameters code
3-11	Don't care
12	VID low byte
13	VID high byte
14	PID low byte
15	PID high byte
16-28	Don't care
29	Chip Power Option (as per USB specs – Chapter 9)
	Bit 7 – Host Powered
	Bit 6 – Self Powered
	Bit 5 – Remote Wake-up Capable
	Bit 4 – Don't Care
	Bit 3 – Don't Care
	Bit 2 – Don't Care
	Bit 1 – Don't Care
	Bit 0 – Don't Care
30	Requested Current Amount from USB Host (quanta of 2 mA) Example: For 100 mA this byte index will have a value of 50 (in decimal) or 0x32.
31-63	Don't Care

FIGURE 3-8:	GET USB KEY PARAMETERS LOGIC FLOW



3.1.9 GET USB MANUFACTURER NAME

TABLE 3-23: COMMAND STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – command code
1	0x50 – Get USB Manufacturer Name – sub-command code
2	0x00 – Reserved
3-63	0x00 – Reserved

3.1.9.1 Responses

TABLE 3-24: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – echos back the given command code
1	0x00 – Command Completed Successfully
2	0x50 – Sub-command Echoed Back for Get USB Manufacturer Name code
3	Don't Care
4	Total USB String Descriptor Length (this is the length of the Manufacturer string multiplied by 2 + 2) <u>Example</u> : "Microchip Technology Inc." has 25 Unicode characters. The ratio and value is: (25 x 2) + 2 = 52 (desime) = 0x24
	- The fetheved value is: $(25 \times 2) + 2 = 52$ (decimal) = $0x34$
5	USB String Descriptor ID – always 0x03
6	Unicode Character Low Byte <u>Example</u> : For the "Microchip Technology Inc." Unicode string, there will be the low byte of the Unicode for character "M".
	- This byte index will have a value of 0x4D
7	Unicode Character High Byte <u>Example</u> : For the "Microchip Technology Inc." Unicode string, there will be the high byte of the Unicode for character "M".
	- This byte index will have a value of 0x00
8-63	Remaining Unicode Characters

FIGURE 3-9: GET USB MANUFACTURER NAME LOGIC FLOW



3.1.10 GET USB PRODUCT NAME

TABLE 3-25: COMMAND STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – command code
1	0x40 – Get USB Product Name – sub-command code
2	0x00 – Reserved
3-63	0x00 – Reserved

3.1.10.1 Responses

TABLE 3-26: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x61 – Get NVRAM Settings – echos back the given command code
1	0x00 – Command Completed Successfully
2	0x40 – Sub-command Echoed Back for Get USB Product Name code
3	Don't Care
4	Example: "MCP2210 USB to SPI Master" has 25 Unicode characters - The retrieved value is: (25 x 2) + 2 = 52 (decimal) = 0x34
5	USB String Descriptor ID – always 0x03
6	 Unicode Character Low byte <u>Example</u>: For the "MCP2210 USB to SPI Master" Unicode string, there will be the low byte of the Unicode for character "M". - This byte index will have a value of 0x4D
7	 Unicode Character High byte <u>Example</u>: For the "MCP2210 USB to SPI Master" Unicode string, there will be the high byte of the Unicode for character "M". This byte index will have a value of 0x00
8-63	Remaining Unicode Characters

FIGURE 3-10: GET USB PRODUCT NAME LOGIC FLOW



3.1.11 SEND ACCESS PASSWORD

TABLE 3-27: COMMAND STRUCTURE

Byte Index	Meaning
0	0x70 – SEND ACCESS Password – command code
1	0x00 – Reserved
2	0x00 – Reserved
3	0x00 – Reserved
4	Password Character 0
5	Password Character 1
6	Password Character 2
7	Password Character 3
8	Password Character 4
9	Password Character 5
10	Password Character 6
11	Password Character 7
12-63	0x00 – Reserved

3.1.11.1 Responses

TABLE 3-28: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x70 – SEND ACCESS Password – echos back the given command code
1	0x00 – Command Completed Successfully – chip settings not protected
2	Don't Care
3-63	Don't Care

TABLE 3-29: RESPONSE 2 STRUCTURE

Byte Index	Meaning
0	0x70 – SEND ACCESS Password – echos back the given command code
1	0xFC – Access Not Allowed – access rejected
2	Don't Care
3-63	Don't Care

TABLE 3-30: RESPONSE 3 STRUCTURE

Byte Index	Meaning
0	0x70 – SEND ACCESS Password – echos back the given command code
1	0xFD – Access Not Allowed – Chip conditional access is on, the password does not match and the number of attempts is less than the accepted threshold of 5.
2	Don't Care
3-63	Don't Care

TABLE 3-31: RESPONSE 4 STRUCTURE

Byte Index	Meaning
0	0x70 – SEND ACCESS Password – echos back the given command code
1	0xFB – Access Not Allowed – Chip conditional access is on, the password does not match and the number of attempts is above the accepted threshold of 5. The Access Password mechanism is temporarily blocked and no further password access will be accepted until the next power-up.
2	Don't Care
3-63	Don't Care

TABLE 3-32: RESPONSE 5 STRUCTURE

Byte Index	Meaning
0	0x70 – SEND ACCESS Password – echos back the given command code
1	0x00 – Command Completed Successfully – Chip conditional access is on, the supplied password is matching the one stored in the chip's NVRAM.
2	Don't Care
3-63	Don't Care

FIGURE 3-11: SEND ACCESS PASSWORD LOGIC FLOW



3.2 Read/Write RAM Settings

The set of commands/responses described in this section relates to the manipulation of the RAM settings (volatile).

3.2.1 GET (VM) SPI TRANSFER SETTINGS

TABLE 3-33: COMMAND STRUCTURE

Byte Index	Meaning
0	0x41 – Get (VM) SPI Transfer Settings – command code
1	0x00 – Reserved
2	0x00 – Reserved
3-63	0x00 – Reserved

3.2.1.1 Responses

TABLE 3-34: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x41 – Get SPI Transfer Settings (volatile memory)
1	0x00 – Command Completed Successfully
2	Size in Bytes of the SPI Transfer Structure: 17 (in decimal) = 0x11
3	Don't Care
4	Bit Rate (Byte 3) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00
	- This byte position will have a value of = 0x00
5	Bit Rate (Byte 2) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte position will have a value of = 0x1B
6	Bit Rate (Byte 1) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte position will have a value of = 0xB7
7	Bit Rate (Byte 0) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3)Example: Bit rate = 12,000,000 bps = 00B7 1B00- This byte position will have a value of = 0x00
8	Idle Chip Select Value – 16-bit value (low byte):
	• MSB LSB CS7 CS6 CS5 CS4 CS3 CS2 CS1 CS0
9	Idle Chip Select Value – 16-bit value (high byte):
	• MSB LSB x x x x x x CS8
10	Active Chip Select Value – 16-bit value (low byte):
	• MSB LSB CS7 CS6 CS5 CS4 CS3 CS2 CS1 CS0
11	Active Chip Select Value – 16-bit value (high byte):
	• MSB LSB x x x x x x CS8
12	 Chip Select to Data Delay (quanta of 100 μs) – 16-bit value (low byte) Example: If we have 500 μs delay between the CS being asserted and the first byte of data, the value will be 0x0005. This byte position will have a value of: 0x05

Byte Index	Meaning
13	Chip Select to Data Delay (quanta of 100 μs) – 16-bit value (high byte) <u>Example</u> : If we have 500 μs delay between the CS being asserted and the first byte of data, the value will be 0x0005.
	- This byte position will have a value of: 0x00
14	Last Data Byte to CS (de-asserted) Delay (quanta of 100 μs) – 16-bit value (low byte) <u>Example</u> : If we have 500 μs delay between the last data byte sent and the CS being de-asserted, the value will be 0x0005.
	- This byte position will have a value of: 0x05
15	Last Data Byte to CS (de-asserted) Delay (quanta of 100 μs) – 16-bit value (high byte) <u>Example</u> : If we have 500 μs delay between the last data byte sent and the CS being de-asserted, the value will be 0x0005.
	- This byte position will have a value of: 0x00
16	Delay Between Subsequent Data Bytes (quanta of $100 \ \mu$ s) – 16-bit value (low byte) <u>Example</u> : If we have 500 μ s delay between two consecutive data bytes, the value will be 0x0005.
	- This byte position will have a value of: 0x05
17	Delay Between Subsequent Data Bytes (quanta of 100 μs) – 16-bit value (high byte) <u>Example</u> : If we have 500 μs delay between two consecutive data bytes, the value will be 0x0005.
	- This byte position will have a value of: 0x00
18	Bytes to Transfer per SPI Transaction – 16-bit value (low byte) <u>Example</u> : If an SPI transaction of 1250 bytes long is required, the corresponding hex value will be 0x04E2.
	 This byte position will have a value of: 0xE2
19	Bytes to Transfer per SPI Transaction – 16-bit value (high byte) <u>Example</u> : If an SPI transaction of 1250 bytes long is required, the corresponding hex value will be 0x04E2.
	- This byte position will have a value of: 0x04
20	SPI Mode
	• 0x00 – SPI mode 0
	• 0x01 – SPI mode 1
	• 0x02 – SPI mode 2
	0x03 – SPI mode 3
21 - 63	Don't Care

TABLE 3-34: RESPONSE 1 STRUCTURE

FIGURE 3-12: GET (VM) SPI TRANSFER SETTINGS LOGIC FLOW



3.2.2 SET (VM) SPI TRANSFER SETTINGS

TABLE 3-35: COMMAND 1 STRUCTURE

Byte Index	Meaning
0	0x40 – Set (VM) SPI Transfer Settings (volatile memory)
1	0x00 – Reserved
2	0x00 – Reserved
3	0x00 – Reserved
4	Bit Rate (Byte 3) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00
	- This byte position will have a value of = 0x00
5	Bit Rate (Byte 2) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte position will have a value of = 0x1B
6	Bit Rate (Byte 1) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3)
	<u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00
	 This byte position will have a value of = 0xB7
7	Bit Rate (Byte 0) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3)
	Example: Bit rate = $12,000,000$ bps = $00B7$ 1B00
0	- This byte position will have a value of = 0x00
ð	MSB
	CS7 CS6 CS5 CS4 CS3 CS2 CS1 CS0
9	Idle Chip Select Value – 16-bit value (high byte):
	• MSB LSB
	x x x x x x CS8
10	Active Chip Select Value – 16-bit value (low byte):
	• MSB LSB CS7 CS6 CS5 CS4 CS3 CS2 CS1 CS0
11	Active Chip Select Value – 16-bit value (high byte):
	• MSB LSB
10	X X X X X X X X X X
12	Example: If we have 500 us delay between the CS being asserted and the first byte of data, the value
	will be 0x0005.
	- This byte position will have a value of: 0x05
13	Chip Select to Data Delay (quanta of 100 μs) – 16-bit value (high byte) <u>Example</u> : If a 500 μs delay between the CS being asserted and the first byte of data is required, the value will be 0x0005.
	- This byte position will have a value of: 0x00
14	Last Data Byte to CS (de-asserted) Delay (quanta of 100 μs) – 16-bit value (low byte) <u>Example</u> : If a 500 μs delay between the last data byte sent and the CS being asserted is required, the value will be 0x0005.
	- This byte position will have a value of: 0x05
15	Last Data Byte to CS (de-asserted) Delay (quanta of 100 μs) – 16-bit value (high byte) <u>Example</u> : If a 500 μs delay between the last data byte sent and the CS being de-asserted is required, the value will be 0x0005.
	 This byte position will have a value of: 0x00
Byte Index	Meaning
---------------	---
16	Delay Between Subsequent Data Bytes (quanta of 100 μ s) – 16-bit value (low byte) Example: If a 500 us delay between two consecutive data bytes is required, the value will be 0x0005
	 This byte position will have a value of: 0x05
17	 Delay Between Subsequent Data Bytes (quanta of 100 μs) – 16-bit value (high byte) <u>Example</u>: If a 500 μs delay between two consecutive data bytes is required, the value will be 0x0005. This byte position will have a value of: 0x00
18	Bytes to Transfer per SPI Transaction – 16-bit value (low byte) <u>Example</u> : If an SPI transaction of 1250 bytes long is required, the corresponding hex value will be 0x04E2.
	- This byte position will have a value of: 0xE2
19	Bytes to Transfer per SPI Transaction – 16-bit value (high byte) <u>Example</u> : If an SPI transaction of 1250 bytes long is required, the corresponding hex value will be 0x04E2.
	- This byte position will have a value of: 0x04
20	SPI Mode
	• 0x00 – SPI mode 0
	• 0x01 – SPI mode 1
	• 0x02 – SPI mode 2
	• 0x03 – SPI mode 3
21-63	Don't care

TABLE 3-35: COMMAND 1 STRUCTURE (CONTINUED)

3.2.2.1 Responses

TABLE 3-36: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x40 – Echoes back the completed command for Set (VM) SPI Transfer Settings code
1	0x00 – Command Completed Successfully
2	Don't Care
3	Don't Care
4	 Bit Rate (Byte 3) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u>: Bit rate = 12,000,000 bps = 00B7 1B00 This byte position will have a value of = 0x00
5	Bit Rate (Byte 2) - 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3)Example: Bit rate = 12,000,000 bps = 00B7 1B00- This byte position will have a value of = 0x1B
6	Bit Rate (Byte 1) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u> : Bit rate = 12,000,000 bps = 00B7 1B00 - This byte position will have a value of = 0xB7
7	 Bit Rate (Byte 0) – 32-bit value (Byte 0, Byte 1, Byte 2, Byte 3) <u>Example</u>: Bit rate = 12,000,000 bps = 00B7 1B00 This byte position will have a value of = 0x00
8	Idle Chip Select Value – 16-bit value (low byte): • MSB – – – – – LSB CS7 CS6 CS5 CS4 CS3 CS2 CS1 CS0
9	Idle Chip Select Value – 16-bit value (high byte): • MSB – – – – LSB x x x x CS8

Byte Index	Meaning
10	Active Chip Select Value – 16-bit value (low byte):
	• MSB LSB
	CS7 CS6 CS5 CS4 CS3 CS2 CS1 CS0
11	Active Chip Select Value – 16-bit value (high byte):
	$\begin{bmatrix} \bullet MSB LSB \\ x x x x x x x CS8 \end{bmatrix}$
12	Chip Select to Data Delay (quanta of 100 us) – 16-bit value (low byte)
	Example: If we have 500 µs delay between the CS being asserted and the first byte of data, the
	value will be 0x0005.
	- This byte position will have a value of: 0x05
13	Chip Select to Data Delay (quanta of 100 μ s) – 16-bit value (high byte)
	Example: If we have 500 µs delay between the CS being asserted and the first byte of data, the value will be 0x0005
	- This byte position will have a value of: 0x00
14	Last Data Byte to CS (de-asserted) Delay (quanta of 100 us) – 16-bit value (low byte)
	Example: If we have 500 µs delay between the last data byte sent and the CS being de-asserted,
	the value will be 0x0005.
	- This byte position will have a value of: 0x05
15	Last Data Byte to CS (de-asserted) Delay (quanta of 100 µs) – 16-bit value (high byte)
	Example: If we have 500 µs delay between the last data byte sent and the US being de-asserted,
	- This byte position will have a value of: 0x00
16	Delay Between Subsequent Data Bytes (quanta of 100 µs) – 16-bit value (low byte)
	Example: If we have 500 µs delay between two consecutive data bytes, the value will be 0x0005.
	- This byte position will have a value of: 0x05
17	Delay Between Subsequent Data Bytes (quanta of 100 µs) – 16-bit value (low byte)
	Example. If we have 500 µs delay between two consecutive data bytes, the value will be 0x0005.
18	Bytes to Transfer per SPI Transaction - 16-bit value (low byte)
10	Example: If an SPI transaction of 1250 bytes long is required, the corresponding hex value
	will be 0x04E2.
	- This byte position will have a value of: 0xE2
19	Bytes to Transfer per SPI Transaction – 16-bit value (high byte)
	Example: If an SPI transaction of 1250 bytes long is required, the corresponding nex value will be 0x04E2
	- This byte position will have a value of: 0x04
20	SPI Mode
	• 0x00 – SPI mode 0
	• 0x01 – SPI mode 1
	• 0x02 – SPI mode 2
	• 0x03 – SPI mode 3
21 - 63	Don't Care

TABLE 3-37: RESPONSE 2 STRUCTURE

Byte Index	Meaning
0	0x40 – Set (VM) SPI Transfer Settings – echos back the given command code
1	0xF8 – USB transfer in progress – Settings not written
2	Don't Care
3-63	Don't Care

FIGURE 3-13: SET (VM) SPI TRANSFER SETTINGS LOGIC FLOW



3.2.3 GET (VM) CURRENT CHIP SETTINGS

TABLE 3-38: COMMAND STRUCTURE

Byte Index	Meaning
0	0x20 – Get (VM) GPIO Current Chip Settings
1	0x00 – Reserved
2	0x00 – Reserved
3-63	0x00 – Reserved

3.2.3.1 Responses

TABLE 3-39: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x20 – Get (VM) GPIO Current Chip Settings – echos back the given command code
1	0x00 – Command Completed Successfully
2	Don't Care
3	Don't Care
4	GP0 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
5	GP1 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
6	GP2 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
7	GP3 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
8	GP4 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
9	GP5 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01 Dediasted Experimentian pin = 0x02
10	Dedicated Function pin = 0x02
10	
	• GFIO – $0x00$
	• Dedicated Euleric pin = $0x02$
11	GP7 Bin Designation
	• $GPIO = 0 \times 00$
	• Chin Selects = $0x01$
	• Dedicated Function pin = $0x02$
12	GP8 Pin Designation
.2	• $GPIO = 0x00$
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
13	Default GPIO Output – 16-bit value (low byte):
	• MSB LSB
	GP7 GP6 GP5 GP4 GP3 GP2 GP1 GP0

Byte Index	Meaning
14	Default GPIO Output – 16-bit value (high byte):
	• MSB – – – – – LSB
	x x x x x x x GP8
	where x = Don't Care
15	Default GPIO Direction – 16-bit value (low byte):
10	GP7DIR GP6DIR GP5DIR GP4DIR GP3DIR GP2DIR GP1DIR GP0DIR
16	Default GPIO Direction – 16-bit value (high byte):
17	Other Chin Settings – Enable/Disable Wake-up Interrupt Counting SPI Bus Release Ontions
17	• Bit 7 – Don't Care
	Bit 6 – Don't Care
	• Bit 5 – Don't Care
	Bit 4 – Remote Wake-up Enabled/Disabled
	- 0 – Remote Wake-up Disabled
	- 1 – Remote Wake-up Enabled
	Bit 3 – Dedicated Function – Interrupt Pin mode
	Bit 2 – Dedicated Function – Interrupt Pin mode
	Bit 1 – Dedicated Function – Interrupt Pin mode
	- b111 - Reserved
	- b110 - Reserved
	- b101 - Reserved
	- b100 – Count High Pulses
	- b011 – Count Low Pulses
	- b100 – Count High Pulses
	- b011 – Count Low Pulses
	- b010 – Count Rising Edges
	- b001 – Count Falling Edges
	- b000 – No Interrupt Counting
	Bit 0 – SPI Bus Release Enable
	- 0 = SPI Bus is Released between transfer
10	$- \pm - 3r_1$ dus is indice deseu by the indice 22 to between transfers
18	NVKAW Chip Parameters Access Control
	• 0x00 – Chip settings not protected by password access
	 0x80 – Chip settings protected by password access 0x80 – Chip settings permapently locked
19-63	Don't Care
19-00	

TABLE 3-39: RESPONSE 1 STRUCTURE (CONTINUED)

FIGURE 3-14: GET (VM) CURRENT CHIP SETTINGS LOGIC FLOW



3.2.4 SET (VM) CURRENT CHIP SETTINGS

TABLE 3-40: COMMAND STRUCTURE

Byte Index	Meaning
0	0x21 – Set (VM) Current Chip Settings
1	0x00 – Reserved
2	0x00 – Reserved
3	0x00 – Reserved
4	GP0 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
5	GP1 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	 Dedicated Function pin = 0x02
6	GP2 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
7	GP3 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
8	GP4 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02

Byte Index	Meaning
9	GP5 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
10	GP6 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
11	GP7 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
12	GP8 Pin Designation
	• GPIO = 0x00
	Chip Selects = 0x01
	Dedicated Function pin = 0x02
13	Default GPIO Output – 16-bit value (low byte):
	MSB LSB
14	GP7 GP6 GP5 GP4 GP3 GP2 GP1 GP0
14	Default GPIO Output – To-bit value (nigh byte):
	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
	where x = Don't Care
15	Default GPIO Direction – 16-bit value (low byte):
	• MSB LSB
	GP7DIR GP6DIR GP5DIR GP4DIR GP3DIR GP2DIR GP1DIR GP0DIR
16	Default GPIO Direction – 16-bit value (high byte):
	• MSB – – – – – LSB
	x x x x x x x GP8DIR

TABLE 3-40: COMMAND STRUCTURE (CONTINUED)

MCP2210

Byte Index	Meaning
17	Other Chip Settings – Enable/Disable Wake-up, Interrupt Counting, SPI Bus Release Options
	Bit 7 – Don't Care
	Bit 6 – Don't Care
	Bit 5 – Don't Care
	Bit 4 – Remote Wake-up Enabled/Disabled
	- 0 – Remote Wake-up Disabled
	- 1 – Remote Wake-up Enabled
	Bit 3 – Dedicated Function – Interrupt Pin mode
	Bit 2 – Dedicated Function – Interrupt Pin mode
	Bit 1 – Dedicated Function – Interrupt Pin mode
	- b111 - Reserved
	- b110 - Reserved
	- b101 - Reserved
	- b100 – Count High Pulses
	- b011 – Count Low Pulses
	- b100 – Count High Pulses
	- b011 – Count Low Pulses
	- b010 – Count Rising Edges
	- b001 – Count Falling Edges
	- b000 – No Interrupt Counting
	 Bit 0 – SPI Bus Release Enable
	- 0 = SPI Bus is Released between transfer
	 1 = SPI Bus is Not Released by the MCP2210 between transfers
18-63	Reserved (fill in with 0x00)

TABLE 3-40: COMMAND STRUCTURE (CONTINUED)

TABLE 3-41: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x21 – Set (VM) Current Chip Settings – echos back the given command code
1	0x00 – Command Completed Successfully
2	Don't Care
3-63	Don't Care

FIGURE 3-15: SET (VM) CURRENT CHIP SETTINGS LOGIC FLOW



3.2.5 GET (VM) GPIO CURRENT PIN DIRECTION

TABLE 3-42: COMMAND STRUCTURE

Byte Index	Meaning
0	0x33 – Get (VM) GPIO Current Pin Direction
1	0x00 - Reserved
2	0x00 – Reserved
3-63	0x00 – Reserved

3.2.5.1 Responses

TABLE 3-43: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x33 – Get (VM) GPIO Current Pin Direction – echos back the given command code
1	0x00 – Command Completed Successfully
2	Don't Care
3	Don't Care
4	GPIO Direction – 16-bit value (low byte):
	MSB – – – – – LSB GP7DIR GP6DIR GP5DIR GP4DIR GP3DIR GP2DIR GP1DIR GP0DIR
5	GPIO Direction – 16-bit value (high byte):
	• MSB – – – – – LSB
	x x x x x x x GP8DIR
6-63	Don't Care

Note 1: This command will only have an effect on those GPs previously configured as GPIOs.

FIGURE 3-16: GET (VM) GPIO CURRENT PIN DIRECTION LOGIC FLOW



3.2.6 SET (VM) GPIO CURRENT PIN DIRECTION

TABLE 3-44: COMMAND STRUCTURE

Byte Index	Meaning
0	0x32 – Set (VM) GPIO Current Pin Direction
1	0x00 – Reserved
2	0x00 – Reserved
3	0x00 – Reserved
4	GPIO Direction – 16-bit value (low byte):
	• MSB – – – – – LSB GP7DIR GP6DIR GP5DIR GP4DIR GP3DIR GP2DIR GP1DIR GP0DIR
5	GPIO Direction – 16-bit value (high byte):
	• MSB LSB
	x x x x x x x GP8DIR
6-63	0x00 – Reserved

3.2.6.1 Responses

TABLE 3-45: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x32 – Set (VM) GPIO Current Pin Direction – echos back the given command code
1	0x00 – Command Completed Successfully
2	Don't Care
3-63	Don't Care

FIGURE 3-17: SET (VM) GPIO CURRENT PIN DIRECTION LOGIC FLOW



3.2.7 GET GPIO CURRENT PIN VALUE

TABLE 3-46: COMMAND STRUCTURE

Byte Index	Meaning
0	0x31 – Get (VM) GPIO Current Pin Value
1	0x00 – Reserved
2	0x00 – Reserved
3-63	0x00 – Reserved

3.2.7.1 Responses

TABLE 3-47: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x31 – Get (VM) GPIO Current Pin Value – echos back the given command code
1	0x00 – Command Completed Successfully
2	Don't Care
3	Don't Care
4	GPIO Pin Value – 16-bit value (low byte):
	• MSB – – – – – – LSB GP7VAL GP6VAL GP5VAL GP4VAL GP3VAL GP2VAL GP1VAL GP0VAL
5	GPIO Pin Value – 16-bit value (high byte):
	• MSB – – – – – LSB
	x x x x x x GP8VAL
6-63	Don't Care

Note 1: This command will only have an effect on those GPs previously assigned to a GPIO functionality.

FIGURE 3-18: GET GPIO CURRENT PIN VALUE LOGIC FLOW



3.2.8 SET GPIO CURRENT PIN VALUE

TABLE 3-48: COMMAND STRUCTURE

Byte Index	Meaning
0	0x30 – Set (VM) GPIO Current Pin Value
1	0x00 – Reserved
2	0x00 – Reserved
3	0x00 – Reserved
4	GPIO Pin Value – 16-bit value (low byte):
	• MSB – – – – – LSB GP7VAL GP6VAL GP5VAL GP4VAL GP3VAL GP2VAL GP1VAL GP0VAL
5	GPIO Pin Value – 16-bit value (high byte):
	• MSB – – – – – LSB
	x x x x x x GP8VAL
6-63	0x00 – Reserved

Note 1: The GPIO pin value will have an effect only on those GPs previously configured as GPIOs.

3.2.8.1 Responses

TABLE 3-49: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x30 – Set (VM) GPIO Current Pin Value – echos back the given command code
1	0x00 - Command Completed Successfully
2	Don't Care
3	Don't Care
4	Read Back Actual GPIO Pin Value – 16-bit value (low byte):
	• MSB – – – – – LSB GP7VAL GP6VAL GP5VAL GP4VAL GP3VAL GP2VAL GP1VAL GP0VAL
5	Read Back Actual GPIO Pin Value – 16-bit value (high byte):
	• MSB – – – – – LSB
	x x x x x x x GP8VAL
6-63	Don't Care

FIGURE 3-19: SET GPIO CURRENT PIN VALUE LOGIC FLOW



3.3 Read/Write EEPROM Memory

This set of commands/responses described in this section relates to the manipulation of the EEPROM memory.

3.3.1 READ EEPROM MEMORY

TABLE 3-50: COMMAND STRUCTURE

Byte Index	Meaning
0	0x50 – READ EEPROM Memory – command code
1	EEPROM Memory Address to be read
2	0x00 – Reserved
3-63	0x00 – Reserved

3.3.1.1 Responses

TABLE 3-51: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x50 – READ EEPROM Memory – echos back the given command code
1	0x00 – Command Completed Successfully
2	EEPROM Memory Address
3	EEPROM Memory content at the requested address
4-63	Don't Care

FIGURE 3-20: READ EEPROM MEMORY LOGIC FLOW



3.3.2 WRITE EEPROM MEMORY

TABLE 3-52: COMMAND STRUCTURE

Byte Index	Meaning
0	0x51 – WRITE EEPROM Memory – command code
1	EEPROM Memory Address to be written
2	The value to be written to at the given address
3-63	0x00 – Reserved

3.3.2.1 Responses

TABLE 3-53: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x51 – WRITE EEPROM Memory – echos back the given command code
1	0x00 – Command Completed Successfully
2	Don't Care
3-63	Don't Care

TABLE 3-54: RESPONSE 2 STRUCTURE

Byte Index	Meaning
0	0x51 – WRITE EEPROM Memory – echos back the given command code
1	0xFA – EEPROM Write Failure
2	Don't Care
3-63	Don't Care

TABLE 3-55: RESPONSE 3 STRUCTURE

Byte Index	Meaning
0	0x51 – WRITE EEPROM Memory – echos back the given command code
1	0xFB – EEPROM is password protected or permanently locked
2	Don't Care
3-63	Don't Care





3.4 External Interrupt Pin (GP6) Event Status

The External Interrupt pin event status command is used by the USB host to query the external interrupt events recorded by the MCP2210. In order to have the MCP2210 record the number of external interrupt events, GP6 must be configured to have its dedicated function active.

3.4.1 GET (VM) THE CURRENT NUMBER OF EVENTS FROM THE INTERRUPT PIN

TABLE 3-56: COMMAND STRUCTURE

Byte Index	Meaning
0	0x12 – Get (VM) the Current Number of Events From the Interrupt Pin
1	Reset or Not the Event Counter
	 0x00 – reads, then resets the event counter
	 Any other value – the event counter is read, however, the counter is not reset
2-63	0x00 - Reserved

3.4.1.1 Responses

TABLE 3-57: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x12 – Get (VM) the Current Number of Events from the Interrupt Pin – echos back the given command code
1	0x00 – Command Completed Successfully
2	Don't Care
3	Don't Care
4	Interrupt Event Counter – 16-bit value (low byte)
5	Interrupt Event Counter – 16-bit value (high byte)
63-63	Don't Care

FIGURE 3-22: GET (VM) THE CURRENT NUMBER OF EVENTS FROM THE INTERRUPT PIN LOGIC FLOW



3.5 SPI Data Transfer

The set of commands/responses described in this section relates to the SPI data transfer functionality.

3.5.1 TRANSFER SPI DATA

TABLE 3-58: COMMAND STRUCTURE

Byte Index	Meaning
0	0x42 – Transfer SPI Data – command code
1	The number of bytes to be transferred in this packet (from 0 to 60 inclusively)
2	0x00 – Reserved
3	0x00 – Reserved
4-63	The SPI Data to be sent on the data transfer

3.5.1.1 Responses

TABLE 3-59: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x42 – Transfer SPI Data – echos back the given command code
1	0xF7 – SPI Data Not Accepted – SPI bus not available (the external owner has control over it)
2	Don't Care
3-63	Don't Care

TABLE 3-60: RESPONSES 2 STRUCTURE

Byte Index	Meaning
0	0x42 – Transfer SPI Data – echos back the given command code
1	0x00 - SPI Data accepted - Command Completed Successfully - SPI data accepted
2	How many SPI received data bytes the chip is sending back to the host
3	SPI Transfer Engine Status
	 0x20 – SPI transfer started – no data to receive
4-63	SPI Received Data Bytes. The number of data bytes is specified at byte index 2

TABLE 3-61: RESPONSE 3 STRUCTURE

Byte Index	Meaning
0	0x42 – Transfer SPI Data – echos back the given command code
1	0xF8 – SPI Data Not Accepted – SPI transfer in progress – cannot accept any data for the moment
2	Don't Care
3-63	Don't Care

TABLE 3-62: RESPONSE 4 STRUCTURE

Byte Index	Meaning
0	0x42 – Transfer SPI Data – echos back the given command code
1	0x00 - SPI Data accepted - Command Completed Successfully - SPI data accepted
2	How many SPI received data bytes the chip is sending back to the host
3	0x30 – SPI Transfer Engine Status: SPI transfer not finished; received data available
4-63	SPI received data bytes. The number of data bytes is specified at byte index 2

TABLE 3-63: RESPONSE 5 STRUCTURE

Byte Index	Meaning
0	0x42 – Transfer SPI Data – echos back the given command code
1	0x00 – SPI Data accepted – Command Completed Successfully – SPI data accepted
2	How many SPI received data bytes the chip is sending back to the host
3	0x10 – SPI Transfer Engine Status: SPI transfer finished – no more data to send
4-63	SPI received data bytes. The number of data bytes is specified at byte index 2

FIGURE 3-23: TRANSFER SPI DATA LOGIC FLOW



3.5.2 CANCEL THE CURRENT SPI TRANSFER

TABLE 3-64: COMMAND STRUCTURE

Byte Index	Meaning
0	0x11 – CANCEL the current SPI transfer – command code
1	0x00 – Reserved
2	0x00 – Reserved
3-63	0x00 – Reserved

3.5.2.1 Responses

TABLE 3-65: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x11 - CANCEL the current SPI transfer - echos back the given command code
1	0x00 – Command Completed Successfully
2	SPI Bus Release External Request Status
	0x01 – No External Request for SPI Bus Release
	0x00 – Pending External Request for SPI Bus Release
3	SPI Bus Current Owner
	• 0x00 – No Owner
	0x01 – USB Bridge
	0x02 – External Master
4	Attempted Password Accesses – informs the USB host on how many times the NVRAM password was tried
5	Password Guessed
	0x00 – Password Not Guessed
	0x01 – Password Guessed
6-63	Don't Care

FIGURE 3-24: CANCEL THE CURRENT SPI TRANSFER LOGIC FLOW



3.5.3 REQUEST SPI BUS RELEASE

TABLE 3-66: COMMAND STRUCTURE

Byte Index	Meaning
0	0x80 – Request SPI bus Release – command code
1	The value of the SPI Bus Release ACK pin (only if GP7 is assigned to this dedicated function)
2	0x00 – Reserved
3-63	0x00 – Reserved

3.5.3.1 Responses

TABLE 3-67: RESPONSE 1 STRUCTURE

Byte Index	Meaning					
0	0x80 – Request SPI bus Release – echos back the given command code					
1	0x00 – Command Completed Successfully – SPI bus released					
2	Don't Care					
3-63	Don't Care					

TABLE 3-68: RESPONSES 2 STRUCTURE

Byte Index	Meaning					
0	0x80 – Request SPI bus Release – echos back the given command code					
1	0xF8 – SPI Bus Not Released – SPI transfer in process					
2	Don't Care					
3-63	Don't Care					





3.6 Chip Status

The chip status command is used to retrieve status information regarding the state of the SPI transfer engine.

3.6.1 GET MCP2210 STATUS

TABLE 3-69: COMMAND STRUCTURE

Byte Index	Meaning			
0	0x10 – Get MCP2210 Status – command code			
1	0x00 – Reserved			
2	0x00 – Reserved			
3-63	0x00 – Reserved			

3.6.1.1 Responses

TABLE 3-70: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	0x10 – Get MCP2210 Status – echos back the given command code
1	0x00 – Command Completed Successfully
2	SPI Bus Release External Request Status
	 0x01 – No External Request for SPI Bus Release
	 0x00 – Pending External Request for SPI Bus Release
3	SPI Bus Current Owner
	• 0x00 – No Owner
	0x01 – USB Bridge
	0x02 – External Master
4	Attempted Password Accesses – informs the USB host on how many times the NVRAM password was tried
5	Password Guessed
	0x00 – Password Not Guessed
	0x01 – Password Guessed
6-63	Don't Care

FIGURE 3-26: GET MCP2210 STATUS LOGIC FLOW



3.6.2 UNSUPPORTED COMMAND CODES

TABLE 3-71: COMMAND STRUCTURE

Byte Index	Meaning
0	Usupported Command Code
1	Don't Care
2-63	Don't Care

3.6.2.1 Responses

TABLE 3-72: RESPONSE 1 STRUCTURE

Byte Index	Meaning
0	Unsupported Command Code Sent – echos back the given command code
1	0xF9 – Unknown Command – No effect
2-63	Don't Care

NOTES:

4.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Ambient temperature under bias	40°C to +85°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0.3V to +6.0V
Voltage on MCLR with respect to Vss	-0.3V to +9.0V
Voltage on VUSB pin with respect to VSS	-0.3V to +4.0V
Voltage on D+ and D- pins with respect to Vss	0.3V to (VUSB + 0.3V)
Voltage on all other pins with respect to Vss	0.3V to (VDD + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of Vss pin	95 mA
Maximum current into VDD pin	95 mA
Clamp current, Ik (VPIN < 0 or VPIN > VDD)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	90 mA
Maximum current sourced by all ports	90 mA
Note 1: Power dissipation is calculated as follows: PDIS = VDD x {IDD - ∑ IOH} + ∑ {(VDD - 2: VUSB must always be ≤ VDD + 0.3V	– Voн) x Ioн} + ∑(Vol x IoL).
† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause pe	ermanent damage to the

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

4.1 DC CHARACTERISTICS

DC Characteristics		Operating Conditions (unless otherwise indicated): $3.0V \le VDD \le 5.5V$ at $-40^{\circ}C \le TA \le +85^{\circ}C$ (I-Temp)						
Param No.	Characteristic	Sym	Min	Тур	Мах	Units	Conditions	
D001	Supply Voltage	Vdd	3.3		5.5	V		
	Power-on Reset Release Voltage	VPOR		1.6		V		
	Power-on Reset Rearm Voltage			0.8		V		
D003	VDD Rise Rate to Ensure Power-on Reset	SVDD	0.05	—	—	V/ms	Design guidance only Not tested	
D004	Supply Current	IDD						
	VDD = 3.0V		—	10	12	mA	Fosc = 12 MHz,	
	VDD = 5.0V		—	13	15	mA	(330 nF on VUSB)	
D005	Standby current	IDDS	—	9	—	μA		
	Input Low Voltage	•	•					
D031	Schmitt Trigger (GP0–3, 6–8, MOSI, MISO, SCK)	VIL	_	_	0.2 VDD	V	$3.0V \le VDD \le 5.5V$	
	TTL (GP4, GP5)		_		0.8		$4.5V \leq V\text{DD} \leq 5.5V$	
	Input High Voltage	1			1			
D041	Schmitt Trigger (GP0–3, 6–8, MOSI, MISO, SCK)	Vih	0.8 Vdd	_	V _{DD}	V	$3.0V \le V\text{DD} \le 5.5V$	
	TTL (GP4, GP5)		2.0		V _{DD}		$4.5V \leq V\text{DD} \leq 5.5V$	
	Input Leakage Current		L					
D060	GP0-8, MOSI, MISO, SCK	lı∟	—	±50	±100	nA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ pin \text{ at Hi-Z} \end{array}$	
	RST	1		±50	±200			
	OSC1	1		±50	±100			
	Output Low Voltage							
D080	GP0-8, MOSI, MISO, SCK	Vol	—	_	0.6	V	IOL = 8.0 mA, VDD = 5.0V	
			—		0.6		IOL = 6.0 mA, VDD = 3.3V	
Output High Voltage								
D090	GP0-8, MOSI, MISO, SCK	Voh	Vdd - 0.7		_	V	IOH = -3.5 mA, VDD = 5.0V	
			VDD - 0.7		—		IOH = -3.0 mA, VDD = 3.3V	
	Capacitive Loading Specs	on Outp	ut Pins					
D101	OSC2	Cosc ₂	_		15	pF	Note 1	
D102	GP0-8, MOSI, MISO, SCK	Сю	—	—	50	pF	Note 1	

Note 1: This parameter is characterized, but not tested.

MCP2210



TABLE 4-1: USB MODULE SPECIFICATIONS

DC Characteristics		Operating Conditions (unless otherwise indicated): $3.0V \le VDD \le 5.5V$ at -40°C \le TA \le +85°C (I-Temp)						
Param No.	Characteristic	Sym	Min	Тур	Мах	Units	Conditions	
D313	USB Voltage	VUSB	3.0	_	3.6	V	Voltage on VUSB pin must be in this range for proper USB operation	
D314	Input Leakage on Pin	Ιι∟	—	_	± 1	μA	Vss ≤ VPIN ≤ VDD pin at high-impedance	
D315	Input Low Voltage for USB Buffer	VILUSB	—	—	0.8	V	For VUSB range	
D316	Input High Voltage for USB Buffer	VIHUSB	2.0	—	—	V	For VUSB range	
D318	Differential Input Sensitivity	VDIFS	_	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met	
D319	Differential Common Mode Range	Vсм	0.8	—	2.5	V		
D320	Driver Output Impedance ⁽¹⁾	Zout	28	—	44	Ω		
D321	Voltage Output Low	Vol	0.0		0.3	V	1.5 k Ω load connected to 3.6V	
D322	Voltage Output High	Vон	2.8	—	3.6	V	1.5 k Ω load connected to ground	

Note 1: The D+ and D- signal lines have been built-in impedance matching resistors. No external resistors, capacitors or magnetic components are necessary on the D+/D- signal paths between the MCP2210 family device and the USB cable.

TABLE 4-2: THERMAL CONSIDERATIONS

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ (I-Temp)							
Param No.	Sym	Characteristic	Тур	Units	Conditions		
TH01	θја	Thermal Resistance Junction to	85.2	°C/W	20-pin SOIC package		
		Ambient	108.1	°C/W	20-pin SSOP package		
			36.1	°C/W	20-pin QFN 5x5 mm package		
TH02	θις	Thermal Resistance Junction to	24	°C/W	20-pin SOIC package		
		Case	24	°C/W	20-pin SSOP package		
			1.7	°C/W	20-pin QFN 5x5 mm package		
TH03	TJMAX	Maximum Junction Temperature	150	°C			
TH04	PD	Power Dissipation	—	W	PD = PINTERNAL + PI/O		
TH05	PINTERNAL	Internal Power Dissipation		W	PINTERNAL = IDD x VDD ⁽¹⁾		
TH06	Pi/o	I/O Power Dissipation		W	$PI/O = \Sigma (IOL * VOL) + \Sigma (IOH * (VDD - VOH))$		
TH07	PDER	Derated Power		W	Pder = PDmax (Τj - Τa)/θja ^(2,3)		

Note 1: IDD is the current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

3: T_J = Junction Temperature.

4.2 AC Characteristics

4.2.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created in one of the following formats:

1. TppS2ppS	8	2. TppS	
Т			
F	Frequency	Т	Time
E	Error		
Lowercase le	etters (pp) and their meanings:		
рр			
io	Input or Output pin	osc	Oscillator
rx	Receive	tx	Transmit
bitclk	RX/TX BITCLK	RST	Reset
drt	Device Reset Timer		
Uppercase l	etters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (high-impedance)	V	Valid
L	Low	Z	High-impedance

4.2.2 TIMING CONDITIONS

The operating temperature and voltage specified in Table 4-3 apply to all timing specifications unless otherwise noted. Figure 4-2 specifies the load conditions for the timing specifications.

TABLE 4-3: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

	Standard Operating Conditions (unless otherwise stated)
	Operating temperature -40°C \leq TA \leq +85°C
AC CHARACTERISTICS	Operating voltage VDD range as described in DC spec,
	Section 4.1 "DC Characteristics".

FIGURE 4-2:	LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



4.2.3 TIMING DIAGRAMS AND SPECIFICATIONS

TABLE 4-4: RESET, OSCILLATOR START-UP TIMER AND POWER-UP TIMER PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C \leq TA \leq +85°C								
Param No.SymCharacteristicMinTyp [†] MaxUnitsConditions								
30	TRST	MCLR Pulse Width (low)	2	—	—	μs		
31	TPWRT	Power-up timer	40	65	140	ms		
32	Tost	Oscillator start-up time		1024	_	Tost		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

20-Lead 5x5 QFN



Logona	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e_3)) can be found on the outer packaging for this package.
Note: I	n the even be carried characters	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available of or customer-specific information.

Example



20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

	Units	N	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	Ν		20		
Pitch	е		0.65 BSC		
Overall Height	Α	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.20 REF			
Overall Width	E	5.00 BSC			
Exposed Pad Width	E2	3.15	3.25	3.35	
Overall Length	D	5.00 BSC			
Exposed Pad Length	D2	3.15	3.25	3.35	
Contact Width	b	0.25	0.30	0.35	
Contact Length	L	0.35	0.40	0.45	
Contact-to-Exposed Pad	K	0.20	-	-	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-139B

20-Lead Plastic Quad Flat, No Lead Package (MQ) - 5x5 mm Body [QFN] With 0.40mm Contact Length





RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2		3.35	
Contact Pad Spacing	C1		4.50	
Contact Pad Spacing	C2		4.50	
Contact Pad Width (X20)	X1			0.40
Contact Pad Length (X20)	ontact Pad Length (X20) Y1			0.55
Distance Between Pads G		0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2139A



20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

For the most current package drawings, please see the Microchip Packaging Specification located at

Note:

A



VIEW A-A

Microchip Technology Drawing C04-094C Sheet 1 of 2

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS						
Dimension Limits		MIN	NOM	MAX			
Number of Pins	N		20				
Pitch	е	1.27 BSC					
Overall Height	Α	-	-	2.65			
Molded Package Thickness	A2	2.05	-	-			
Standoff §	A1	0.10	-	0.30			
Overall Width	E	10.30 BSC					
Molded Package Width	E1 7.50 BSC						
Overall Length	D	12.80 BSC					
Chamfer (Optional)	h	0.25 - 0.75					
Foot Length	L	0.40	-	1.27			
Footprint	L1	1.40 REF					
Lead Angle	Θ	0°		-			
Foot Angle	φ	0°	-	8°			
Lead Thickness	С	0.20		0.33			
Lead Width	b	0.31	-	0.51			
Mold Draft Angle Top	α	5°	_	15°			
Mold Draft Angle Bottom	ß	5°	_	15°			

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2
20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		9.40	
Contact Pad Width (X20)	X			0.60
Contact Pad Length (X20)	Y			1.95
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2094A

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
Dimensior	n Limits	MIN	NOM	MAX	
Number of Pins	N		20		
Pitch	е	0.65 BSC			
Overall Height	Α	-	-	2.00	
Molded Package Thickness	A2	1.65	1.75	1.85	
Standoff	A1	0.05	-	-	
Overall Width	E	7.40	7.80	8.20	
Molded Package Width	E1	5.00	5.30	5.60	
Overall Length	D	6.90	7.20	7.50	
Foot Length	L	0.55	0.75	0.95	
Footprint	L1	1.25 REF			
Lead Thickness	С	0.09	-	0.25	
Foot Angle	φ	0°	4°	8°	
Lead Width	b	0.22	_	0.38	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (December, 2011)

• Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>× /××</u>	Examples:
Device	Temperature Package Range	a) MCP2210- I/MQ: Industrial temperature, 20LD QFN Package.
Devices		b) MCP22101- I/MQ: Tape and Reel, Industrial temperature, 20LD QFN Package.
Device:	MCP2210: USB to SPI Protocol Converter with GPIO MCP2210T: USB to SPI Protocol Converter with GPIO (Tape and Reel)	a) MCP2210- I/SO: Industrial temperature, 20LD SOIC Package.
Temperature	I = -40°C to +85°C (Industrial)	b) MCP2210T- I/SO: Tape and Reel, Industrial temperature, 20LD SOIC Package.
itungo.		a) MCP2210- I/SS: Industrial temperature, 20LD SSOP Package.
Package:	MQ = Plastic Quad Flat, No Lead Package 5x5x0.9 mm Body (QFN), 20-Lead SO = Plastic Small Outline - Wide, 7.50 mm Body (SO), 20-Lead SS = SS = Plastic Shrink Small Outline - 5.30 mm Body (SS) 20-Lead	b) MCP2210T- I/SS: Tape and Reel, Industrial temperature, 20LD SSOP Package.

NOTES:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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UK - Wokingham Tel: 44-118-921-5869 Fax: 44-118-921-5820



ООО "ЛайфЭлектроникс"

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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