

74HC4053-Q100; 74HCT4053-Q100

Triple 2-channel analog multiplexer/demultiplexer

Rev. 3 — 5 March 2020

Product data sheet

1. General description

The 74HC4053-Q100; 74HCT4053-Q100 is a triple single-pole double-throw analog switch (3x SPDT) suitable for use in analog or digital 2:1 multiplexer/demultiplexer applications. Each switch features a digital select input (Sn), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ). A digital enable input (E) is common to all switches. When \bar{E} is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide analog input voltage range from -5 V to +5 V
- Low ON resistance:
 - 80 Ω (typical) at $V_{CC} - V_{EE} = 4.5$ V
 - 70 Ω (typical) at $V_{CC} - V_{EE} = 6.0$ V
 - 60 Ω (typical) at $V_{CC} - V_{EE} = 9.0$ V
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical 'break before make' built-in
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
 - CDM AEC-Q100-011 revision B exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4053D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4053D-Q100				
74HC4053PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4053PW-Q100				
74HC4053BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4053BQ-Q100				

5. Functional diagram

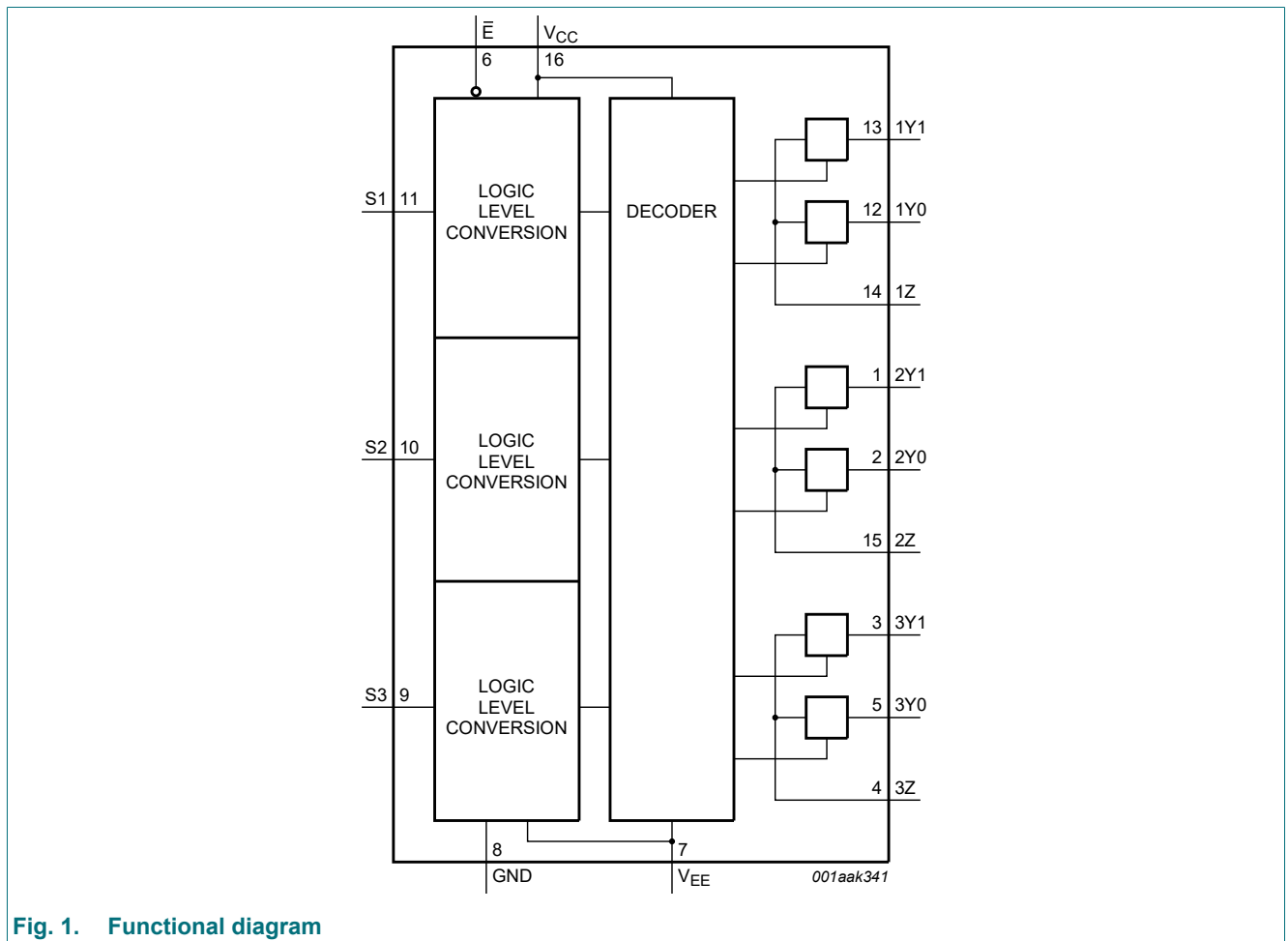


Fig. 1. Functional diagram



Fig. 2. Logic symbol

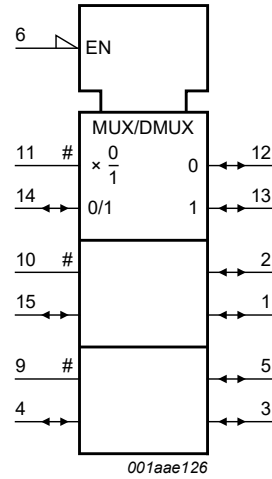


Fig. 3. IEC logic symbol



Fig. 4. Schematic diagram (one switch)

6. Pinning information

6.1. Pinning

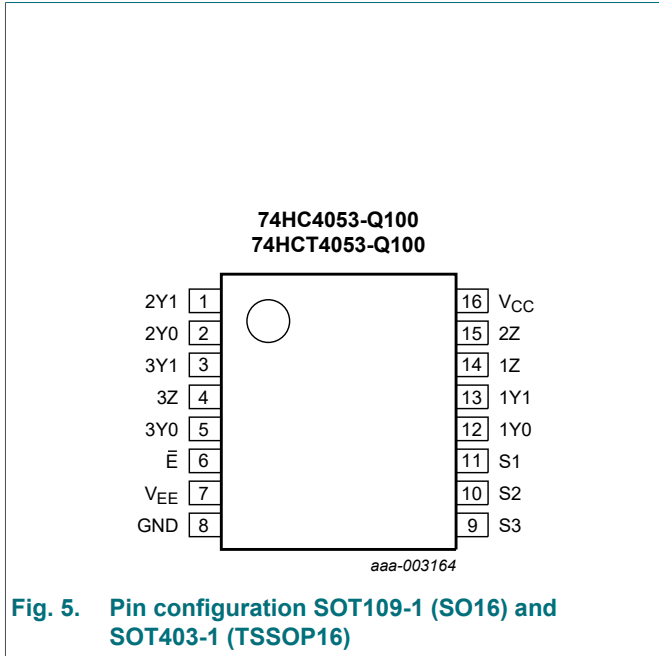


Fig. 5. Pin configuration SOT109-1 (SO16) and SOT403-1 (TSSOP16)

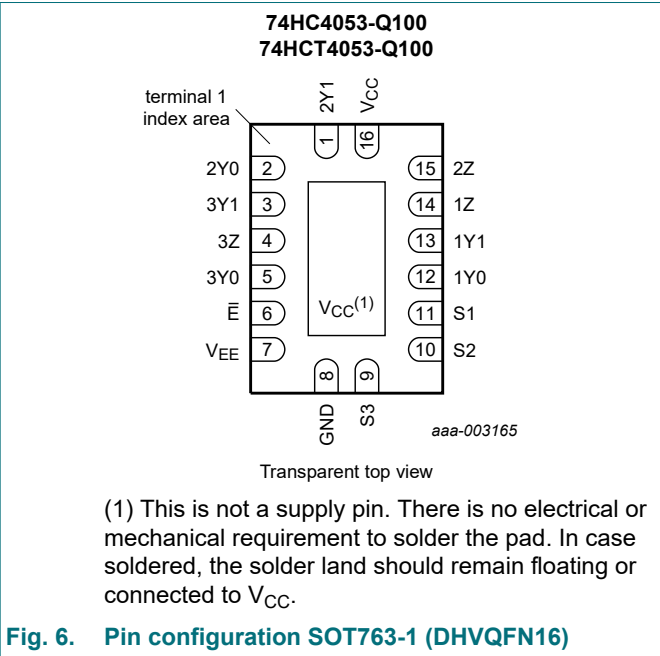


Fig. 6. Pin configuration SOT763-1 (DHVQFN16)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
\bar{E}	6	enable input (active LOW)
V_{EE}	7	supply voltage
GND	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
1Y0, 2Y0, 3Y0	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	13, 1, 3	independent input or output
1Z, 2Z, 3Z	14, 15, 4	common output or input
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs		Channel on
\bar{E}	S_n	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0\text{ V}$ (ground).

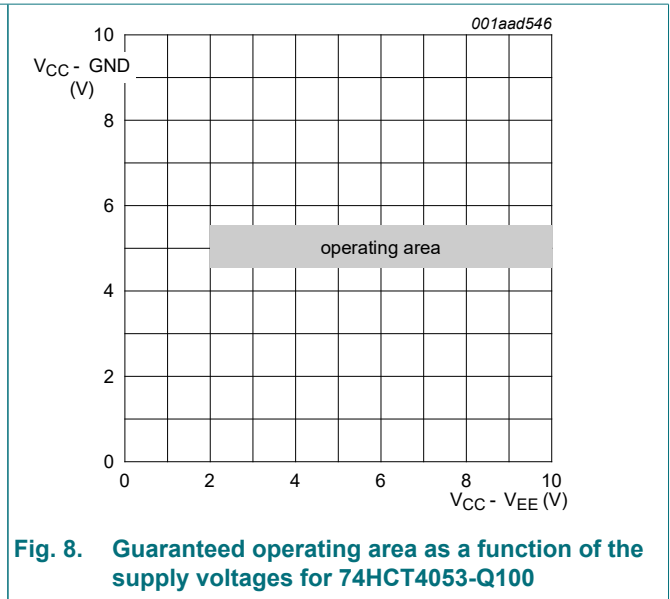
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	[1]	-0.5	+11.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5\text{ V}$ or $V_{SW} > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{SW}	switch current	$-0.5\text{ V} < V_{SW} < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{EE}	supply current		-	± 20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-	-50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[2]	-	500	mW
P	power dissipation	per switch	-	100	mW

- [1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminals nYn, and in this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE} .
- [2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
 For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
 For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4053-Q100			74HCT4053-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage	see Fig. 7 and Fig. 8							
		$V_{CC} - GND$	2.0	5.0	10.0	4.5	5.0	5.5	V
		$V_{CC} - V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V
V_I	input voltage		GND	-	V_{CC}	GND	-	V_{CC}	V
V_{SW}	switch voltage		V_{EE}	-	V_{CC}	V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V
		$V_{CC} = 10.0\text{ V}$	-	-	31	-	-	-	ns/V



10. Static characteristics

Table 6. RON resistance per switch for 74HC4053-Q100 and 74HCT4053-Q100

$V_I = V_{IH}$ or V_{IL} ; for test circuit see Fig. 9.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

For 74HC4053-Q100: $V_{CC} - GND$ or $V_{CC} - V_{EE} = 2.0\text{ V}$, 4.5 V , 6.0 V and 9.0 V .

For 74HCT4053-Q100: $V_{CC} - GND = 4.5\text{ V}$ and 5.5 V , $V_{CC} - V_{EE} = 2.0\text{ V}$, 4.5 V , 6.0 V and 9.0 V .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
T_{amb} = 25 °C							
R _{ON(peak)}	ON resistance (peak)	$V_{is} = V_{CC}$ to V_{EE}					
		$V_{CC} = 2.0\text{ V}$; $V_{EE} = 0\text{ V}$; $I_{SW} = 100\text{ }\mu\text{A}$	[1]	-	-	-	Ω
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$		-	100	180	Ω
		$V_{CC} = 6.0\text{ V}$; $V_{EE} = 0\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$		-	90	160	Ω
R _{ON(rail)}	ON resistance (rail)	$V_{is} = V_{EE}$					
		$V_{CC} = 2.0\text{ V}$; $V_{EE} = 0\text{ V}$; $I_{SW} = 100\text{ }\mu\text{A}$	[1]	-	150	-	Ω
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$		-	80	140	Ω
		$V_{CC} = 6.0\text{ V}$; $V_{EE} = 0\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$		-	70	120	Ω
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$		-	60	105	Ω
		$V_{is} = V_{CC}$					
		$V_{CC} = 2.0\text{ V}$; $V_{EE} = 0\text{ V}$; $I_{SW} = 100\text{ }\mu\text{A}$	[1]	-	150	-	Ω
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$; $I_{SW} = 1000\text{ }\mu\text{A}$		-	90	160	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_{is} = V_{CC}$ to V_{EE}					
		$V_{CC} = 2.0\text{ V}$; $V_{EE} = 0\text{ V}$	[1]	-	-	-	Ω
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$		-	9	-	Ω
		$V_{CC} = 6.0\text{ V}$; $V_{EE} = 0\text{ V}$		-	8	-	Ω
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$		-	6	-	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
T_{amb} = -40 °C to +85 °C							
R _{ON(peak)}	ON resistance (peak)	V _{is} = V _{CC} to V _{EE}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA	[1]	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	225	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	200	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA		-	-	165	Ω
R _{ON(rail)}	ON resistance (rail)	V _{is} = V _{EE}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA	[1]	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	175	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	150	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA		-	-	130	Ω
		V _{is} = V _{CC}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA	[1]	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	200	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	175	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA		-	-	150	Ω
		T_{amb} = -40 °C to +125 °C					
R _{ON(peak)}	ON resistance (peak)	V _{is} = V _{CC} to V _{EE}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA	[1]	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	270	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	240	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA		-	-	195	Ω
R _{ON(rail)}	ON resistance (rail)	V _{is} = V _{EE}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA	[1]	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	210	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	180	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA		-	-	160	Ω
		V _{is} = V _{CC}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA	[1]	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	240	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA		-	-	210	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA		-	-	180	Ω

[1] When supply voltages (V_{CC} - V_{EE}) near 2.0 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.



Fig. 9. Test circuit for measuring R_{ON}



Fig. 10. Typical R_{ON} as a function of input voltage V_{is}

Table 7. Static characteristics for 74HC4053-Q100

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25 \text{ }^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5 \text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	V
		$V_{CC} = 9.0 \text{ V}$	6.3	4.7	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5 \text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	V
		$V_{CC} = 9.0 \text{ V}$	-	4.3	2.7	V
I_I	input leakage current	$V_{EE} = 0 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}$				
		$V_{CC} = 6.0 \text{ V}$	-	-	± 0.1	μA
		$V_{CC} = 10.0 \text{ V}$	-	-	± 0.2	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL}; V_{SW} = V_{CC} - V_{EE};$ see Fig. 11				
		per channel	-	-	± 0.1	μA
		all channels	-	-	± 0.1	μA
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL}; V_{SW} = V_{CC} - V_{EE};$ see Fig. 12	-	-	± 0.1	μA
I_{CC}	supply current	$V_{EE} = 0 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}; V_{is} = V_{EE} \text{ or } V_{CC}; V_{os} = V_{CC} \text{ or } V_{EE}$				
		$V_{CC} = 6.0 \text{ V}$	-	-	8.0	μA
		$V_{CC} = 10.0 \text{ V}$	-	-	16.0	μA
C_I	input capacitance		-	3.5	-	pF

Triple 2-channel analog multiplexer/demultiplexer

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{sw}	switch capacitance	independent pins nYn	-	5	-	pF
		common pins nZ	-	8	-	pF
$T_{amb} = -40\text{ °C to }+85\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
		$V_{CC} = 9.0\text{ V}$	6.3	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V
		$V_{CC} = 9.0\text{ V}$	-	-	2.7	V
I_I	input leakage current	$V_{EE} = 0\text{ V}; V_I = V_{CC}\text{ or GND}$				
		$V_{CC} = 6.0\text{ V}$	-	-	± 1.0	μA
		$V_{CC} = 10.0\text{ V}$	-	-	± 2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0\text{ V}; V_{EE} = 0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; V_{SW} = V_{CC} - V_{EE}; \text{ Fig. 11}$				
		per channel	-	-	± 1.0	μA
		all channels	-	-	± 1.0	μA
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 10.0\text{ V}; V_{EE} = 0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; V_{SW} = V_{CC} - V_{EE}; \text{ see Fig. 12}$	-	-	± 1.0	μA
I_{CC}	supply current	$V_{EE} = 0\text{ V}; V_I = V_{CC}\text{ or GND}; V_{is} = V_{EE}\text{ or }V_{CC}; V_{os} = V_{CC}\text{ or }V_{EE}$				
		$V_{CC} = 6.0\text{ V}$	-	-	80.0	μA
		$V_{CC} = 10.0\text{ V}$	-	-	160.0	μA
$T_{amb} = -40\text{ °C to }+125\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
		$V_{CC} = 9.0\text{ V}$	6.3	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V
		$V_{CC} = 9.0\text{ V}$	-	-	2.7	V
I_I	input leakage current	$V_{EE} = 0\text{ V}; V_I = V_{CC}\text{ or GND}$				
		$V_{CC} = 6.0\text{ V}$	-	-	± 1.0	μA
		$V_{CC} = 10.0\text{ V}$	-	-	± 2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0\text{ V}; V_{EE} = 0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; V_{SW} = V_{CC} - V_{EE}; \text{ see Fig. 11}$				
		per channel	-	-	± 1.0	μA
		all channels	-	-	± 1.0	μA
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 10.0\text{ V}; V_{EE} = 0\text{ V}; V_I = V_{IH}\text{ or }V_{IL}; V_{SW} = V_{CC} - V_{EE}; \text{ see Fig. 12}$	-	-	± 1.0	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CC}	supply current	V _{EE} = 0 V; V _I = V _{CC} or GND; V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}				
		V _{CC} = 6.0 V	-	-	160.0	μA
		V _{CC} = 10.0 V	-	-	320.0	μA

Table 8. Static characteristics for 74HCT4053-Q100

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	±0.1	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Fig. 11				
		per channel	-	-	±0.1	μA
		all channels	-	-	±0.1	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Fig. 12	-	-	±0.1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}				
		V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	8.0	μA
		V _{CC} = 5.0 V; V _{EE} = -5.0 V	-	-	16.0	μA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; V _{EE} = 0 V	-	50	180	μA
C _I	input capacitance		-	3.5	-	pF
C _{sw}	switch capacitance	independent pins nYn	-	5	-	pF
		common pins nZ	-	8	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	±1.0	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Fig. 11				
		per channel	-	-	±1.0	μA
		all channels	-	-	±1.0	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Fig. 12	-	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}				
		V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	80.0	μA
		V _{CC} = 5.0 V; V _{EE} = -5.0 V	-	-	160.0	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC} - 2.1\text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	-	225	μA
$T_{amb} = -40\text{ }^\circ\text{C to }+125\text{ }^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	0.8	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	-	± 1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0\text{ V}$; $V_{EE} = 0\text{ V}$; $V_I = V_{IH}$ or V_{IL} ; $ V_{SW} = V_{CC} - V_{EE}$; see Fig. 11				
		per channel	-	-	± 1.0	μA
		all channels	-	-	± 1.0	μA
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 10.0\text{ V}$; $V_{EE} = 0\text{ V}$; $V_I = V_{IH}$ or V_{IL} ; $ V_{SW} = V_{CC} - V_{EE}$; see Fig. 12	-	-	± 1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or V_{CC} ; $V_{os} = V_{CC}$ or V_{EE}				
		$V_{CC} = 5.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	-	160.0	μA
		$V_{CC} = 5.0\text{ V}$; $V_{EE} = -5.0\text{ V}$	-	-	320.0	μA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC} - 2.1\text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	-	245	μA



Fig. 11. Test circuit for measuring OFF-state current

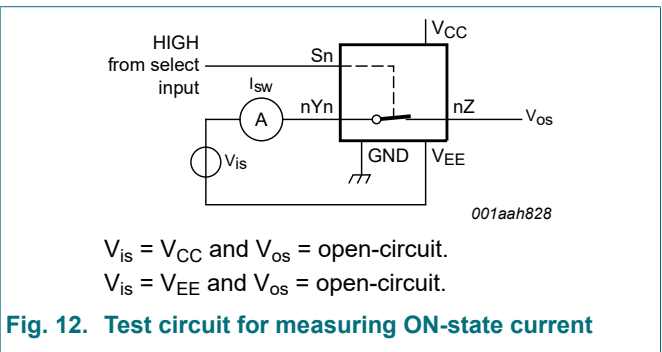


Fig. 12. Test circuit for measuring ON-state current

11. Dynamic characteristics

Table 9. Dynamic characteristics for 74HC4053-Q100

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see Fig. 15.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25\text{ }^\circ\text{C}$						
t_{pd}	propagation delay	V_{is} to V_{os} ; $R_L = \infty\ \Omega$; see Fig. 13	[1]			
		$V_{CC} = 2.0\text{ V}$; $V_{EE} = 0\text{ V}$	-	15	60	ns
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	5	12	ns
		$V_{CC} = 6.0\text{ V}$; $V_{EE} = 0\text{ V}$	-	4	10	ns
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	4	8	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{on}	turn-on time	\bar{E} to V _{os} ; R _L = ∞ Ω; see Fig. 14 [2]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	60	220	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	20	44	ns
		V _{CC} = 5.0 V; V _{EE} = 0 V; C _L = 15 pF	-	17	-	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	16	37	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	15	31	ns
		Sn to V _{os} ; R _L = ∞ Ω; see Fig. 14 [2]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	75	220	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	25	44	ns
		V _{CC} = 5.0 V; V _{EE} = 0 V; C _L = 15 pF	-	21	-	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	20	37	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	15	31	ns
t _{off}	turn-off time	\bar{E} to V _{os} ; R _L = 1 kΩ; see Fig. 14 [3]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	63	210	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	21	42	ns
		V _{CC} = 5.0 V; V _{EE} = 0 V; C _L = 15 pF	-	18	-	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	17	36	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	15	29	ns
		Sn to V _{os} ; R _L = 1 kΩ; see Fig. 14 [3]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	60	210	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	20	42	ns
		V _{CC} = 5.0 V; V _{EE} = 0 V; C _L = 15 pF	-	17	-	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	16	36	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	15	29	ns
C _{PD}	power dissipation capacitance	per switch; V _I = GND to V _{CC} [4]	-	36	-	pF
T_{amb} = -40 °C to +85 °C						
t _{pd}	propagation delay	V _{is} to V _{os} ; R _L = ∞ Ω; see Fig. 13 [1]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	75	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	15	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	13	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	10	ns
t _{on}	turn-on time	\bar{E} to V _{os} ; R _L = ∞ Ω; see Fig. 14 [2]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	275	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	55	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	47	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	39	ns
		Sn to V _{os} ; R _L = ∞ Ω; see Fig. 14 [2]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	275	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	55	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	47	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	39	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{off}	turn-off time	\bar{E} to V _{os} ; R _L = 1 kΩ; see Fig. 14 [3]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	265	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	53	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	45	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	36	ns
		Sn to V _{os} ; R _L = 1 kΩ; see Fig. 14 [3]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	265	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	53	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	45	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	36	ns
T_{amb} = -40 °C to +125 °C						
t _{pd}	propagation delay	V _{is} to V _{os} ; R _L = ∞ Ω; see Fig. 13 [1]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	90	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	18	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	15	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	12	ns
t _{on}	turn-on time	\bar{E} to V _{os} ; R _L = ∞ Ω; see Fig. 14 [2]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	330	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	66	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	56	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	47	ns
		Sn to V _{os} ; R _L = ∞ Ω; see Fig. 14 [2]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	330	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	66	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	56	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	47	ns
t _{off}	turn-off time	\bar{E} to V _{os} ; R _L = 1 kΩ; see Fig. 14 [3]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	315	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	63	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	54	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	44	ns
		Sn to V _{os} ; R _L = 1 kΩ; see Fig. 14 [3]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	315	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	63	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	54	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	44	ns

- [1] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [2] t_{on} is the same as t_{PZH} and t_{PZL}.
- [3] t_{off} is the same as t_{PHZ} and t_{PLZ}.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:
 f_i = input frequency in MHz; f_o = output frequency in MHz;
 N = number of inputs switching; $\Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;
 C_L = output load capacitance in pF; C_{sw} = switch capacitance in pF;
 V_{CC} = supply voltage in V.

Table 10. Dynamic characteristics for 74HCT4053-Q100

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see Fig. 15.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
T_{amb} = 25 °C							
t _{pd}	propagation delay	V_{is} to V_{os} ; $R_L = \infty\ \Omega$; see Fig. 13 [1]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	5	12	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	4	8	ns	
t _{on}	turn-on time	\bar{E} to V_{os} ; $R_L = 1\text{ k}\Omega$; see Fig. 14 [2]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	27	48	ns	
		$V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$; $C_L = 15\text{ pF}$	-	23	-	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	16	34	ns	
		Sn to V_{os} ; $R_L = 1\text{ k}\Omega$; see Fig. 14 [2]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	25	48	ns	
		$V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$; $C_L = 15\text{ pF}$	-	21	-	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	16	34	ns	
t _{off}	turn-off time	\bar{E} to V_{os} ; $R_L = 1\text{ k}\Omega$; see Fig. 14 [3]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	24	44	ns	
		$V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$; $C_L = 15\text{ pF}$	-	20	-	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	15	31	ns	
		Sn to V_{os} ; $R_L = 1\text{ k}\Omega$; see Fig. 14 [3]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	22	44	ns	
		$V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$; $C_L = 15\text{ pF}$	-	19	-	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	15	31	ns	
C _{PD}	power dissipation capacitance	per switch; $V_I = GND$ to $V_{CC} - 1.5\text{ V}$ [4]	-	36	-	pF	
T_{amb} = -40 °C to +85 °C							
t _{pd}	propagation delay	V_{is} to V_{os} ; $R_L = \infty\ \Omega$; see Fig. 13 [1]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	-	15	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	-	10	ns	
t _{on}	turn-on time	\bar{E} to V_{os} ; $R_L = 1\text{ k}\Omega$; see Fig. 14 [2]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	-	60	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	-	43	ns	
		Sn to V_{os} ; $R_L = 1\text{ k}\Omega$; see Fig. 14 [2]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	-	60	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	-	43	ns	
t _{off}	turn-off time	\bar{E} to V_{os} ; $R_L = 1\text{ k}\Omega$; see Fig. 14 [3]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	-	55	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	-	39	ns	
		Sn to V_{os} ; $R_L = 1\text{ k}\Omega$; see Fig. 14 [3]					
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	-	55	ns	
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	-	39	ns	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
t _{pd}	propagation delay	V _{is} to V _{os} ; R _L = ∞ Ω; see Fig. 13 [1]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	18	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	12	ns
t _{on}	turn-on time	\bar{E} to V _{os} ; R _L = 1 kΩ; see Fig. 14 [2]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	72	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	51	ns
		Sn to V _{os} ; R _L = 1 kΩ; see Fig. 14 [2]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	72	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	51	ns
t _{off}	turn-off time	\bar{E} to V _{os} ; R _L = 1 kΩ; see Fig. 14 [3]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	66	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	47	ns
		Sn to V _{os} ; R _L = 1 kΩ; see Fig. 14 [3]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	66	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	47	ns

- [1] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [2] t_{on} is the same as t_{PZH} and t_{PZL}.
- [3] t_{off} is the same as t_{PHZ} and t_{PLZ}.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:
 f_i = input frequency in MHz; f_o = output frequency in MHz;
 N = number of inputs switching; $\sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;
 C_L = output load capacitance in pF; C_{sw} = switch capacitance in pF;
 V_{CC} = supply voltage in V.

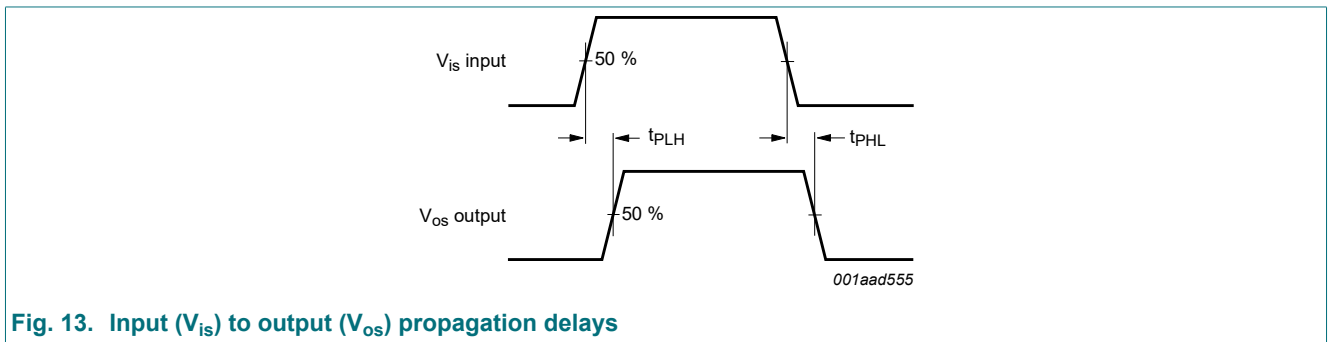


Fig. 13. Input (V_{is}) to output (V_{os}) propagation delays



For 74HC4053-Q100: $V_M = 0.5 \times V_{CC}$.
 For 74HCT4053-Q100: $V_M = 1.3 \text{ V}$.

Fig. 14. Turn-on and turn-off times



Definitions for test circuit; see [Table 11](#):

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

S1 = Test selection switch.

Fig. 15. Test circuit for measuring AC performance

Table 11. Test data

Test	Input				Load		S1 position
	V _I [1]	V _{is}	t _r , t _f		C _L	R _L	
			at f _{max}	other [2]			
t _{PHL} , t _{PLH}	V _{CC}	pulse	< 2 ns	6 ns	50 pF	1 kΩ	open
t _{PZH} , t _{PHZ}	V _{CC}	V _{CC}	< 2 ns	6 ns	50 pF	1 kΩ	V _{EE}
t _{PZL} , t _{PLZ}	V _{CC}	V _{EE}	< 2 ns	6 ns	50 pF	1 kΩ	V _{CC}

[1] For 74HCT4053-Q100: V_I = 3 V

[2] t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint to t_r and t_f with 50 % duty factor.

11.1. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V; T_{amb} = 25 °C; C_L = 50 pF.

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{os} is the output voltage at pins nYn or nZ, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
d _{sin}	sine-wave distortion	f _i = 1 kHz; R _L = 10 kΩ; see Fig. 16				
		V _{is} = 4.0 V (p-p); V _{CC} = 2.25 V; V _{EE} = -2.25 V	-	0.04	-	%
		V _{is} = 8.0 V (p-p); V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	0.02	-	%
		f _i = 10 kHz; R _L = 10 kΩ; see Fig. 16				
		V _{is} = 4.0 V (p-p); V _{CC} = 2.25 V; V _{EE} = -2.25 V	-	0.12	-	%
		V _{is} = 8.0 V (p-p); V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	0.06	-	%
α _{iso}	isolation (OFF-state)	R _L = 600 Ω; f _i = 1 MHz; see Fig. 17				
		V _{CC} = 2.25 V; V _{EE} = -2.25 V [1]	-	-50	-	dB
		V _{CC} = 4.5 V; V _{EE} = -4.5 V [1]	-	-50	-	dB
Xtalk	crosstalk	between two switches/multiplexers; R _L = 600 Ω; f _i = 1 MHz; see Fig. 18				
		V _{CC} = 2.25 V; V _{EE} = -2.25 V [1]	-	-60	-	dB
		V _{CC} = 4.5 V; V _{EE} = -4.5 V [1]	-	-60	-	dB
V _{ct}	crosstalk voltage	peak-to-peak value; between control and any switch; R _L = 600 Ω; f _i = 1 MHz; \bar{E} or Sn square wave between V _{CC} and GND; t _r = t _f = 6 ns; see Fig. 19				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	110	-	mV
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	220	-	mV
f _(-3dB)	-3 dB frequency response	R _L = 50 Ω; see Fig. 20				
		V _{CC} = 2.25 V; V _{EE} = -2.25 V [2]	-	160	-	MHz
		V _{CC} = 4.5 V; V _{EE} = -4.5 V [2]	-	170	-	MHz

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).



Fig. 16. Test circuit for measuring sine-wave distortion



$V_{CC} = 4.5\text{ V}$; $GND = 0\text{ V}$; $V_{EE} = -4.5\text{ V}$; $R_L = 600\ \Omega$; $R_S = 1\text{ k}\Omega$.
a. Test circuit



b. Isolation (OFF-state) as a function of frequency

Fig. 17. Test circuit for measuring isolation (OFF-state)



Fig. 18. Test circuits for measuring crosstalk between any two switches/multiplexers



Fig. 19. Test circuit for measuring crosstalk between control input and any switch



Fig. 20. Test circuit for frequency response

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

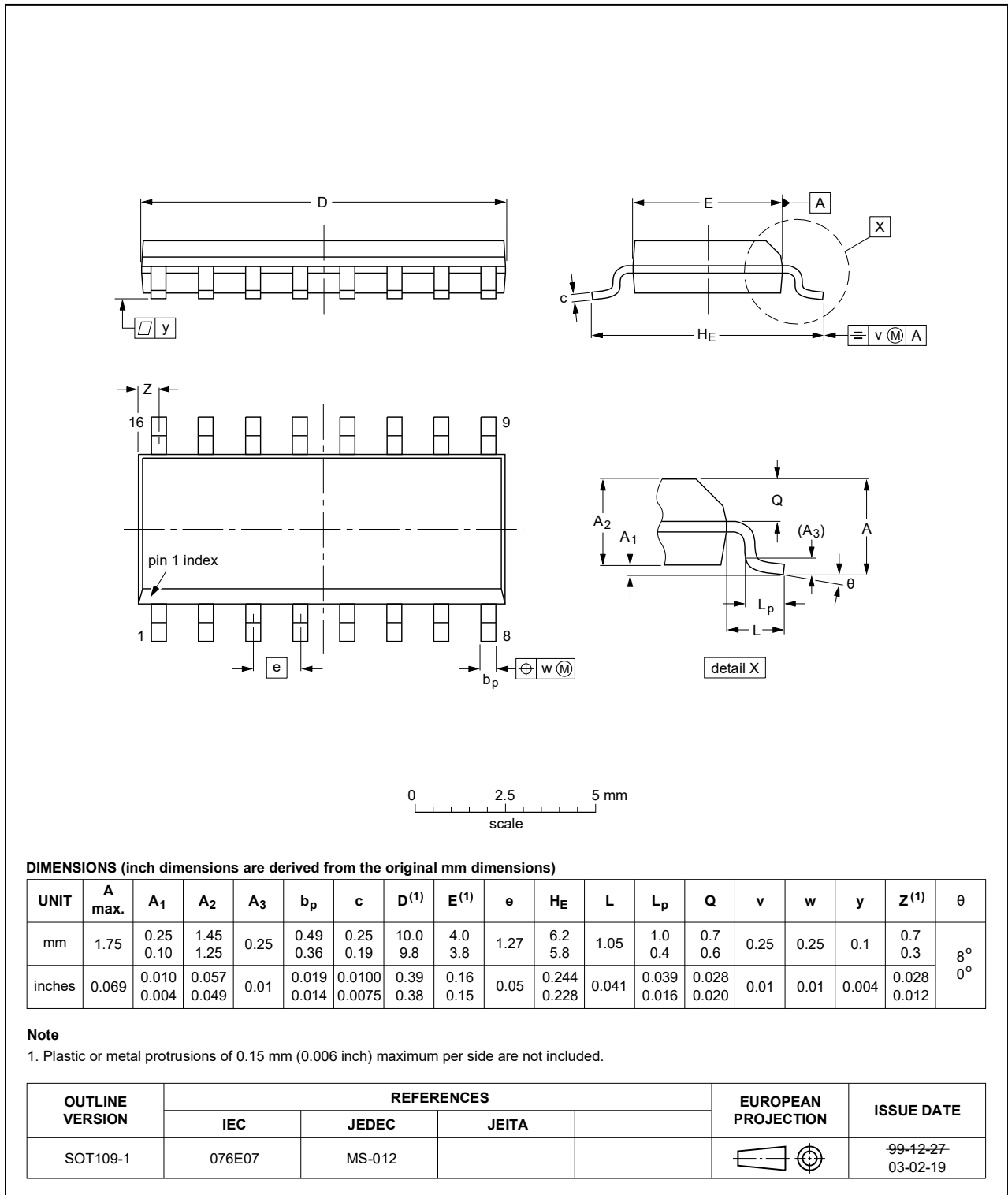


Fig. 21. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Fig. 22. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1



Fig. 23. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4053_Q100 v.3	20200305	Product data sheet	-	74HC_HCT4053_Q100 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 updated. Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. 			
74HC_HCT4053_Q100 v.2	20121122	Product data sheet	-	74HC_HCT4053_Q100 v.1
Modifications:	<ul style="list-style-type: none"> CDM added to features. 			
74HC_HCT4053_Q100 v.1	20120720	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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