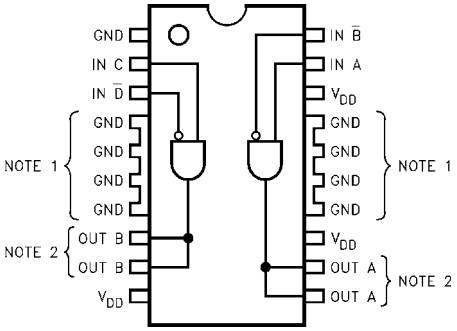
Data Sheet | May 13, 2005 | FN7286.1

## Dual Input, High Speed, Dual Channel CCD Driver

The EL7243 dual input, 2-channel driver achieves the same excellent switching performance of the EL7212 family while providing added flexibility. The power package makes this part extremely well suited for high frequency and heavy loads as in CCD applications. The 2-input logic and configuration is applicable to numerous power MOSFET drive circuits. As with other Elantec drivers, the EL7243 is excellent for driving large capacitive loads with minimal delay and switching times. “Shoot-thru” protection and latching circuits can be implemented by simply “cross-coupling” the 2-channels.

## Pinout

**EL7243**
**(20-PIN THERMAL SOIC)**
TOP VIEW




**Note 1: Pins 4–7 and 14–17 are electrically connected.**
**Note 2: Output pins must be tied together.**

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

## Features

- Logic AND/NAND input
- 3V and 5V Input compatible
- Clocking speeds up to 20MHz
- 20ns Switching/delay time
- 2A Peak drive
- Isolated drains
- Low output impedance
- Low quiescent current
- Wide operating voltage — 4.5V to 16V
- Pb-Free available (RoHS compliant)

## Applications

- CCD Drivers
- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Shoot-thru protection
- Latching drivers

## Ordering Information

| PART NUMBER | PACKAGE | TAPE & REEL | PKG. DWG. # |
|---|---|---|---|
| EL7243CM | 20-Pin SOIC | - | MDP0027 |
| EL7243CM-T13 | 20-Pin SOIC | 13” | MDP0027 |
| EL7243CMZ (See Note) | 20-Pin SOIC (Pb-free) | - | MDP0027 |
| EL7243CMZ-T13 (See Note) | 20-Pin SOIC (Pb-free) | 13” | MDP0027 |

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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## Absolute Maximum Ratings ($T_A$ = 25°C)

Supply (V+ to Gnd) . . . . . 16.5V
Input Pins. . . . . -0.3V to +0.3V above V+
Combined Peak Output Current. . . . . .4A
Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . 125°C
Power Dissipation
20-pin “Batwing” SOIC . . . . . .1500mW

*CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## DC Electrical Specifications

$T_A$ = 25°C, $V_{DD}$ = 15V unless otherwise specified

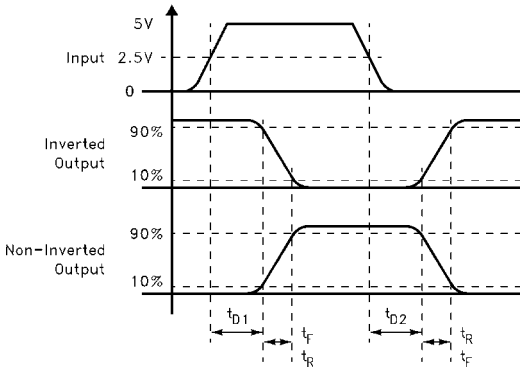
| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| $V_{IH}$ | Logic “1” Input Voltage | | 2.4 | | | V |
| $I_{IH}$ | Logic “1” Input Current | @$V_{DD}$ | | 0.1 | 10 | µA |
| $V_{IL}$ | Logic “0” Input Voltage | | | | 0.8 | V |
| $I_{IL}$ | Logic “0” Input Current | @0V | | 0.1 | 10 | µA |
| $V_{HVS}$ | Input Hysteresis | | | 0.3 | | V |
| **OUTPUT** | | | | | | |
| $R_{OH}$ | Pull-Up Resistance | $I_{OUT}$ = -100mA | | 3 | 6 | Ω |
| $R_{OL}$ | Pull-Down Resistance | $I_{OUT}$ = +100mA | | 4 | 6 | Ω |
| $I_{PK}$ | Peak Output Current | Source<br>Sink | | 2<br>2 | | A |
| $I_{DC}$ | Continuous Output Current | Source/Sink | 200 | | | mA |
| **POWER SUPPLY** | | | | | | |
| $I_S$ | Power Supply Current | Inputs High | | 1 | 2.5 | mA |
| $V_S$ | Operating Voltage | | 4.5 | | 16 | V |

## AC Electrical Specifications

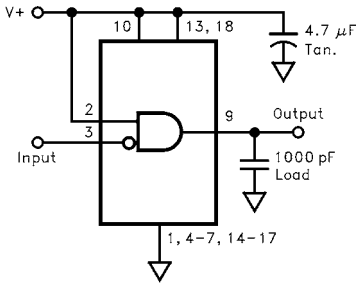
$T_A$ = 25°C, V = 15V unless otherwise specified

| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_R$ | Rise Time | $C_L$ = 500pF<br>$C_L$ = 1000pF | | | 10<br>20 | ns |
| $t_F$ | Fall Time | $C_L$ = 500pF<br>$C_L$ = 1000pF | | | 10<br>20 | ns |
| $t_{D-ON}$ | Turn-On Delay Time | | | 20 | 25 | ns |
| $t_{D-OFF}$ | Turn-Off Delay Time | | | 20 | 25 | ns |

## Timing Table

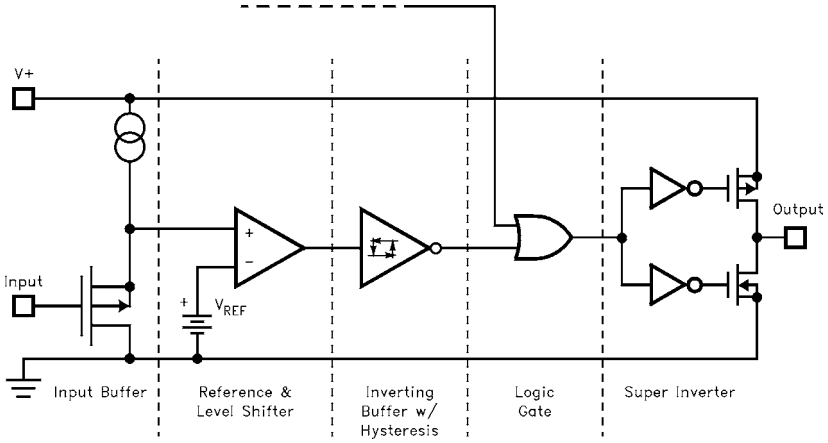



## Standard Test Configuration



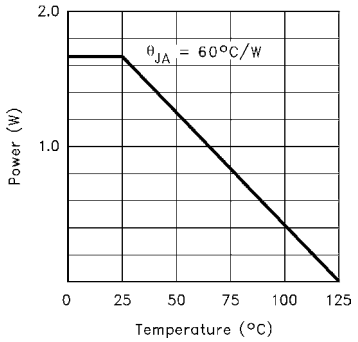

**Pins 19, 20 connected to V+**

## Simplified Schematic

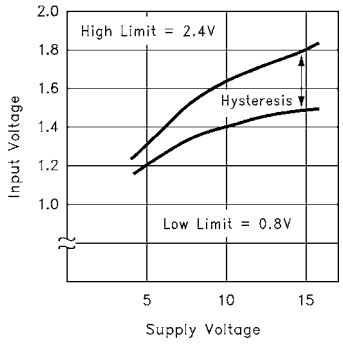


## Typical Performance Curves

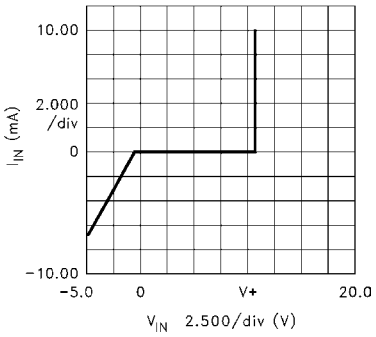
**Max Power/Derating Curves**



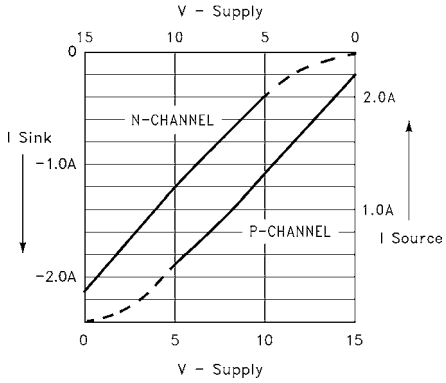

**Switch Threshold vs Supply Voltage**



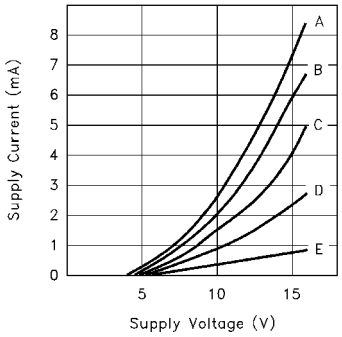

**Input Current vs Voltage**




**Peak Drive vs Supply Voltage**



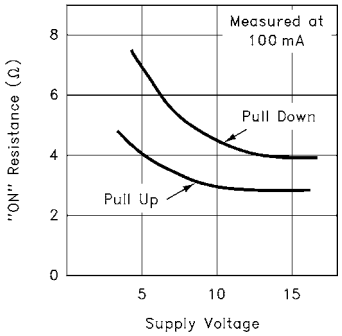

**Quiescent Supply Current**




CASE:

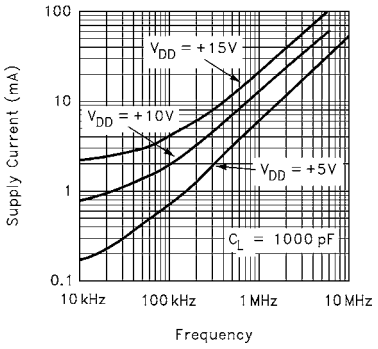
| | |
|---|---|
| A | ALL INPUTS GND |
| B | 3 INPUTS GND |
| C | 2 INPUTS GND |
| D | 1 INPUT GND |
| E | ALL INPUTS V+ |

**"ON" Resistance vs Supply Voltage**

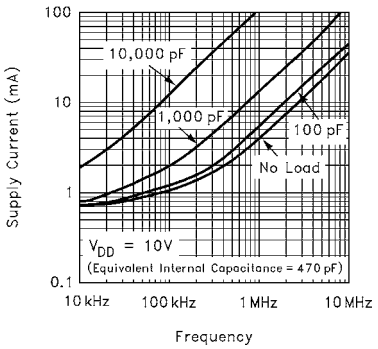


## Typical Performance Curves (Continued)

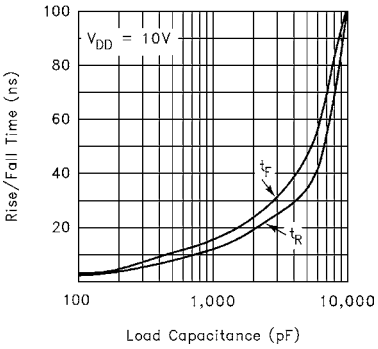
**Average Supply Current vs Voltage and Frequency**



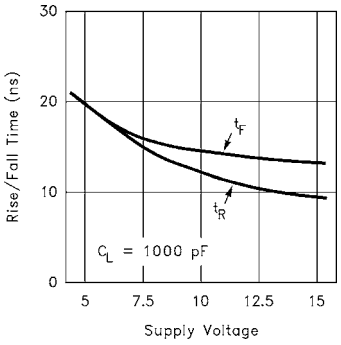

**Average Supply Current vs Capacitive Load**



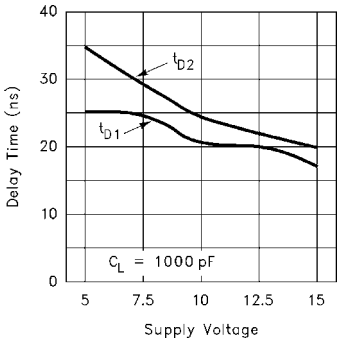

**Rise/Fall Time vs Load**



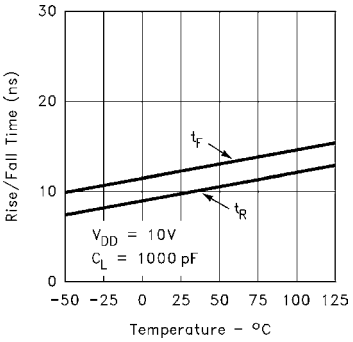

**Rise/Fall Time vs Supply Voltage**



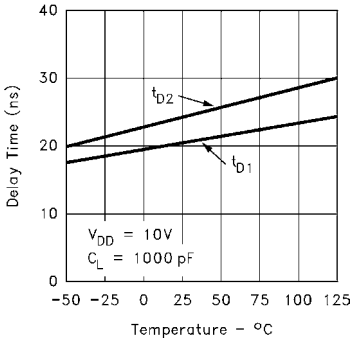

**Rise/Fall Time vs Temperature**




**Propagation Delay vs Supply Voltage**

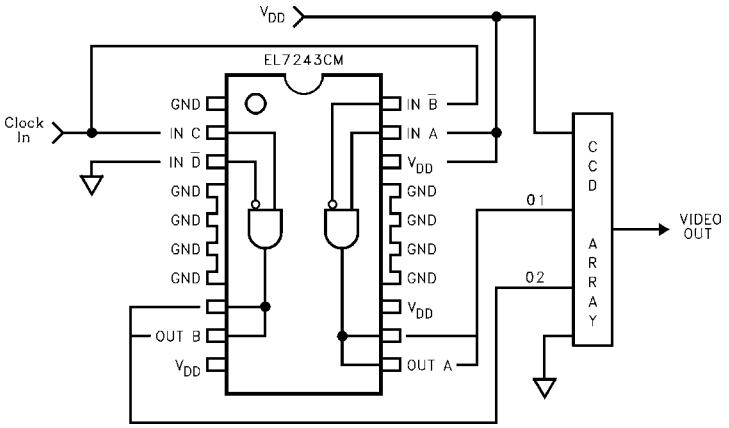



**Delay vs Temperature**

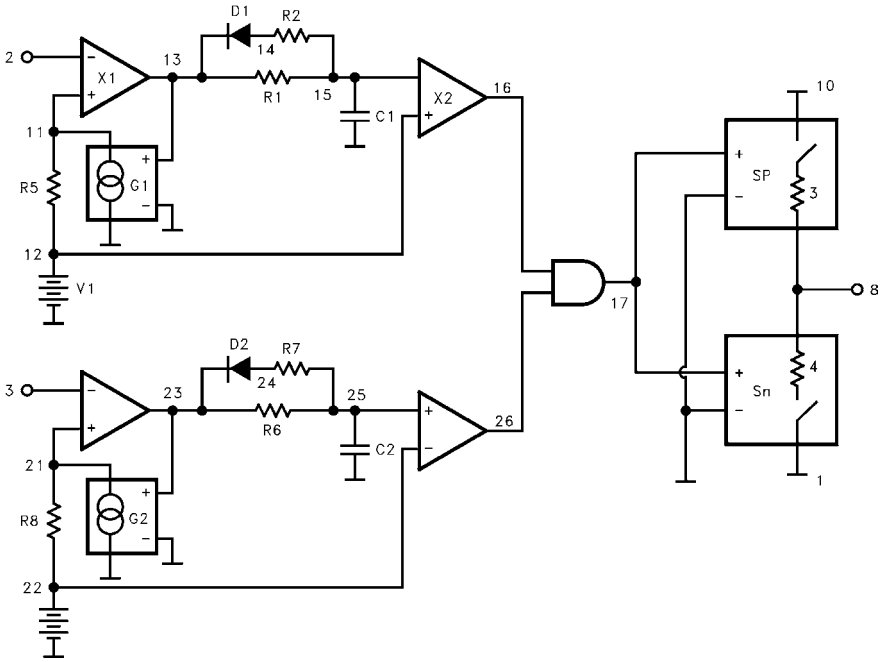


## Applications Information

**Typical CCD Configuration**




**EL7243 Macromodel**



## EL7243 Macromodel

```
* EL7243 Macromodel
* Revision A, January 1996
* Connections      Gnd
*                  |    Inp+
*                  |    |    Inp-
*                  |    |    |    out
*                  |    |    |    |    VCC
.subckt M7243      1    2    3    8    10
V1 12 1 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 1 43.3pF
D1 14 13 dmod
X1 13 11 2 1 comp1
X2 16 12 15 1 comp1
V2 22 1 1.6
R6 23 25 1K
R7 24 25 5K
R8 21 22 100
C2 25 1 43.3pF
D2 24 23 dmod
X3 23 21 3 1 comp1
X4 26 25 22 1 comp1
X5 16 26 17 1 And-gate
sp 10 8 17 1 spmod
sn 8 1 17 1 snmod
g1 11 1 13 1 938u
g2 21 1 23 1 938u
.model dmod d
.model spmod vswitch ron=3 roff=2meg von=1 voff=1.5
.model snmod vswitch ron=4 roff=2meg von=3 voff=2
.ends M7243
* AND Gate Subcircuit*
.subckt And-gate inp1 inp2 out-AS Vss-A
el out-A Vss-A table {v(inp1)*v(inp2)} = (0, 3.2) (3.2, 0)
Rout-a out-a vss-a 10 meg
rinpa inp1 vss-a 10 meg
rinpb inp2 vss-a 10 meg
.ends and-gate
* Comparator Subcircuit *
.subckt comp1 out inp inm vss
el out vss table {(v(inp)-v(inm))*5000} = (0,0) (3.2, 3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends omp1
```

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