

Precision Monolithic Quad SPST CMOS Analog Switches

DESCRIPTION

The DG417B, DG418B, DG419B monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power, low leakages, high speed, low on-resistance and small physical size, the DG417B series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

To achieve high-voltage ratings and superior switching performance, the DG417B series is built on Vishay Siliconix's high voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419B, which is an SPDT configuration. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG417B and DG418B respond to opposite control logic levels as shown in the Truth Table.

FEATURES

- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 15Ω
- Fast switching action - t_{ON} : 110 ns
- TTL and CMOS compatible
- MSOP-8 and SOIC-8 package
- Compliant to RoHS directive 2002/95/EC



RoHS*
COMPLIANT

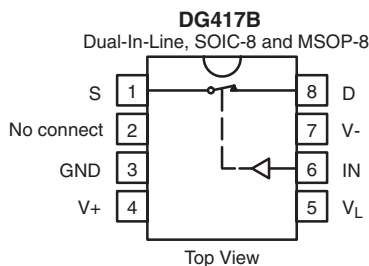
BENEFITS

- Widest dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing
- Reduced board space
- Improved reliability

APPLICATIONS

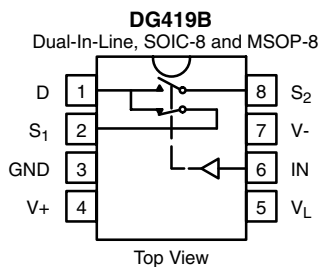
- Precision test equipment
- Precision instrumentation
- Battery powered systems
- Sample-and-hold circuits
- Military radios
- Guidance and control systems
- Hard disk drivers

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	DG417B	DG418B
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V



TRUTH TABLE - DG419B		
Logic	SW ₁	SW ₂
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply

ORDERING INFORMATION		
Temp Range	Package	Part Number
DG417B, DG418B		
- 40 °C to 85 °C	8-Pin Plastic MiniDIP	DG417BDJ DG417BDJ-E3
		DG418BDJ DG418BDJ-E3
	8-Pin Narrow SOIC	DG417BDY DG417BDY-E3 DG417BDY-T1 DG417BDY-T1-E3
		DG418BDY DG418BDY-E3 DG418BDY-T1 DG418BDY-T1-E3
	8-Pin MSOP	DG417BDQ-T1-E3
		DG418BDQ-T1-E3
DG419B		
- 40 °C to 85 °C	8-Pin Plastic MiniDIP	DG419BDJ DG419BDJ-E3
	8-Pin Narrow SOIC	DG419BDY DG419BDY-E3 DG419BDY-T1 DG419BDY-T1-E3
	8-Pin MSOP	DG419BDQ-T1-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter	Limit	Unit	
V-	- 20	V	
V+	20		
GND	25		
V _L	(GND - 0.3) to (V+) + 0.3		
Digital Inputs ^a , V _S , V _D	(V-) - 2 V to (V+) + 2 or 30 mA, whichever occurs first		
Current, (Any Terminal) Continuous	30	mA	
Current (S or D) Pulsed at 1 ms, 10 % Duty Cycle	100		
Storage Temperature	- 65 to 150	°C	
Power Dissipation (Package) ^b	8-Pin Plastic MiniDIP ^c	400	mW
	8-Pin Narrow SOIC ^c	400	
	8-Pin MSOP ^d	400	
	8-Pin CerDIP ^e	600	

Notes:

- a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 5.3 mW/°C above 75 °C.
- d. Derate 4 mW/°C above 70 °C.
- e. Derate 8 mW/°C above 75 °C.

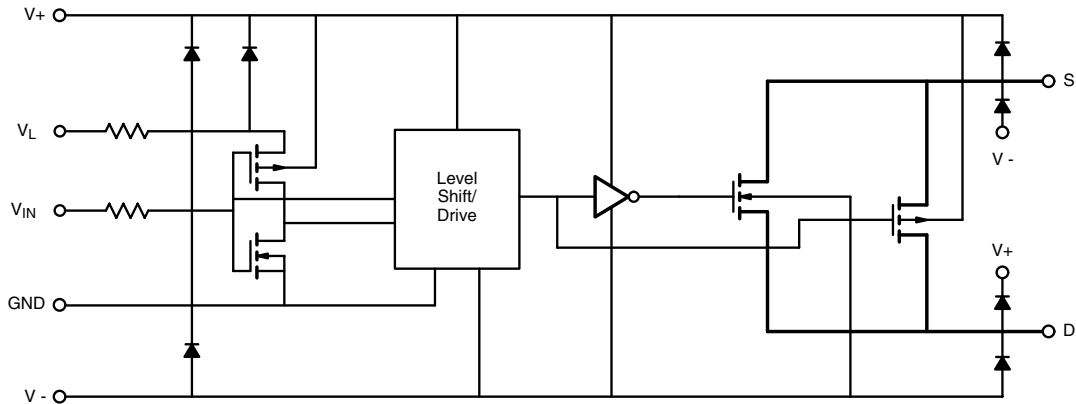
SCHEMATIC DIAGRAM Typical Channel


Figure 1.

SPECIFICATIONS^a												
Parameter	Symbol	Test Conditions Unless Otherwise Specified			Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit	
		V ₊ = 15 V, V ₋ = - 15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f					Min. ^d	Max. ^d	Min. ^d	Max. ^d		
Analog Switch												
Analog Signal Range ^e	V _{ANALOG}				Full		- 15	15	- 15	15	V	
Drain-Source On-Resistance	R _{DS(on)}	I _S = - 10 mA, V _D = ± 12.5 V V ₊ = 13.5 V, V ₋ = - 13.5 V			Room Full	15		25 34		25 29	Ω	
Switch Off Leakage Current	I _{S(off)}	V ₊ = 16.5 V, V ₋ = - 16.5 V V _D = ± 15.5 V, V _S = ± 15.5 V			Room Full	- 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	nA	
	I _{D(off)}				DG417B	Room Full	- 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5		0.25 5
					DG419B	Room Full	- 0.1	- 0.75 - 60	0.75 60	- 0.75 - 12		0.75 12
Channel On Leakage Current	I _{D(on)}	V ₊ = 16.5 V, V ₋ = - 16.5 V V _S = V _D = ± 15.5 V			Room Full	- 0.4	- 0.4 - 40	0.4 40	- 0.4 - 10	0.4 10		
					Room Full	- 0.4	- 0.75 - 60	0.75 60	- 0.75 - 12	0.75 12		
Digital Control												
Input Current, V _{IN} Low	I _{IL}				Full		- 0.5	0.5	- 0.5	0.5	μA	
Input Current, V _{IN} High	I _{IH}				Full		- 0.5	0.5	- 0.5	0.5		
Dynamic Characteristics												
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _S = ± 10 V, See Switching Time Test Circuit			DG417B	Room Full	62		89 106		89 99	ns
Turn-Off Time	t _{OFF}				DG417B	Room Full	53		80 88		80 86	
Transition Time	t _{TRANS}	R _L = 300 Ω, C _L = 35 pF V _{S1} = ± 10 V, V _{S2} = ± 10 V			DG419B	Room Full	60		87 96		87 93	
Break-Before-Make Time Delay	t _D	R _L = 300 Ω, C _L = 35 pF V _{S1} = V _{S2} = ± 10 V			DG419B	Room	16	3		3		
Charge Injection	Q	C _L = 10 nF V _{gen} = 0 V, R _{gen} = 0 Ω			Room	38					pC	
Off Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz			Room	- 82					dB	
Channel-to-Channel Crosstalk ^e	X _{TALK}				DG419B	Room	- 88					

SPECIFICATIONS ^a									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^f	Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Dynamic Characteristics									
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$	Room	12					pF
Drain Off Capacitance ^e	$C_{D(off)}$		DG417B DG418B	Room	12				
Channel On Capacitance ^e	$C_{D(on)}$	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$	DG417B DG418B	Room	50				
			DG419B	Room	57				
Power Supplies									
Positive Supply Current	I_+	$V_+ = 16.5\text{ V}$, $V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room Full	0.001		1 5		1 5	μA
Negative Supply Current	I_-		Room Full	- 0.001	- 1 - 5		- 1 - 5		
Logic Supply Current	I_L		Room Full	0.001		1 5		1 5	
Ground Current	I_{GND}		Room Full	- 0.001	- 1 - 5		- 1 - 5		

SPECIFICATIONS ^a									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^f	Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	$I_S = -10\text{ mA}$, $V_D = 3.8\text{ V}$ $V_+ = 10.8\text{ V}$	Room Full	26		35 52		35 45	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$, See Switching Time Test Circuit	Room Full	100		125 155		125 143	ns
Turn-Off Time	t_{OFF}		Room Full	38		66 73		66 69	
Break-Before-Make Time Delay	t_D	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$	DG419B Room	62	25		25		
Transition Time	t_{TRANS}	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = 0\text{ V}$, 8 V , $V_{S2} = 8\text{ V}$, 0 V	Room Full	95		119 153		119 141	pC
Charge Injection	Q	$C_L = 10\text{ nF}$, $V_{gen} = 0\text{ V}$, $R_{gen} = 0\ \Omega$	Room	18					
Power Supplies									
Positive Supply Current	I_+	$V_+ = 13.2\text{ V}$, $V_L = 5.25\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room Full	0.001		1 5		1 5	μA
Negative Supply Current	I_-		Room	- 0.001	- 1 - 5		- 1 - 5		
Logic Supply Current	I_L		Room	0.001		1 5		1 5	
Ground Current	I_{GND}		Room	- 0.001	- 1 - 5		- 1 - 5		

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

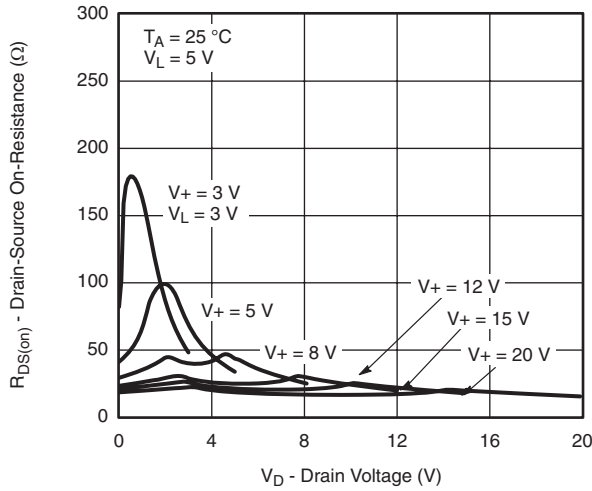
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.

e. Guaranteed by design, not subject to production test.

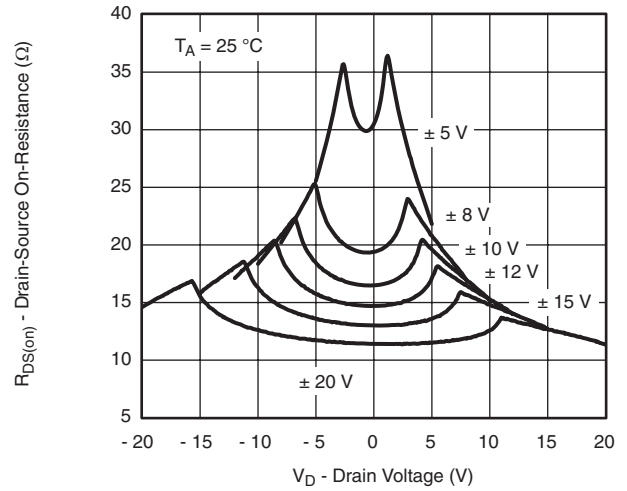
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

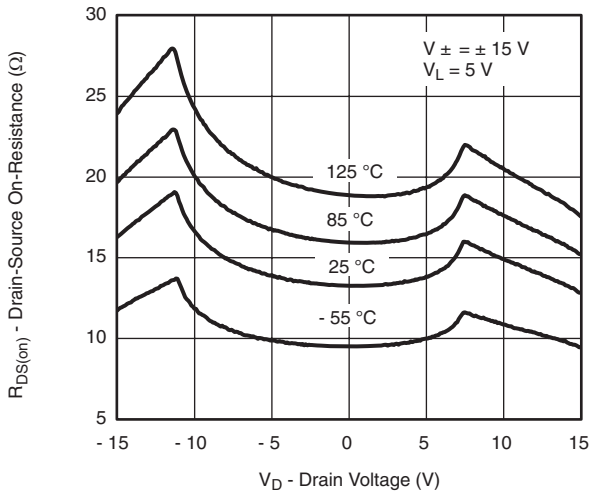
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



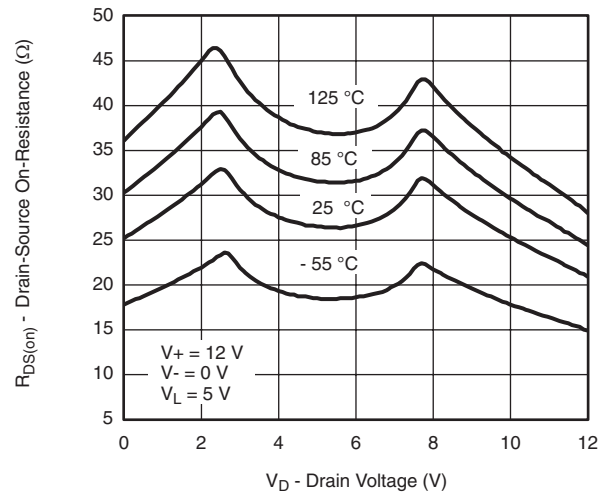
On-Resistance vs. V_D and Unipolar Power Supply Voltage



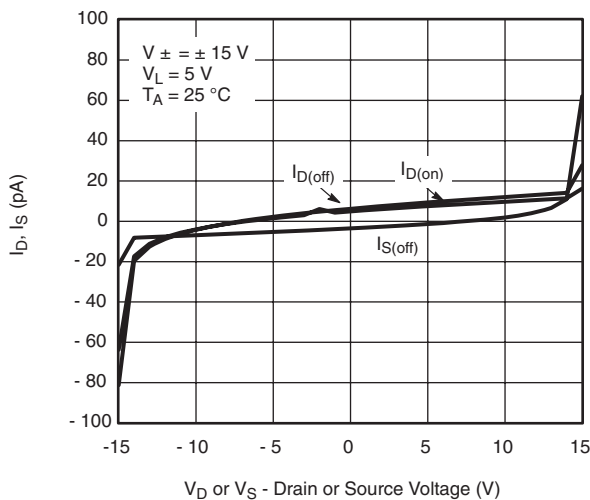
On-Resistance vs. V_D and Dual Supply Voltage



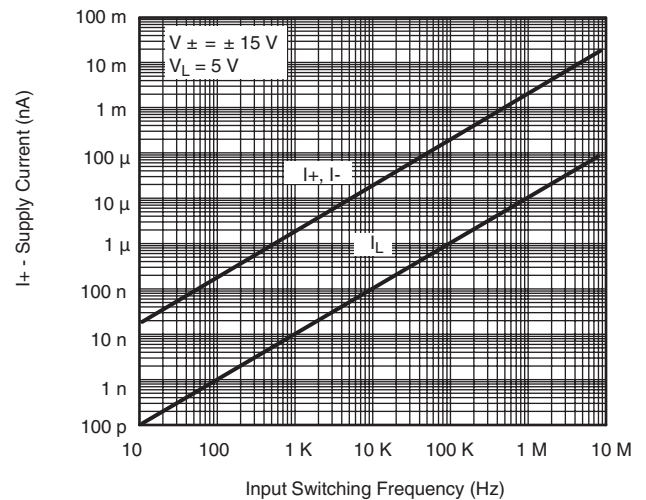
On-Resistance vs. V_D and Temperature



On-Resistance vs. V_D and Temperature

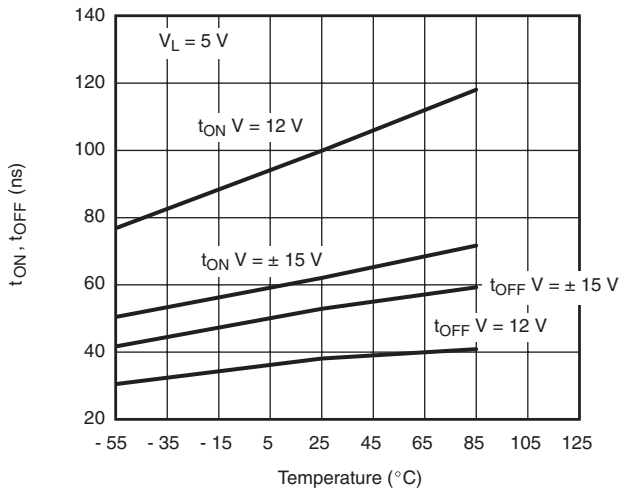


Leakage vs. Analog Voltage

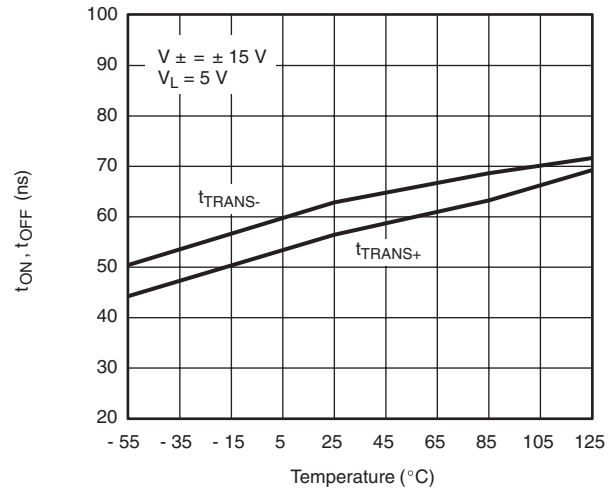


Supply Current vs. Input Switching Frequency

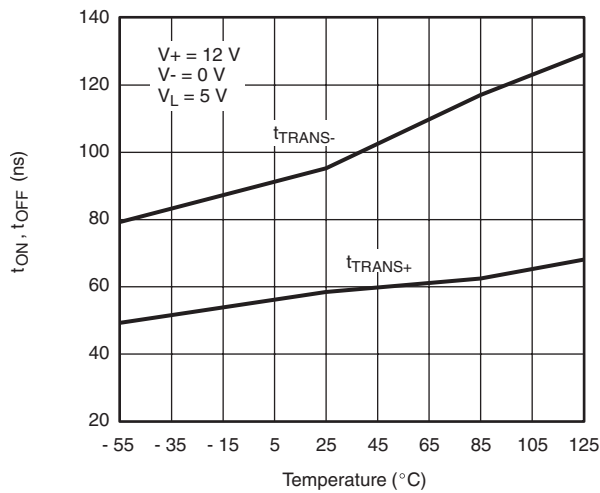
TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



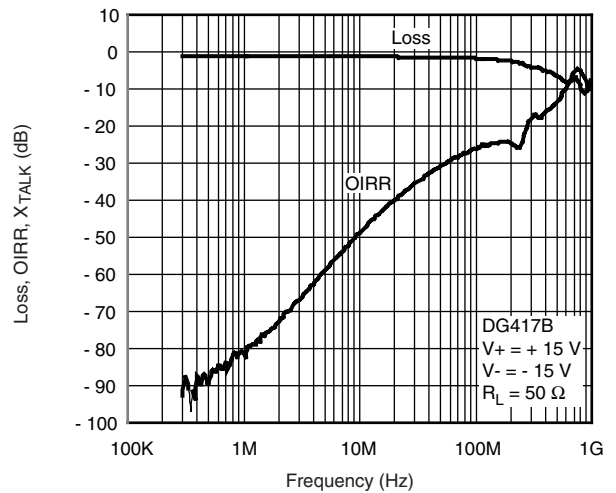
Switching Time vs. Temperature



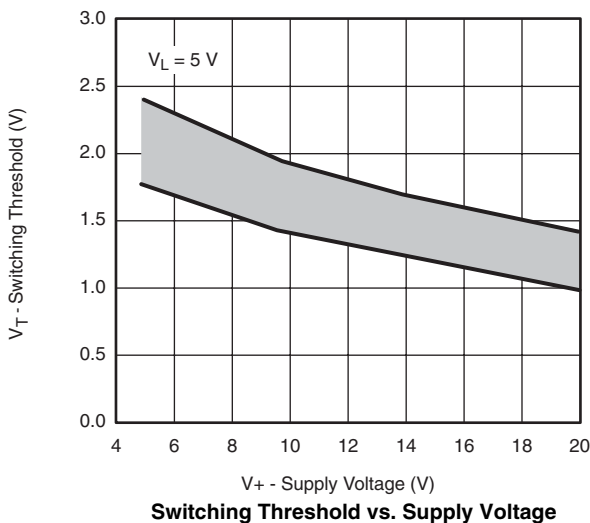
Transition Time vs. Temperature



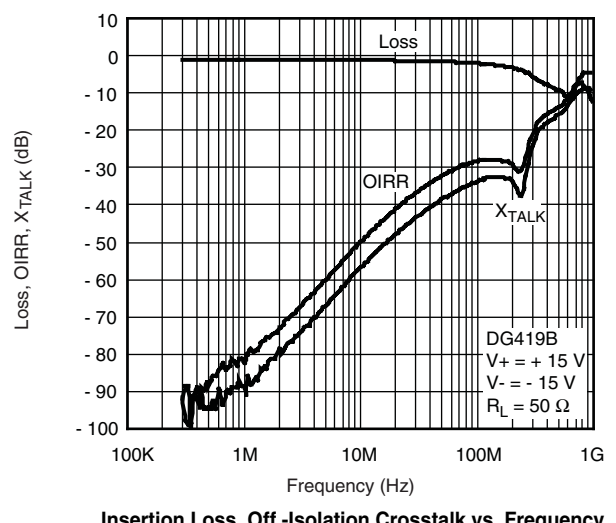
Transition Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

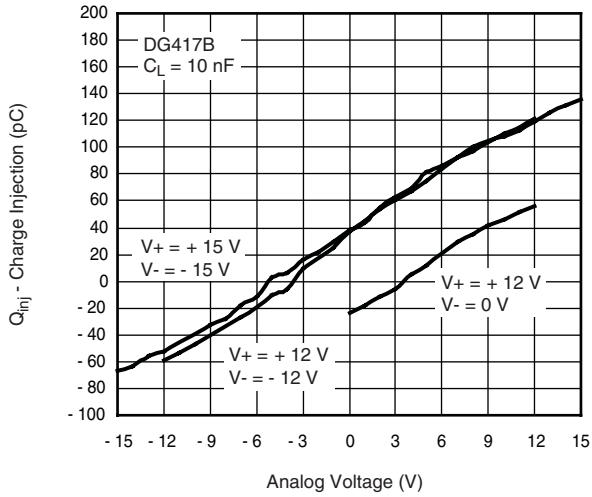


Switching Threshold vs. Supply Voltage

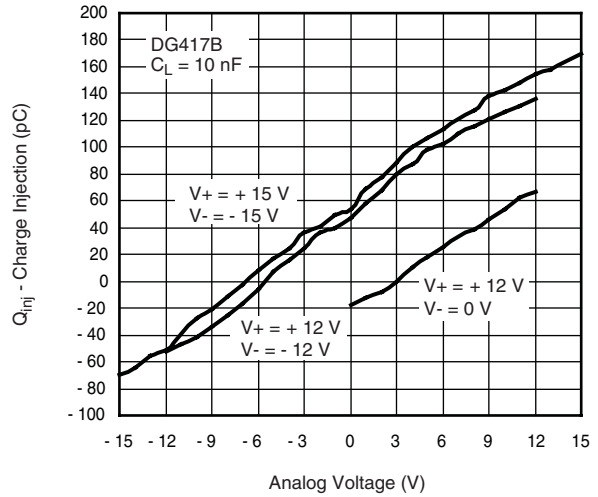


Insertion Loss, Off-Isolation Crosstalk vs. Frequency

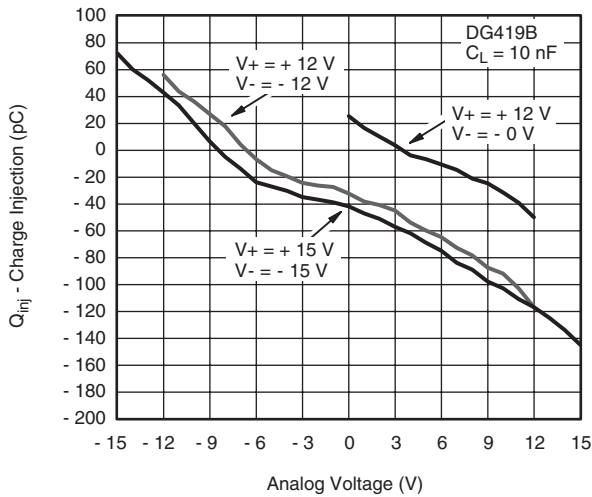
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



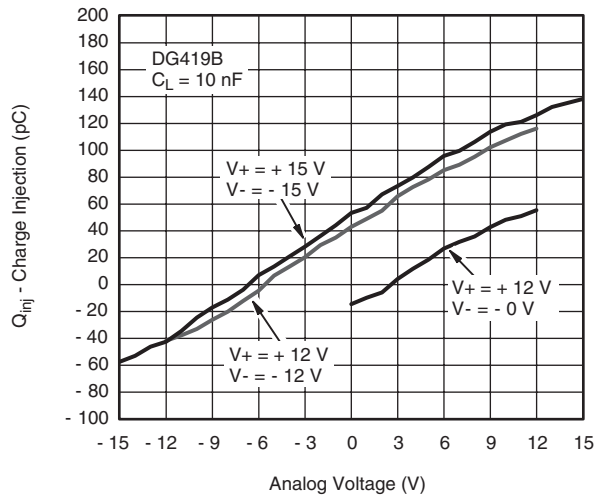
**Charge Injection vs. Analog Voltage
(Measured at drain pin)**



**Charge Injection vs. Analog Voltage
(Measured at source pin)**



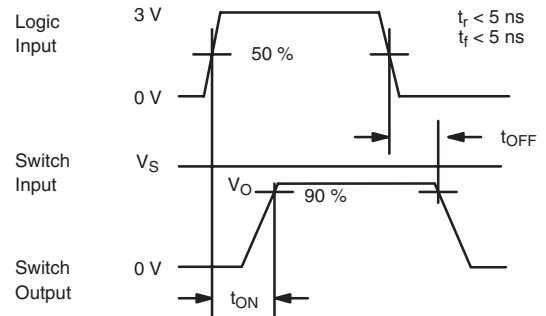
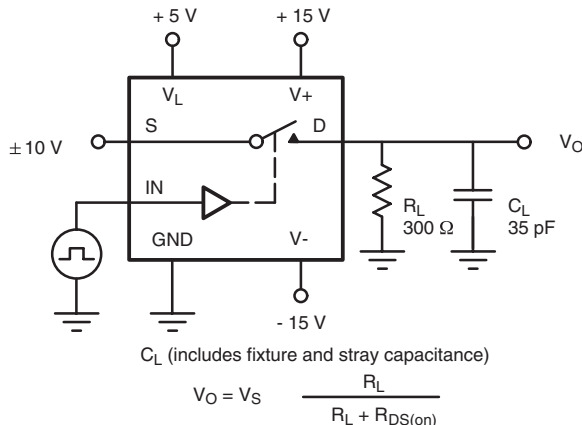
**Charge Injection vs. Analog Voltage
(Measured at drain pin)**



**Charge Injection vs. Analog Voltage
(Measured at source pin)**

TEST CIRCUITS

V_O is the steady state output with the switch on.



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 2. Switching Time (DG417B/418B)

TEST CIRCUITS

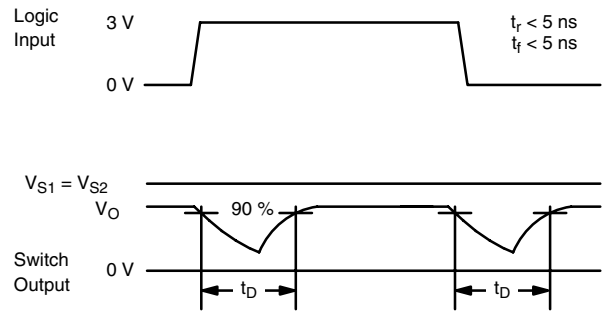
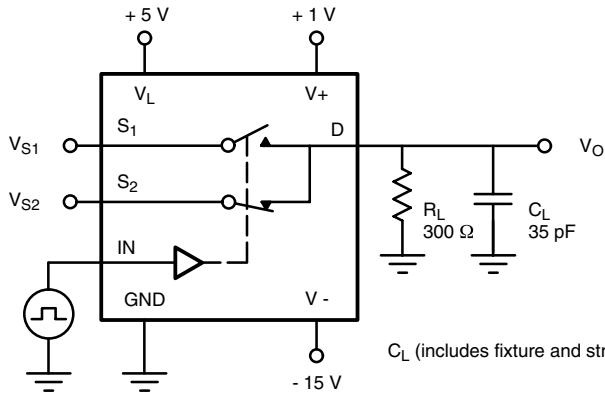
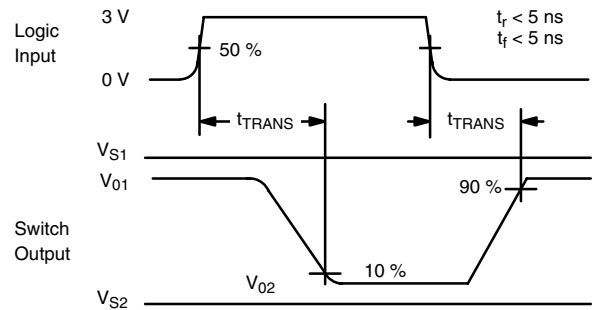
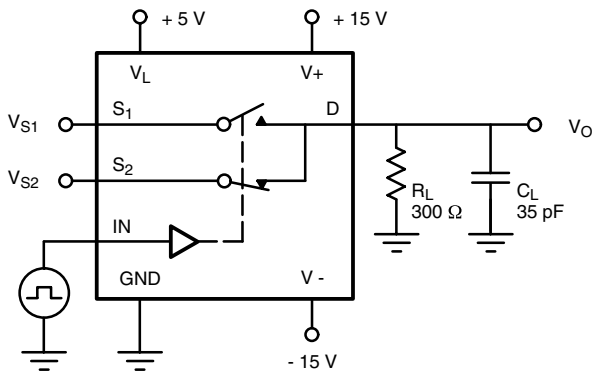


Figure 3. Break-Before-Make (DG419B)



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 4. Transition Time (DG419B)

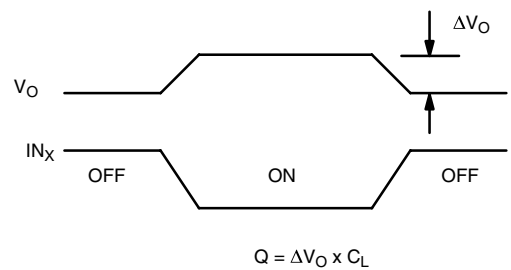
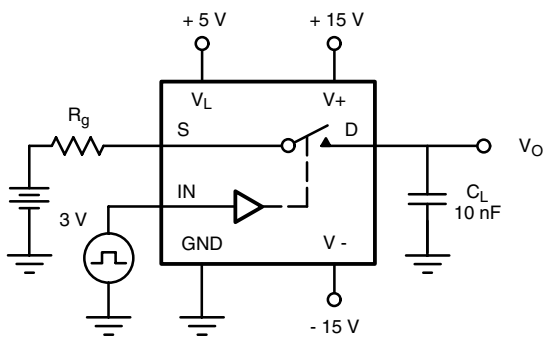


Figure 5. Charge Injection

TEST CIRCUITS

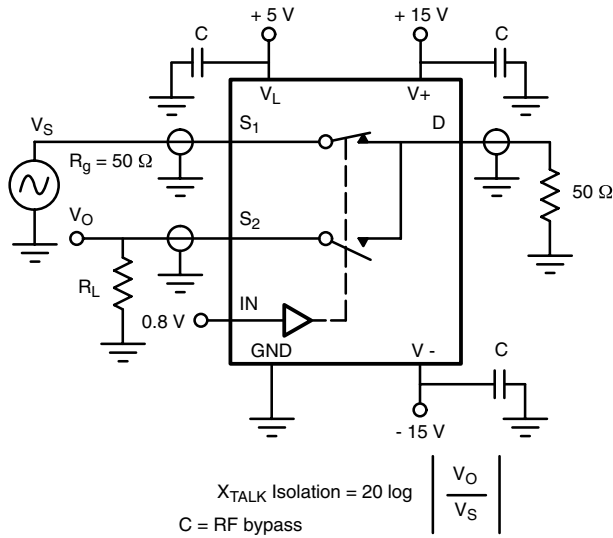


Figure 6. Crosstalk

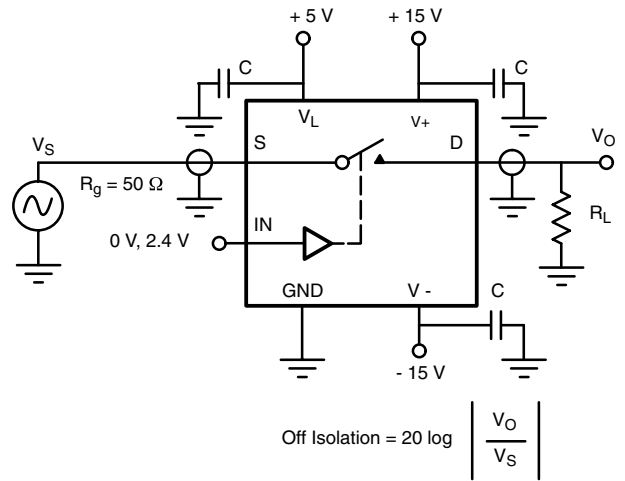


Figure 7. Off isolation

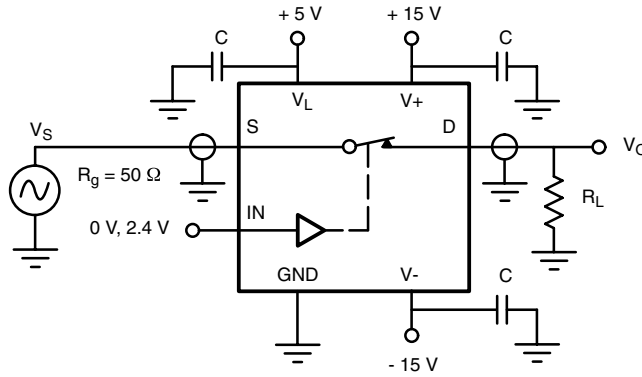


Figure 8. Insertion Loss

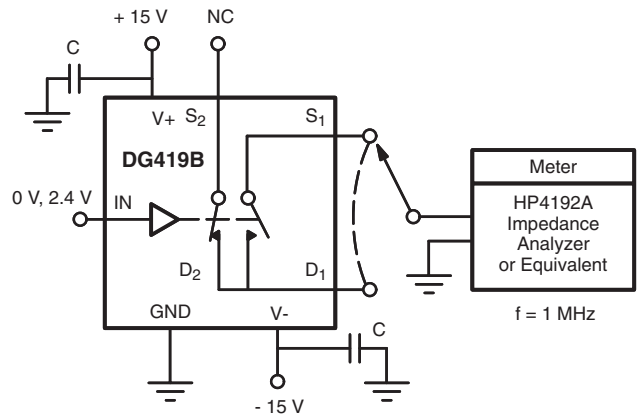
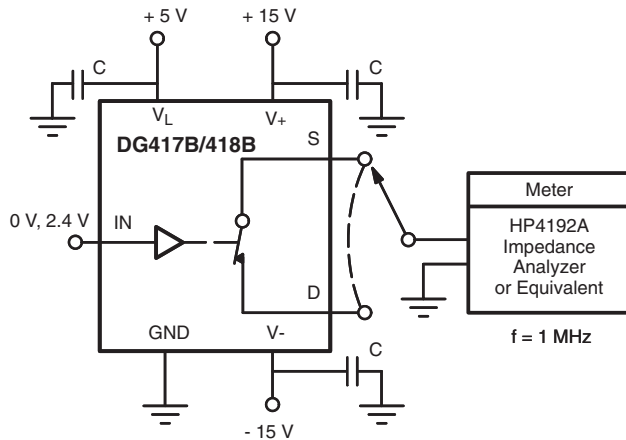
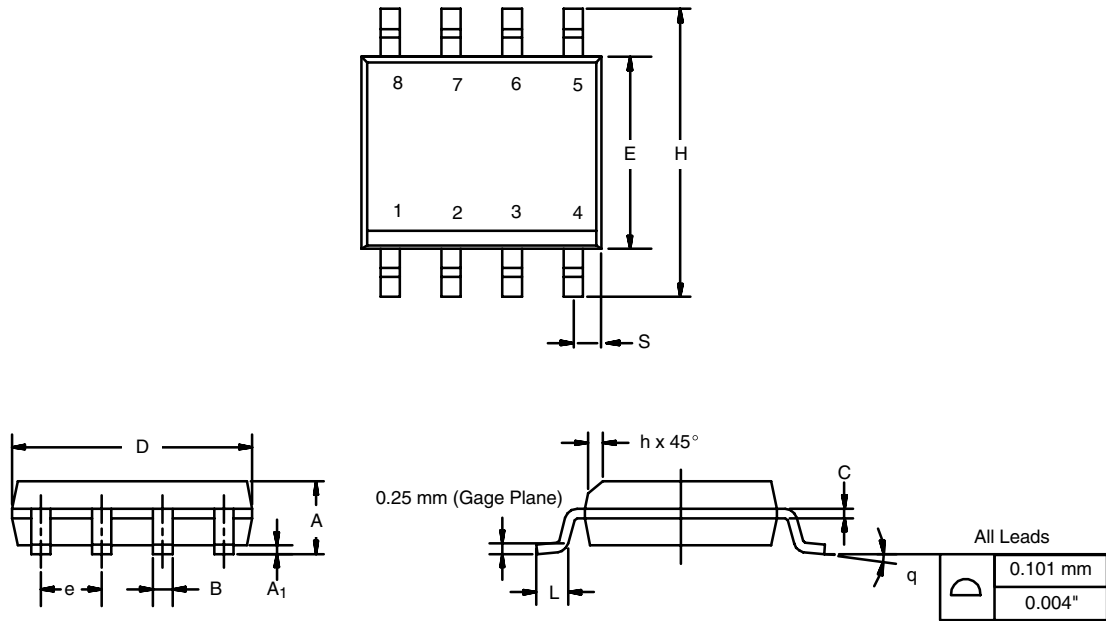


Figure 9. Source/Drain Capacitances

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72107.

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

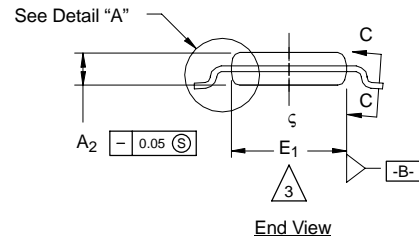
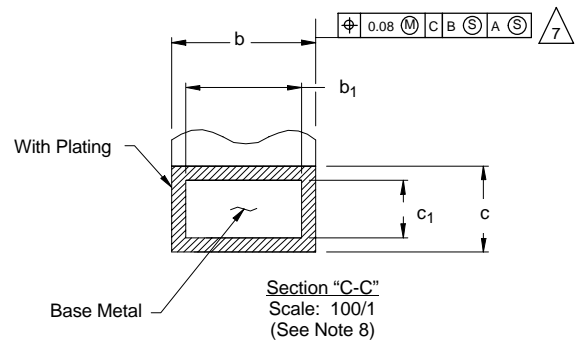
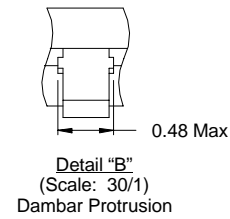
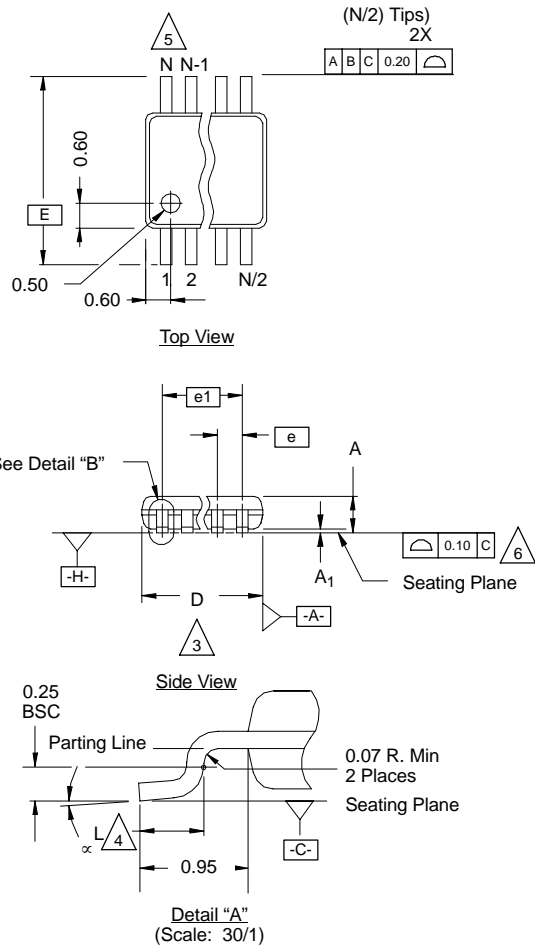


DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				



MSOP: 8-LEADS

JEDEC Part Number: MO-187, (Variation AA and BA)



NOTES:

- Die thickness allowable is 0.203 ± 0.0127 .
- Dimensioning and tolerances per ANSI.Y14.5M-1994.
- Dimensions "D" and "E₁" do not include mold flash or protrusions, and are measured at Datum plane [-H-], mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimension is the length of terminal for soldering to a substrate.
- Terminal positions are shown for reference only.
- Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
- The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
- Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
- Controlling dimension: millimeters.
- This part is compliant with JEDEC registration MO-187, variation AA and BA.
- Datums [-A-] and [-B-] to be determined Datum plane [-H-].
- Exposed pad area in bottom side is the same as teh leadframe pad size.

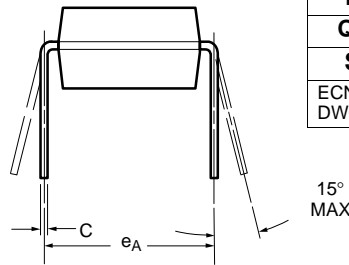
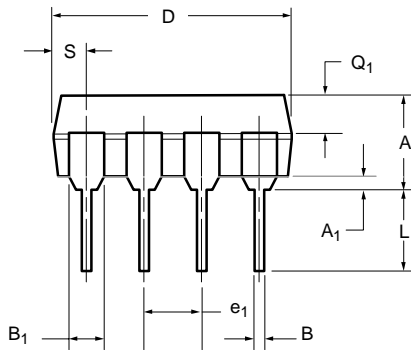
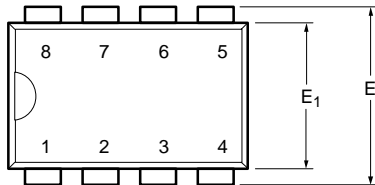
N = 8L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A₁	0.05	0.10	0.15	
A₂	0.75	0.85	0.95	
b	0.25	-	0.38	8
b₁	0.25	0.30	0.33	8
c	0.13	-	0.23	
c₁	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E₁	2.90	3.00	3.10	3
e	0.65 BSC			
e₁	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
α	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
 DWG: 5867



PDIP: 8-LEAD



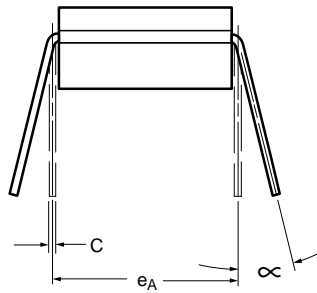
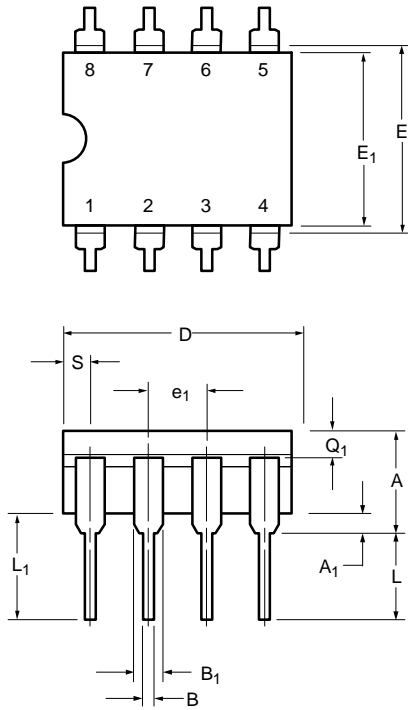
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	9.02	10.92	0.355	0.430
E	7.62	8.26	0.300	0.325
E₁	5.59	7.11	0.220	0.280
e₁	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q₁	1.27	2.03	0.050	0.080
S	0.76	1.65	0.030	0.065

ECN: S-03946—Rev. E, 09-Jul-01
DWG: 5478

NOTE: End leads may be half leads.



CERDIP: 8-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A ₁	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B ₁	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	9.40	10.16	0.370	0.400
E	7.62	8.26	0.300	0.325
E ₁	6.60	7.62	0.260	0.300
e ₁	2.54 BSC		0.100 BSC	
e _A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L ₁	3.18	5.08	0.150	0.200
Q ₁	1.27	2.16	0.050	0.085
S	0.64	1.52	0.025	0.060
∞	0°	15°	0°	15°

ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5348



Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/ppg?72286>), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.



Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

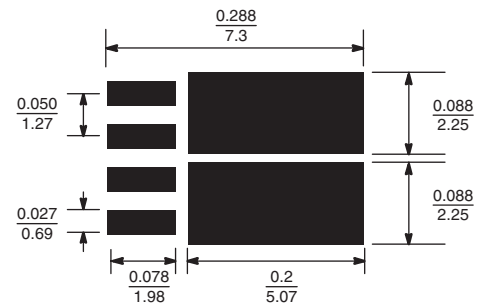


Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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