

# NB3N551

## 3.3 V / 5.0 V Ultra-Low Skew 1:4 Clock Fanout Buffer

### Description

The NB3N551 is a low skew 1-to 4 clock fanout buffer, designed for clock distribution in mind. The NB3N551 specifically guarantees low output-to-output skew. Optimal design, layout and processing minimize skew within a device and from device to device.

The output enable (OE) pin three-states the outputs when low.

### Features

- Input/Output Clock Frequency up to 180 MHz
- Low Skew Outputs (50 ps typical)
- Output goes to Three-State Mode via OE
- Operating Range:  $V_{DD} = 3.0 \text{ V to } 5.5 \text{ V}$
- Ideal for Networking Clocks
- Packaged in 8-pin SOIC
- Industrial Temperature Range
- These are Pb-Free Devices

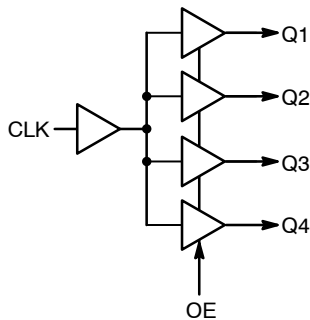


Figure 1. Block Diagram



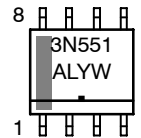
ON Semiconductor®

<http://onsemi.com>

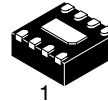
### MARKING DIAGRAMS\*



**SOIC-8  
D SUFFIX  
CASE 751**



3N551 = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package



**DFN8  
MN SUFFIX  
CASE 506AA**

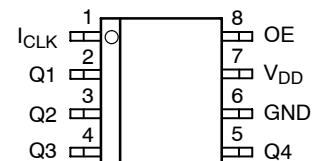


6K = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### PIN CONNECTIONS



### ORDERING INFORMATION

Device	Package	Shipping†
NB3N551DG	SOIC-8 (Pb-Free)	98 Units/Rail
NB3N551DR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel
NB3N551MNR4G	DFN-8 (Pb-Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NB3N551

OE	Function
0	Disable
1	Enable

Table 1. OE, Output Enable Function

## PIN DESCRIPTION

Pin #	Name	Type	Description
1	I <sub>CLK</sub>	(LV)CMOS/(LV)TTL Input	Clock Input. Internal pull-up resistor.
2	Q1	(LV)CMOS/(LV)TTL Output	Clock Output 1
3	Q2	(LV)CMOS/(LV)TTL Output	Clock Output 2
4	Q3	(LV)CMOS/(LV)TTL Output	Clock Output 3
5	Q4	(LV)CMOS/(LV)TTL Output	Clock Output 4
6	GND	Power	Negative supply voltage; Connect to ground, 0 V
7	V <sub>DD</sub>	Power	Positive supply voltage (3.0 V to 5.5 V)
8	OE	(LV)CMOS/(LV)TTL Input	Output Enable for the clock outputs. Outputs are enabled when HIGH or when left open; OE pin has internal pull-up resistor. Three-states outputs when LOW.

## MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>DD</sub>	Positive Power Supply	GND = 0 V	-	7.0	V
V <sub>I</sub> /V <sub>O</sub>	Input/Output Voltage	t ≤ 1.5 ns	-	GND-1.5 ≤ V <sub>I</sub> /V <sub>O</sub> ≤ V <sub>DD</sub> +1.5	V
T <sub>A</sub>	Operating Temperature Range, Industrial	-	-	≥ -40 to ≤ +85	°C
T <sub>stg</sub>	Storage Temperature Range	-	-	-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SOIC-8	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	(Note 1)	SOIC-8	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	DFN-8 DFN-8	129 84	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

## ATTRIBUTES

Characteristic	Value
ESD Protection	Human Body Model Machine Model > 4 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2)	Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL-94 code V-0 @ 0.125 in
Transistor Count	531 Devices
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test	

2. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

# NB3N551

## DC CHARACTERISTICS ( $V_{DD} = 3.0\text{ V to }3.6\text{ V}$ , $GND = 0\text{ V}$ , $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ ) (Note 3)

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{DD}$	Power Supply Current @ 135 MHz, No Load, $V_{DD} = 3.3\text{ V}$	–	20	40	mA
$V_{OH}$	Output HIGH Voltage – $I_{OH} = -25\text{ mA}$ , $V_{DD} = 3.3\text{ V}$	2.4	–	–	V
$V_{OL}$	Output LOW Voltage – $I_{OL} = 25\text{ mA}$	–	–	0.4	V
$V_{OH}$	Output HIGH Voltage – $I_{OH} = -12\text{ mA}$ (CMOS level)	$V_{DD} - 0.4$	–	–	V
$V_{IH}$ , $I_{CLK}$	Input HIGH Voltage, $I_{CLK}$	$(V_{DD}/2)+0.7$	–	3.8	V
$V_{IL}$ , $I_{CLK}$	Input LOW Voltage, $I_{CLK}$	–	–	$(V_{DD}/2)-0.7$	V
$V_{IH}$ , OE	Input HIGH Voltage, OE	2.0	–	$V_{DD}$	V
$V_{IL}$ , OE	Input LOW Voltage, OE	0	–	0.8	V
ZO	Nominal Output Impedance	–	20	–	$\Omega$
RPU	Input Pull-up Resistor, OE	–	220	–	k $\Omega$
CIN	Input Capacitance, OE	–	5.0	–	pF
IOS	Short Circuit Current	–	$\pm 50$	–	mA

## DC CHARACTERISTICS ( $V_{DD} = 4.5\text{ V to }5.5\text{ V}$ , $GND = 0\text{ V}$ , $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ ) (Note 3)

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{DD}$	Power Supply Current @ 135 MHz, No Load, $V_{DD} = 5.0\text{ V}$	–	50	95	mA
$V_{OH}$	Output HIGH Voltage – $I_{OH} = -35\text{ mA}$	2.4	–	–	V
$V_{OL}$	Output LOW Voltage – $I_{OL} = 35\text{ mA}$	–	–	0.4	V
$V_{OH}$	Output HIGH Voltage – $I_{OH} = -12\text{ mA}$ (CMOS level)	$V_{DD} - 0.4$	–	–	V
$V_{IH}$ , $I_{CLK}$	Input HIGH Voltage, $I_{CLK}$	$(V_{DD}/2) + 1$	–	5.5	V
$V_{IL}$ , $I_{CLK}$	Input LOW Voltage, $I_{CLK}$	–	–	$(V_{DD}/2) - 1$	V
$V_{IH}$ , OE	Input HIGH Voltage, OE	2.0	–	$V_{DD}$	V
$V_{IL}$ , OE	Input LOW Voltage, OE	0	–	0.8	V
ZO	Nominal Output Impedance	–	20	–	$\Omega$
RPU	Input Pull-up Resistor, OE	–	220	–	k $\Omega$
CIN	Input Capacitance, OE	–	5.0	–	pF
IOS	Short Circuit Current	–	$\pm 80$	–	mA

## AC CHARACTERISTICS ( $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ , $GND = 0\text{ V}$ , $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ ) (Note 3)

Symbol	Characteristic	Min	Typ	Max	Unit
$f_{in}$	Input Frequency	–	–	180	MHz
$t_{jitter}$ (pd)	Period Jitter (RMS, $1\sigma$ )	–	2.0	–	ps
$t_r/t_f$	Output rise and fall times; 0.8 V to 2.0 V	–	0.5	1.0	ns
$t_{pd}$	Propagation Delay, CLK to Qn, 0 – 180 MHz, (Note 4)	1.5	3.0	6.0	ns
$t_{skew}$	Output-to-output skew; (Note 5)	–	50	160	ps

3. Outputs loaded with external  $R_L = 33\text{-}\Omega$  series resistor and  $C_L = 15\text{ pF}$  to GND for proper operation. Duty cycle out = duty in. A  $0.01\text{ }\mu\text{F}$  decoupling capacitor should be connected between  $V_{DD}$  and GND. A  $33\text{ }\Omega$  series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

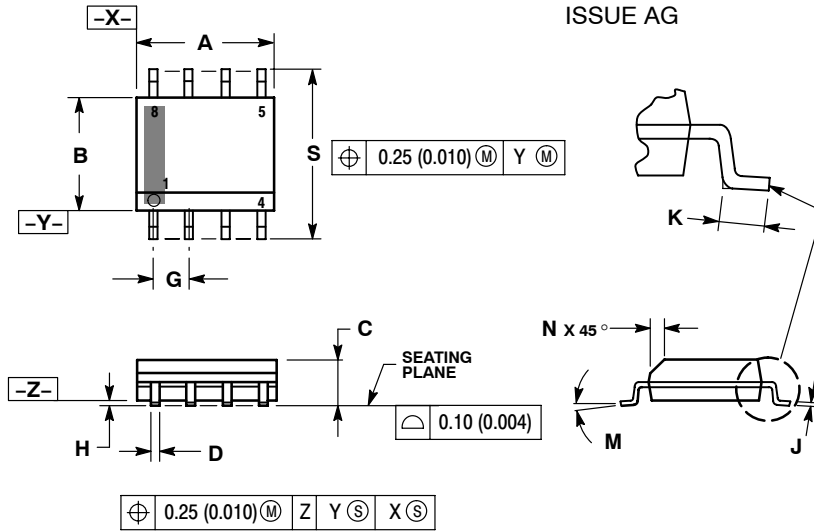
4. Measured with rail-to-rail input clock.

5. Measured on rising edges at  $V_{DD} \div 2$ .

# NB3N551

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AG

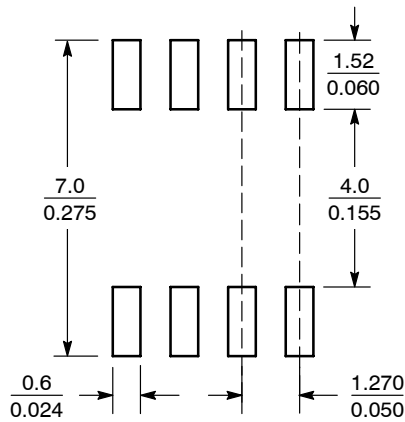


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



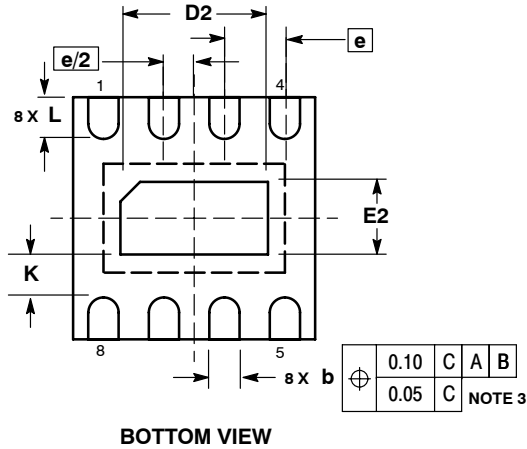
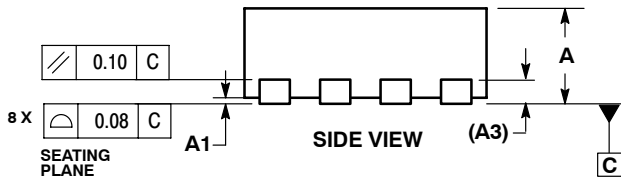
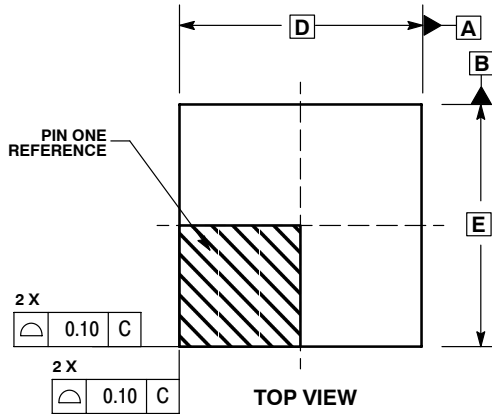
SCALE 6:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NB3N551

## PACKAGE DIMENSIONS


DFN8  
CASE 506AA-01  
ISSUE D



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)  
Email: [org@lifeelectronics.ru](mailto:org@lifeelectronics.ru)