CS2844/CS3844
CS2845/CS3845

Current Mode PWM Control Circuit with 50% Max Duty Cycle

Description

The CS3844/45 provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

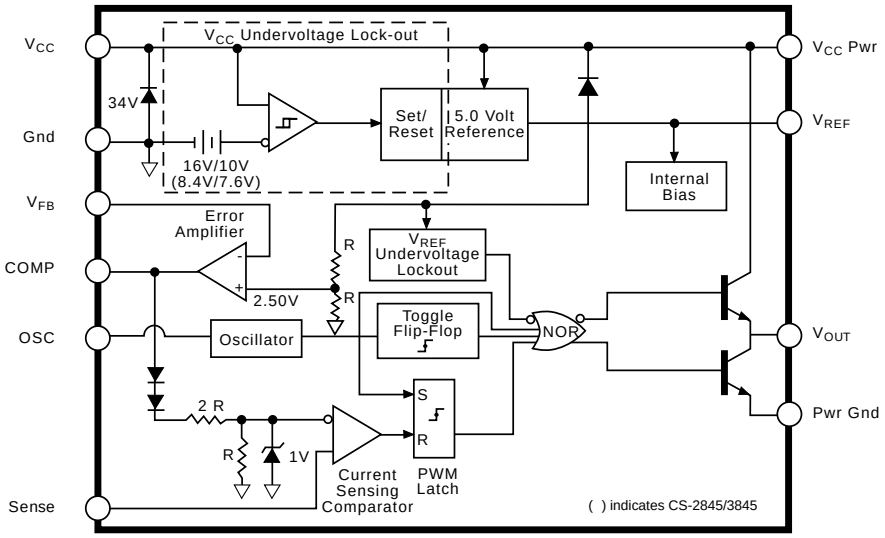
The CS3844 family incorporates a new precision temperature-controlled oscillator to minimize variations in frequency. An internal toggle flip-flop, which blanks the output every other clock cycle, limits the duty-cycle range to less than 50%. An undervoltage lockout ensures that V_{REF} is stabilized before the output stage is enabled. In the CS2844/CS3844 turn on occurs at 16V and turn off at 10V. In the CS2845/CS3845 turn on is at 8.4V and turn off at 7.6V.

Other features include low start-up current, pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads, such as gate of a power MOSFET. The output is low in the off state, consistent with N-channel devices.

Absolute Maximum Ratings

Supply Voltage (I_{CC}<30mA).....Self Limiting
Supply Voltage (Low Impedance Source) 30V
Output Current.....±1A
Output Energy (Capacitive Load).....5μJ
Analog Inputs (V_{FB}, V_{SENSE}) .....-0.3V to 5.5V
Error Amp Output Sink Current 10mA
Lead Temperature Soldering
Wave Solder (through hole styles only) .....10 sec. max, 260°C peak
Reflow (SMD styles only) .....60 sec. max above 183°C, 230°C peak

Block Diagram

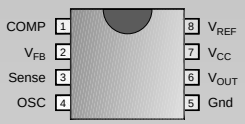


Features

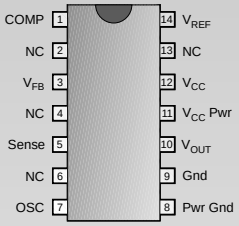
- Optimized for Offline Control
- Temp. Compensated Oscillator
- 50% Max Duty-cycle Clamp
- V_{REF} Stabilized before Output Stage is Enabled
- Low Start-up Current
- Pulse-by-pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 1% Trimmed Bandgap Ref.
- High Current Totem Pole Output

Package Options

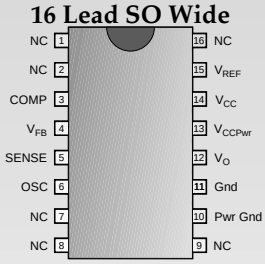
8 Lead PDIP & SO Narrow



14 Lead SO Narrow



16 Lead SO Wide



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Electrical Characteristics: -25 ≤ T_A ≤ 85°C for CS2844/2845, 0 ≤T_A ≤ 70°C for CS3844/3845. V_{CC} = 15V (Note 1); R_T = 10kΩ, C_T = 3.3nF for sawtooth mode., unless otherwise stated.

PARAMETER	TEST CONDITIONS	CS2844/CS2845			CS3844/CS3845			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
■ Reference Section								
Output Voltage	T_J=25°C, I_{REF}=1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12≤V_{CC}≤25V		6	20		6	20	mV
Load Regulation	1≤I_{REF}≤20mA		6	25		6	25	mV
Temperature Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.90		5.10	4.82		5.18	V
Output Noise Voltage	10Hz≤ f≤10kHz, T_J=25°C (Note 2)		50			50		μV
Long Term Stability	T_A=125°C, 1000 Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit	T_A=25°C	-30	-100	-180	-30	-100	-180	mA
■ Oscillator Section								
Initial Accuracy	Sawtooth Mode, T_J=25°C	47	52	57	47	52	57	kHz
Voltage Stability	12≤V_{CC}≤25V		0.2	1.0		0.2	1.0	%
Temperature Stability	Sawtooth Mode T_{MIN}≤T_A≤T_{MAX} (Note 2)		5			5		%
Amplitude	V_{OSC} (peak to peak)		1.7			1.7		V
■ Error Amp Section								
Input Voltage	V_{COMP}=2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current	V_{FB}=0V		-0.3	-1.0		-0.3	-2.0	μA
A_{VOL}	2≤V_{OUT}≤4V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1.0		0.7	1.0		MHz
PSRR	12≤V_{CC}≤25V	60	70		60	70		dB
Output Sink Current	V_{FB}=2.7V, V_{COMP}=1.1V	2	6		2	6		mA
Output Source Current	V_{FB}=2.3V, V_{COMP}=5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} HIGH	V_{FB}=2.3V, R_L=15kΩ to Gnd	5	6		5	6		V
V_{OUT} LOW	V_{FB}=2.7V, R_L=15kΩ to V_{REF}		0.7	1.1		0.7	1.1	V
■ Current Sense Section								
Gain	(Notes 3 & 4)	2.85	3.00	3.15	2.85	3.00	3.15	V/V
Maximum Input Signal	V_{COMP}=5V (Note 3)	0.9	1.0	1.1	0.9	1.0	1.1	V
PSRR	12≤V_{CC}≤25V (Note 3)		70			70		dB
Input Bias Current	V_{Sense}=0V		-2	-10		-2	-10	μA
Delay to Output	T_J=25°C (Note 2)		150	300		150	300	ns
■ Output Section								
Output Low Level	I_{SINK}=20mA		0.1	0.4		0.1	0.4	V
	I_{SINK}=200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE}=20mA	13.0	13.5		13.0	13.5		V
	I_{SOURCE}=200mA	12.0	13.5		12.0	13.5		V
Rise Time	T_J=25°C, C_L=1nF (Note 2)		50	150		50	150	ns
Fall Time	T_J=25°C, C_L=1nF (Note 2)		50	150		50	150	ns

Electrical Characteristics: -25≤T_A≤85°C for CS2844/2845, 0≤T_A≤70°C for CS3844/3845. V_{CC}=15V (Note 1); R_T=10kΩ, C_T=3.3nF for sawtooth mode., unless otherwise stated.

PARAMETER	TEST CONDITIONS	CS2844/CS2845 MIN	CS2844/CS2845 TYP	CS2844/CS2845 MAX	CS3844/CS3845 MIN	CS3844/CS3845 TYP	CS3844/CS3845 MAX	UNITS
■ Total Standby Current								
Start-Up Current			0.5	1.0		0.5	1.0	mA
Operating Supply Current	V_{FB}=V_{Sense}=0V R_T=10kΩ, C_T=3.3nF		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC}=25mA		34			34		V
■ PWM Section								
Maximum Duty Cycle		46	48	50	46	48	50	%
Minimum Duty Cycle				0			0	%

PARAMETER	TEST CONDITIONS	CS2844 MIN	CS2844 TYP	CS2844 MAX	CS3844 MIN	CS3844 TYP	CS3844 MAX	CS2845/CS3845 MIN	CS2845/CS3845 TYP	CS2845/CS3845 MAX	UNITS
■ Under-Voltage Lockout Section											
Start Threshold		15	16	17	14.5	16	17.5	7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	9	10	11	8.5	10	11.5	7.0	7.6	8.2	V

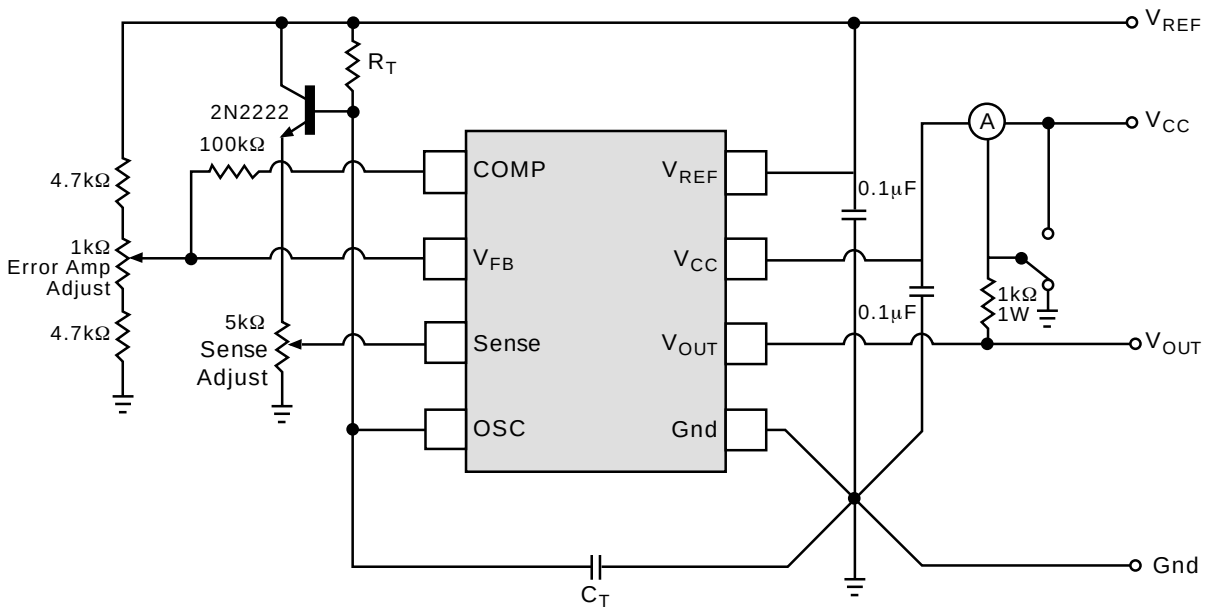
Notes: 1. Adjust V_{cc} above the start threshold before setting at 15V.
2.These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with V_{FB}=0.
4. Gain defined as:

$$A = \frac{\Delta V_{COMP}}{\Delta V_{Sense}} ; 0 \le V_{Sense} \le 0.8V.$$

Package Pin Description

PACKAGE PIN # 8L PDIP/SO	PACKAGE PIN # 14L SO Narrow	PACKAGE PIN # 16L SO Wide	PIN SYMBOL	FUNCTION
1	1	3	COMP	Error amp output, used to compensate error amplifier.
2	3	4	V_{FB}	Error amp inverting input.
3	5	5	Sense	Noninverting input to Current Sense Comparator.
4	7	6	OSC	Oscillator timing network with Capacitor to Ground, resistor to V_{REF}.
5	9	11	Gnd	Ground.
	8	10	Pwr Gnd	Output driver Ground.
6	10	12	V_{OUT}	Output drive pin.
	11	13	V_{CC}Pwr	Output driver positive supply.
7	12	14	V_{CC}	Positive power supply.
8	14	15	V_{REF}	Output of 5V internal reference.
	2,4,6,13	1,2,7,8,9,16	NC	No Connection.

Test Circuit Open Loop Laboratory Test Fixture



Circuit Description

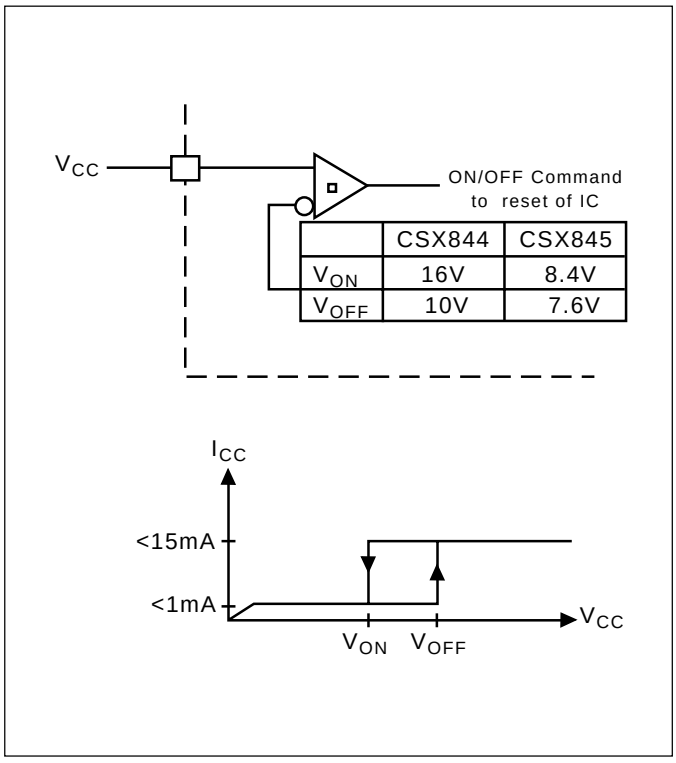


Figure 1: Startup voltage for CSX844 and CSX845.

Undervoltage Lockout

During Undervoltage Lockout (Figure 1), the output driver is biased to sink minor amounts of current. The output should be shunted to ground with a resistor to prevent activating the power switch with extraneous leakage currents.

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 2). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of OSC components.

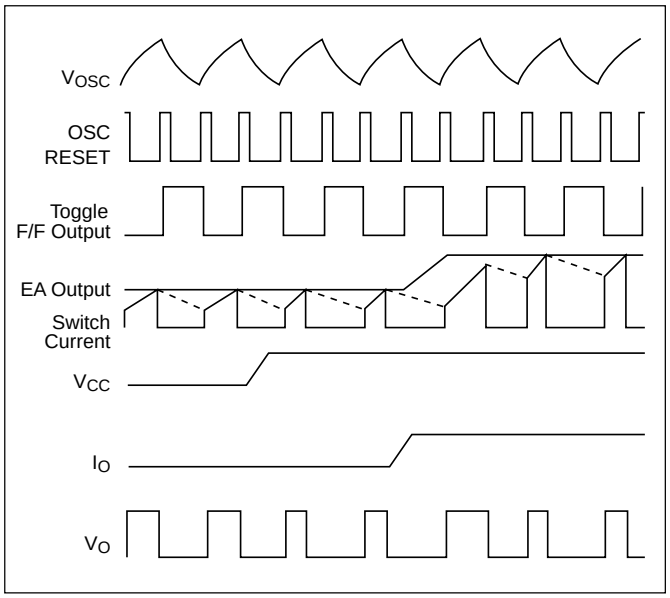


Figure 2: Timing Diagram

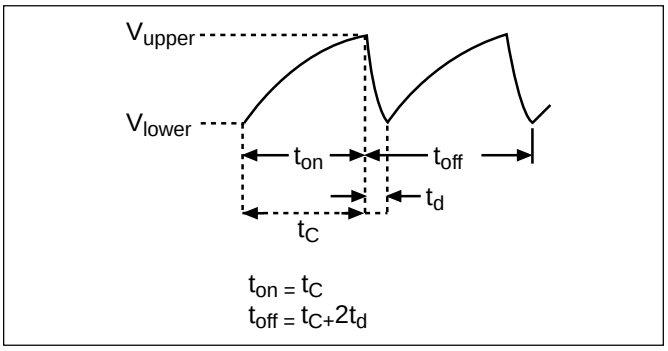


Figure 3: Duty Cycle parameters.

Setting the Oscillator

The times T_c and T_d can be determined as follows:

$$t_c = R_T C_T \ln\left(\frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}}\right)$$

$$t_d = R_T C_T \ln\left(\frac{V_{REF} - I_d R_T - V_{lower}}{V_{REF} - I_d R_T - V_{upper}}\right)$$

Substituting in typical values for the parameters in the above formulas:

$V_{REF} = 5.0V$, $V_{upper} = 2.7V$, $V_{lower} = 1.0V$, $I_d = 8.3mA$, then

$$t_c \approx 0.5534 R_T C_T$$

$$t_d = R_T C_T \ln\left(\frac{2.3 - 0.0083\ R_T}{4.0 - 0.0083\ R_T}\right)$$

For better accuracy R_T should be ≥10kΩ.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Gnd in a single point ground.

The transistor and 5kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

Package Specification

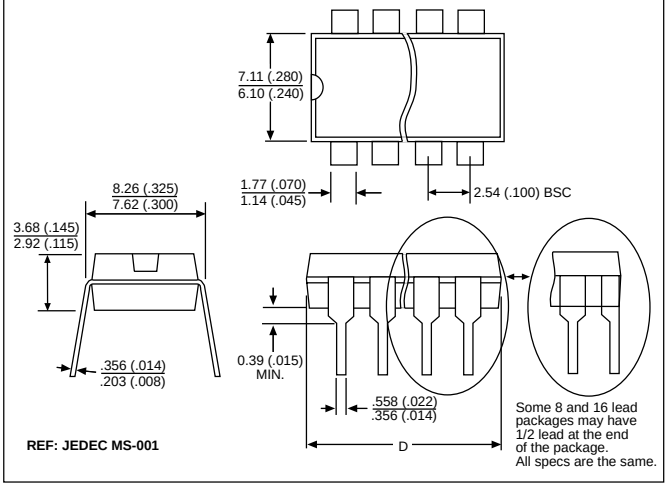
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8 Lead PDIP	10.16	9.02	.400	.355
8 Lead SO Narrow	5.00	4.80	.197	.189
14L SO Narrow	8.75	8.55	.344	.337
16L SO Wide	10.50	10.10	.413	.398

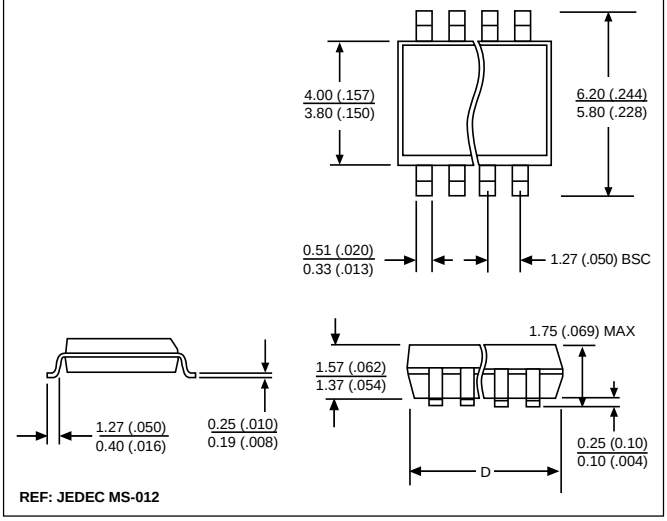
PACKAGE THERMAL DATA

Thermal Data		8 L PDIP	8L SO Narrow	14 L SO Narrow	16L SO Wide	
$R_{\Theta JC}$	typ	52	45	30	23	°C/W
$R_{\Theta JA}$	typ	100	165	125	105	°C/W

Plastic DIP (N); 300 mil wide



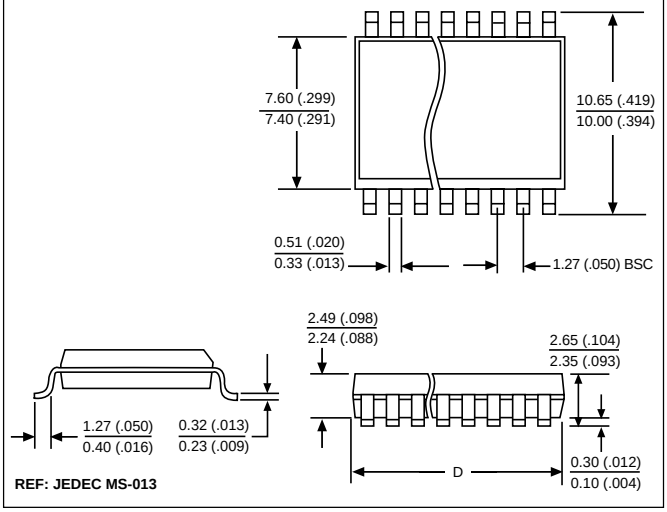
Surface Mount Narrow Body (D); 150 mil wide



Ordering Information

Part Number	0°C to 70°C	-25°C to 85°C	Description
CS2844LN8		•	8L PDIP
CS2844LD14		•	14L SO
CS2844LDR14		•	14L SO (Tape & Reel)
CS2844LDW16		•	16L SO Wide
CS2844LDWR16		•	16L SO Wide (Tape & Reel)
CS2845LN8		•	8L PDIP
CS2845LDW16		•	16L SO Wide
CS2845LDWR16		•	16L SO Wide (Tape & Reel)
CS3844GN8	•		8L PDIP
CS3844GD8	•		8L SO
CS3844GDR8	•		8L SO (Tape & Reel)
CS3844GD14	•		14L SO
CS3844GDR14	•		14L SO (Tape & Reel)
CS3844GDW16	•		16L SO Wide
CS3844GDWR16	•		16L SO Wide (Tape & Reel)
CS3845GN8	•		8L PDIP
CS3845GD8	•		8L SO
CS3845GDR8	•		8L SO (Tape & Reel)
CS3845GD14	•		14L SO
CS3845GDR14	•		14L SO (Tape & Reel)
CS3845GDW16	•		16L SO Wide
CS3845GDWR16	•		16L SO Wide (Tape & Reel)

Surface Mount Wide Body (DW); 300 mil wide



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