

1. General description

Planar passivated Silicon Controlled Rectifier in a SOT429N (TO247) plastic package intended for use in applications requiring very high inrush current capability and high thermal cycling performance.

2. Features and benefits

- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- High voltage capacity
- Very high current surge capability

3. Applications

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control
- Uninterruptible Power Supply (UPS)
- Solid State Relay (SSR)
- Traction battery charging

4. Quick reference data

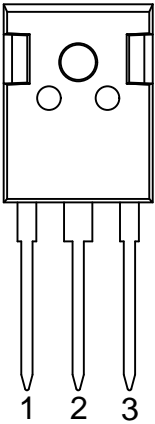

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	1200	V
V_{RRM}	repetitive peak reverse voltage		-	-	1200	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	1100	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	-	1210	A
T_j	junction temperature		-	-	150	°C
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 117\text{ °C}$	-	-	80	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 117\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	126	A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7 ; Fig. 8	-	-	70	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 800\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$; $R_{GK} = 100\text{ }\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform	1500	-	-	V/ μs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 TO-247 (SOT429N)	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT158W-1200T	TO-247	Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247	SOT429N

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	1200	V
V_{RRM}	repetitive peak reverse voltage		-	1200	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 117\text{ }^{\circ}\text{C}$	-	80	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 117\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	126	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	1100	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 8.3\text{ ms}$	-	1210	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; no voltage reapplied	-	6115	A ² s
di_T/dt	rate of rise of on-state current	$I_G = 200\text{ mA}$	-	150	A/ μs
I_{GM}	peak gate current		-	8	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	20	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	1	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	150	$^{\circ}\text{C}$

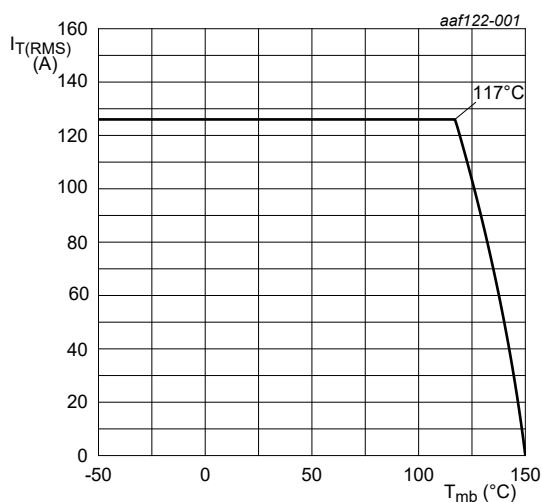
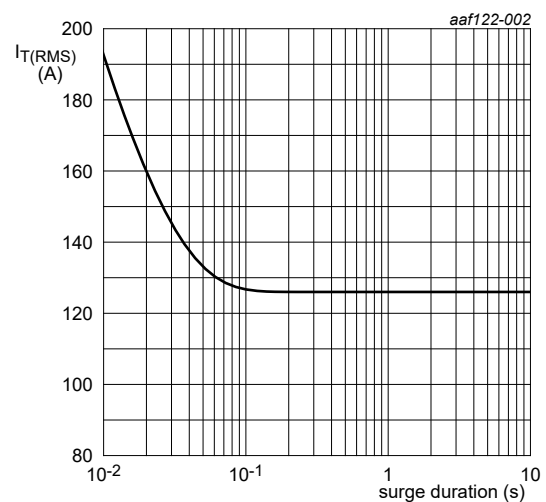
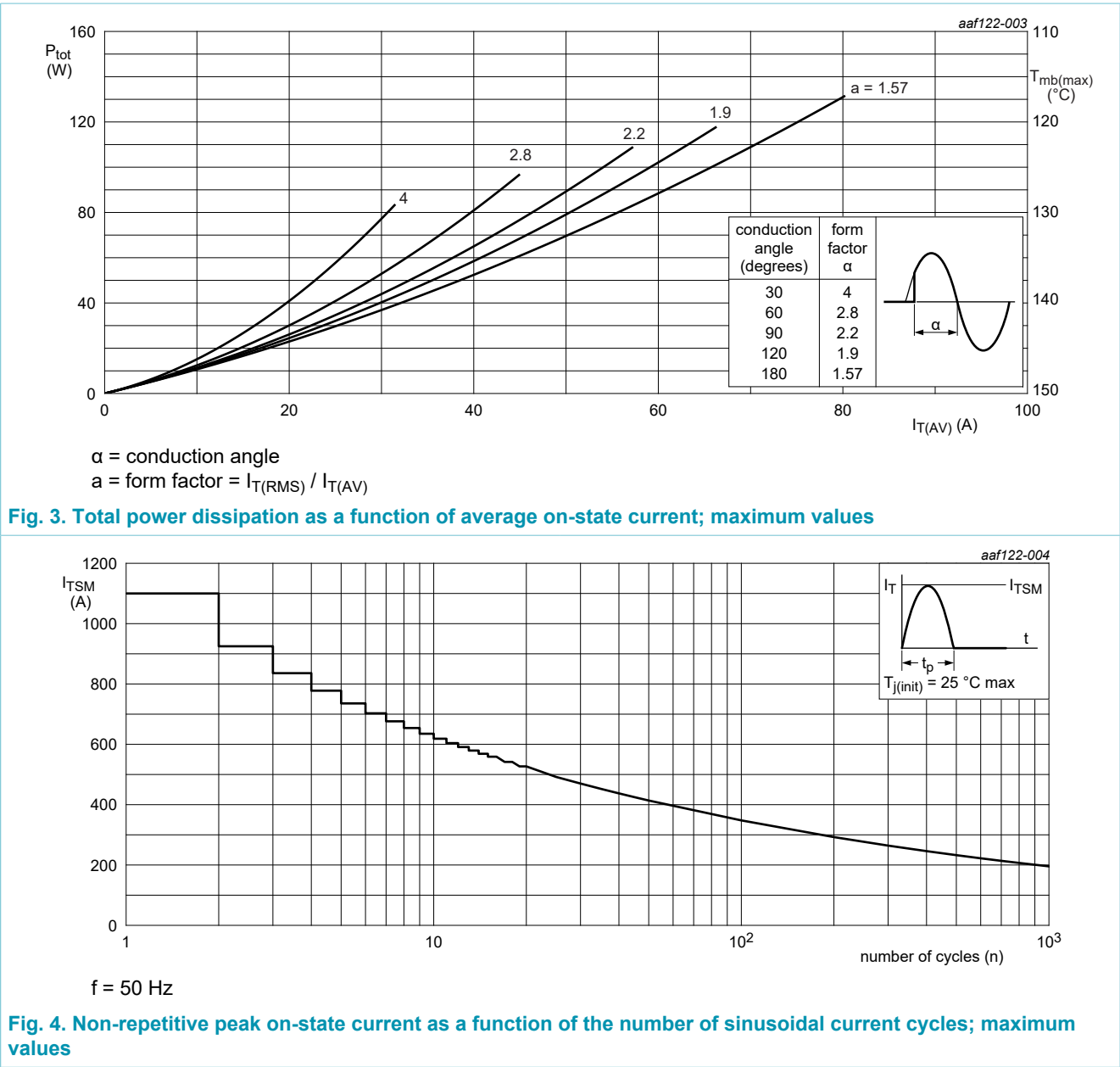


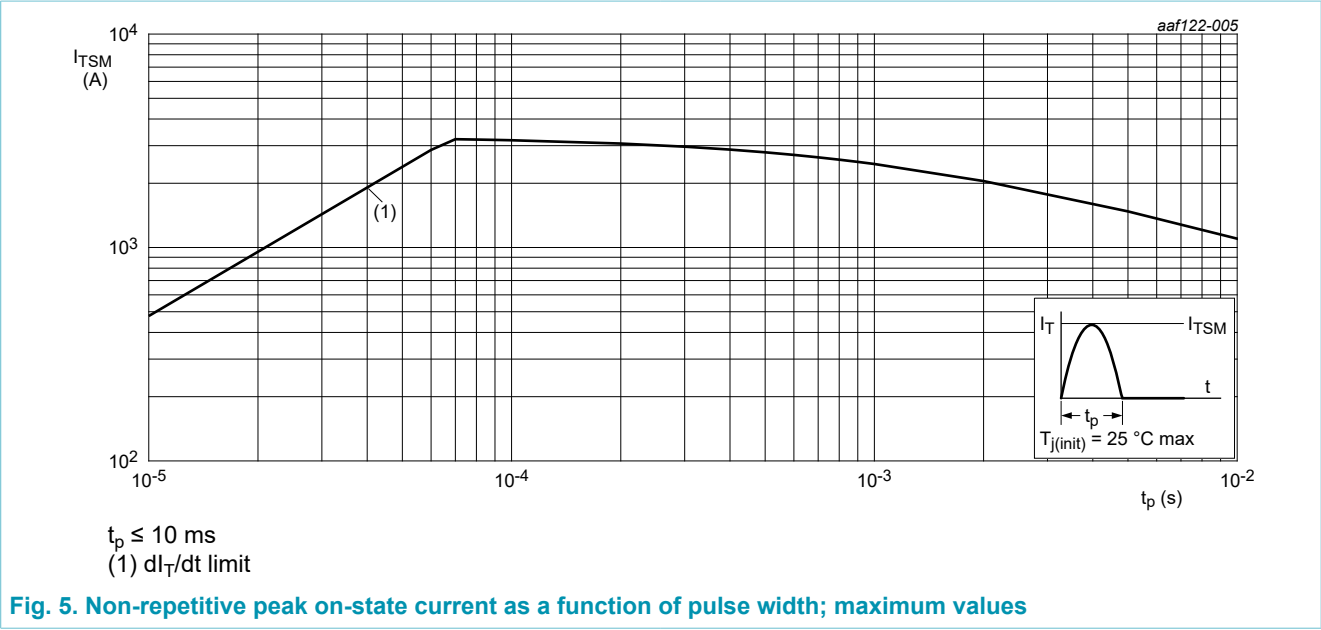
Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



$f = 50\text{ Hz}$; $T_{mb} = 117\text{ }^{\circ}\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

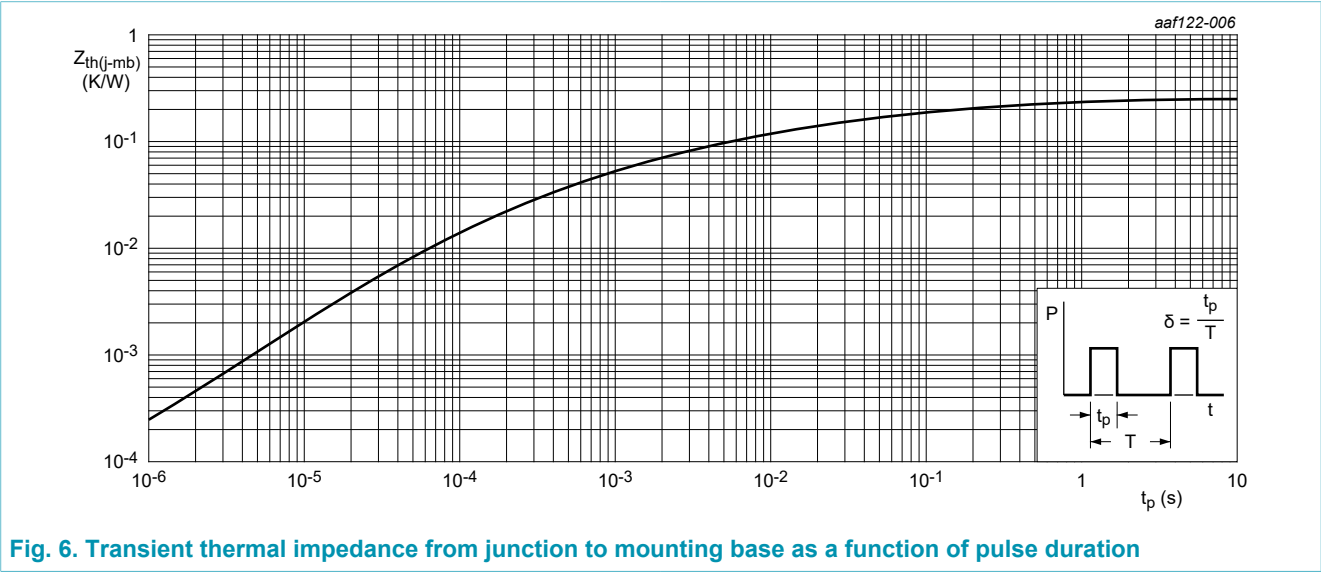




8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 6	-	-	0.25	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	50	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 ; Fig. 8	-	-	70	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	-	300	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	-	200	mA
V_T	on-state voltage	$I_T = 80\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	-	1.35	V
		$I_T = 160\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	-	1.65	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12	-	0.7	1	V
		$V_D = 800\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 12	0.25	0.4	-	V
I_D	off-state current	$V_D = 1200\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	-	3	mA
I_R	reverse current	$V_R = 1200\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	-	3	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 800\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 100\text{ }\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform	1500	-	-	V/ μs
		$V_{DM} = 800\text{ V}$; $T_j = 150\text{ }^\circ\text{C}$; $R_{GK} = 100\text{ }\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform	1000	-	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 40\text{ A}$; $V_D = 800\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$; $T_j = 25\text{ }^\circ\text{C}$	-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 804\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{TM} = 20\text{ A}$; $V_R = 25\text{ V}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 50\text{ V}/\mu\text{s}$; $R_{GK(ext)} = 100\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM})	-	150	-	μs

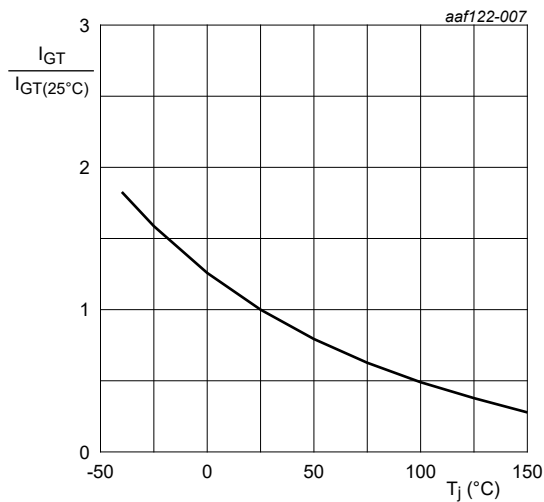


Fig. 7. Normalized gate trigger current as a function of junction temperature

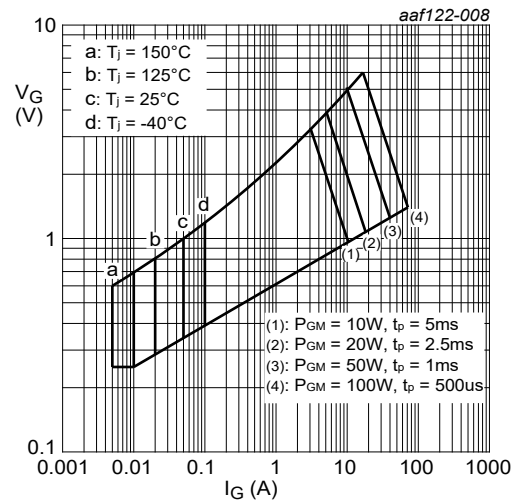


Fig. 8. Gate voltage as a function of gate current

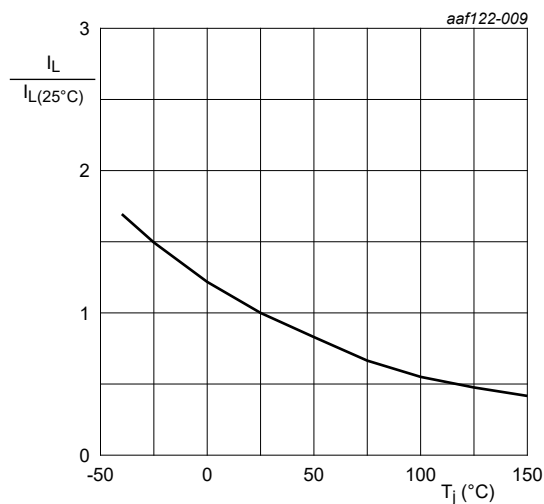


Fig. 9. Normalized latching current as a function of junction temperature

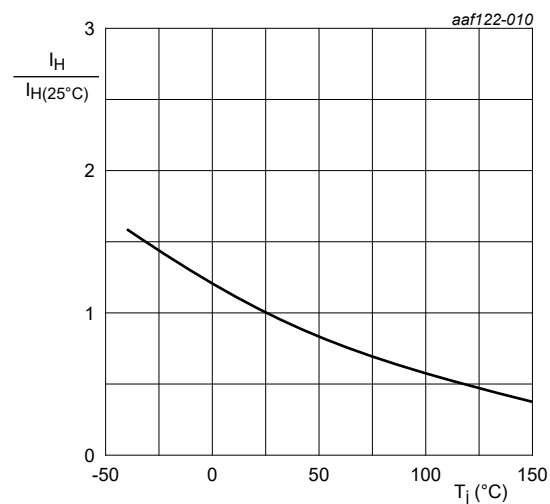


Fig. 10. Normalized holding current as a function of junction temperature

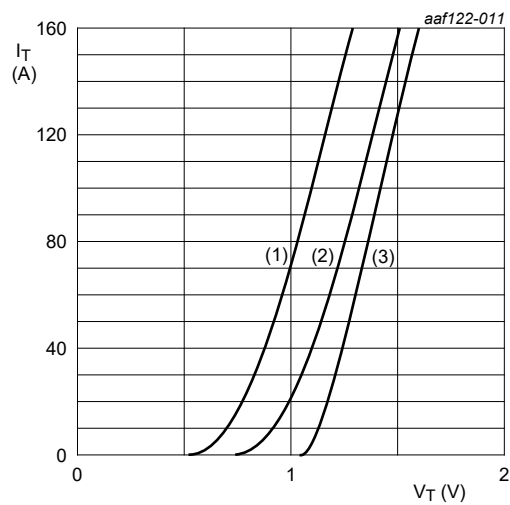


Fig. 11. On-state current as a function of on-state voltage

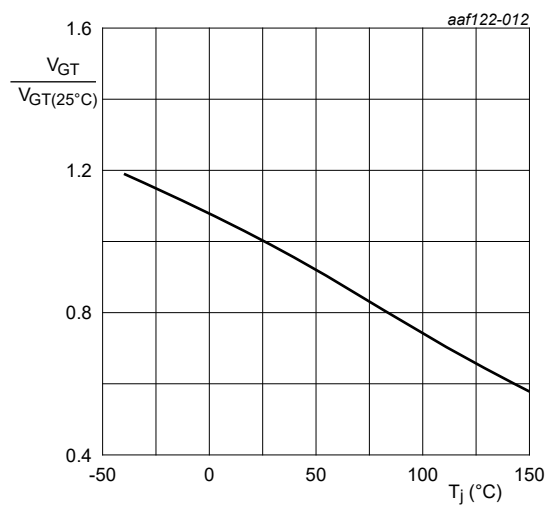


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247

SOT429N

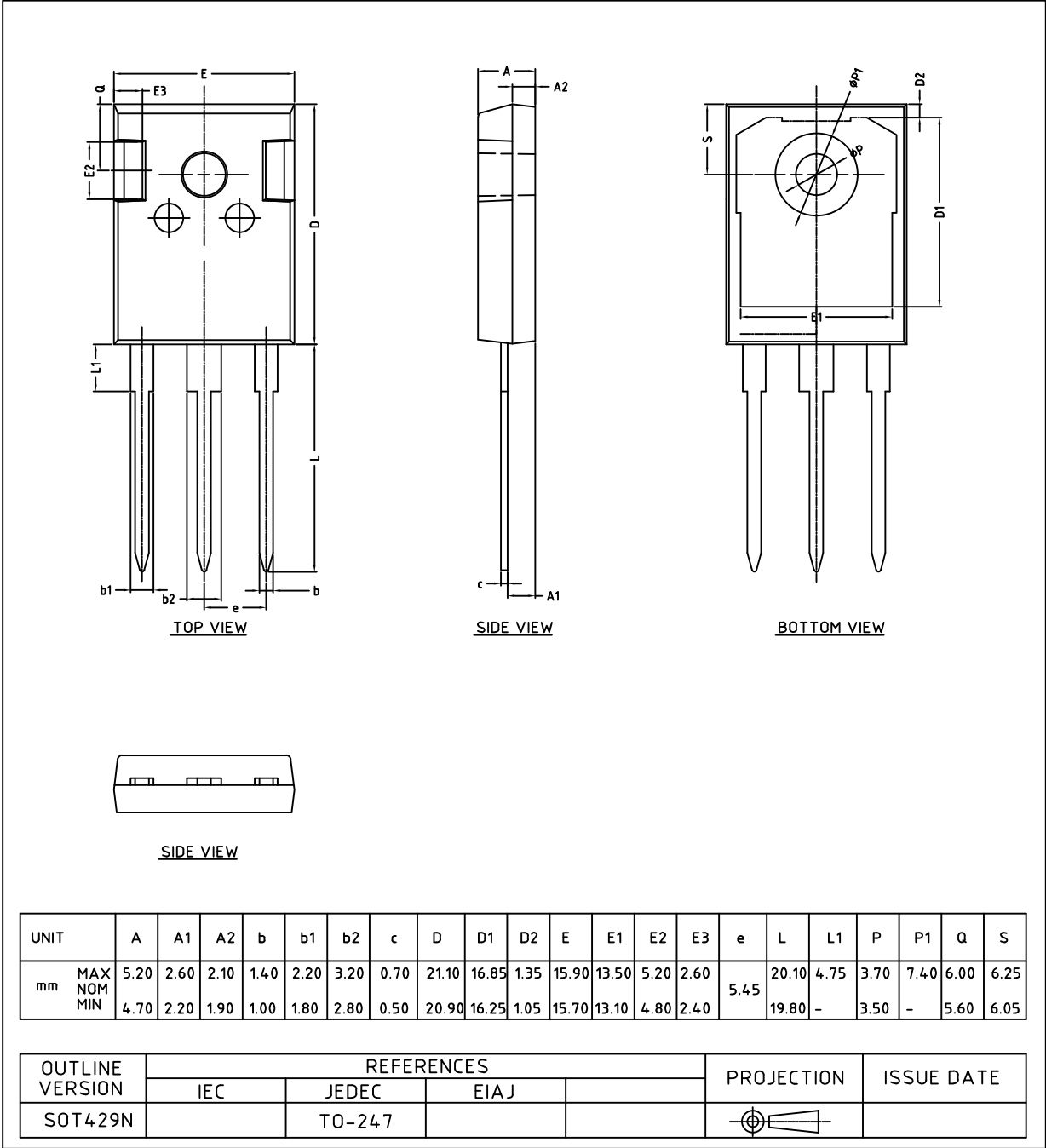


Fig. 13. Package outline TO-247 (SOT429N)

11. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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