

RL78/L13

RENESAS MCU

R01DS0168EJ0210

Rev.2.10

Aug 12, 2016

Integrated LCD controller/driver, True Low Power Platform (as low as 112.5 μ A/MHz, and 0.61 μ A for RTC + LVD), 1.6 V to 5.5 V operation, 16 to 128 Kbyte Flash, 31 DMIPS at 24 MHz, for All LCD Based Applications

1. OUTLINE

<R> 1.1 Features

Ultra-low power consumption technology

- V_{DD} = single power supply voltage of 1.6 to 5.5 V which can operate a 1.8 V device at a low voltage
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.04167 μ s: @ 24 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5 μ s: @ 32.768 kHz operation with subsystem clock)
- Address space: 1 MB
- General-purpose registers: (8-bit register $\times$ 8) $\times$ 4 banks
- On-chip RAM: 1 to 8 KB

Code flash memory

- Code flash memory: 16 to 128 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 4 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 5.5 V

High-speed on-chip oscillator

- Select from 48 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: $\pm 1.0\%$ (V_{DD} = 1.8 to 5.5 V, T_A = -20 to +85°C)

Operating ambient temperature

- T_A = -40 to +85°C (A: Consumer applications)
- T_A = -40 to +105°C (G: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

DMA (Direct Memory Access) controller

- 4 channels
- Number of clocks during transfer between 8/16-bit SFR and internal RAM: 2 clocks

Multiplier and divider/multiplier-accumulator

- 16 bits $\times$ 16 bits = 32 bits (Unsigned or signed)
- 32 bits $\div$ 32 bits = 32 bits (Unsigned)
- 16 bits $\times$ 16 bits + 32 bits = 32 bits (Unsigned or signed)

Serial interface

- CSI: 2 channels
- UART/UART (LIN-bus supported): 3, 4 channels/1 channel
- I²C/Simplified I²C communication: 1 channel/2 channels

Timer

- 16-bit timer: 8 channels (with remote control output function)
- 16-bit timer KB20 (IH): 1 channel (IH-only PWM output function)
- 12-bit interval timer: 1 channel
- Real-time clock 2: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

A/D converter

- 8/10-bit resolution A/D converter (V_{DD} = 1.6 to 5.5 V)
- Analog input: 9 to 12 channels
- Internal reference voltage (1.45 V) and temperature sensor^{Note 1}

Comparator

- 2 channels
- Operation mode: Comparator high-speed mode, comparator low-speed mode, or window mode
- External reference voltage and internal reference voltage are selectable

LCD controller/driver

- Segment signal output: 36 (32)^{Note 2} to 51 (47)^{Note 2}
- Common signal output: 4 (8)^{Note 2}
- Internal voltage boosting method, capacitor split method, and external resistance division method are switchable

I/O port

- I/O port: 49 to 65 (N-ch open drain I/O [withstand voltage of 6 V]: 2, N-ch open drain I/O [V_{DD} withstand voltage]: 12 to 18)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

Notes 1. Can be selected only in HS (high-speed main) mode
2. The values in parentheses are the number of signal outputs when 8 com is used.

Remark The functions mounted depend on the product. See 1.6 Outline of Functions.

* There are differences in specifications between every product.
Please refer to specification for details.

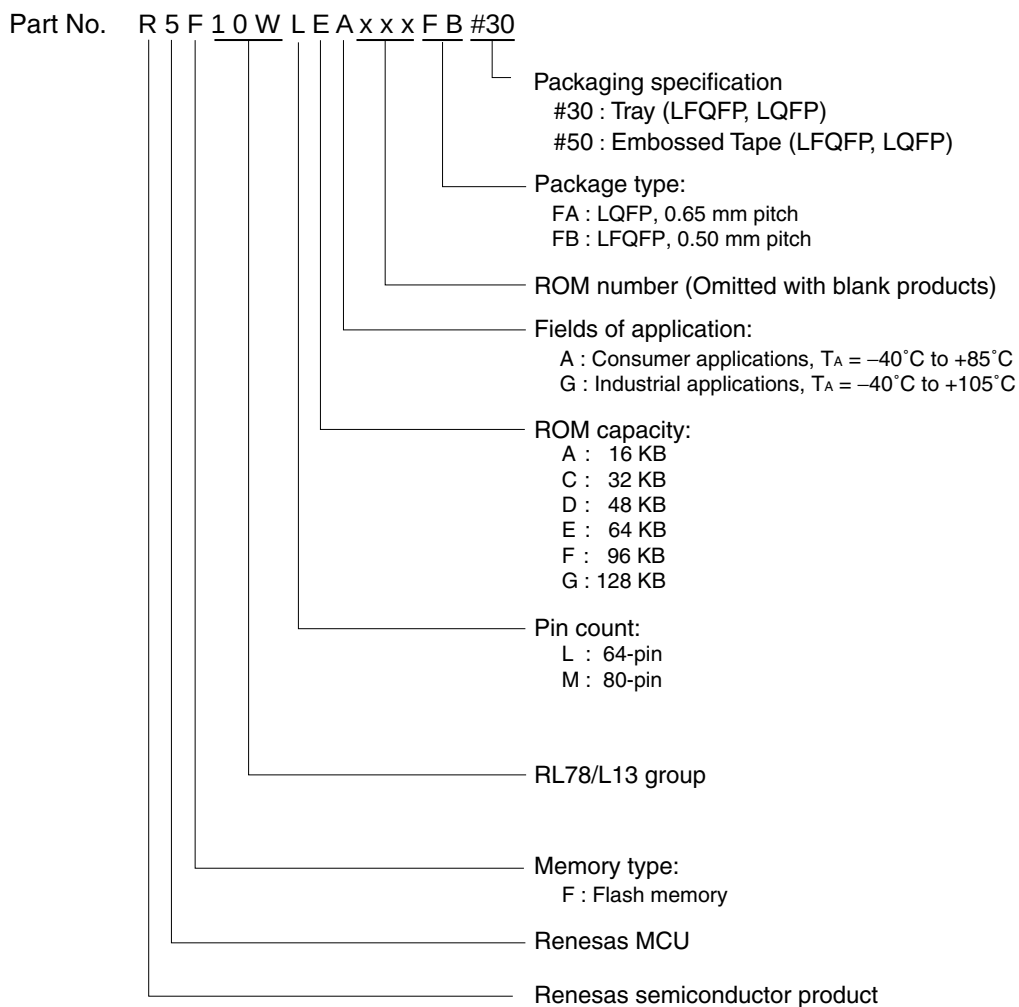
○ ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/L13	
			64 pins	80 pins
128 KB	4 KB	8 KB ^{Note}	R5F10WLG	R5F10WMG
96 KB	4 KB	6 KB	R5F10WLF	R5F10WMF
64 KB	4 KB	4 KB	R5F10WLE	R5F10WME
48 KB	4 KB	2 KB	R5F10WLD	R5F10WMD
32 KB	4 KB	1.5 KB	R5F10WLC	R5F10WMC
16 KB	4 KB	1 KB	R5F10WLA	R5F10WMA

Note This is about 7 KB when the self-programming function and data flash function are used. (For details, see **CHAPTER 3** in the RL78/L13 User's Manual.)

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/L13



Pin Count	Package	Data Flash	Fields of Application ^{Note}	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F10WLAFA#30, R5F10WLAFA#50, R5F10WLCAFA#30, R5F10WLCAFA#50, R5F10WLDAFA#30, R5F10WLDAFA#50, R5F10WLEAFA#30, R5F10WLEAFA#50, R5F10WLFAFA#30, R5F10WLFAFA#50, R5F10WLGAF#30, R5F10WLGAF#50
	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	Mounted	A G	R5F10WLAFA#30, R5F10WLAFA#50, R5F10WLCAFA#30, R5F10WLCAFA#50, R5F10WLDAFA#30, R5F10WLDAFA#50, R5F10WLEAFA#30, R5F10WLEAFA#50, R5F10WLFAFA#30, R5F10WLFAFA#50, R5F10WLGAF#30, R5F10WLGAF#50, R5F10WLAGAF#30, R5F10WLAGAF#50, R5F10WLCGAF#30, R5F10WLCGAF#50, R5F10WLDGAF#30, R5F10WLDGAF#50, R5F10WLEGAF#30, R5F10WLEGAF#50, R5F10WLFGAF#30, R5F10WLFGAF#50, R5F10WLGGA#30, R5F10WLGGA#50
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F10WMAFA#30, R5F10WMAFA#50, R5F10WMCAFA#30, R5F10WMCAFA#50, R5F10WMDAFA#30, R5F10WMDAFA#50, R5F10WMEAFA#30, R5F10WMEAFA#50, R5F10WMFAFA#30, R5F10WMFAFA#50, R5F10WMGAFA#30, R5F10WMGAFA#50
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A G	R5F10WMAFA#30, R5F10WMAFA#50, R5F10WMCAFA#30, R5F10WMCAFA#50, R5F10WMDAFA#30, R5F10WMDAFA#50, R5F10WMEAFA#30, R5F10WMEAFA#50, R5F10WMFAFA#30, R5F10WMFAFA#50, R5F10WMGAFA#30, R5F10WMGAFA#50, R5F10WMAGAF#30, R5F10WMAGAF#50, R5F10WMCAGAF#30, R5F10WMCAGAF#50, R5F10WMDGAF#30, R5F10WMDGAF#50, R5F10WMEGAF#30, R5F10WMEGAF#50, R5F10WMFGAF#30, R5F10WMFGAF#50, R5F10WMGGA#30, R5F10WMGGA#50

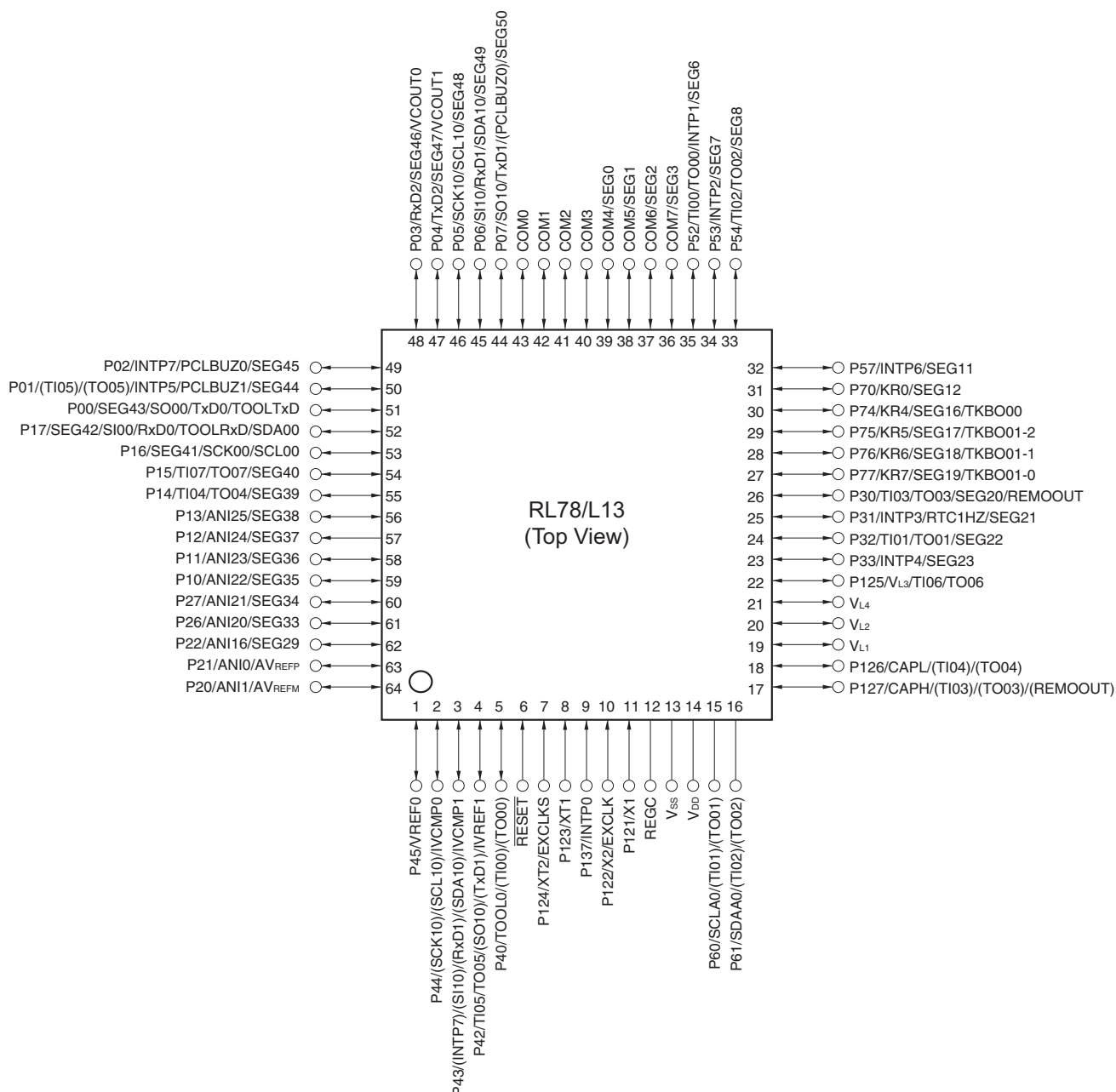
Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/L13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

<R> 1.3.1 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



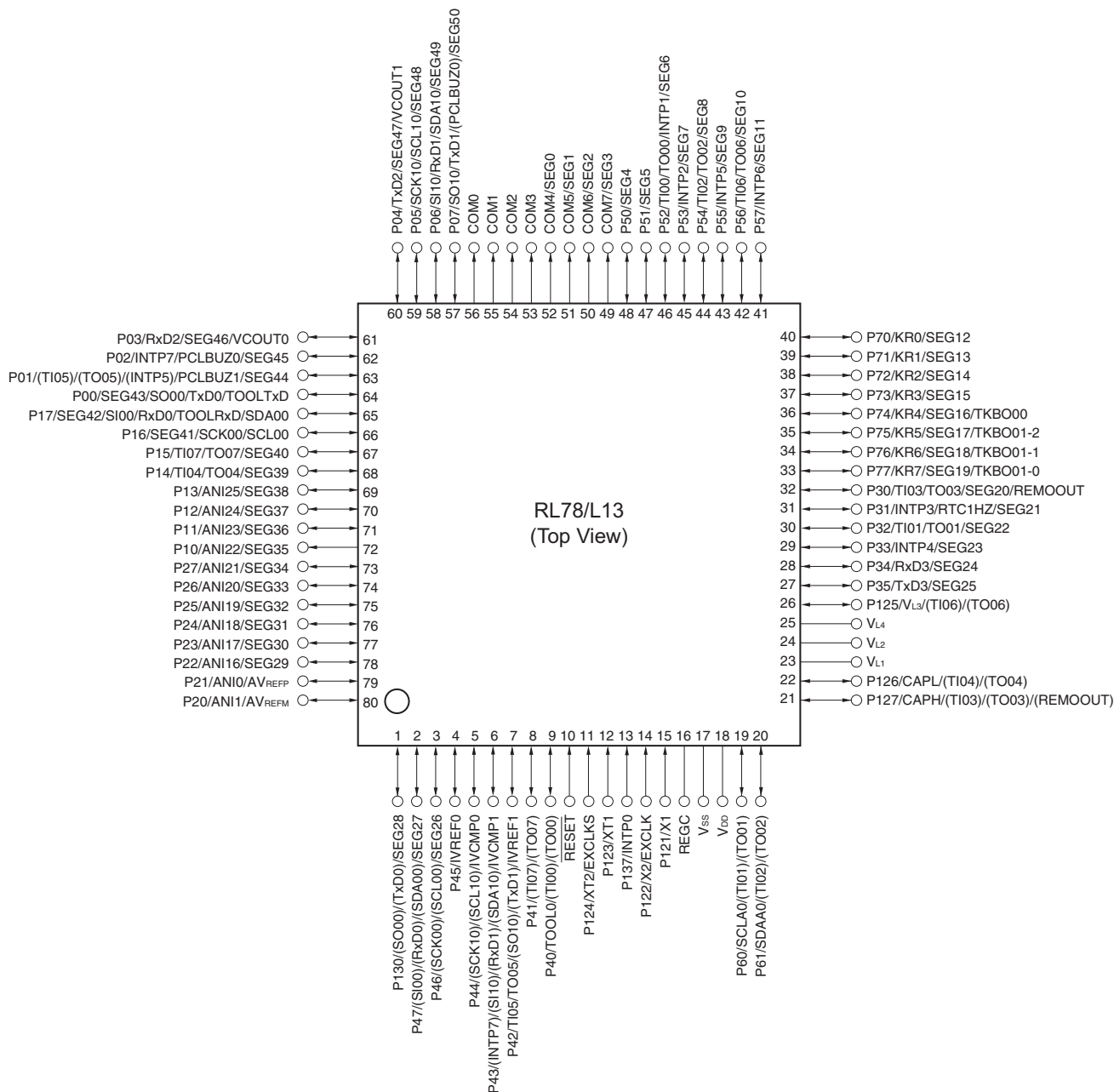
Caution Connect the REGC pin to VSS via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/L13 User's Manual.

<R> 1.3.2 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

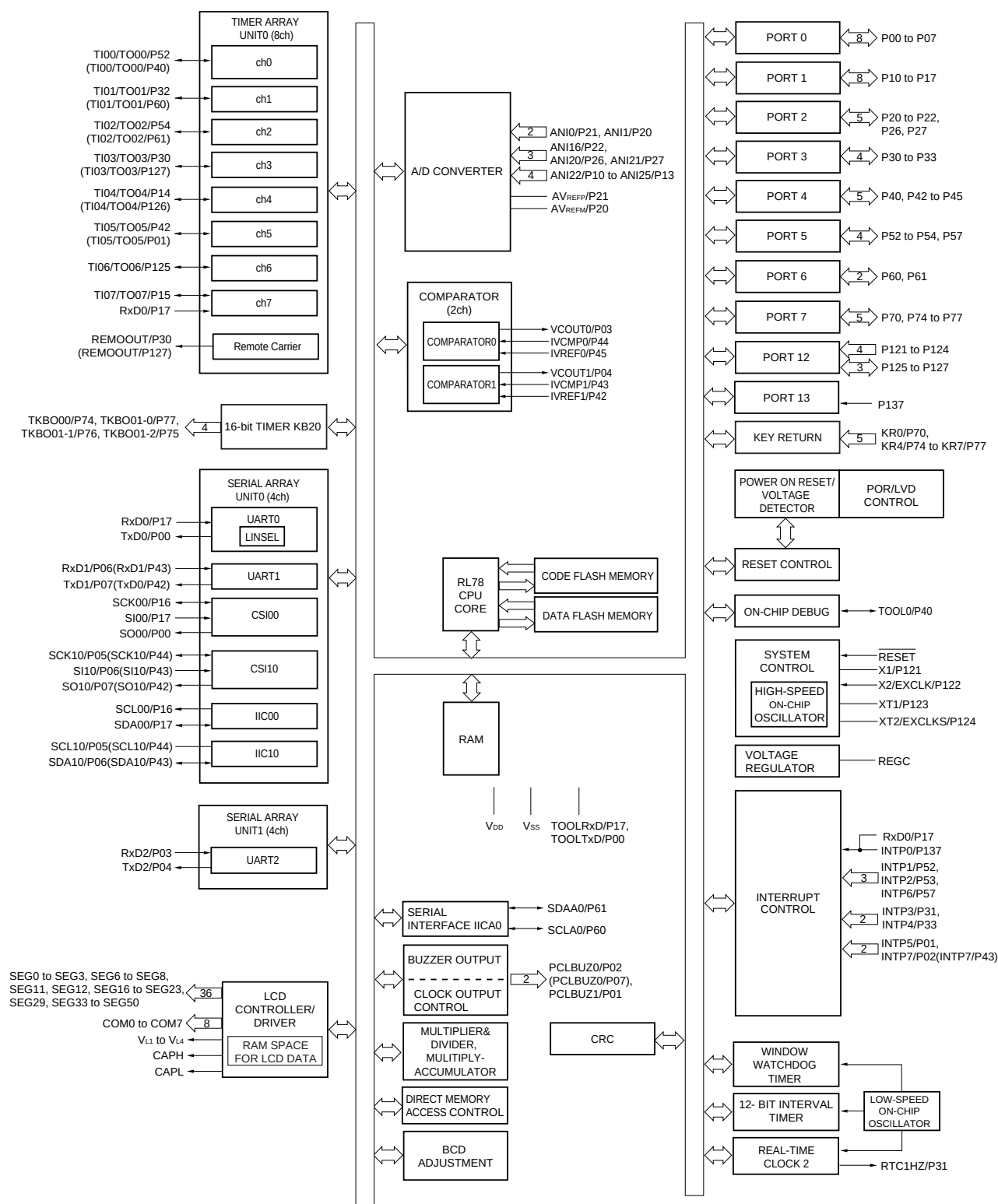
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/L13 User's Manual.

1.4 Pin Identification

ANI0, ANI1,		PCLBUZ0, PCLBUZ1:	Programmable Clock Output/ Buzzer Output
ANI16 to ANI25:	Analog Input	REGC:	Regulator Capacitance
AVREFM:	Analog Reference Voltage Minus	REMOOUT:	Remote control Output
AVREFP:	Analog Reference Voltage Plus	RESET:	Reset
CAPH, CAPL:	Capacitor for LCD	RTC1HZ:	Real-time Clock 2 Correction Clock (1 Hz) Output
COM0 to COM7:	LCD Common Output	RxD0 to RxD3:	Receive Data
EXCLK:	External Clock Input (Main System Clock)	SCK00, SCK10, SCLA0:	Serial Clock Input/Output
EXCLKS:	External Clock Input (Subsystem Clock)	SCL00, SCL10:	Serial Clock Output
INTP0 to INTP7:	External Interrupt Input	SDAA0, SDA00, SDA10:	Serial Data Input/Output
IVCMP0, IVCMP1:	Comparator Input	SEG0 to SEG50:	LCD Segment Output
IVREF0, IVREF1:	Comparator Reference Input	SI00, SI10:	Serial Data Input
KR0 to KR7:	Key Return	SO00, SO10:	Serial Data Output
P00 to P07:	Port 0	TI00 to TI07:	Timer Input
P10 to P17:	Port 1	TO00 to TO07,	
P20 to P27:	Port 2	TKBO00, TKBO01-0,	
P30 to P35:	Port 3	TKBO01-1, TKBO01-2:	Timer Output
P40 to P47:	Port 4	TOOL0:	Data Input/Output for Tool
P50 to P57:	Port 5	TOOLRxD, TOOLTxD:	Data Input/Output for External Device
P60, P61:	Port 6	TxD0 to TxD3:	Transmit Data
P70 to P77:	Port 7	VCOUT0, VCOUT1:	Comparator Output
P121 to P127:	Port 12	VDD:	Power Supply
P130, P137:	Port 13	VL1 to VL4:	LCD Power Supply
		VSS:	Ground
		X1, X2:	Crystal Oscillator (Main System Clock)
		XT1, XT2:	Crystal Oscillator (Subsystem Clock)

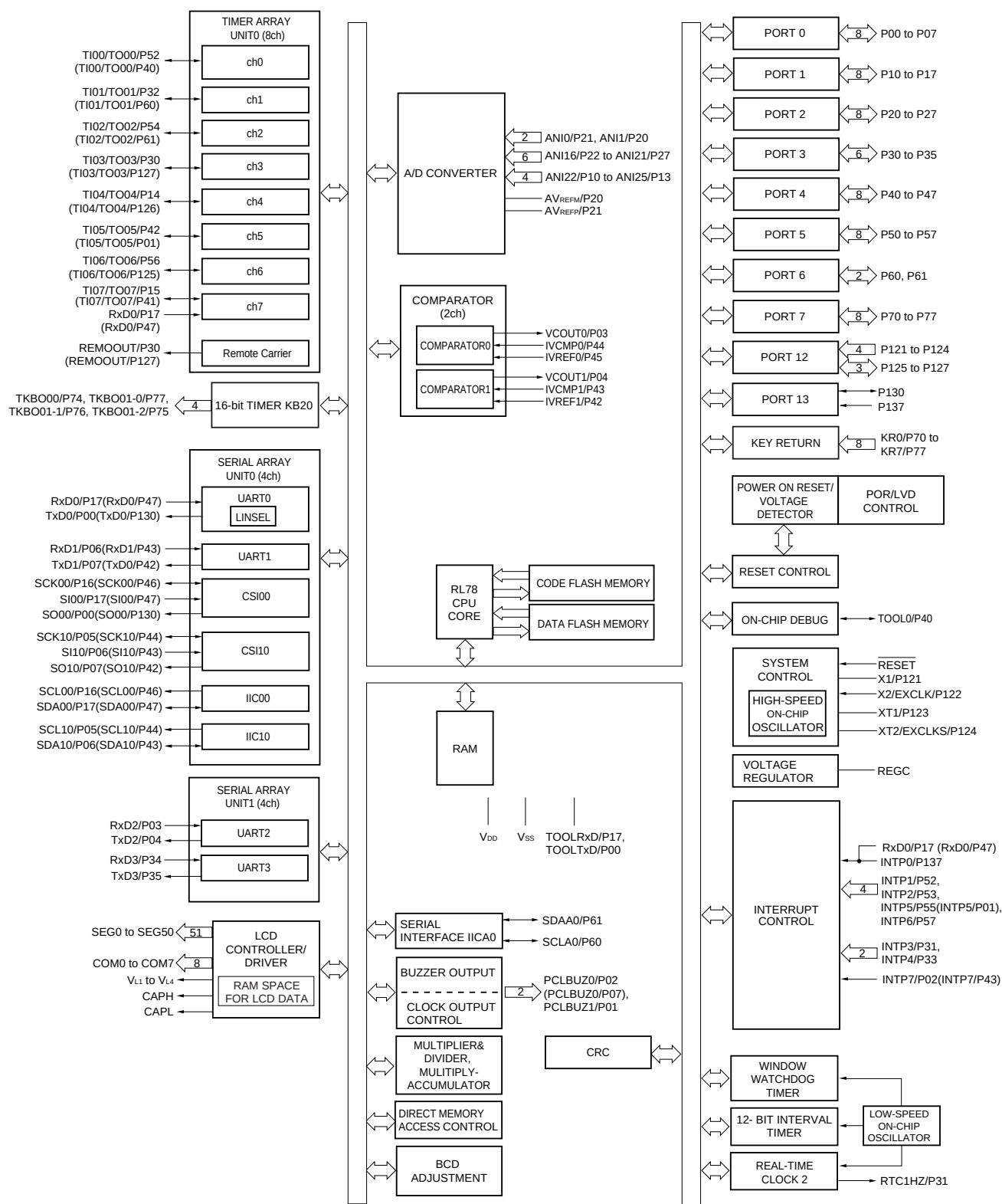
1.5 Block Diagram

1.5.1 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/L13 User's Manual.

1.5.2 80-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/L13 User's Manual.

1.6 Outline of Functions

(1/2)

<R>

Item		64-pin	80-pin
		R5F10WLx (x = A, C-G)	R5F10WMx (x = A, C-G)
Code flash memory (KB)		16 to 128	16 to 128
Data flash memory (KB)		4	4
RAM (KB)		1 to 8 ^{Note 1}	1 to 8 ^{Note 1}
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)	
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 24 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)	
Clock for 16-bit timer KB20		48 MHz (TYP.): $V_{DD} = 2.7$ to 5.5 V	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V	
Low-speed on-chip oscillator		15 kHz (TYP.)	
General-purpose register		(8-bit register $\times$ 8) $\times$ 4 banks	
Minimum instruction execution time		0.04167 μ s (High-speed on-chip oscillator: $f_{IH} = 24$ MHz operation)	
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)	
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits $\times$ 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	49	65
	CMOS I/O	42 (N-ch O.D. I/O [V_{DD} withstand voltage]: 12)	58 (N-ch O.D. I/O [V_{DD} withstand voltage]: 18)
	CMOS input	5	5
	CMOS output	–	–
	N-ch O.D. I/O (withstand voltage: 6 V)	2	2
Timer	16-bit timer TAU	8 channels	
	16-bit timer KB20	1 channel	
	Watchdog timer	1 channel	
	12-bit interval timer (IT)	1 channel	
	Real-time clock 2	1 channel	
	RTC2 output	1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)	
	Timer output	8 channels (PWM outputs: 7 ^{Note 2}) (TAU used) 1 channel (timer KB20 used)	
	Remote control output function	1 (TAU used)	

Notes 1. In the case of the 8 KB, this is about 7 KB when the self-programming function and data flash function are used.

2. The number of outputs varies depending on the setting of the channels in use and the number of master channels (see **6.9.3 Operation as multiple PWM output function** in the RL78/L13 User's Manual.).

(2/2)

Item		64-pin	80-pin
		R5F10WLx (x = A, C-G)	R5F10WMx (x = A, C-G)
Clock output/buzzer output controller		2	
		2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)	
8/10-bit resolution A/D converter		9 channels	12 channels
Comparator		2 channels	
Serial interface		[64-pin] - CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - UART: 1 channel [80-pin] - CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel - CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel - UART: 2 channels	
	I ² C bus	1 channel	
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.	
	Segment signal output	36 (32) ^{Note 1}	51 (47) ^{Note 1}
	Common signal output	4 (8) ^{Note 1}	
Multiplier and divider/multiply-accumulator		16 bits × 16 bits = 32 bits (Unsigned or signed) 32 bits ÷ 32 bits = 32 bits (Unsigned) 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)	
DMA controller		4 channels	
Vectored interrupt sources	Internal	32	35
	External	11	11
Key interrupt		5	8
Reset		- Reset by RESET pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution^{Note 2} - Internal reset by RAM parity error - Internal reset by illegal-memory access	
Power-on-reset circuit		- Power-on-reset: 1.51 V (TYP.) - Power-down-reset: 1.50 V (TYP.)	
Voltage detector		- Rising edge: 1.67 V to 4.06 V (14 steps) - Falling edge: 1.63 V to 3.98 V (14 steps)	
On-chip debug function		Provided	
Power supply voltage		$V_{DD} = 1.6$ to 5.5 V ($T_A = -40$ to $+85^{\circ}\text{C}$) $V_{DD} = 2.4$ to 5.5 V ($T_A = -40$ to $+105^{\circ}\text{C}$)	
Operating ambient temperature		Consumer applications: $T_A = -40$ to $+85^{\circ}\text{C}$ Industrial applications: $T_A = -40$ to $+105^{\circ}\text{C}$	

Notes 1. The values in parentheses are the number of signal outputs when 8 com is used.

2. This reset occurs when instruction code FFH is executed.

This reset does not occur during emulation using an in-circuit emulator or an on-chip debugging emulator.

2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$)

Target products A: Consumer applications; $T_A = -40$ to $+85^\circ\text{C}$

R5F10WLAAFA, R5F10WLCAFA, R5F10WLDAFA,
R5F10WLEAFA, R5F10WLFAFA, R5F10WLGAFB,
R5F10WLAAFB, R5F10WLCAFB, R5F10WLDAFB,
R5F10WLEAFB, R5F10WLFAFB, R5F10WLGAFB,
R5F10WMAAFA, R5F10WMCAFA, R5F10WMDAFA,
R5F10WMEAFA, R5F10WMFAFA, R5F10WMGAFA,
R5F10WMAAFB, R5F10WMCAFB, R5F10WMDAFB,
R5F10WMEAFA, R5F10WMFAFB, R5F10WMGAFA

G: Industrial applications; when using $T_A = -40$ to $+105^\circ\text{C}$ specification products at $T_A = -40$ to $+85^\circ\text{C}$

R5F10WLAGFB, R5F10WLCGFB, R5F10WLDGFB,
R5F10WLEGFB, R5F10WLFGFB, R5F10WLGGFB,
R5F10WMAGFB, R5F10WMCGB, R5F10WMDGFB,
R5F10WMEGFB, R5F10WMFGFB, R5F10WMGGFB

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 With functions for each product in the RL78/L13 User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/3)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to $+6.5$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to $+2.8$ and -0.3 to $V_{DD} + 0.3$ ^{Note 1}	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I2}	P60 and P61 (N-ch open-drain)	-0.3 to $+6.5$	V
	V_{I3}	EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Analog input voltage	V_{AI1}	ANI0, ANI1, ANI16 to ANI26	-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to $1\ \mu\text{F}$). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be $6.5\ \text{V}$ or lower.

3. Do not exceed $AV_{REF(+)} + 0.3\ \text{V}$ in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF (+)}$: + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

Absolute Maximum Ratings (2/3)

Parameter	Symbol	Conditions	Ratings	Unit
LCD voltage	V _{L1}	V _{L1} voltage ^{Note 1}	-0.3 to +2.8 and -0.3 to V _{L4} +0.3	V
	V _{L2}	V _{L2} voltage ^{Note 1}	-0.3 to V _{L4} +0.3 ^{Note 2}	V
	V _{L3}	V _{L3} voltage ^{Note 1}	-0.3 to V _{L4} +0.3 ^{Note 2}	V
	V _{L4}	V _{L4} voltage ^{Note 1}	-0.3 to +6.5	V
	V _{LCAP}	CAPL, CAPH voltage ^{Note 1}	-0.3 to V _{L4} +0.3 ^{Note 2}	V
	V _{OUT}	COM0 to COM7 SEG0 to SEG50 output voltage	External resistance division method	-0.3 to V _{DD} +0.3 ^{Note 2}
			Capacitor split method	-0.3 to V _{DD} +0.3 ^{Note 2}
			Internal voltage boosting method	-0.3 to V _{L4} +0.3 ^{Note 2}

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μ F $\pm$ 30%) and connect a capacitor (0.47 μ F $\pm$ 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS}: Reference voltage

Absolute Maximum Ratings (3/3)

Absolute Maximum Ratings (3/3)						
	Parameter	Symbol	Conditions		Ratings	Unit
<R>	Output current, high	I _{OH1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	–40	mA
<R>			Total of all pins –170 mA	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	–170	mA
<R>		I _{OH2}	Per pin	P20, P21	–0.5	mA
<R>			Total of all pins		–1	mA
<R>	Output current, low	I _{OL1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
<R>			Total of all pins 170 mA	P40 to P47, P130	70	mA
				P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
<R>		I _{OL2}	Per pin	P20, P21	1	mA
<R>			Total of all pins		2	mA
		Operating ambient temperature	T _A	In normal operation mode		–40 to +85
	In flash memory programming mode					
	Storage temperature	T _{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1 and XT1 oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f _X) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ V _{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V _{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V _{DD} < 1.8 V	1.0		4.0	
XT1 clock oscillation frequency (f _{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see 5.4 System Clock Oscillator in the RL78/L13 User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85°C	1.8 V ≤ V _{DD} ≤ 5.5 V	–1.0		+1.0	%
			1.6 V ≤ V _{DD} < 1.8 V	–5.0		+5.0	%
		–40 to –20°C	1.8 V ≤ V _{DD} ≤ 5.5 V	–1.5		+1.5	%
			1.6 V ≤ V _{DD} < 1.8 V	–5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f _{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for the instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	1.6 V ≤ V _{DD} ≤ 5.5 V		–10.0 ^{Note 2}	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	4.0 V ≤ V _{DD} ≤ 5.5 V		–90.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		–15.0	mA
			1.8 V ≤ V _{DD} < 2.7 V		–7.0	mA
		(When duty = 70% ^{Note 3})	1.6 V ≤ V _{DD} < 1.8 V		–3.0	mA
	I _{OH2}	Per pin for P20 and P21	1.6 V ≤ V _{DD} ≤ 5.5 V		–0.1 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V		–0.2	mA

Notes 1. Value of the current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin

2. Do not exceed the total current value.

3. Output current value under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –90.0 mA

$$\text{Total output current of pins} = (-90.0 \times 0.7) / (80 \times 0.01) \cong -78.75 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			20.0 ^{Note 2}	mA
		Per pin for P60 and P61			15.0 ^{Note 2}	mA
		Total of P40 to P47, P130 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		70.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		15.0	mA
			1.8 V ≤ V _{DD} < 2.7 V		9.0	mA
			1.6 V ≤ V _{DD} < 1.8 V		4.5	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P70 to P77, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		90.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		35.0	mA
			1.8 V ≤ V _{DD} < 2.7 V		20.0	mA
			1.6 V ≤ V _{DD} < 1.8 V		10.0	mA
		Total of all pins (When duty = 70% ^{Note 3})			160.0	mA
	I _{OL2}	Per pin for P20 and P21			0.4 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V		0.8	mA

Notes 1. Value of the current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin

2. Do not exceed the total current value.

3. Output current value under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 70.0 mA

$$\text{Total output current of pins} = (70.0 \times 0.7) / (80 \times 0.01) \cong 61.25 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	$0.8V_{DD}$	V_{DD}	V
	V_{IH2}	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.2	V_{DD}	V
			TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	2.0	V_{DD}	V
			TTL input buffer $1.6\text{ V} \leq V_{DD} < 3.3\text{ V}$	1.5	V_{DD}	V
	V_{IH3}	P20, P21	$0.7V_{DD}$		V_{DD}	V
	V_{IH4}	P60, P61	$0.7V_{DD}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	0	$0.2V_{DD}$	V
	V_{IL2}	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0	0.8	V
			TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	0	0.5	V
			TTL input buffer $1.6\text{ V} \leq V_{DD} < 3.3\text{ V}$	0	0.32	V
	V_{IL3}	P20, P21	0		$0.3V_{DD}$	V
	V_{IL4}	P60, P61	0		$0.3V_{DD}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		$0.2V_{DD}$	V

Caution The maximum value of V_{IH} of pins P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 is V_{DD} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -10.0\text{ mA}$	$V_{DD} - 1.5$		V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$	$V_{DD} - 0.7$		V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$	$V_{DD} - 0.6$		V
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$	$V_{DD} - 0.5$		V
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.0\text{ mA}$	$V_{DD} - 0.5$		V
	V_{OH2}	P20 and P21	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.5$		V
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 20\text{ mA}$		1.3	V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$		0.7	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$		0.4	V
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$		0.4	V
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$, $I_{OL1} = 0.3\text{ mA}$		0.4	V
	V_{OL2}	P20 and P21	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$		0.4	V
	V_{OL3}	P60 and P61	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 3.0\text{ mA}$		0.4	V
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 2.0\text{ mA}$		0.4	V
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$, $I_{OL3} = 1.0\text{ mA}$		0.4	V

Caution P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I _{LH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{DD}				1	μA
	I _{LH2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{DD}				1	μA
	I _{LH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port mode and when external clock is input			1	μA
				Resonator connected			10	μA
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{SS}				−1	μA
	I _{LIL2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{SS}				−1	μA
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port mode and when external clock is input			−1	μA
				Resonator connected			−10	μA
On-chip pull-up resistance	R _{U1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P45 to P47, P50 to P57, P70 to P77, P125 to P127, P130	V _I = V _{SS}	2.4 V ≤ V _{DD} < 5.5 V	10	20	100	kΩ
				1.6 V ≤ V _{DD} < 2.4 V	10	30	100	kΩ
	R _{U2}	P40 to P44	V _I = V _{SS}		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

 $(T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V})$

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Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current ¹	I_{DD1}	Operating mode	HS (high-speed main) mode ^{Note 5}	$f_{HOCO} = 48\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 24\text{ MHz}^{\text{Note 3}}$	Basic operation	$V_{DD} = 5.0\text{ V}$	2.0		mA
						$V_{DD} = 3.0\text{ V}$	2.0		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$	3.8	6.5	mA
						$V_{DD} = 3.0\text{ V}$	3.8	6.5	mA
				$f_{HOCO} = 24\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 24\text{ MHz}^{\text{Note 3}}$	Basic operation	$V_{DD} = 5.0\text{ V}$	1.7		mA
						$V_{DD} = 3.0\text{ V}$	1.7		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$	3.6	6.1	mA
						$V_{DD} = 3.0\text{ V}$	3.6	6.1	mA
				$f_{HOCO} = 16\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 16\text{ MHz}^{\text{Note 3}}$	Normal operation	$V_{DD} = 5.0\text{ V}$	2.7	4.7	mA
						$V_{DD} = 3.0\text{ V}$	2.7	4.7	mA
			LS (low-speed main) mode ^{Note 5}	$f_{HOCO} = 8\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 8\text{ MHz}^{\text{Note 3}}$	Normal operation	$V_{DD} = 3.0\text{ V}$	1.2	2.1	mA
						$V_{DD} = 2.0\text{ V}$	1.2	2.1	mA
			LV (low-voltage main) mode ^{Note 5}	$f_{HOCO} = 4\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 4\text{ MHz}^{\text{Note 3}}$	Normal operation	$V_{DD} = 3.0\text{ V}$	1.2	1.8	mA
						$V_{DD} = 2.0\text{ V}$	1.2	1.8	mA
			HS (high-speed main) mode ^{Note 5}	$f_{MX} = 20\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input	3.0	5.1	mA
						Resonator connection	3.2	5.2	mA
				$f_{MX} = 20\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input	2.9	5.1	mA
						Resonator connection	3.2	5.2	mA
				$f_{MX} = 16\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input	2.5	4.4	mA
						Resonator connection	2.7	4.5	mA
				$f_{MX} = 16\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input	2.5	4.4	mA
						Resonator connection	2.7	4.5	mA
				$f_{MX} = 10\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input	1.9	3.0	mA
						Resonator connection	1.9	3.0	mA
				$f_{MX} = 10\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input	1.9	3.0	mA
						Resonator connection	1.9	3.0	mA
			LS (low-speed main) mode ^{Note 5}	$f_{MX} = 8\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input	1.1	2.0	mA
						Resonator connection	1.1	2.0	mA
				$f_{MX} = 8\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 2.0\text{ V}$	Normal operation	Square wave input	1.1	2.0	mA
						Resonator connection	1.1	2.0	mA
			Subsystem clock operation	$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = -40^\circ\text{C}$	Normal operation	Square wave input	4.0	5.4	μA
						Resonator connection	4.3	5.4	μA
				$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = +25^\circ\text{C}$	Normal operation	Square wave input	4.0	5.4	μA
						Resonator connection	4.3	5.4	μA
				$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = +50^\circ\text{C}$	Normal operation	Square wave input	4.1	7.1	μA
						Resonator connection	4.4	7.1	μA
				$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = +70^\circ\text{C}$	Normal operation	Square wave input	4.3	8.7	μA
						Resonator connection	4.7	8.7	μA
				$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = +85^\circ\text{C}$	Normal operation	Square wave input	4.7	12.0	μA
						Resonator connection	5.2	12.0	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation ($AMPHS1 = 1$). The current flowing into the LCD controller/driver, 16-bit timer KB20, real-time clock 2, 12-bit interval timer, and watchdog timer is not included.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (48 MHz max.)
 3. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)
 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 5. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

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Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD2} ^{Note 2}	HALT mode	HS (high-speed main) mode ^{Note 7}	f _{HOCO} = 48 MHz ^{Note 4} , f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.71	1.95	mA	
					V _{DD} = 3.0 V		0.71	1.95		
				f _{HOCO} = 24 MHz ^{Note 4} , f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.49	1.64	mA	
					V _{DD} = 3.0 V		0.49	1.64		
				f _{HOCO} = 16 MHz ^{Note 4} , f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.43	1.11	mA	
					V _{DD} = 3.0 V		0.43	1.11		
			LS (low-speed main) mode ^{Note 7}	f _{HOCO} = 8 MHz ^{Note 4} , f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		280	770	μA	
					V _{DD} = 2.0 V		280	770		
			LV (low-voltage main) mode ^{Note 7}	f _{HOCO} = 4 MHz ^{Note 4} , f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V		430	700	μA	
					V _{DD} = 2.0 V		430	700		
			HS (high-speed main) mode ^{Note 7}	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.31	1.42	mA	
					Resonator connection		0.48	1.42		
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.29	1.42	mA	
					Resonator connection		0.48	1.42		
				f _{MX} = 16 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.26	0.86	mA	
					Resonator connection		0.45	1.15		
				f _{MX} = 16 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.25	0.86	mA	
					Resonator connection		0.44	1.15		
		f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V		Square wave input		0.20	0.63	mA		
				Resonator connection		0.28	0.71			
		f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V		Square wave input		0.19	0.63	mA		
				Resonator connection		0.28	0.71			
		LS (low-speed main) mode ^{Note 7}	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		100	560	μA		
				Resonator connection		160	560			
			f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		100	560	μA		
				Resonator connection		160	560			
		Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} , T _A = −40°C	Square wave input		0.34	0.62	μA		
				Resonator connection		0.51	0.80			
			f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +25°C	Square wave input		0.38	0.62	μA		
				Resonator connection		0.57	0.80			
			f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +50°C	Square wave input		0.46	2.30	μA		
				Resonator connection		0.67	2.49			
			f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +70°C	Square wave input		0.65	4.03	μA		
				Resonator connection		0.91	4.22			
		f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +85°C	Square wave input		1.00	8.04	μA			
			Resonator connection		1.31	8.23				
	I _{DD3} ^{Note 6}	STOP mode ^{Note 8}	T _A = −40°C					0.18	0.52	μA
			T _A = +25°C					0.24	0.52	
			T _A = +50°C					0.33	2.21	
			T _A = +70°C					0.53	3.94	
			T _A = +85°C					0.93	7.95	

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped.
When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the real-time clock 2 is included. However, not including the current flowing into the clock output/buzzer output, 12-bit interval timer, and watchdog timer.
 6. Not including the current flowing into the real-time clock 2, clock output/buzzer output, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 24 MHz
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{HOCO} : High-speed on-chip oscillator clock frequency (48 MHz max.)
3. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)
4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} ^{Note 1}						0.20		μA
RTC2 operating current	I _{RTC} ^{Notes 1, 2, 3}	f _{SUB} = 32.768 kHz					0.02		μA
12-bit interval timer operating current	I _{TMKA} ^{Notes 1, 2, 4}						0.04		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 2, 5}	f _{IL} = 15 kHz					0.22		μA
A/D converter operating current	I _{ADC} ^{Notes 1, 6}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V			1.3	1.7	mA	
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V			0.5	0.7	mA	
A/D converter reference voltage current	I _{ADREF} ^{Note 1}						75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}						75.0		μA
LVD operating current	I _{LVD} ^{Notes 1, 7}						0.08		μA
Comparator operating current	I _{CMP} ^{Notes 1, 11}	V _{DD} = 5.0 V, Regulator output voltage = 2.1 V	Window mode			12.5		μA	
			Comparator high-speed mode			6.5		μA	
			Comparator low-speed mode			1.7		μA	
		V _{DD} = 5.0 V, Regulator output voltage = 1.8 V	Window mode			8.0		μA	
			Comparator high-speed mode			4.0		μA	
			Comparator low-speed mode			1.3		μA	
Self-programming operating current	I _{FSP} ^{Notes 1, 9}					2.00	12.20	mA	
BGO operating current	I _{BGO} ^{Notes 1, 8}						2.00	12.20	mA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	While the mode is shifting ^{Note 10}				0.50	0.60	mA
			During A/D conversion, in low voltage mode, AV _{REFP} = V _{DD} = 3.0 V				1.20	1.44	mA
		CSI/UART operation						0.70	0.84
LCD operating current	I _{LCD1} ^{Notes 1, 12, 13}	External resistance division method	f _{LCD} = f _{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V _{DD} = 5.0 V, V _{L4} = 5.0 V		0.04	0.20	μA
					I _{LCD2} ^{Note 1, 12}	Internal voltage boosting method	f _{LCD} = f _{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V _{DD} = 3.0 V, V _{L4} = 3.0 V (V _{LCD} = 04H)
	V _{DD} = 5.0 V, V _{L4} = 5.1 V (V _{LCD} = 12H)		1.55	3.70					μA
		I _{LCD3} ^{Note 1, 12}	Capacitor split method	f _{LCD} = f _{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V _{DD} = 3.0 V, V _{L4} = 3.0 V		0.20	0.50

(Notes and Remarks are listed on the next page.)

Notes 1. Current flowing to V_{DD} .

2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The value of the current for the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock 2 operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of real-time clock 2.
4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The value of the current for the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{TMKA} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.
6. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
7. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. **For shift time to the SNOOZE mode, see 21.3.3 SNOOZE mode in the RL78/L13 User's Manual.**
11. Current flowing only to the comparator circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{CMP} when the comparator circuit operates.
12. Current flowing only to the LCD controller/driver. The value of the current for the RL78 microcontrollers is the sum of the supply current (I_{DD1} or I_{DD2}) and LCD operating current (I_{LCD1} , I_{LCD2} , or I_{LCD3}), when the LCD controller/driver operates in operation mode or HALT mode. However, not including the current flowing into the LCD panel. Conditions of the TYP. value and MAX. value are as follows.
 - Setting 20 pins as the segment function and blinking all
 - Selecting f_{SUB} for system clock when LCD clock = 128 Hz ($LCDC0 = 07H$)
 - Setting four time slices and 1/3 bias
13. Not including the current flowing into the external division resistor when using the external resistance division method.

Remarks 1. f_{IL} : Low-speed on-chip oscillator clock frequency

2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
3. f_{CLK} : CPU/peripheral hardware clock frequency
4. The temperature condition for the TYP. value is $T_A = 25^\circ\text{C}$.

2.4 AC Characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
		Subsystem clock (f _{SUB}) operation ^{Note}		1.8 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V			1.0		4.0	MHz
	f _{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
		1.8 V ≤ V _{DD} < 2.4 V			60			ns
		1.6 V ≤ V _{DD} < 1.8 V			120			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} +10			ns
TO00 to TO07, TKBO00, TKBO01-0 to TKBO01-2 output frequency	f _{TO}	HS (high-speed main) mode	4.0 V ≤ V _{DD} ≤ 5.5 V			12	MHz	
			2.7 V ≤ V _{DD} < 4.0 V			8	MHz	
			2.4 V ≤ V _{DD} < 2.7 V			4	MHz	
		LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V			2	MHz	
		LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V			4	MHz	
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ V _{DD} ≤ 5.5 V			16	MHz	
			2.7 V ≤ V _{DD} < 4.0 V			8	MHz	
			2.4 V ≤ V _{DD} < 2.7 V			4	MHz	
		LV (low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V			4	MHz	
			1.6 V ≤ V _{DD} < 1.8 V			2	MHz	
		LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V			4	MHz	
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0 to INTP7		1.6 V ≤ V _{DD} ≤ 5.5 V	1			μs
Key interrupt input high-level width, low-level width	t _{KRH} , t _{KRL}	KR0 to KR7		1.8 V ≤ V _{DD} ≤ 5.5 V	250			ns
				1.6 V ≤ V _{DD} < 1.8 V	1			μs
IH-PWM output restart input high-level width	t _{IHR}	INTP0 to INTP7			2			f _{CLK}
TMKB2 forced output stop input high-level width	t _{IHR}	INTP0 to INTP2			2			f _{CLK}
RESET low-level width	t _{RSL}				10			μs

(Note and Remark are listed on the next page.)

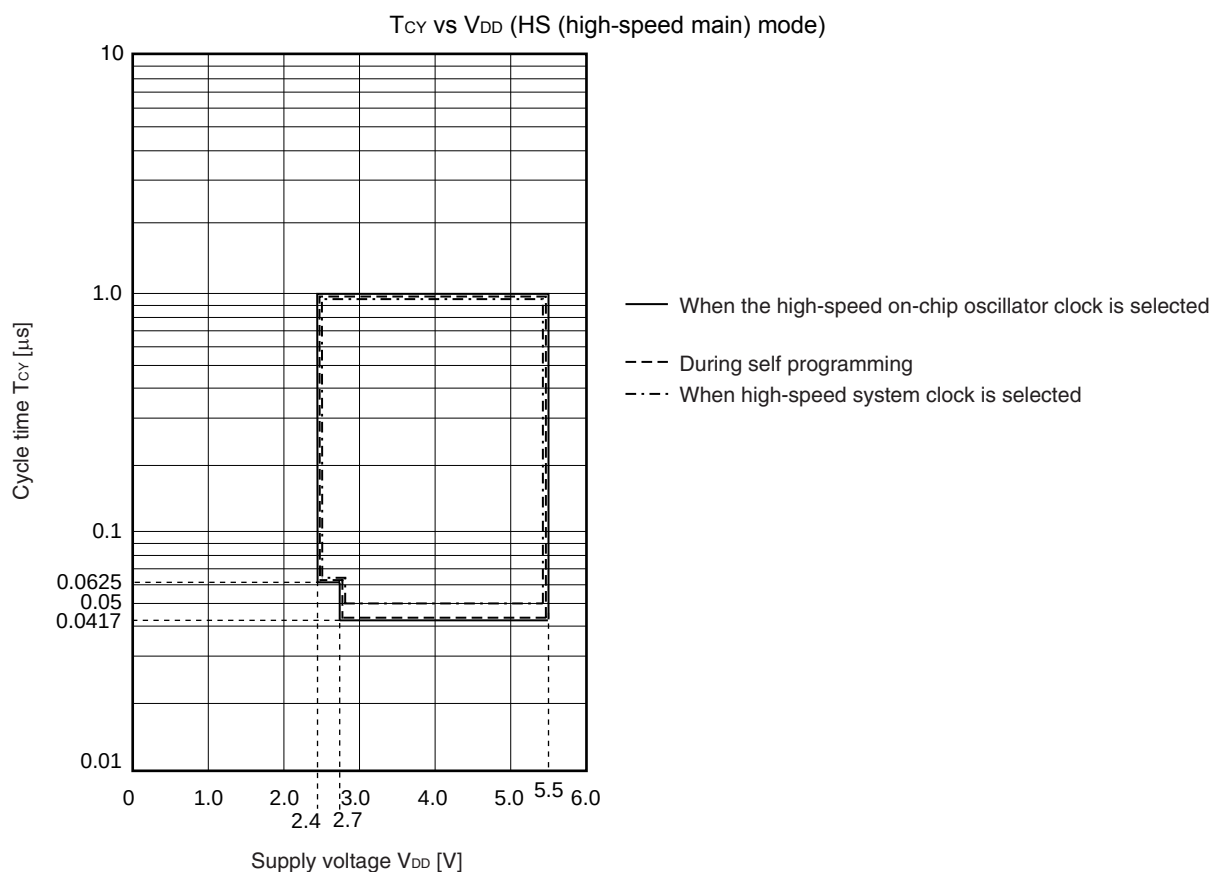
Note Operation is not possible if $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$ in LV (low-voltage main) mode while the system is operating on the subsystem clock.

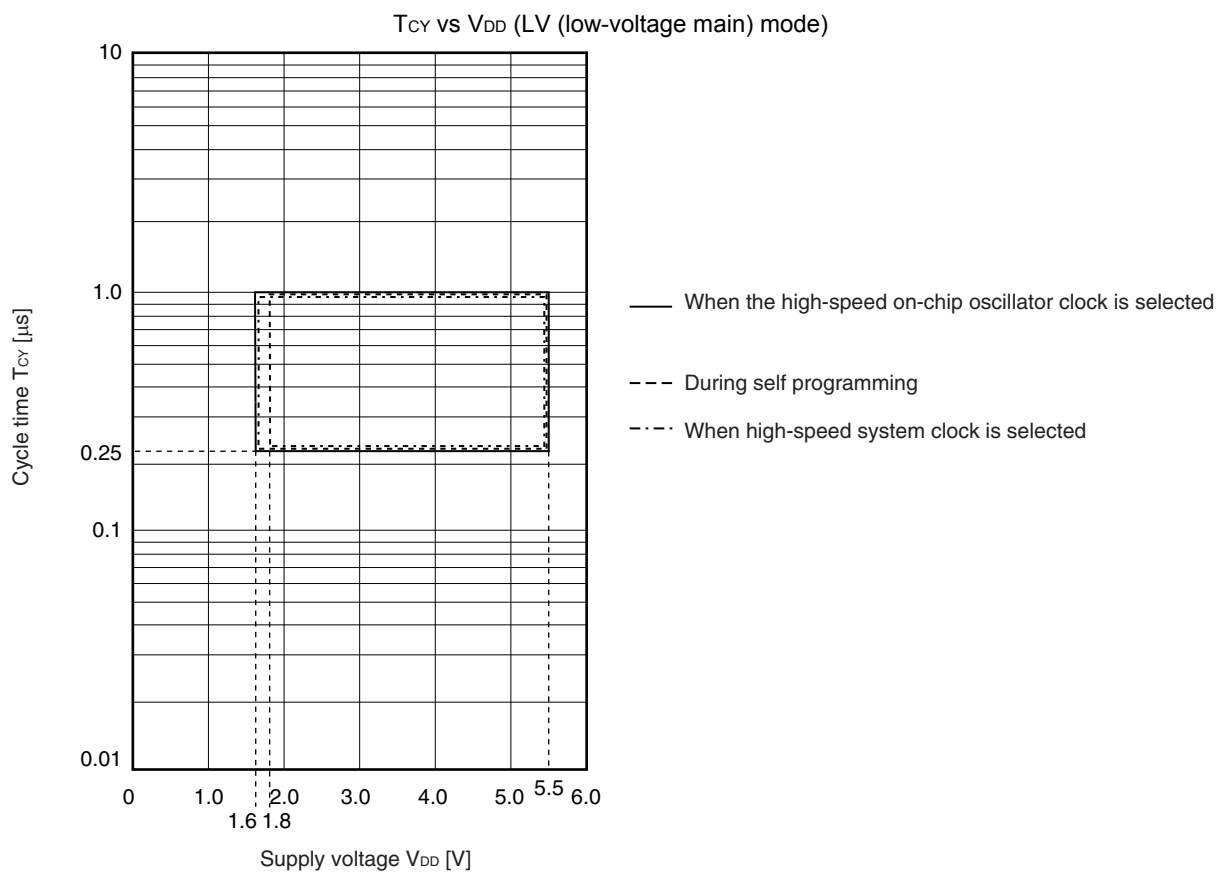
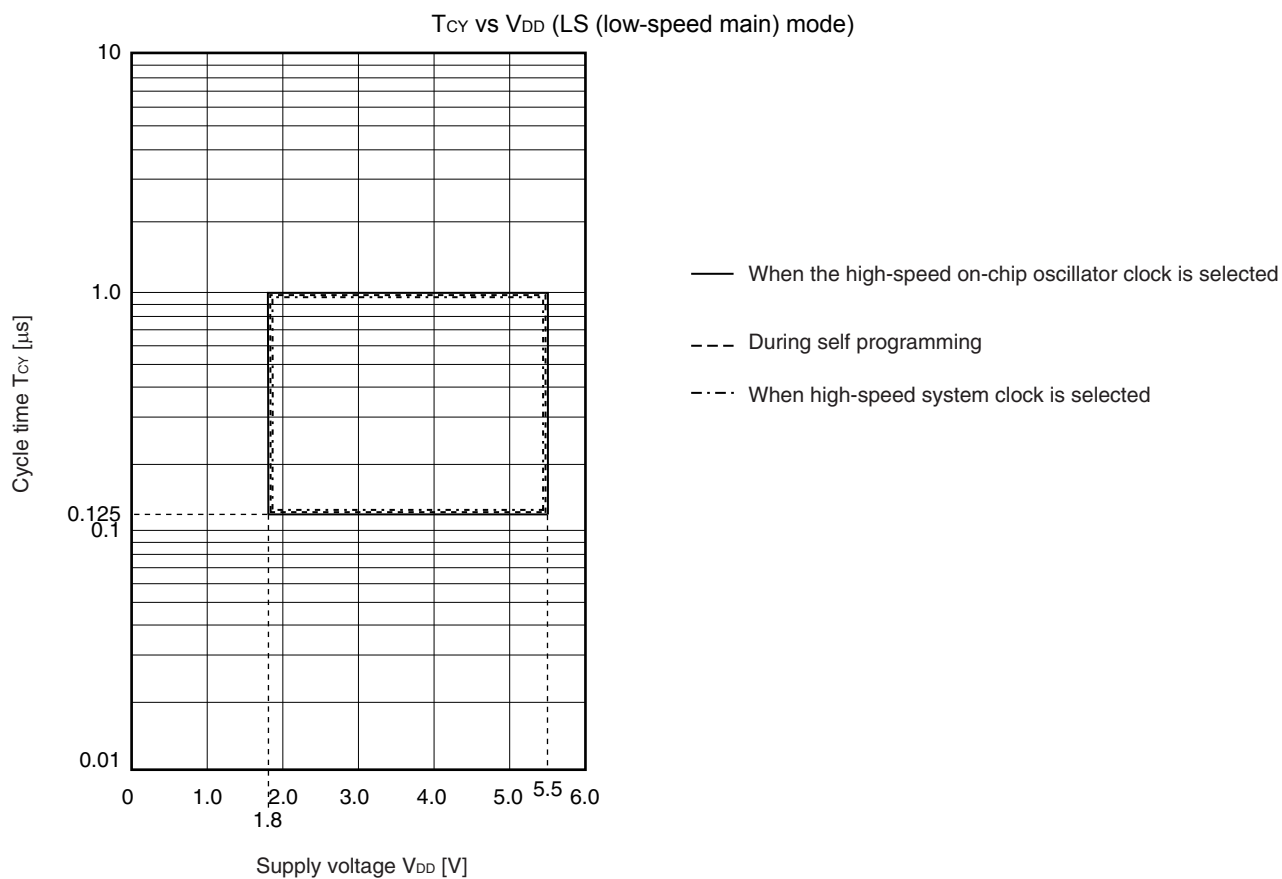
Remark f_{MCK} : Timer array unit operation clock frequency

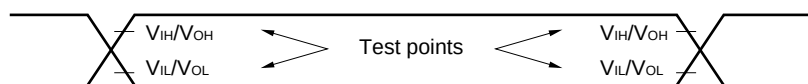
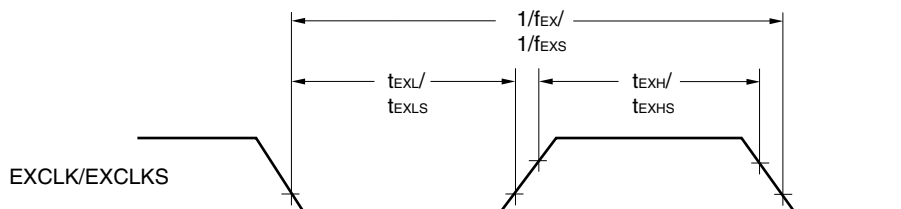
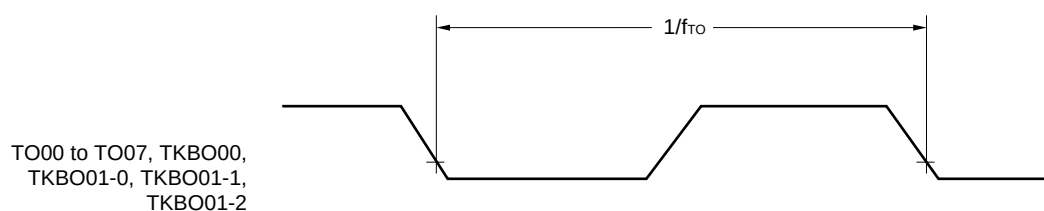
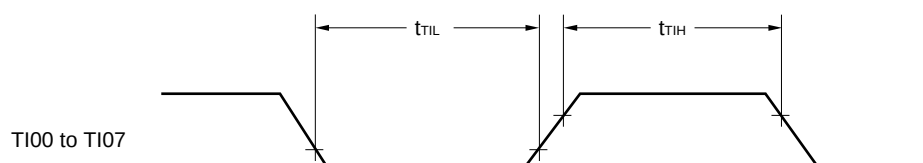
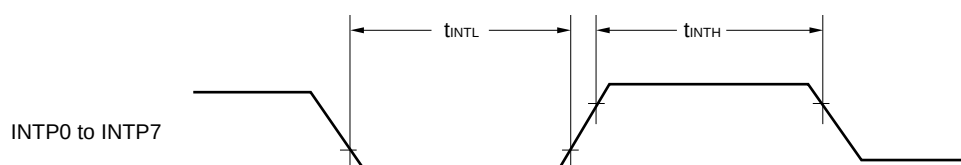
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn)

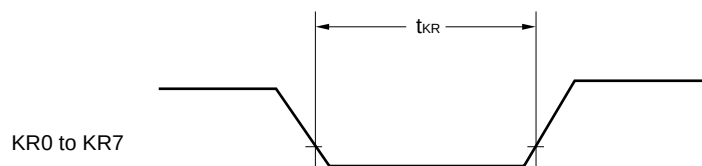
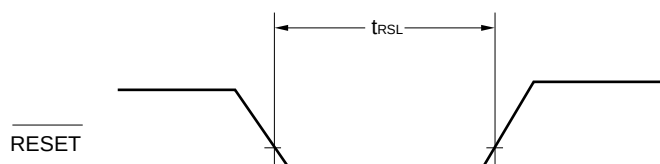
m: Unit number ($m = 0$), n: Channel number ($n = 0$ to 7))

Minimum Instruction Execution Time during Main System Clock Operation



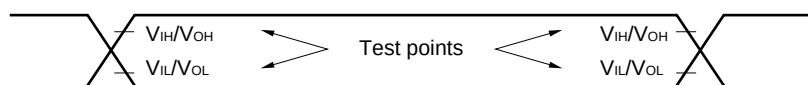


AC Timing Test Points**External System Clock Timing****TI/TO Timing****Interrupt Request Input Timing**

Key Interrupt Input Timing **$\overline{\text{RESET}}$ Input Timing**

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate ^{Note 1}		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}		4.0		1.3		0.6	Mbps
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}		—		1.3		0.6	Mbps
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		—		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}		—		—		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

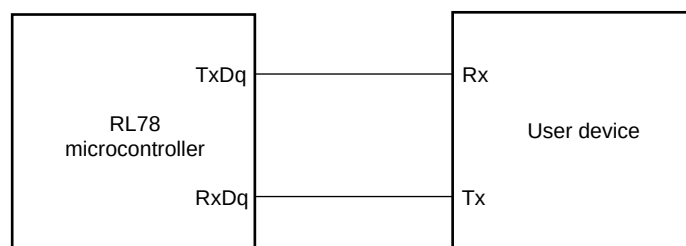
HS (high-speed main) mode: 24 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)
16 MHz ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

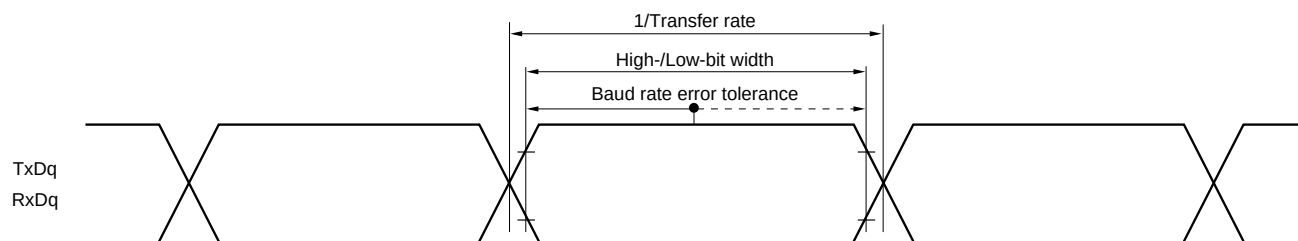
LS (low-speed main) mode: 8 MHz ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

LV (low-voltage main) mode: 4 MHz ($1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)

- Remarks**
1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	167 ^{Note 1}		500 ^{Note 1}		1000 ^{Note 1}		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	250 ^{Note 1}		500 ^{Note 1}		1000 ^{Note 1}		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		500 ^{Note 1}		1000 ^{Note 1}		ns
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		—		1000 ^{Note 1}		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	t _{KCY1} /2–12		t _{KCY1} /2–50		t _{KCY1} /2–50		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	t _{KCY1} /2–18		t _{KCY1} /2–50		t _{KCY1} /2–50		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	t _{KCY1} /2–38		t _{KCY1} /2–50		t _{KCY1} /2–50		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		t _{KCY1} /2–50		t _{KCY1} /2–50		ns
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		—		t _{KCY1} /2–100		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	44		110		110		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	75		110		110		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		110		110		ns
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		—		220		ns
Slp hold time (from SCKp↑) ^{Note 3}	t _{KSI1}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	19		19		19		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		19		19		ns
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		—		19		ns
Delay time from SCKp↓ to SOp output ^{Note 4}	t _{KSO1}	C = 30 pF ^{Note 5}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	25		25		25	ns
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		25		25	ns
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—		—		25	ns

Notes 1. The value must also be equal to or more than $2/f_{CLK}$ for CSI00 and equal to or more than $4/f_{CLK}$ for CSI10.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
5. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10), m: Unit number (m = 0), n: Channel number (n = 0, 2),
g: PIM and POM numbers (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00, 02))

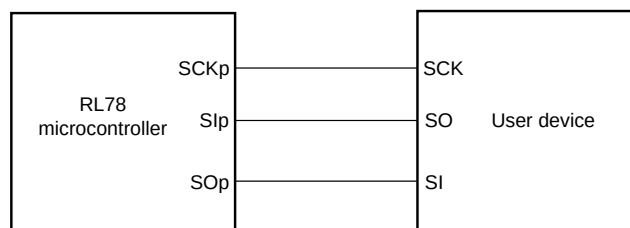
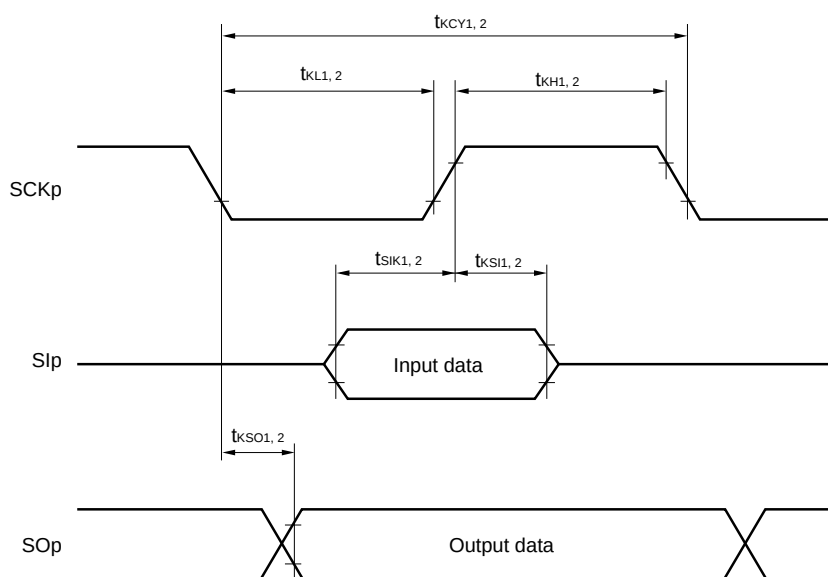
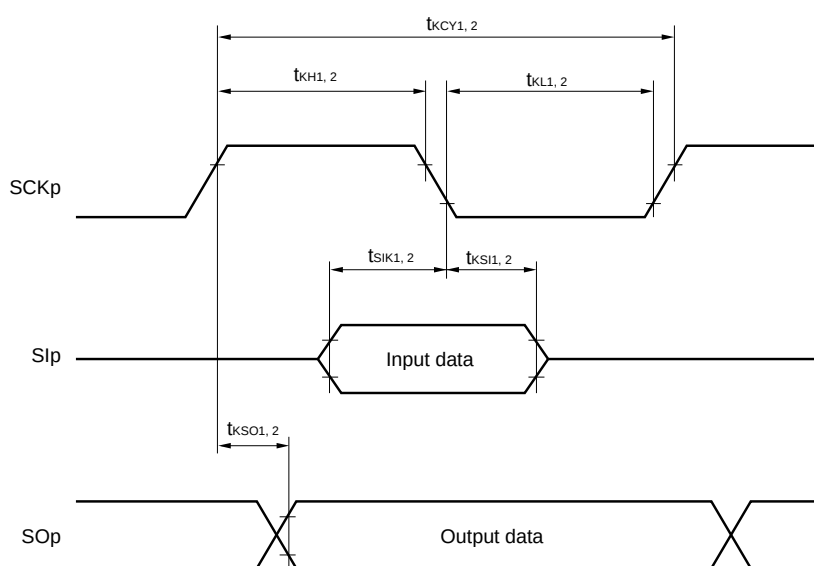
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 5}	t_{KCY2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$f_{MCK} > 20\text{ MHz}$	$8/f_{MCK}$		—		—		ns
			$f_{MCK} \leq 20\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$f_{MCK} > 16\text{ MHz}$	$8/f_{MCK}$		—		—		ns
			$f_{MCK} \leq 16\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$6/f_{MCK}$ and 500		$6/f_{MCK}$		$6/f_{MCK}$		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$6/f_{MCK}$		$6/f_{MCK}$		ns
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		—		$6/f_{MCK}$		ns
SCKp high-/low-level width	t_{KH2} , t_{KL2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-7$		$t_{KCY2}/2-7$		$t_{KCY2}/2-7$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-8$		$t_{KCY2}/2-8$		$t_{KCY2}/2-8$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-18$		$t_{KCY2}/2-18$		$t_{KCY2}/2-18$		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$t_{KCY2}/2-18$		$t_{KCY2}/2-18$		ns
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		—		$t_{KCY2}/2-66$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK2}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK}+20$		$1/f_{MCK}+30$		$1/f_{MCK}+30$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK}+30$		$1/f_{MCK}+30$		$1/f_{MCK}+30$		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$1/f_{MCK}+30$		$1/f_{MCK}+30$		ns
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		—		$1/f_{MCK}+40$		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 2}	t_{SI2}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK}+31$		$1/f_{MCK}+31$		$1/f_{MCK}+31$		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$1/f_{MCK}+31$		$1/f_{MCK}+31$		ns
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		—		$1/f_{MCK}+250$		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 3}	t_{KS02}	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK}+44$		$2/f_{MCK}+110$		$2/f_{MCK}+110$	ns
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK}+75$		$2/f_{MCK}+110$		$2/f_{MCK}+110$	ns
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$2/f_{MCK}+110$		$2/f_{MCK}+110$	ns
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		—		$2/f_{MCK}+220$	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp $\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp $\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 10), m: Unit number (m = 0), n: Channel number (n = 0, 2),
g: PIM number (g = 0, 1)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

CSI mode connection diagram (during communication at same potential)
CSI mode serial transfer timing (during communication at same potential)
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (during communication at same potential)
 (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)


- Remarks 1.** p: CSI number (p = 00, 10)
2. m: Unit number, n: Channel number (mn = 00, 02)

(4) During communication at same potential (simplified I²C mode)**(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

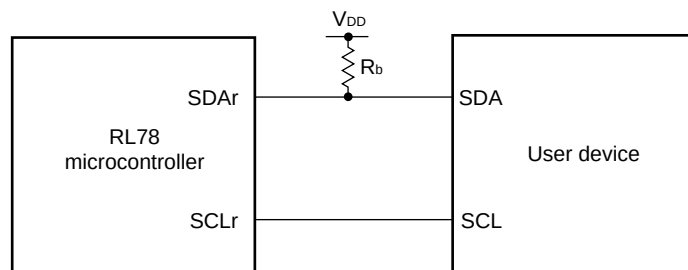
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 ^{Note 1}		400 ^{Note 1}		400 ^{Note 1}	kHz
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		400 ^{Note 1}		400 ^{Note 1}		400 ^{Note 1}	kHz
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ		300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		1.6 V ≤ V _{DD} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ		—		—		250 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		1150		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		1150		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ V _{DD} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		—		1850		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		1150		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		1150		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ V _{DD} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		—		1850		ns
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 ^{Note 2}		1/f _{MCK} + 145 ^{Note 2}		1/f _{MCK} + 145 ^{Note 2}		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 ^{Note 2}		1/f _{MCK} + 145 ^{Note 2}		1/f _{MCK} + 145 ^{Note 2}		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 230 ^{Note 2}		1/f _{MCK} + 230 ^{Note 2}		1/f _{MCK} + 230 ^{Note 2}		ns
		1.6 V ≤ V _{DD} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		—		1/f _{MCK} + 290 ^{Note 2}		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ V _{DD} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—	—	—	—	0	405	ns

(Notes, Caution, and Remarks are listed on the next page.)

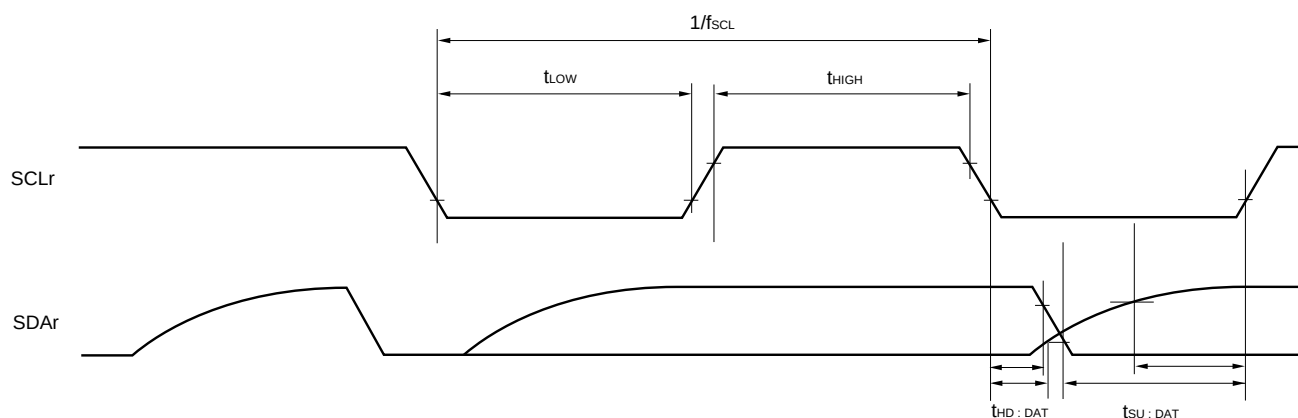
- Notes**
1. The value must also be equal to or less than $f_{MCK}/4$.
 2. Set the f_{MCK} value to keep the hold time of $SCLr = "L"$ and $SCLr = "H"$.
 3. Condition in the HS (high-speed main) mode

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the $SDAr$ pin and the normal output mode for the $SCLr$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



- Remarks**
1. $R_b[\Omega]$: Communication line ($SDAr$) pull-up resistance, $C_b[F]$: Communication line ($SDAr$, $SCLr$) load capacitance
 2. r: IIC number (r = 00, 10), g: PIM and POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the $CKSmn$ bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0-3), mn = 00-03, 10-13)

<R>

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}		4.0		1.3		0.6	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}		4.0		1.3		0.6	Mbps
			1.8 V (2.4 V ^{Note 4}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		f _{MCK} /6 ^{Note s1, 2}		f _{MCK} /6 ^{Notes 1, 2}		f _{MCK} /6 ^{Notes 1, 2}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}		4.0		1.3		0.6	Mbps

Notes 1. Transfer rate in SNOOZE mode is 4800 bps only.**2.** Use it with $V_{DD} \geq V_b$.**3.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)16 MHz ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)LS (low-speed main) mode: 8 MHz ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)LV (low-voltage main) mode: 4 MHz ($1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)**4.** Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks 1. $V_b[V]$: Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)**3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Trans mission	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V)			2.8 ^{Note 2}		2.8 ^{Note 2}	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V)			1.2 ^{Note 4}		1.2 ^{Note 4}	Mbps
			1.8 V (2.4 V ^{Note 8}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V)			0.43 ^{Note 7}		0.43 ^{Note 7}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.
- Use it with V_{DD} ≥ V_b.

Notes 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ($2.4\text{ V}^{\text{Note 8}}$) $\leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

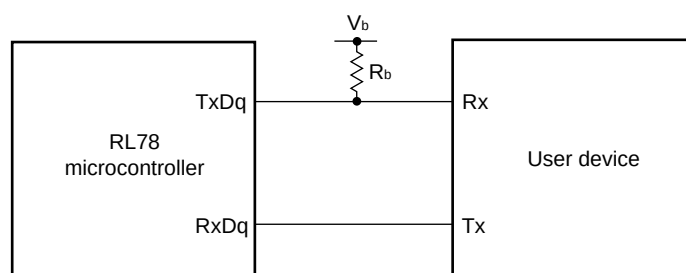
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

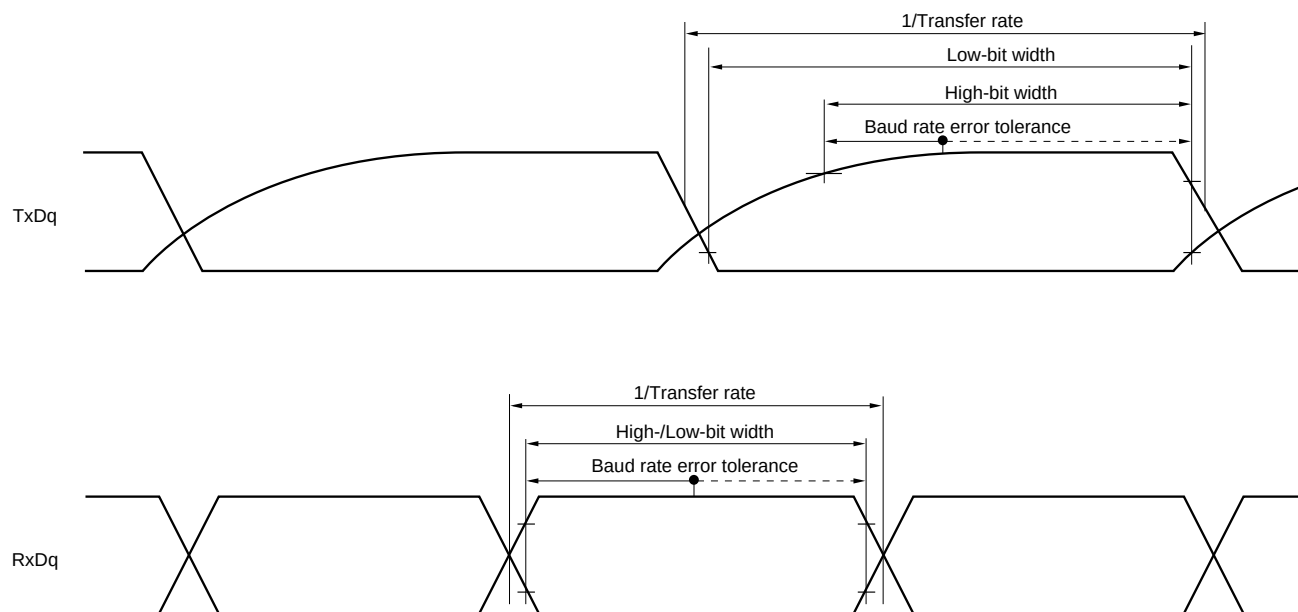
7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.
8. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



- Remarks 1.** $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
- 2.** q : UART number ($q = 0$ to 3), g : PIM and POM number ($g = 0, 1, 3$)
- 3.** f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m : Unit number, n : Channel number ($mn = 00$ to $03, 10$ to 13))

(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	200		1150		1150		ns
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	300		1150		1150		ns
SCKp high-level width	t_{KH1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		ns
SCKp low-level width	t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		$t_{KCY1}/2 - 7$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		$t_{KCY1}/2 - 10$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		58		479		479		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		121		479		479		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 1}	t_{KS1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		10		10		10		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		10		10		10		ns
Delay time from SCKp $\downarrow$ to SOP output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			60		60		60	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			130		130		130	ns
Slp setup time (to SCKp $\downarrow$) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		23		110		110		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		33		110		110		ns
Slp hold time (from SCKp $\downarrow$) ^{Note 2}	t_{KS1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		10		10		10		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		10		10		10		ns
Delay time from SCKp $\uparrow$ to SOP output ^{Note 2}	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			10		10		10	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			10		10		10	ns

(Notes, Caution and Remarks are listed on the next page.)

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number ($p = 00$), m: Unit number ($m = 0$), n: Channel number ($n = 0$),
g: PIM and POM number ($g = 1$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number ($mn = 00$))
 4. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)
(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	500		1150		1150		ns
			1.8 V (2.4 V ^{Note 1}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 1.8 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t _{KH1}		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 – 75		t _{KCY1} /2 – 75		t _{KCY1} /2 – 75		ns
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 170		t _{KCY1} /2 – 170		t _{KCY1} /2 – 170		ns
			1.8 V (2.4 V ^{Note 1}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 – 458		t _{KCY1} /2 – 458		t _{KCY1} /2 – 458		ns
SCKp low-level width	t _{KL1}		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 – 12		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 18		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
			1.8 V (2.4 V ^{Note 1}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK1}		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81		479		479		ns
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		ns
			1.8 V (2.4 V ^{Note 1}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) ^{Note 3}	t _{KH1}		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
			1.8 V (2.4 V ^{Note 1}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO1}		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		100		100		100	ns
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		195		195		195	ns
			1.8 V (2.4 V ^{Note 1}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ		483		483		483	ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

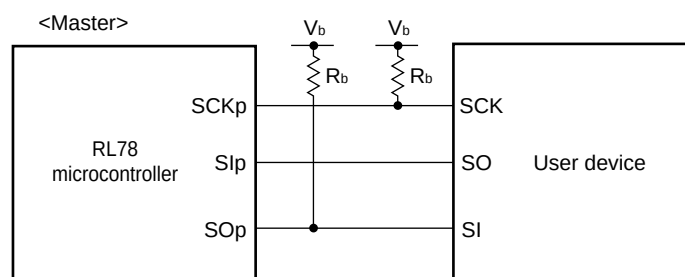
(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)
(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note 4}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	44		110		110		ns
		1.8 V (2.4 V ^{Note 1}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	110		110		110		ns
Slp hold time (from SCKp↓) ^{Note 4}	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		1.8 V (2.4 V ^{Note 1}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output ^{Note 4}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		25		25		25	ns
		1.8 V (2.4 V ^{Note 1}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ		25		25		25	ns

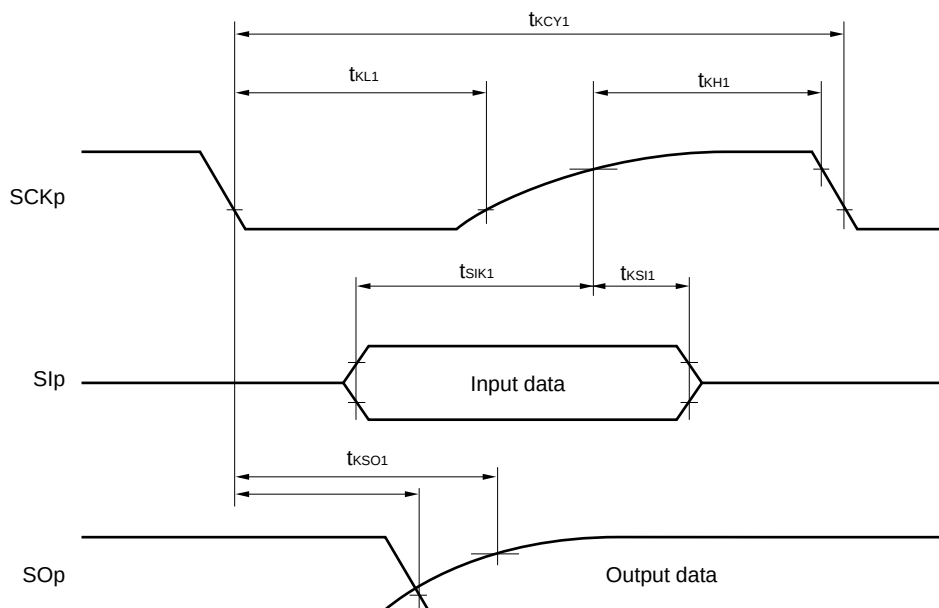
- Notes**
1. Condition in HS (high-speed main) mode
 2. Use it with V_{DD} ≥ V_b.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 4. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

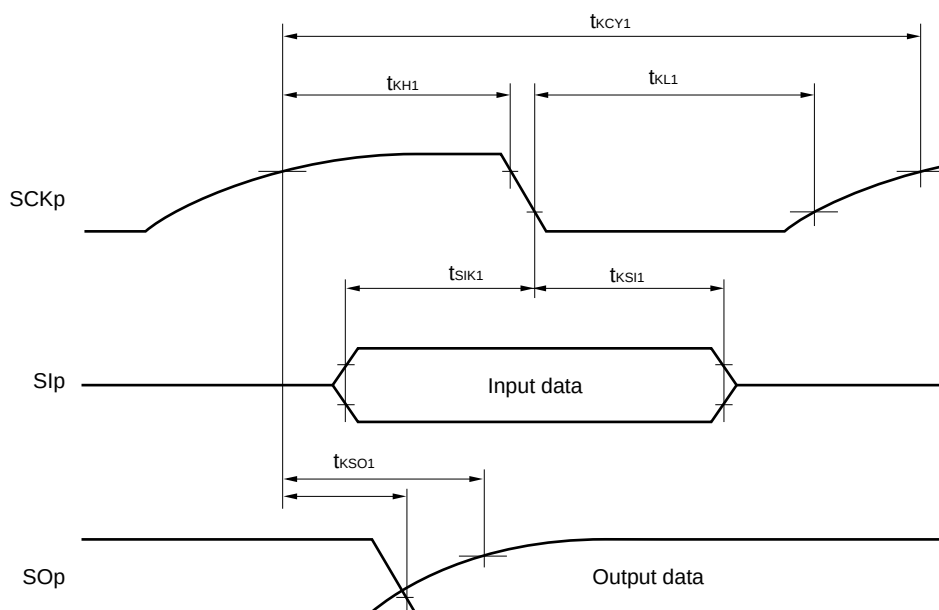
CSI mode connection diagram (during communication at different potential)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
- 2.** p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02), g: PIM and POM number (g = 0, 1)
- 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00))

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

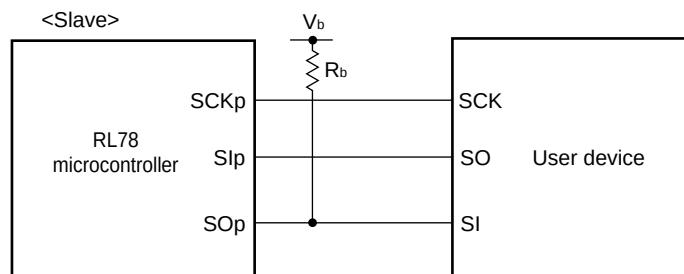
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK}	12/f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK}	16/f _{MCK}		—		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3}	20 MHz < f _{MCK}	36/f _{MCK}		—		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		16/f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	10/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		t _{KCY2} /2 – 12		t _{KCY2} /2 – 50		t _{KCY2} /2 – 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		t _{KCY2} /2 – 18		t _{KCY2} /2 – 50		t _{KCY2} /2 – 50		ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3}		t _{KCY2} /2 – 50		t _{KCY2} /2 – 50		t _{KCY2} /2 – 50		ns
Slp setup time (to SCKp↑) ^{Note 4}	t _{SIK2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3}		1/f _{MCK} + 30		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
Slp hold time (from SCKp↑) ^{Note 5}	t _{SI2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3}		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
Delay time from SCKp↓ to SOP output ^{Note 6}	t _{KSO2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 120		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 214		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 573		2/f _{MCK} + 573		2/f _{MCK} + 573	ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

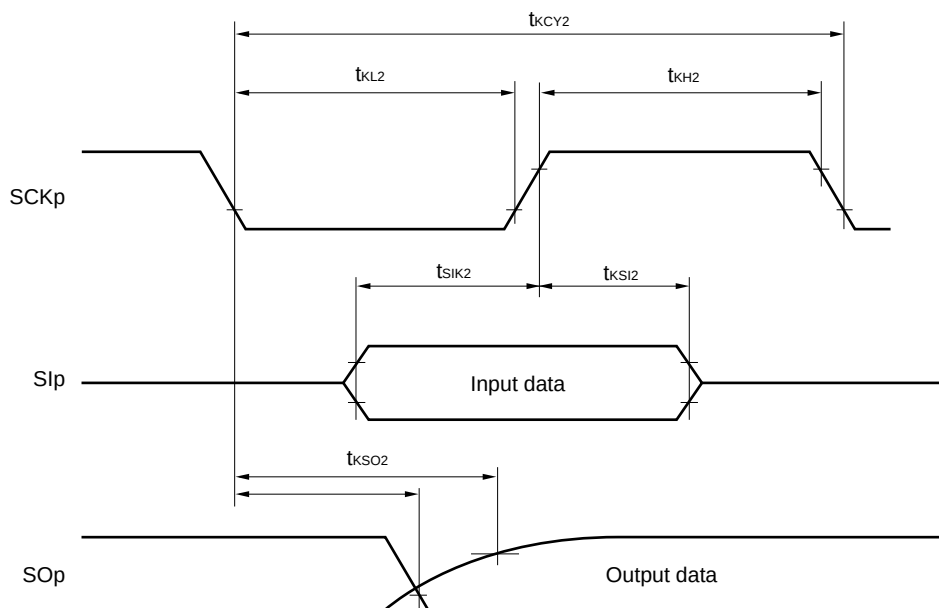
- Notes**
1. Transfer rate in SNOOZE mode: MAX. 1 Mbps
 2. Condition in HS (high-speed main) mode
 3. Use it with $V_{DD} \geq V_b$.
 4. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Sip setup time becomes “to $SCKp\downarrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 5. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Sip hold time becomes “from $SCKp\downarrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 6. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from $SCKp\uparrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.

Caution Select the TTL input buffer for the Sip pin and $SCKp$ pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

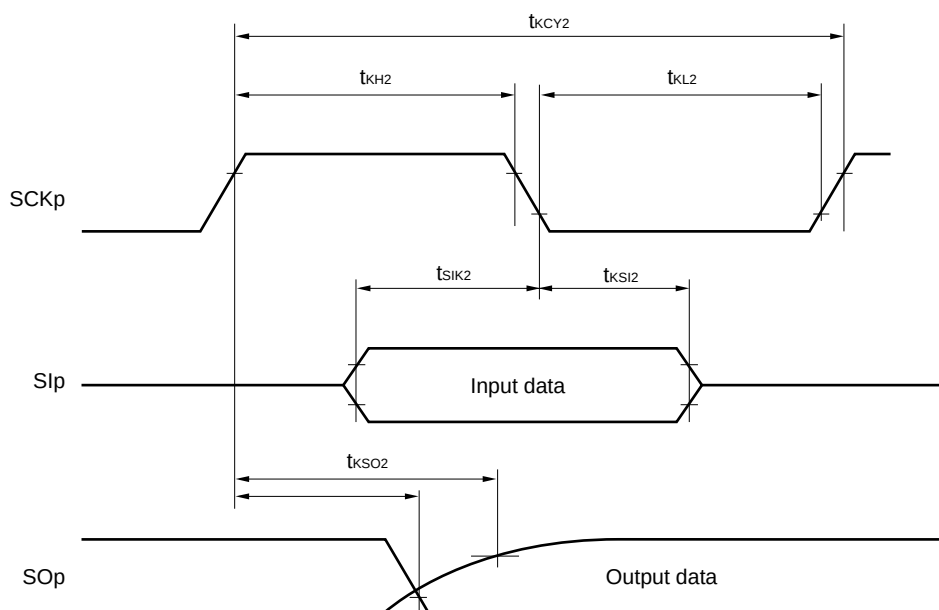
CSI mode connection diagram (during communication at different potential)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
- 2.** p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02), g: PIM and POM number (g = 0, 1)
- 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn)
 m: Unit number, n: Channel number (mn = 00, 02))

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)(T_A = -40 to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		1000 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		1000 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$		400 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	475		1550		1550		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	475		1550		1550		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	1150		1550		1550		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1150		1550		1550		ns
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	1550		1550		1550		ns
Hold time when SCLr = "H"	t _{HIGH}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	245		610		610		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	200		610		610		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	675		610		610		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	600		610		610		ns
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	610		610		610		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

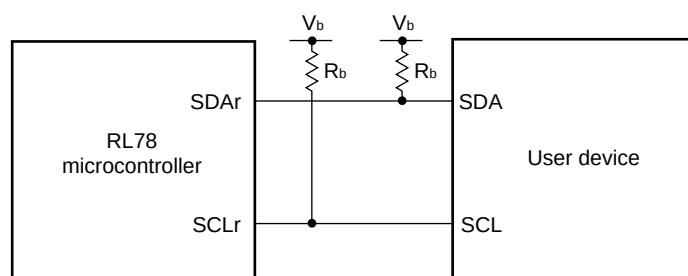
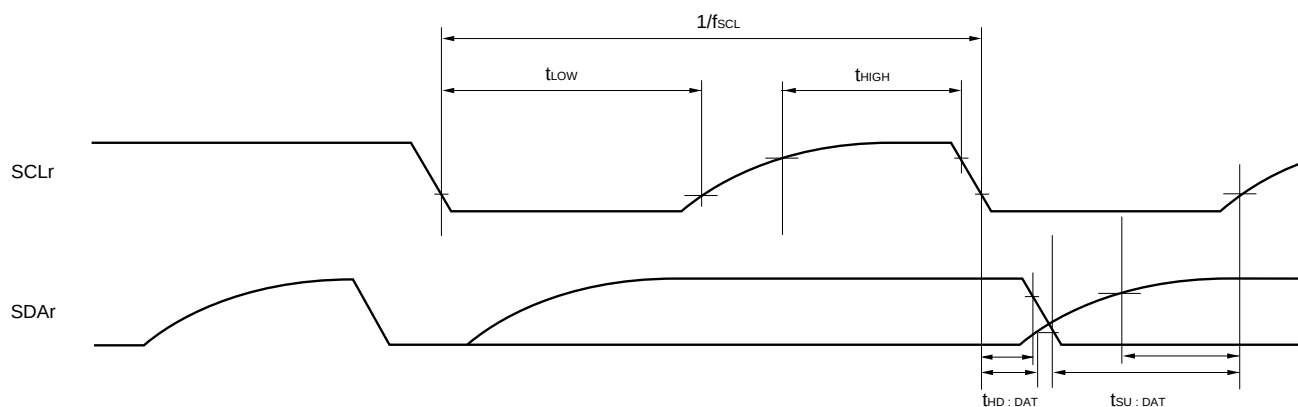
(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 135^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 135^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
Data hold time (transmission)	$t_{HD:DAT}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	305	0	305	0	305	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	305	0	305	0	305	ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	0	355	0	355	0	355	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	355	0	355	0	355	ns
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	0	405	0	405	0	405	ns

- Notes**
1. The value must also be equal to or less than $f_{MCK}/4$.
 2. Condition in HS (high-speed main) mode
 3. Use it with $V_{DD} \geq V_b$.
 4. Set the f_{MCK} value to keep the hold time of $SCLr = "L"$ and $SCLr = "H"$.

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)Simplified I²C mode serial transfer timing (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number ($r = 00, 10$), g: PIM, POM number ($g = 0, 1$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00, 02$))

2.5.2 Serial interface IICA

(1) I²C standard mode (1/2)(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Normal mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ V _{DD} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.6 V ≤ V _{DD} ≤ 5.5 V	–	–	–	–	0	100	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		1.6 V ≤ V _{DD} ≤ 5.5 V		–	–	–	–	4.7		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		1.6 V ≤ V _{DD} ≤ 5.5 V		–	–	–	–	4.0		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		1.6 V ≤ V _{DD} ≤ 5.5 V		–	–	–	–	4.7		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		1.6 V ≤ V _{DD} ≤ 5.5 V		–	–	–	–	4.0		μs

(Notes, Caution and Remark are listed on the next page.)

(1) I²C standard mode (2/2)(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V	250		250		250		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	250		250		250		ns
		1.6 V ≤ V _{DD} ≤ 5.5 V	—	—	—	—	250		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.6 V ≤ V _{DD} ≤ 5.5 V	—	—	—	—	0	3.45	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 5.5 V	4.0		4.0		4.0		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	4.0		4.0		4.0		μs
		1.6 V ≤ V _{DD} ≤ 5.5 V	—	—	—	—	4.0		μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 5.5 V	4.7		4.7		4.7		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	4.7		4.7		4.7		μs
		1.6 V ≤ V _{DD} ≤ 5.5 V	—	—	—	—	4.7		μs

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.
 3. Condition in HS (high-speed main) mode

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	2.7 V ≤ V _{DD} ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		100		100		100		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		100		100		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

3. Condition in HS (high-speed main) mode

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

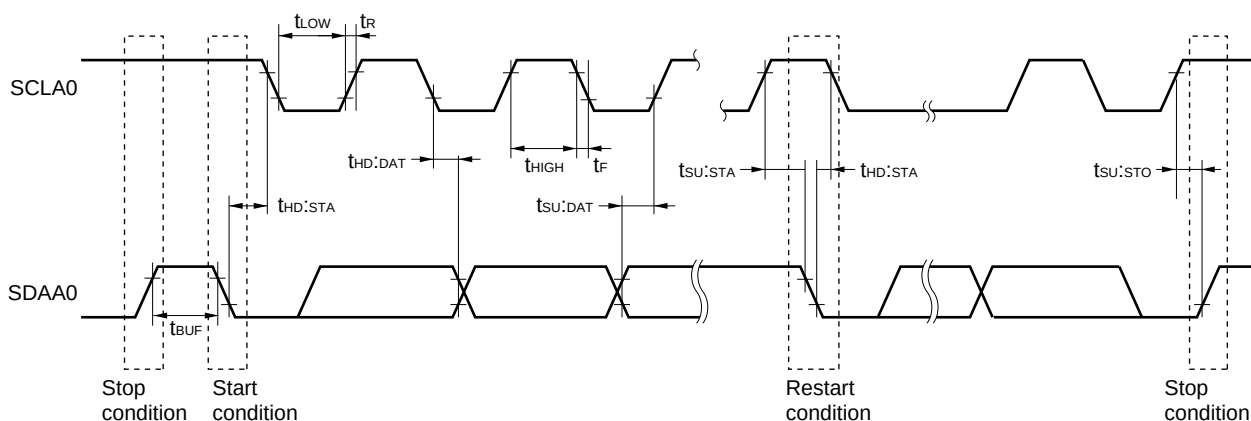
(3) I²C fast mode plus**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: $f_{CLK} \geq 10\text{ MHz}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0	1000	—	—	—	—	kHz
Setup time of restart condition	$t_{SU:STA}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.26		—	—	—	—	μs
Hold time ^{Note 1}	$t_{HD:STA}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.26		—	—	—	—	μs
Hold time when SCLA0 = "L"	t_{LOW}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.5		—	—	—	—	μs
Hold time when SCLA0 = "H"	t_{HIGH}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.26		—	—	—	—	μs
Data setup time (reception)	$t_{SU:DAT}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		50		—	—	—	—	ns
Data hold time (transmission) ^{Note 2}	$t_{HD:DAT}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0	0.45	—	—	—	—	μs
Setup time of stop condition	$t_{SU:STO}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.26		—	—	—	—	μs
Bus-free time	t_{BUF}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.5		—	—	—	—	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1} , I_{OL1} , V_{OH1} , V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: $C_b = 120\text{ pF}$, $R_b = 1.1\text{ k}\Omega$ **I²C serial transfer timing**

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0, ANI1	–	See 2.6.1 (2).	See 2.6.1 (3).
ANI16 to ANI25	See 2.6.1 (1).		
Internal reference voltage Temperature sensor output voltage	See 2.6.1 (1).		–

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (–) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pins: ANI16 to ANI25, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (–) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 5.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}	1.2	± 8.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI16 to ANI25	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}		± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}		± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}		± 6.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}		± 2.5	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI25	0		AV_{REFP}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode))			V_{BGR} ^{Note 5}	V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode))			V_{TMPS25} ^{Note 5}	V

(Notes are listed on the next page.)

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.2\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. Values when the conversion time is set to $57\ \mu\text{s}$ (min.) and $95\ \mu\text{s}$ (max.).

5. See 2.6.2 Temperature sensor/internal reference voltage characteristics.

(2) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pins: ANI0, ANI1, ANI16 to ANI25, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$, $V_{SS} = 0\ \text{V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Notes 1, 2}	AINL	10-bit resolution	$1.8\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$		1.2	± 7.0	LSB
			$1.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$ ^{Note 3}		1.2	± 10.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0, ANI1, ANI16 to ANI25 ^{Note 3}	$3.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	2.125		39	μs
			$2.7\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	3.1875		39	μs
			$1.8\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	17		39	μs
			$1.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	2.375		39	μs
			$2.7\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	3.5625		39	μs
			$2.4\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution	$1.8\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$			± 0.60	%FSR
			$1.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$ ^{Note 3}			± 0.85	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution	$1.8\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$			± 0.60	%FSR
			$1.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$ ^{Note 3}			± 0.85	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$1.8\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$			± 4.0	LSB
			$1.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$ ^{Note 3}			± 6.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	$1.8\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$			± 2.0	LSB
			$1.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$ ^{Note 3}			± 2.5	LSB
Analog input voltage	V_{AIN}	ANI0, ANI1, ANI16 to ANI25		0		V_{DD}	V
		Internal reference voltage ($2.4\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$, HS (high-speed main) mode))		V_{BGR} ^{Note 4}			V
		Temperature sensor output voltage ($2.4\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$, HS (high-speed main) mode))		V_{TMPS25} ^{Note 4}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Values when the conversion time is set to $57\ \mu\text{s}$ (min.) and $95\ \mu\text{s}$ (max.).

4. See 2.6.2 Temperature sensor/internal reference voltage characteristics.

(3) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pins: ANI0, ANI16 to ANI25

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR}^{Note 3},
Reference voltage (-) = AVREFM^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V _{AIN}			0		V _{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See 2.6.2 Temperature sensor/internal reference voltage characteristics.

4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the AVREFM MAX. value.

Integral linearity error: Add ±0.5 LSB to the AVREFM MAX. value.

Differential linearity error: Add ±0.2 LSB to the AVREFM MAX. value.

2.6.2 Temperature sensor /internal reference voltage characteristics

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V _{TMPS25}	ADS register = 80H, T _A = +25°C		1.05		V
Internal reference output voltage	V _{BGR}	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F _{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t _{AMP}				5	μs

2.6.3 Comparator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref		0		$V_{DD} - 1.4$	V
	Ivcmp		-0.3		$V_{DD} + 0.3$	V
Output delay	td	$V_{DD} = 3.0\text{ V}$ Input slew rate $> 50\text{ mV}/\mu\text{s}$ Comparator high-speed mode, standard mode			1.2	μs
		Comparator high-speed mode, window mode			2.0	μs
		Comparator low-speed mode, standard mode		3.0	5.0	μs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode, window mode	$0.66V_{DD}$	$0.76V_{DD}$	$0.86V_{DD}$	V
Low-electric-potential reference voltage	VTW-	Comparator high-speed mode, window mode	$0.14V_{DD}$	$0.24V_{DD}$	$0.34V_{DD}$	V
Operation stabilization wait time	tCMP		100			μs
Internal reference output voltage ^{Note}	V _{BGR}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode	1.38	1.45	1.50	V

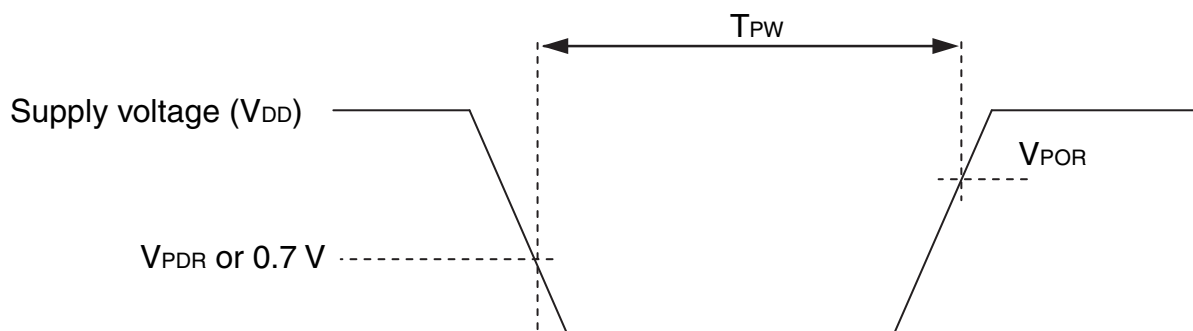
Note Cannot be used in LS (low-speed main) mode, LV (low-voltage main) mode, subsystem clock operation, and STOP mode.

2.6.4 POR circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{POR}	When power supply rises	1.47	1.51	1.55	V
	V _{PDR}	When power supply falls	1.46	1.50	1.54	V
Minimum pulse width ^{Note}	T _{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset operation when V_{DD} falls below V_{PDR} . When the microcontroller enters STOP mode and when the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset operation between when V_{DD} falls below 0.7 V and when V_{DD} rises to V_{POR} or higher.



2.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V _{LVD0}	When power supply rises	3.98	4.06	4.14	V
			When power supply falls	3.90	3.98	4.06	V
		V _{LVD1}	When power supply rises	3.68	3.75	3.82	V
			When power supply falls	3.60	3.67	3.74	V
		V _{LVD2}	When power supply rises	3.07	3.13	3.19	V
			When power supply falls	3.00	3.06	3.12	V
		V _{LVD3}	When power supply rises	2.96	3.02	3.08	V
			When power supply falls	2.90	2.96	3.02	V
		V _{LVD4}	When power supply rises	2.86	2.92	2.97	V
			When power supply falls	2.80	2.86	2.91	V
		V _{LVD5}	When power supply rises	2.76	2.81	2.87	V
			When power supply falls	2.70	2.75	2.81	V
		V _{LVD6}	When power supply rises	2.66	2.71	2.76	V
			When power supply falls	2.60	2.65	2.70	V
		V _{LVD7}	When power supply rises	2.56	2.61	2.66	V
			When power supply falls	2.50	2.55	2.60	V
		V _{LVD8}	When power supply rises	2.45	2.50	2.55	V
			When power supply falls	2.40	2.45	2.50	V
		V _{LVD9}	When power supply rises	2.05	2.09	2.13	V
			When power supply falls	2.00	2.04	2.08	V
		V _{LVD10}	When power supply rises	1.94	1.98	2.02	V
			When power supply falls	1.90	1.94	1.98	V
		V _{LVD11}	When power supply rises	1.84	1.88	1.91	V
			When power supply falls	1.80	1.84	1.87	V
		V _{LVD12}	When power supply rises	1.74	1.77	1.81	V
			When power supply falls	1.70	1.73	1.77	V
		V _{LVD13}	When power supply rises	1.64	1.67	1.70	V
			When power supply falls	1.60	1.63	1.66	V
Minimum pulse width		t _{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVD13}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V _{LVD12}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V _{LVD11}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V _{LVD4}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD11}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V _{LVD10}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V _{LVD9}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V _{LVD2}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V _{LVD8}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V _{LVD7}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V _{LVD6}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V _{LVD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V _{LVD5}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V _{LVD4}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V _{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.6 Supply voltage rising slope characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{DD} rising slope	SV _{DD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 LCD Characteristics

2.7.1 External resistance division method

(1) Static display mode

($T_A = -40$ to $+85^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

($T_A = -40$ to $+85^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

($T_A = -40$ to $+85^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

2.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
LCD output voltage variation range	VL1	C1 to C4 ^{Note 1} = 0.47 μ F ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	VL2	C1 to C4 ^{Note 1} = 0.47 μ F	2 VL1 – 0.10	2 VL1	2 VL1	V	
Tripler output voltage	VL4	C1 to C4 ^{Note 1} = 0.47 μ F	3 VL1 – 0.15	3 VL1	3 VL1	V	
Reference voltage setup time ^{Note 2}	tVWAIT1		5			ms	
Voltage boost wait time ^{Note 3}	tVWAIT2	C1 to C4 ^{Note 1} = 0.47 μ F	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = 0.47 μF ± 30 %

- 2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- 3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V _{L1}	C1 to C5 ^{Note 1} = 0.47 μF ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V _{L2}	C1 to C5 ^{Note 1} = 0.47 μF	2 V _{L1} −0.08	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L3}	C1 to C5 ^{Note 1} = 0.47 μF	3 V _{L1} −0.12	3 V _{L1}	3 V _{L1}	V	
Quadruply output voltage	V _{L4}	C1 to C5 ^{Note 1} = 0.47 μF	4 V _{L1} −0.16	4 V _{L1}	4 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{VWAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{VWAIT2}	C1 to C5 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L3} and GNDC5: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = C5 = 0.47 μF ± 30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

2.7.3 Capacitor split method**(1) 1/3 bias method**(T_A = -40 to +85°C, 2.2 V ≤ V_D ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{L4} voltage	V _{L4}	C1 to C4 = 0.47 μF ^{Note 2}		V _{DD}		V
V _{L2} voltage	V _{L2}	C1 to C4 = 0.47 μF ^{Note 2}	2/3 V _{L4} - 0.1	2/3 V _{L4}	2/3 V _{L4} + 0.1	V
V _{L1} voltage	V _{L1}	C1 to C4 = 0.47 μF ^{Note 2}	1/3 V _{L4} - 0.1	1/3 V _{L4}	1/3 V _{L4} + 0.1	V
Capacitor split wait time ^{Note 1}	t _{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = 0.47 μF ± 30%

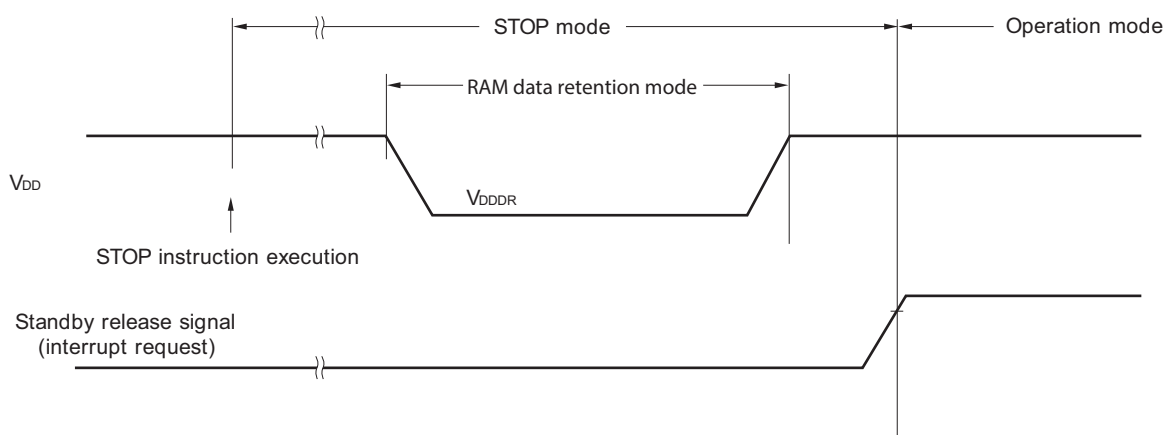
<R> 2.8 RAM Data Retention Characteristics

 $(T_A = -40$ to $+85^\circ\text{C})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 ^{Note}		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R> **Caution** Data in RAM are not retained if the CPU operates outside the specified operating voltage range. Therefore, place the CPU in STOP mode before the operating voltage drops below the specified range.



2.9 Flash Memory Programming Characteristics

 $(T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	1.8 V ≤ VDD ≤ 5.5 V	1		24	MHz
Number of code flash rewrites ^{Notes 1, 2, 3}	C _{erwr}	Retained for 20 years T _A = 85°C	1,000			Times
Number of data flash rewrites ^{Notes 1, 2, 3}		Retained for 1 year T _A = 25°C		1,000,000		
		Retained for 5 years T _A = 85°C	100,000			
		Retained for 20 years T _A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

2.10 Dedicated Flash Memory Programmer Communication (UART)

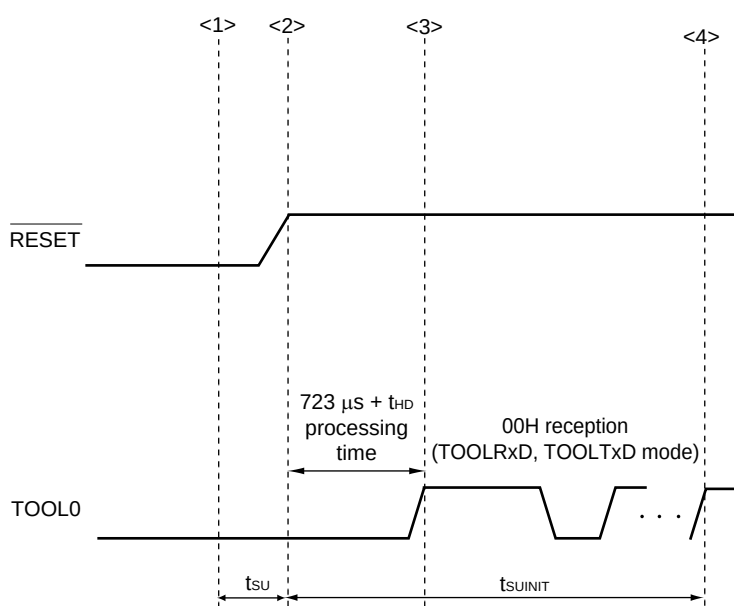
 $(T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.11 Timing Specifications for Switching Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUNIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and completion the baud rate setting.

Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A = -40$ to $+105^\circ\text{C}$

R5F10WLAGFB, R5F10WLCGFB, R5F10WLDGFB,
R5F10WLEGFB, R5F10WLFGFB, R5F10WLGGFB
R5F10WMAGFB, R5F10WMCGB, R5F10WMDGFB,
R5F10WMEGFB, R5F10WMFGFB, R5F10WMGGFB

- Cautions**
1. The RL78/L13 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 With functions for each product in the RL78/L13 User's Manual.
 3. Consult Renesas salesperson and distributor for derating when the product is used at $T_A = +85^\circ\text{C}$ to $+105^\circ\text{C}$. Note that derating means "systematically lowering the load from the rated value to improve reliability".

<R> **Remark** When RL78/L13 is used in the range of $T_A = -40$ to $+85^\circ\text{C}$, see **CHAPTER 2 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$)**.

“G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$) differ from “A: Consumer applications” in function as follows:

Fields of Application	A: Consumer applications	G: Industrial applications
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$	$T_A = -40$ to $+105^\circ\text{C}$
Operation mode operating voltage range	HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$ $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$ LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$ LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$	HS (high-speed main) mode only: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$ $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
High-speed on-chip oscillator clock accuracy	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$: $\pm 1.0\%$ @ $T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\%$ @ $T_A = -40$ to -20°C $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$: $\pm 5.0\%$ @ $T_A = -20$ to $+85^\circ\text{C}$ $\pm 5.5\%$ @ $T_A = -40$ to -20°C	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$: $\pm 2.0\%$ @ $T_A = +85$ to $+105^\circ\text{C}$ $\pm 1.0\%$ @ $T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\%$ @ $T_A = -40$ to -20°C
Serial array unit	UART CSI: $f_{CLK}/2$ (16 Mbps supported), $f_{CLK}/4$ Simplified I ² C	UART CSI: $f_{CLK}/4$ Simplified I ² C
IICA	Standard mode Fast mode Fast mode plus	Standard mode Fase mode
Voltage detector	- Rising: 1.67 V to 4.06 V (14 levels) - Falling: 1.63 V to 3.98 V (14 levels)	- Rising: 2.61 V to 4.06 V (8 levels) - Falling: 2.55 V to 3.98 V (8 levels)

Remark Electrical specifications of G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$) differ from “A: Consumer applications”. For details, see **3.1** to **3.11** below.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/3)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to $+6.5$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to $+2.8$ and -0.3 to $V_{DD} + 0.3$ ^{Note 1}	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I2}	P60 and P61 (N-ch open-drain)	-0.3 to $+6.5$	V
	V_{I3}	EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Analog input voltage	V_{AI1}	ANI0, ANI1, ANI16 to ANI26	-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)} + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. Vss: Reference voltage

Absolute Maximum Ratings (2/3)

Parameter	Symbol	Conditions	Ratings	Unit
LCD voltage	V_{L1}	V_{L1} voltage ^{Note 1}	-0.3 to $+2.8$ and -0.3 to $V_{L4} + 0.3$	V
	V_{L2}	V_{L2} voltage ^{Note 1}	-0.3 to $V_{L4} + 0.3$ ^{Note 2}	V
	V_{L3}	V_{L3} voltage ^{Note 1}	-0.3 to $V_{L4} + 0.3$ ^{Note 2}	V
	V_{L4}	V_{L4} voltage ^{Note 1}	-0.3 to $+6.5$	V
	V_{LCAP}	CAPL, CAPH voltage ^{Note 1}	-0.3 to $V_{L4} + 0.3$ ^{Note 2}	V
	V_{OUT}	COM0 to COM7 SEG0 to SEG50 output voltage	External resistance division method	-0.3 to $V_{DD} + 0.3$ ^{Note 2}
			Capacitor split method	-0.3 to $V_{DD} + 0.3$ ^{Note 2}
			Internal voltage boosting method	-0.3 to $V_{L4} + 0.3$ ^{Note 2}

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1} , V_{L2} , V_{L3} , and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor ($0.47 \mu\text{F} \pm 30\%$) and connect a capacitor ($0.47 \mu\text{F} \pm 30\%$) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS} : Reference voltage

Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$) (3/3)

Absolute Maximum Ratings (TA = 25 °C) (3/3)						
	Parameter	Symbol	Conditions		Ratings	Unit
<R>	Output current, high	IOH1	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−40	mA
<R>			Total of all pins −170 mA	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−170	mA
<R>		IOH2	Per pin	P20, P21	−0.5	mA
<R>			Total of all pins		−1	mA
<R>	Output current, low	IOL1	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
<R>			Total of all pins 170 mA	P40 to P47, P130	70	mA
<R>				P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
<R>		IOL2	Per pin	P20, P21	1	mA
<R>			Total of all pins		2	mA
	Operating ambient temperature	TA	In normal operation mode		−40 to +105	°C
			In flash memory programming mode			°C
	Storage temperature	Tstg			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1 and XT1 oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) ^{Note}	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	
XT1 clock oscillation frequency (f_{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see 5.4 **System Clock Oscillator** in the RL78/L13 User's Manual.

3.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		+85 to $+105^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-2		+2	%
		-20 to $+85^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1		+1	%
		-40 to -20°C	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for the instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			-3.0 ^{Note 2}	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			-45.0	mA
					-15.0	mA
					-7.0	mA
	I _{OH2}	Per pin for P20 and P21			-0.1 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})			-0.2	mA

Notes 1. Value of the current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin

2. Do not exceed the total current value.

3. Output current value under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OH} = -45.0\text{ mA}$

$$\text{Total output current of pins} = (-45.0 \times 0.7)/(80 \times 0.01) = -39.375\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			8.5 ^{Note 2}	mA
		Per pin for P60 and P61			15.0 ^{Note 2}	mA
		Total of P40 to P47, P130 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		40.0	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		15.0	mA
			$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		9.0	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P70 to P77, P125 to P127 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		60.0	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		35.0	mA
			$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		20.0	mA
		Total of all pins (When duty = 70% ^{Note 3})			100.0	mA
	I _{OL2}	Per pin for P20 and P21			0.4 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.8	mA

Notes 1. Value of the current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin

2. Do not exceed the total current value.

3. Output current value under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OL} = 40.0\text{ mA}$

$$\text{Total output current of pins} = (40.0 \times 0.7)/(80 \times 0.01) = 35.0\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	$0.8V_{DD}$	V_{DD}	V
	V_{IH2}	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.2	V_{DD}	V
			TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	2.0	V_{DD}	V
			TTL input buffer $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$	1.5	V_{DD}	V
	V_{IH3}	P20, P21	$0.7V_{DD}$		V_{DD}	V
	V_{IH4}	P60, P61	$0.7V_{DD}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	0	$0.2V_{DD}$	V
	V_{IL2}	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0	0.8	V
			TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	0	0.5	V
			TTL input buffer $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$	0	0.32	V
	V_{IL3}	P20, P21	0		$0.3V_{DD}$	V
	V_{IL4}	P60, P61	0		$0.3V_{DD}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		$0.2V_{DD}$	V

Caution The maximum value of V_{IH} of pins P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 is V_{DD} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$	$V_{DD} - 0.7$		V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$	$V_{DD} - 0.6$		V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$	$V_{DD} - 0.5$		V
	V _{OH2}	P20 and P21	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.5$		V
Output voltage, low	V _{OL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$		0.7	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$		0.4	V
	V _{OL2}	P20 and P21	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$		0.4	V
	V _{OL3}	P60 and P61	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 2.0\text{ mA}$		0.4	V

Caution P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I _{LIH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{DD}				1 μA
	I _{LIH2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{DD}				1 μA
	I _{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port mode and when external clock is input			1 μA
				Resonator connected			10 μA
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{SS}				−1 μA
	I _{LIL2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{SS}				−1 μA
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port mode and when external clock is input			−1 μA
				Resonator connected			−10 μA
On-chip pull-up resistance	R _{U1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P45 to P47, P50 to P57, P70 to P77, P125 to P127, P130	V _I = V _{SS}		10	20	100 kΩ
	R _{U2}	P40 to P44	V _I = V _{SS}		10	20	100 kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} ^{Note 1}	Operating mode	HS (high-speed main) mode ^{Note 5}	$f_{HOCO} = 48\text{ MHz}$ ^{Note 3} , $f_{IH} = 24\text{ MHz}$ ^{Note 3}	Basic operation	$V_{DD} = 5.0\text{ V}$		2.0		mA
						$V_{DD} = 3.0\text{ V}$		2.0		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$		3.8	7.0	mA
						$V_{DD} = 3.0\text{ V}$		3.8	7.0	mA
				$f_{HOCO} = 24\text{ MHz}$ ^{Note 3} , $f_{IH} = 24\text{ MHz}$ ^{Note 3}	Basic operation	$V_{DD} = 5.0\text{ V}$		1.7		mA
						$V_{DD} = 3.0\text{ V}$		1.7		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$		3.6	6.5	mA
						$V_{DD} = 3.0\text{ V}$		3.6	6.5	mA
				$f_{HOCO} = 16\text{ MHz}$ ^{Note 3} , $f_{IH} = 16\text{ MHz}$ ^{Note 3}	Normal operation	$V_{DD} = 5.0\text{ V}$		2.7	5.0	mA
						$V_{DD} = 3.0\text{ V}$		2.7	5.0	mA
			HS (high-speed main) mode ^{Note 5}	$f_{MX} = 20\text{ MHz}$ ^{Note 2} , $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		3.0	5.4	mA
						Resonator connection		3.2	5.6	mA
				$f_{MX} = 20\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		2.9	5.4	mA
						Resonator connection		3.2	5.6	mA
				$f_{MX} = 10\text{ MHz}$ ^{Note 2} , $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		1.9	3.2	mA
						Resonator connection		1.9	3.2	mA
				$f_{MX} = 10\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		1.9	3.2	mA
						Resonator connection		1.9	3.2	mA
			Subsystem clock operation	$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.0	5.4	μA
						Resonator connection		4.3	5.4	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.0	5.4	μA
						Resonator connection		4.3	5.4	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.1	7.1	μA
						Resonator connection		4.4	7.1	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		4.3	8.7	μA
						Resonator connection		4.7	8.7	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		4.7	12.0	μA
						Resonator connection		5.2	12.0	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		6.4	35.0	μA
						Resonator connection		6.6	35.0	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation ($AMP_{HS1} = 1$). The current flowing into the LCD controller/driver, 16-bit timer KB20, real-time clock 2, 12-bit interval timer, and watchdog timer is not included.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (48 MHz max.)
 3. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)
 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 5. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(TA = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	IDD2 ^{Note 2}	HALT mode	HS (high-speed main) mode ^{Note 7}	fHOCO = 48 MHz ^{Note 4} , fIH = 24 MHz ^{Note 4}	VDD = 5.0 V		0.71	2.55	mA
					VDD = 3.0 V		0.71	2.55	mA
				fHOCO = 24 MHz ^{Note 4} , fIH = 24 MHz ^{Note 4}	VDD = 5.0 V		0.49	1.95	mA
					VDD = 3.0 V		0.49	1.95	mA
				fHOCO = 16 MHz ^{Note 4} , fIH = 16 MHz ^{Note 4}	VDD = 5.0 V		0.43	1.50	mA
			VDD = 3.0 V			0.43	1.50	mA	
			HS (high-speed main) mode ^{Note 7}	fMX = 20 MHz ^{Note 3} , VDD = 5.0 V	Square wave input		0.31	1.76	mA
					Resonator connection		0.48	1.92	mA
				fMX = 20 MHz ^{Note 3} , VDD = 3.0 V	Square wave input		0.29	1.76	mA
					Resonator connection		0.48	1.92	mA
		fMX = 10 MHz ^{Note 3} , VDD = 5.0 V		Square wave input		0.20	0.96	mA	
				Resonator connection		0.28	1.07	mA	
		fMX = 10 MHz ^{Note 3} , VDD = 3.0 V		Square wave input		0.19	0.96	mA	
				Resonator connection		0.28	1.07	mA	
		Subsystem clock operation	fSUB = 32.768 kHz ^{Note 5} , TA = −40°C	Square wave input		0.34	0.62	μA	
				Resonator connection		0.51	0.80	μA	
			fSUB = 32.768 kHz ^{Note 5} , TA = +25°C	Square wave input		0.38	0.62	μA	
				Resonator connection		0.57	0.80	μA	
	fSUB = 32.768 kHz ^{Note 5} , TA = +50°C		Square wave input		0.46	2.30	μA		
			Resonator connection		0.67	2.49	μA		
	fSUB = 32.768 kHz ^{Note 5} , TA = +70°C		Square wave input		0.65	4.03	μA		
			Resonator connection		0.91	4.22	μA		
	fSUB = 32.768 kHz ^{Note 5} , TA = +85°C		Square wave input		1.00	8.04	μA		
			Resonator connection		1.31	8.23	μA		
fSUB = 32.768 kHz ^{Note 5} , TA = +105°C	Square wave input		3.05	27.00	μA				
	Resonator connection		3.24	27.00	μA				
IDD3 ^{Note 6}	STOP mode ^{Note 8}	TA = −40°C					0.18	0.52	μA
		TA = +25°C					0.24	0.52	μA
		TA = +50°C					0.33	2.21	μA
		TA = +70°C					0.53	3.94	μA
		TA = +85°C					0.93	7.95	μA
		TA = +105°C					2.91	25.00	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped.
When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the real-time clock 2 is included. The current flowing into the clock output/buzzer output, 12-bit interval timer, and watchdog timer is not included.
 6. The current flowing into the real-time clock 2, clock output/buzzer output, 12-bit interval timer, and watchdog timer is not included.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (48 MHz max.)
 3. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)
 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(TA = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} ^{Note 1}						0.20		μA
RTC2 operating current	I _{RTC} ^{Notes 1, 2, 3}	f _{SUB} = 32.768 kHz					0.02		μA
12-bit interval timer operating current	I _{TMKA} ^{Notes 1, 2, 4}						0.04		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 2, 5}	f _{IL} = 15 kHz					0.22		μA
A/D converter operating current	I _{ADC} ^{Notes 1, 6}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V				1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V				0.5	0.7	mA
A/D converter reference voltage current	I _{ADREF} ^{Note 1}						75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}						75.0		μA
LVD operating current	I _{LVD} ^{Notes 1, 7}						0.08		μA
Comparator operating current	I _{CMP} ^{Notes 1, 11}	V _{DD} = 5.0 V, Regulator output voltage = 2.1 V	Window mode				12.5		μA
			Comparator high-speed mode				6.5		μA
			Comparator low-speed mode				1.7		μA
		V _{DD} = 5.0 V, Regulator output voltage = 1.8 V	Window mode				8.0		μA
			Comparator high-speed mode				4.0		μA
			Comparator low-speed mode				1.3		μA
Self-programming operating current	I _{FSP} ^{Notes 1, 9}						2.00	12.20	mA
BGO operating current	I _{BGO} ^{Notes 1, 8}						2.00	12.20	mA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	While the mode is shifting ^{Note 10}				0.50	0.60	mA
			During A/D conversion, in low voltage mode, AV _{REFP} = V _{DD} = 3.0 V				1.20	1.44	mA
		CSI/UART operation							0.70
LCD operating current	I _{LCD1} ^{Notes 1, 12, 13}	External resistance division method	f _{LCD} = f _{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V _{DD} = 5.0 V, V _{L4} = 5.0 V		0.04	0.20.	μA
					V _{DD} = 3.0 V, V _{L4} = 3.0 V (V _{LCD} = 04H)		0.85	2.20	μA
	I _{LCD2} ^{Note 1, 12}	Internal voltage boosting method	f _{LCD} = f _{SUB} LCD clock = 128 Hz	1/3 bias, four time slices		V _{DD} = 5.0 V, V _{L4} = 5.1 V (V _{LCD} = 12H)		1.55	3.70
					I _{LCD3} ^{Note 1, 12}	Capacitor split method	f _{LCD} = f _{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V _{DD} = 3.0 V, V _{L4} = 3.0 V

(Notes and Remarks are listed on the next page.)

Notes 1. Current flowing to V_{DD} .

2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The value of the current for the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock 2 operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of real-time clock 2.
4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The value of the current for the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{TMKA} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.
6. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
7. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. For shift time to the SNOOZE mode, see **21.3.3 SNOOZE mode** in the RL78/L13 User's Manual.
11. Current flowing only to the comparator circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{CMP} when the comparator circuit operates.
12. Current flowing only to the LCD controller/driver. The value of the current for the RL78 microcontrollers is the sum of the supply current (I_{DD1} or I_{DD2}) and LCD operating current (I_{LCD1} , I_{LCD2} , or I_{LCD3}), when the LCD controller/driver operates in operation mode or HALT mode. However, not including the current flowing into the LCD panel. Conditions of the TYP. value and MAX. value are as follows.
 - Setting 20 pins as the segment function and blinking all
 - Selecting f_{SUB} for system clock when LCD clock = 128 Hz (LCDC0 = 07H)
 - Setting four time slices and 1/3 bias
13. Not including the current flowing into the external division resistor when using the external resistance division method.

Remarks 1. f_{IL} : Low-speed on-chip oscillator clock frequency

2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK} : CPU/peripheral hardware clock frequency

4. The temperature condition for the TYP. value is $T_A = 25^{\circ}\text{C}$.

3.4 AC Characteristics

(T_A = -40 to $+105^\circ\text{C}$, 2.4 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f _{SUB}) operation		2.4 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
	f _{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} +10			ns
TO00 to TO07, TKBO00 ^{Note} , TKBO01-0 to TKBO01-2 ^{Note} output frequency	f _{TO}	HS (high-speed main) mode	4.0 V ≤ V _{DD} ≤ 5.5 V				12	MHz
			2.7 V ≤ V _{DD} < 4.0 V				8	MHz
			2.4 V ≤ V _{DD} < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ V _{DD} ≤ 5.5 V				16	MHz
			2.7 V ≤ V _{DD} < 4.0 V				8	MHz
			2.4 V ≤ V _{DD} < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0 to INTP7	2.4 V ≤ V _{DD} ≤ 5.5 V		1			μs
Key interrupt input high-level width, low-level width	t _{KRH} , t _{KRL}	KR0 to KR7	2.4 V ≤ V _{DD} ≤ 5.5 V		250			ns
IH-PWM output restart input high-level width	t _{IHR}	INTP0 to INTP7			2			f _{CLK}
TMKB2 forced output stop input high-level width	t _{IHR}	INTP0 to INTP2			2			f _{CLK}
RESET low-level width	t _{RSL}				10			μs

(Note and Remark are listed on the next page.)

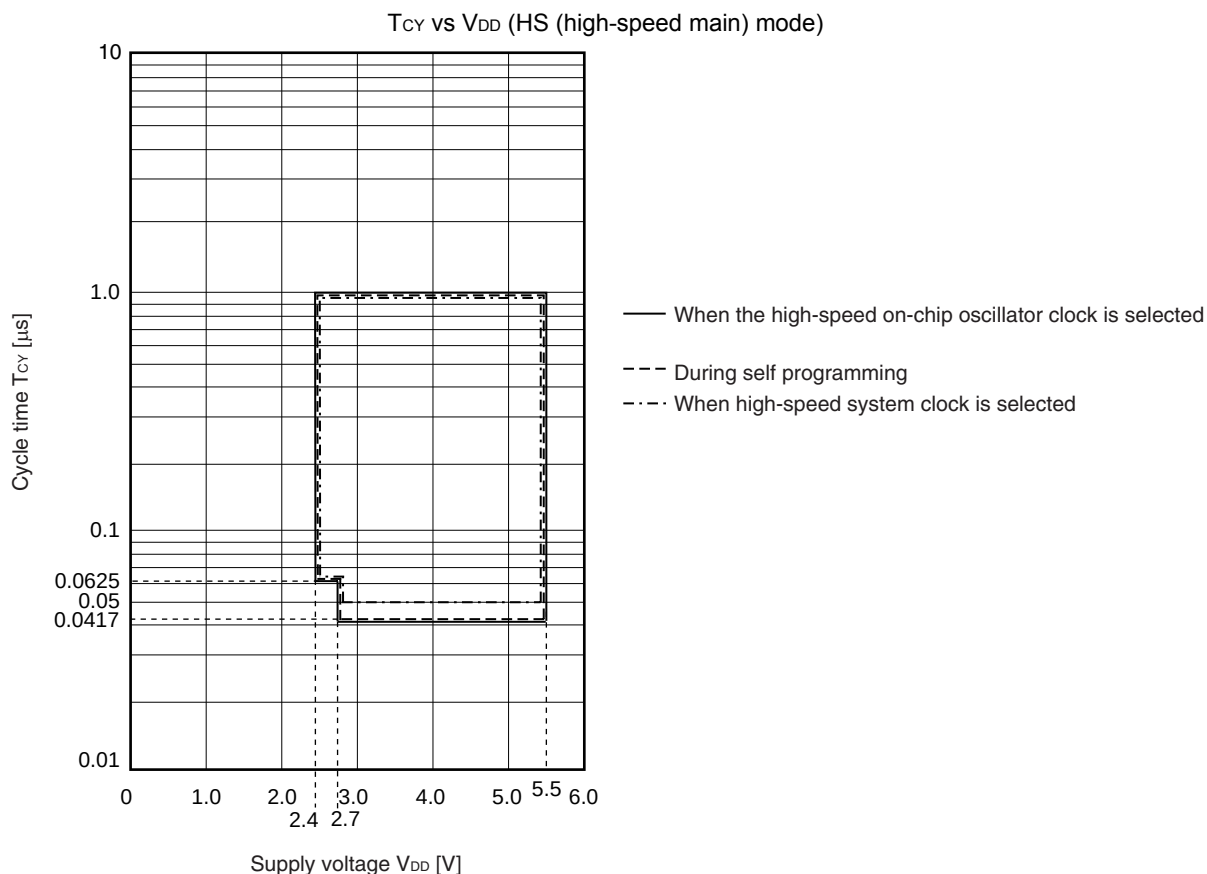
Note Specification under conditions where the duty factor is 50%.

Remark f_{MCK} : Timer array unit operation clock frequency

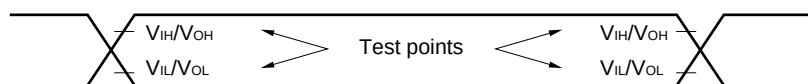
(Operation clock to be set by the CKS_{mn0}, CKS_{mn1} bits of timer mode register mn (TMR_{mn})

m: Unit number (m = 0), n: Channel number (n = 0 to 7))

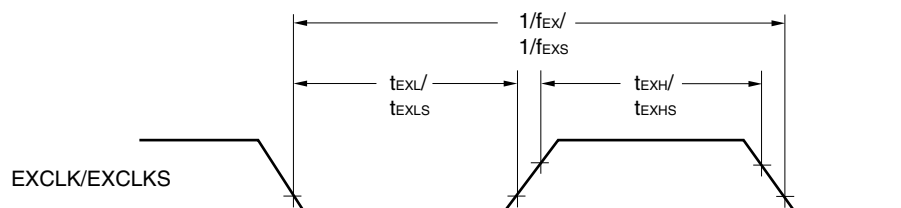
Minimum Instruction Execution Time during Main System Clock Operation

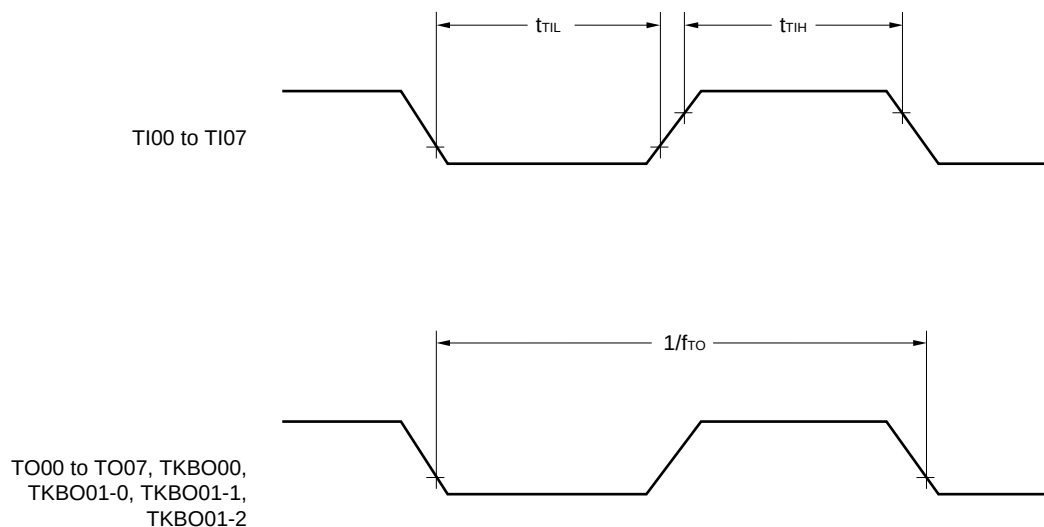
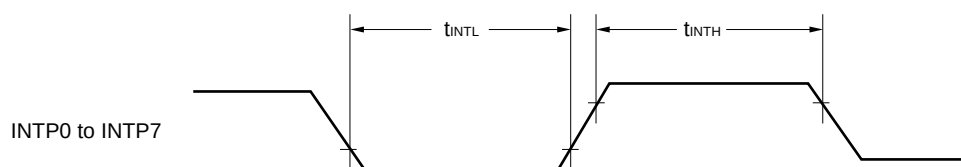
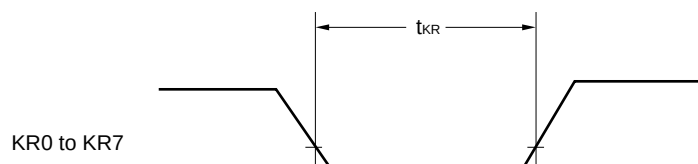
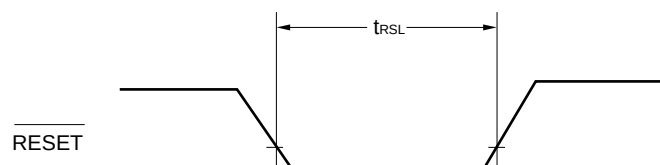


AC Timing Test Points



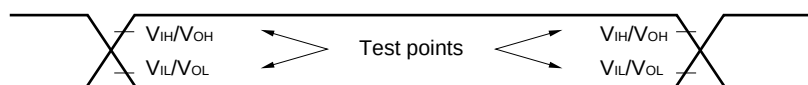
External System Clock Timing



TI/TO Timing**Interrupt Request Input Timing****Key Interrupt Input Timing** **$\overline{\text{RESET}}$ Input Timing**

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

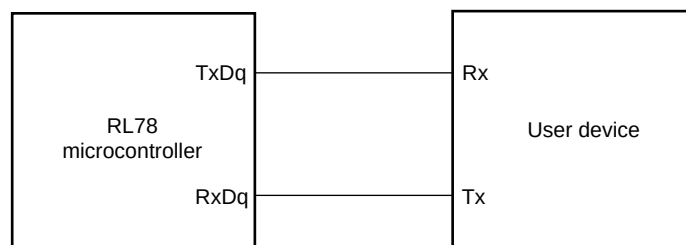
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate ^{Note}				$f_{MCK}/12$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps

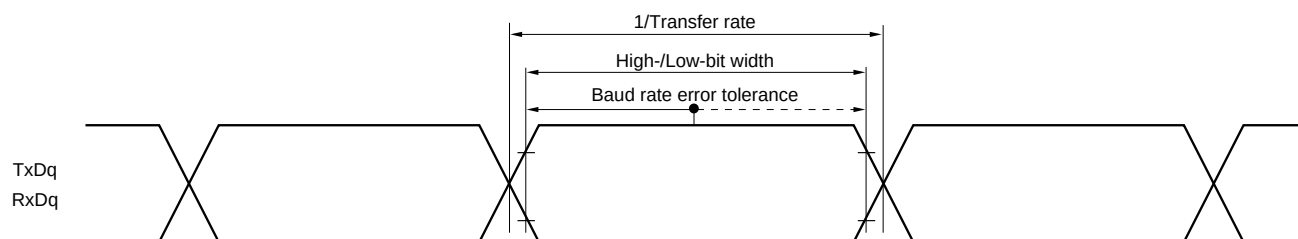
Note Transfer rate in the SNOOZE mode is 4800 bps only.

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



- Remarks**
1. q: UART number ($q = 0$ to 3), g: PIM and POM number ($g = 0, 1, 3$)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	334 ^{Note 1}		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	500 ^{Note 1}		ns
SCKp high-/low-level width	t_{KH1} , t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 24$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 36$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 76$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	113		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 3}	t_{KSI1}		38		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 4}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 5}		50	ns

Notes 1. The value must also be equal to or more than $4/f_{CLK}$.**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp $\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp $\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**5.** C is the load capacitance of the SCKp and SOp output lines.**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remarks 1.** p: CSI number (p = 00, 10), m: Unit number (m = 0), n: Channel number (n = 0, 2),
g: PIM and POM numbers (g = 0, 1)**2.** f_{MCK} : Serial array unit operation clock frequency(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 02))

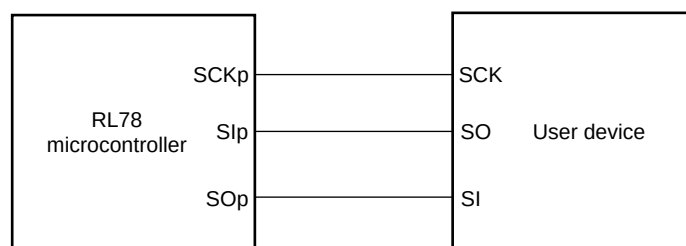
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 5}	t_{KCY2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$f_{MCK} > 20\text{ MHz}$	$16/f_{MCK}$		ns
			$f_{MCK} \leq 20\text{ MHz}$	$12/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$f_{MCK} > 16\text{ MHz}$	$16/f_{MCK}$		ns
			$f_{MCK} \leq 16\text{ MHz}$	$12/f_{MCK}$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$12/f_{MCK}$ and 1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-14$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-16$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-36$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK2}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK}+40$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK}+60$		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 2}	t_{KSI2}			$1/f_{MCK}+62$		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 3}	t_{KSO2}	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK}+66$	ns
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK}+113$	ns

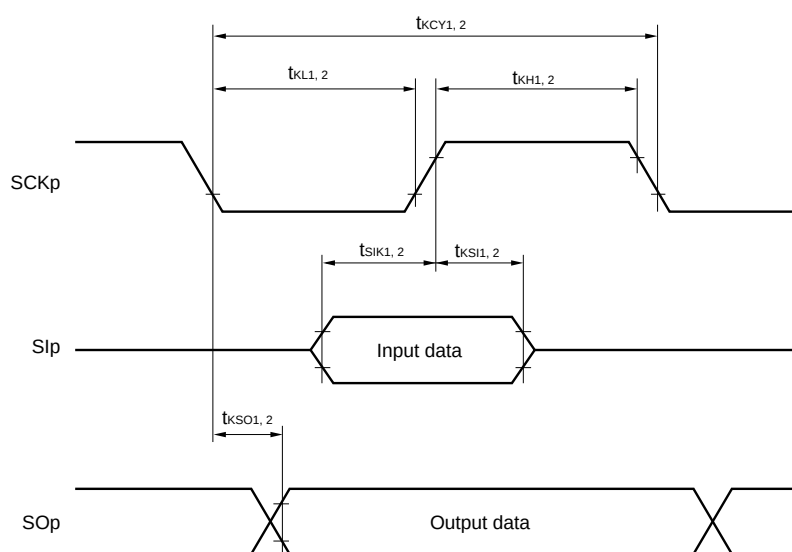
- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp $\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp $\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

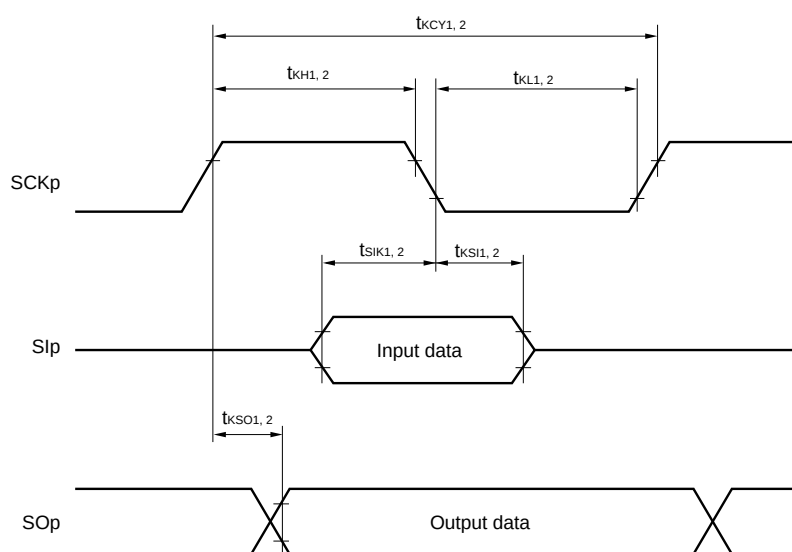
- Remarks**
1. p: CSI number (p = 00, 10), m: Unit number (m = 0), n: Channel number (n = 0, 2),
g: PIM number (g = 0, 1)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 02))

CSI mode connection diagram (during communication at same potential)**CSI mode serial transfer timing (during communication at same potential)**

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

**CSI mode serial transfer timing (during communication at same potential)**

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 10)
 2. m: Unit number, n: Channel number (mn = 00, 02)

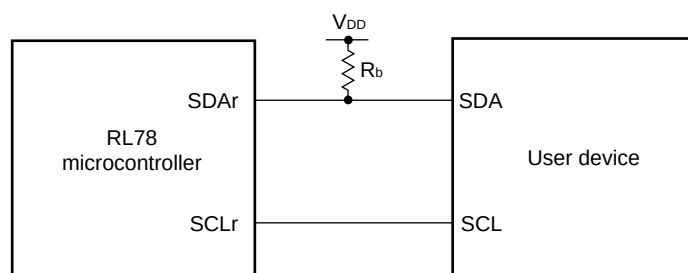
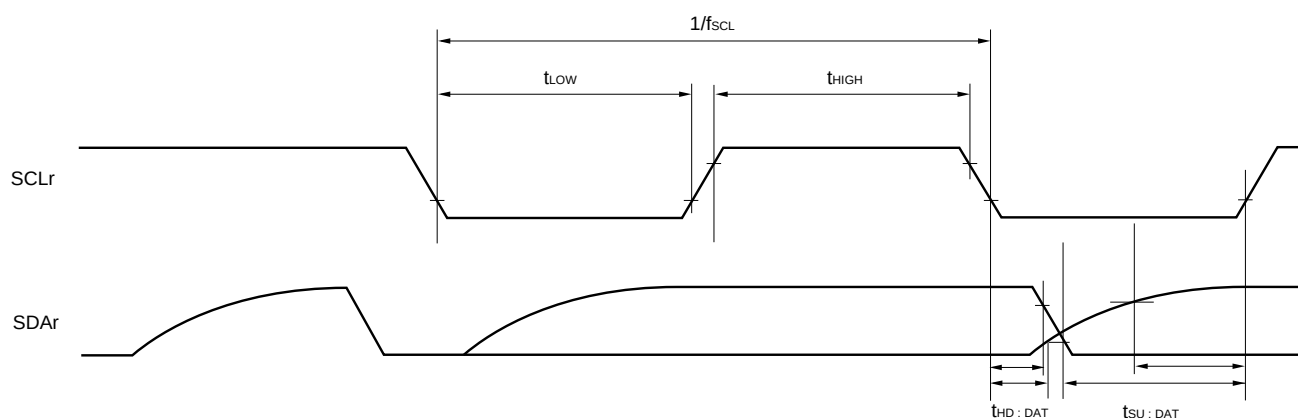
(4) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 220$ ^{Note 2}		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ ^{Note 2}		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	1420	ns

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 2. r: IIC number (r = 00, 10), g: PIM and POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0-3), mn = 00-03, 10-13)

<R>

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Reception			
		4.0 V $\leq V_{DD} \leq 5.5\text{ V}$, 2.7 V $\leq V_b \leq 4.0\text{ V}$		$f_{MCK}/12^{\text{Note}}$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps
		2.7 V $\leq V_{DD} < 4.0\text{ V}$, 2.3 V $\leq V_b \leq 2.7\text{ V}$		$f_{MCK}/12^{\text{Note}}$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps
		2.4 V $\leq V_{DD} < 3.3\text{ V}$, 1.6 V $\leq V_b \leq 2.0\text{ V}$		$f_{MCK}/12^{\text{Note}}$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps

Note Transfer rate in SNOOZE mode is 4800 bps only.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $V_b[\text{V}]$: Communication line voltage
 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V	2.0 ^{Note 2}	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V	1.2 ^{Note 4}	Mbps
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V	0.43 ^{Note 6}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Notes 5. The smaller maximum transfer rate derived by using $f_{\text{MCK}}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq V_{\text{DD}} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

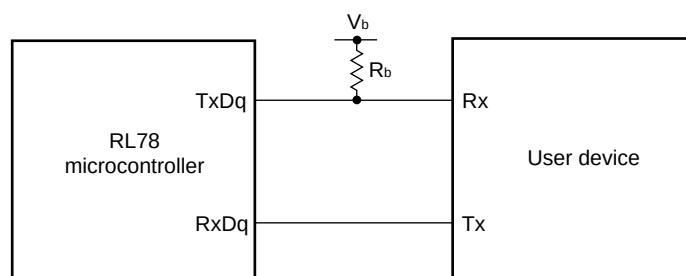
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

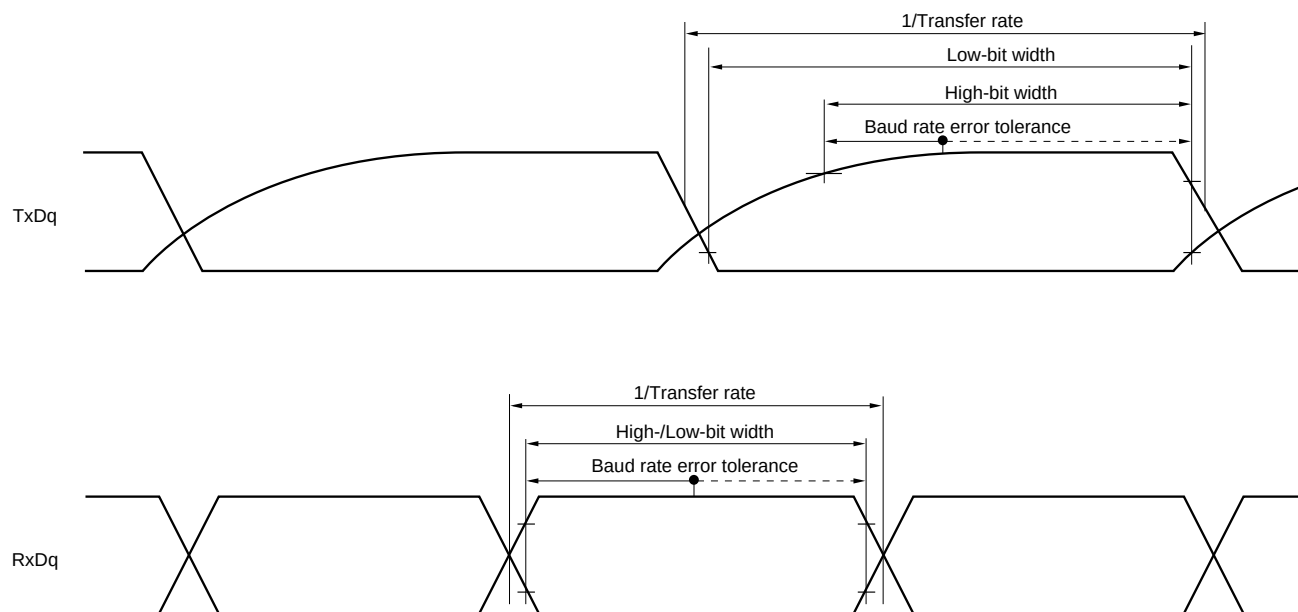
* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

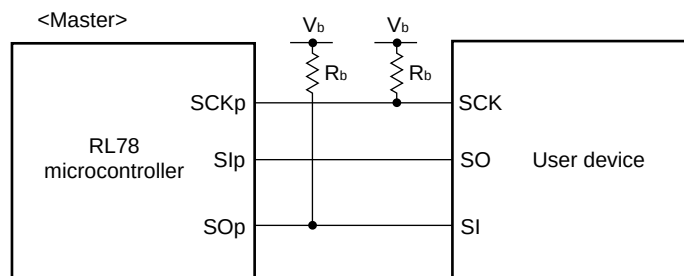
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$ $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	600		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1000		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 1.8\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	2300		ns
SCKp high-level width	t_{KH1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 150$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 340$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{KCY1}/2 - 916$		ns
SCKp low-level width	t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 24$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 36$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{KCY1}/2 - 100$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 1}	t_{SH1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		966	ns

(Note, Caution and Remark are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	88		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	88		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	220		ns
Slp hold time (from SCKp↓) ^{Note 2}	t_{KSI1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp↑ to SOp output ^{Note 2}	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		50	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		50	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		50	ns

CSI mode connection diagram (during communication at different potential)

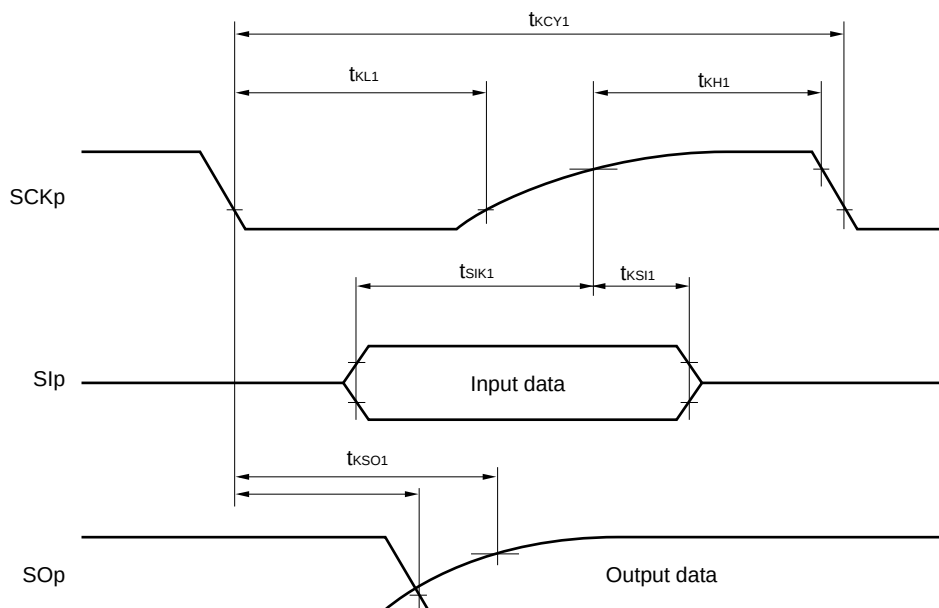


- Notes**
1. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$.
 2. When $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.

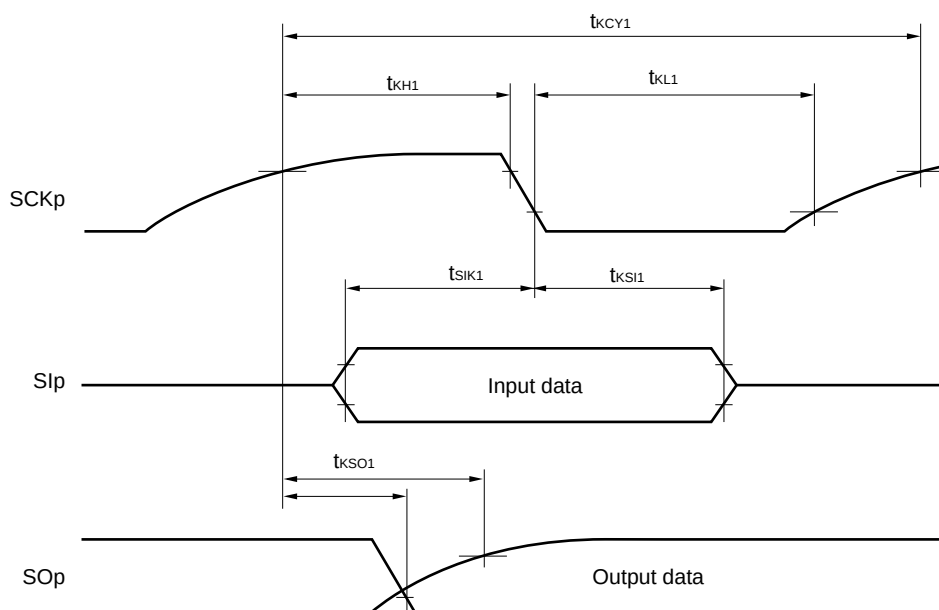
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02),
g: PIM and POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

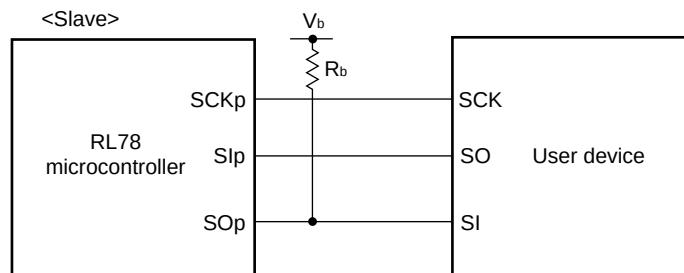


Remark p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02),
g: PIM and POM number (g = 0, 1)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time ^{Note 1}	t_{KCY2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$20\text{ MHz} < f_{MCK}$	$24/f_{MCK}$	ns
			$8\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$20/f_{MCK}$	ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$	ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$20\text{ MHz} < f_{MCK}$	$32/f_{MCK}$	ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$28/f_{MCK}$	ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$24/f_{MCK}$	ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$	ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$20\text{ MHz} < f_{MCK}$	$72/f_{MCK}$	ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$64/f_{MCK}$	ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$52/f_{MCK}$	ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$32/f_{MCK}$	ns
			$f_{MCK} \leq 4\text{ MHz}$	$20/f_{MCK}$	ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$t_{KCY2}/2 - 24$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$t_{KCY2}/2 - 36$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$t_{KCY2}/2 - 100$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 2}	t_{SIK2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$1/f_{MCK} + 40$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$1/f_{MCK} + 40$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$1/f_{MCK} + 60$		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 3}	t_{KSI2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$1/f_{MCK} + 62$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$1/f_{MCK} + 62$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$1/f_{MCK} + 62$		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 4}	t_{KSO2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		$2/f_{MCK} + 240$	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		$2/f_{MCK} + 428$	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		$2/f_{MCK} + 1146$	ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

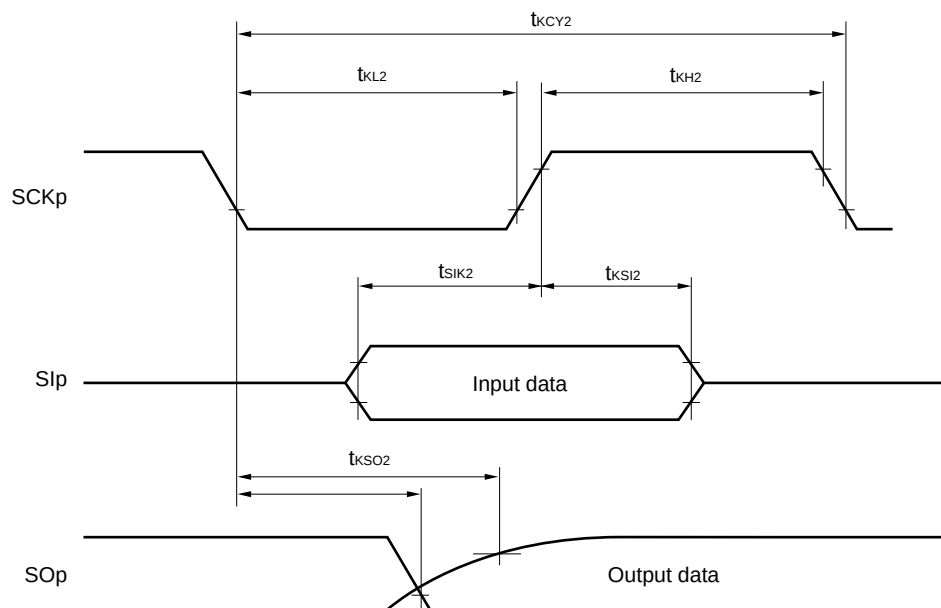
CSI mode connection diagram (during communication at different potential)

Notes 1. Transfer rate in SNOOZE mode: MAX. 1 Mbps

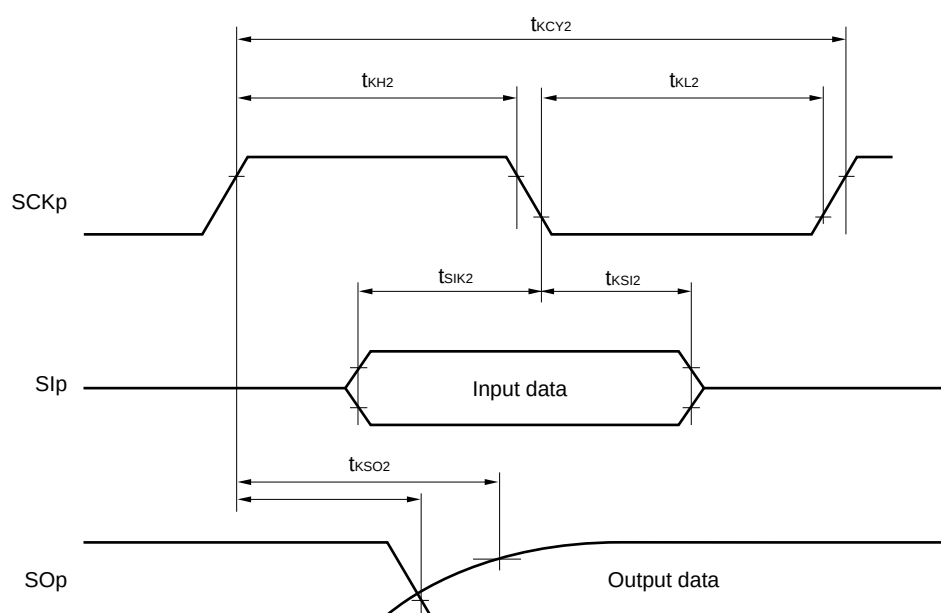
2. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The SIp setup time becomes “to SCKp↓” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
3. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The SIp hold time becomes “from SCKp↓” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
4. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from SCKp↑” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
- 2.** p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02), g: PIM and POM number (g = 0, 1)
- 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn)
 m: Unit number, n: Channel number (mn = 00, 02))

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$		100 ^{Note 1}	kHz
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		100 ^{Note 1}	kHz
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	4600		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	4600		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	4650		ns
Hold time when SCLr = "H"	t_{HIGH}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	620		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b < 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	500		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	2700		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	2400		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	1830		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

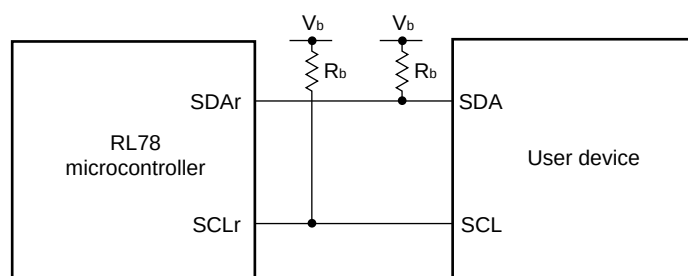
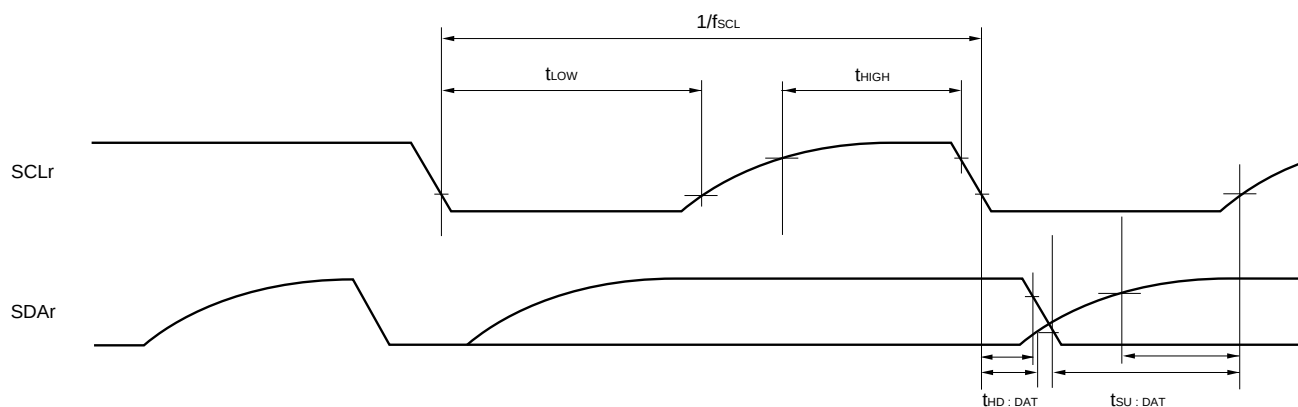
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 340$ ^{Note 2}		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 340$ ^{Note 2}		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	$1/f_{MCK} + 760$ ^{Note 2}		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 760$ ^{Note 2}		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$1/f_{MCK} + 570$ ^{Note 2}		ns
Data hold time (transmission)	$t_{HD:DAT}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	0	1420	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	1420	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	0	1215	ns

Notes 1. The value must also be equal to or less than $f_{MCK}/4$.**2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

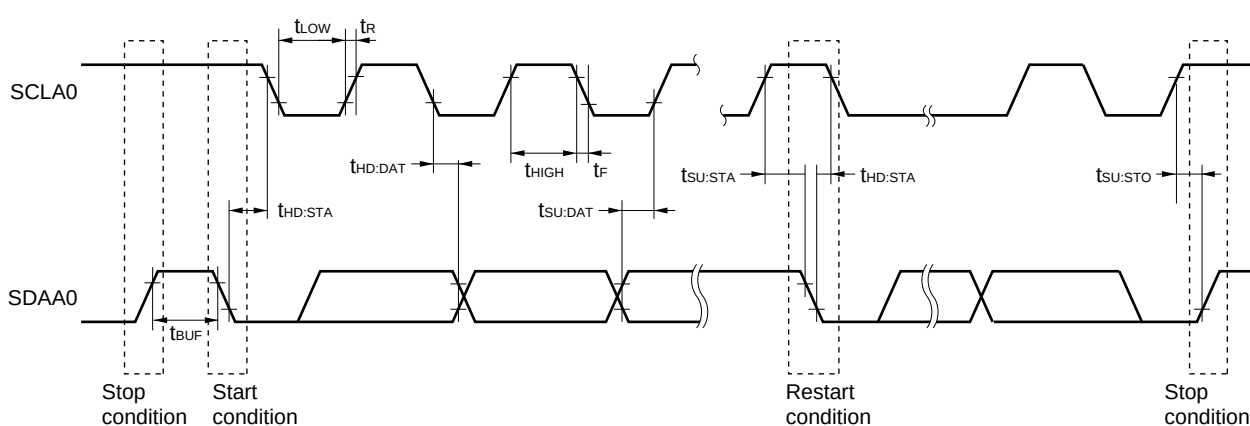
3.5.2 Serial interface IICA

(T_A = -40 to $+105^\circ\text{C}$, 2.4 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	–	–	0	400	kHz
		Normal mode: f _{CLK} ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0 ^{Note 3}	3.45	0 ^{Note 3}	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Remark** The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.Standard mode: C_b = 400 pF, R_b = 2.7 k Ω Fast mode: C_b = 320 pF, R_b = 1.1 k Ω

IICA serial transfer timing



3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM}
ANI0, ANI1	—	See 3.6.1 (2).	See 3.6.1 (3).
ANI16 to ANI25	See 3.6.1 (1).		
Internal reference voltage Temperature sensor output voltage	See 3.6.1 (1).		—

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pins: ANI16 to ANI25, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.2	± 5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI16 to ANI25	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		± 0.35	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		± 0.35	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		± 3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		± 2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI25	0		AV_{REFP}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode))	V_{BGR} ^{Note 4}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode))	V_{TMPS25} ^{Note 4}			V

(Notes are listed on the next page.)

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.2\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. See 3.6.2 Temperature sensor/internal reference voltage characteristics.

(2) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pins: ANI0, ANI1, ANI16 to ANI25, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0, ANI1, ANI16 to ANI25	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI0, ANI1, ANI16 to ANI25	0		V_{DD}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode))	V_{BGR} ^{Note 3}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode))	V_{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See 3.6.2 Temperature sensor/internal reference voltage characteristics.

(3) When reference voltage (+) = internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), target pins: ANI0, ANI16 to ANI25

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3},
Reference voltage (–) = AV_{REFM} ^{Note 4} = 0 V , HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See 3.6.2 Temperature sensor/internal reference voltage characteristics.

4. When reference voltage (–) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the AV_{REFM} MAX. value.

Integral linearity error: Add ± 0.5 LSB to the AV_{REFM} MAX. value.

Differential linearity error: Add ± 0.2 LSB to the AV_{REFM} MAX. value.

3.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference output voltage	V_{BGR}	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	t_{AMP}				5	μs

3.6.3 Comparator

(T_A = -40 to $+105^\circ\text{C}$, 2.4 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref		0		V _{DD} – 1.4	V
	Ivcmp		–0.3		V _{DD} + 0.3	V
Output delay	td	V _{DD} = 3.0 V Input slew rate > 50 mV/ μs	Comparator high-speed mode, standard mode		1.2	μs
			Comparator high-speed mode, window mode		2.0	μs
			Comparator low-speed mode, standard mode		3.0	5.0 μs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode, window mode	0.66V _{DD}	0.76V _{DD}	0.86V _{DD}	V
Low-electric-potential reference voltage	VTW–	Comparator high-speed mode, window mode	0.14V _{DD}	0.24V _{DD}	0.34V _{DD}	V
Operation stabilization wait time	t _{CMP}		100			μs
Internal reference output voltage ^{Note}	V _{BGR}	2.4 V $\leq$ V _{DD} $\leq$ 5.5 V, HS (high-speed main) mode	1.38	1.45	1.50	V

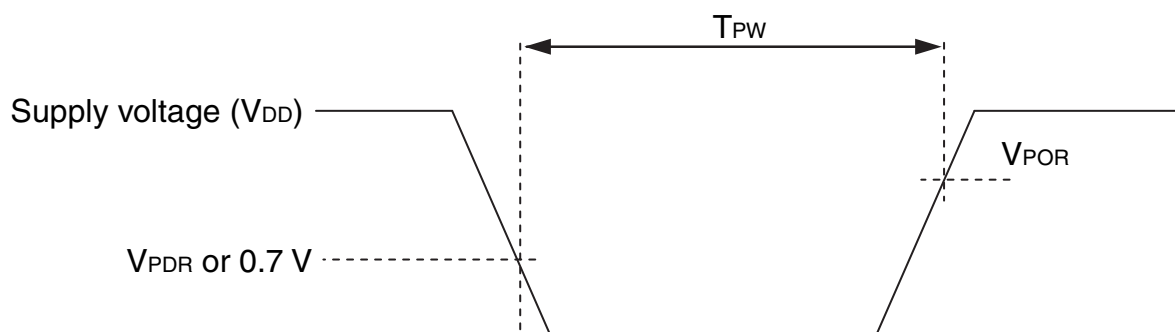
Note Cannot be used in subsystem clock operation and STOP mode.

3.6.4 POR circuit characteristics

(T_A = -40 to $+105^\circ\text{C}$, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{POR}	When power supply rises	1.45	1.51	1.57	V
	V _{PDR}	When power supply falls	1.44	1.50	1.56	V
Minimum pulse width ^{Note}	T _{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset operation when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode and when the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset operation between when V_{DD} falls below 0.7 V and when V_{DD} rises to V_{POR} or higher.



3.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode $(T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V _{LVD0}	When power supply rises	3.90	4.06	4.22	V
			When power supply falls	3.83	3.98	4.13	V
		V _{LVD1}	When power supply rises	3.60	3.75	3.90	V
			When power supply falls	3.53	3.67	3.81	V
		V _{LVD2}	When power supply rises	3.01	3.13	3.25	V
			When power supply falls	2.94	3.06	3.18	V
		V _{LVD3}	When power supply rises	2.90	3.02	3.14	V
			When power supply falls	2.85	2.96	3.07	V
		V _{LVD4}	When power supply rises	2.81	2.92	3.03	V
			When power supply falls	2.75	2.86	2.97	V
		V _{LVD5}	When power supply rises	2.71	2.81	2.92	V
			When power supply falls	2.64	2.75	2.86	V
		V _{LVD6}	When power supply rises	2.61	2.71	2.81	V
			When power supply falls	2.55	2.65	2.75	V
		V _{LVD7}	When power supply rises	2.51	2.61	2.71	V
			When power supply falls	2.45	2.55	2.65	V
Minimum pulse width		t _{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode $(T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVD5}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V _{LVD4}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V _{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.6 Supply voltage rise time

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} rise slope	SV_{DD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

3.7 LCD Characteristics

3.7.1 External resistance division method

(1) Static display mode

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

3.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
LCD output voltage variation range	VL1	C1 to C4 ^{Note 1} = 0.47 μ F ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	VL2	C1 to C4 ^{Note 1} = 0.47 μ F	2 VL1 – 0.10	2 VL1	2 VL1	V	
Tripler output voltage	VL4	C1 to C4 ^{Note 1} = 0.47 μ F	3 VL1 – 0.15	3 VL1	3 VL1	V	
Reference voltage setup time ^{Note 2}	tVWAIT1		5			ms	
Voltage boost wait time ^{Note 3}	tVWAIT2	C1 to C4 ^{Note 1} = 0.47 μ F	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GNDC1 = C2 = C3 = C4 = $0.47\ \mu\text{F} \pm 30\%$

- 2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- 3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V _{L1}	C1 to C5 ^{Note 1} = 0.47 μF ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V _{L2}	C1 to C5 ^{Note 1} = 0.47 μF	2 V _{L1} – 0.08	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L3}	C1 to C5 ^{Note 1} = 0.47 μF	3 V _{L1} – 0.12	3 V _{L1}	3 V _{L1}	V	
Quadruply output voltage	V _{L4}	C1 to C5 ^{Note 1} = 0.47 μF	4 V _{L1} – 0.16	4 V _{L1}	4 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{VWAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{VWAIT2}	C1 to C5 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L3} and GNDC5: A capacitor connected between V_{L4} and GND $C1 = C2 = C3 = C4 = C5 = 0.47\ \mu\text{F} \pm 30\%$

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3.7.3 Capacitor split method**(1) 1/3 bias method****($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_D \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 $= 0.47\ \mu\text{F}$ ^{Note 2}		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 $= 0.47\ \mu\text{F}$ ^{Note 2}	$\frac{2}{3} V_{L4} - 0.1$	$\frac{2}{3} V_{L4}$	$\frac{2}{3} V_{L4} + 0.1$	V
V_{L1} voltage	V_{L1}	C1 to C4 $= 0.47\ \mu\text{F}$ ^{Note 2}	$\frac{1}{3} V_{L4} - 0.1$	$\frac{1}{3} V_{L4}$	$\frac{1}{3} V_{L4} + 0.1$	V
Capacitor split wait time ^{Note 1}	t_{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GND $C1 = C2 = C3 = C4 = 0.47\ \mu\text{F} \pm 30\%$

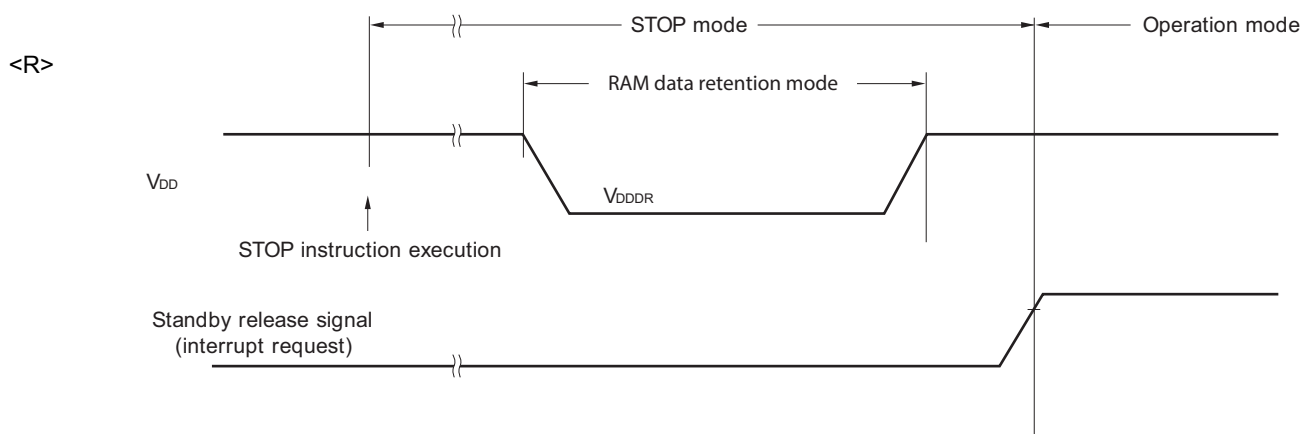
3.8 RAM Data Retention Characteristics

<R>

 $(T_A = -40$ to $+105^\circ\text{C})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.9 Flash Memory Programming Characteristics

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	2.4 V ≤ VDD ≤ 5.5 V	1		24	MHz
Number of code flash rewrites ^{Note 1, 2, 3}	Cenwr	Retained for 20 years TA = 85°C ^{Note 4}	1,000			Times
Number of data flash rewrites ^{Note 1, 2, 3}		Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C ^{Note 4}	100,000			
		Retained for 20 years TA = 85°C ^{Note 4}	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

4. This temperature is the average value at which data are retained.

Remark When updating data multiple times, use the flash memory as one for updating data.

3.10 Dedicated Flash Memory Programmer Communication (UART)

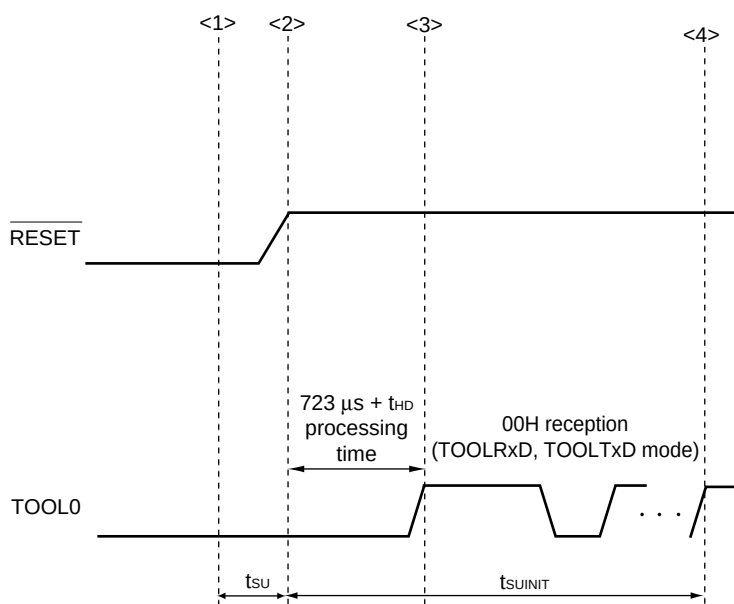
 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.11 Timing Specifications for Switching Flash Memory Programming Modes

(T_A = -40 to $+105^\circ\text{C}$, 2.4 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t _{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t _{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t _{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and completion the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

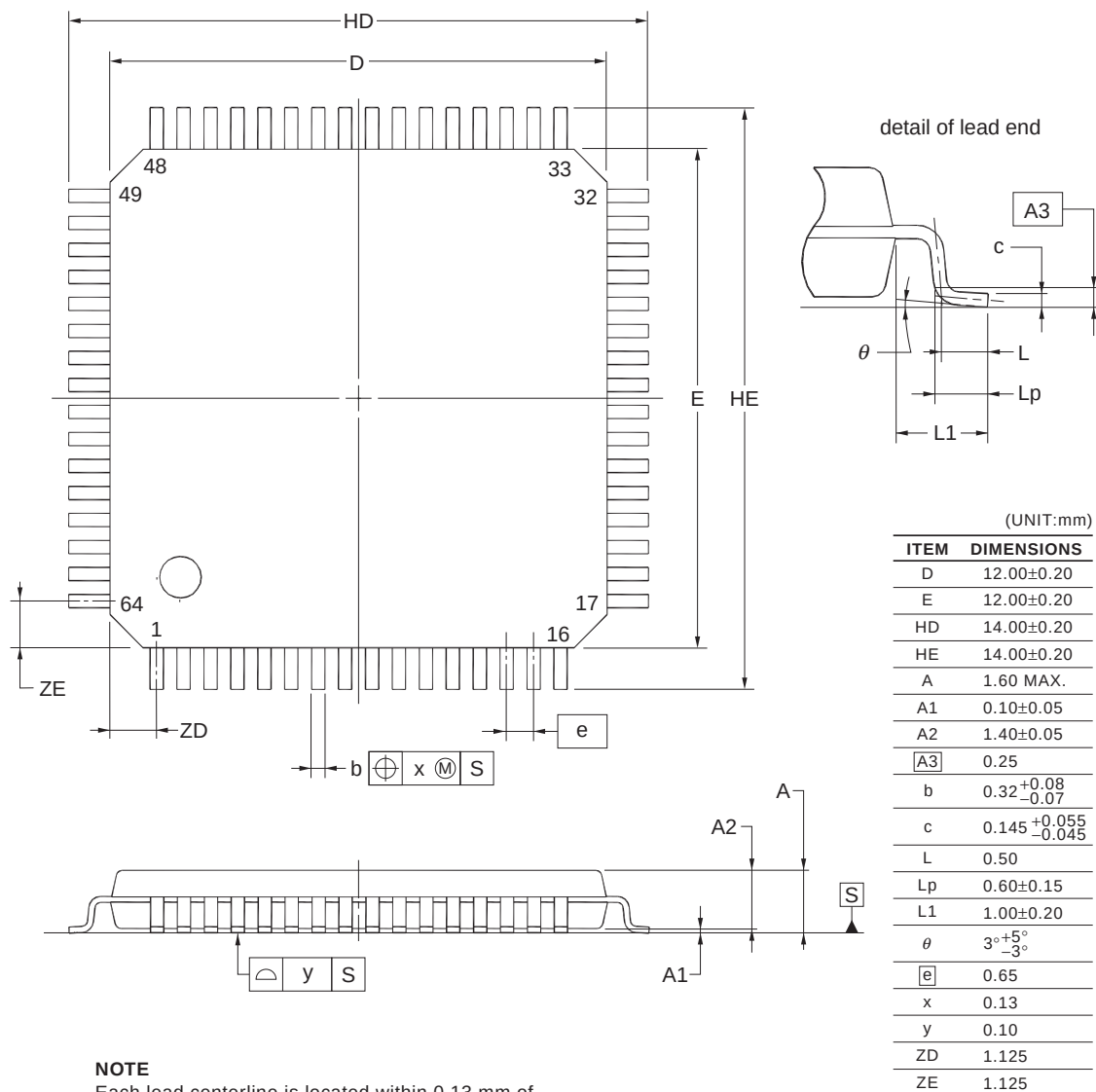
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

4. PACKAGE DRAWINGS

4.1 64-pin Products

R5F10WLAFA, R5F10WLCAFA, R5F10WLDAFA, R5F10WLEAFA, R5F10WLFafa, R5F10WLGafa

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

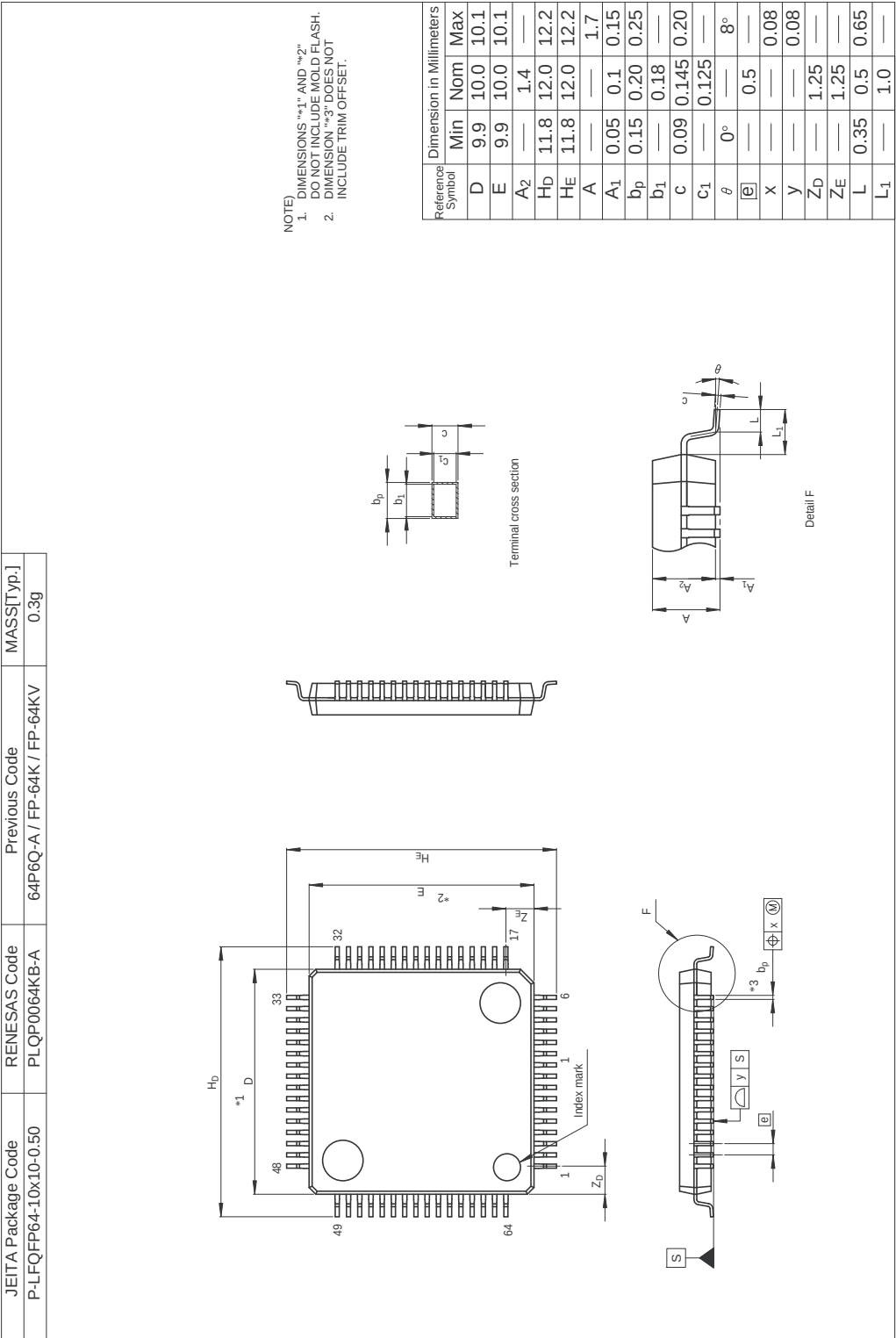


NOTE

Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

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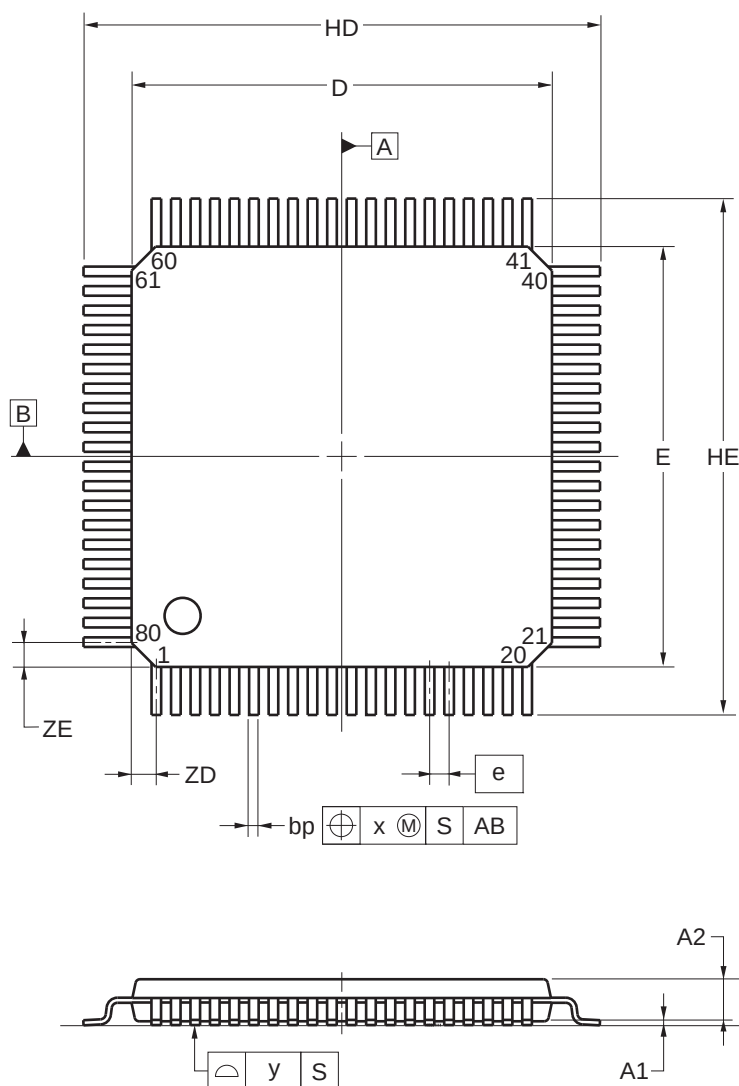
R5F10WLAAFB, R5F10WLCAFB, R5F10WLDAFB, R5F10WLEAFB, R5F10WLFAFB, R5F10WLGAFB,
R5F10WLAGFB, R5F10WLCGFB, R5F10WLDGFB, R5F10WLEGFB, R5F10WLFGB, R5F10WLGGB



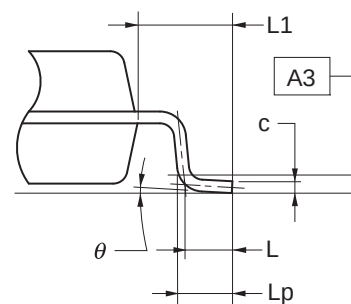
4.2 80-pin Products

R5F10WMAAFA, R5F10WMCAFA, R5F10WMDAFA, R5F10WMEAFA, R5F10WMFAFA, R5F10WMGAFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69

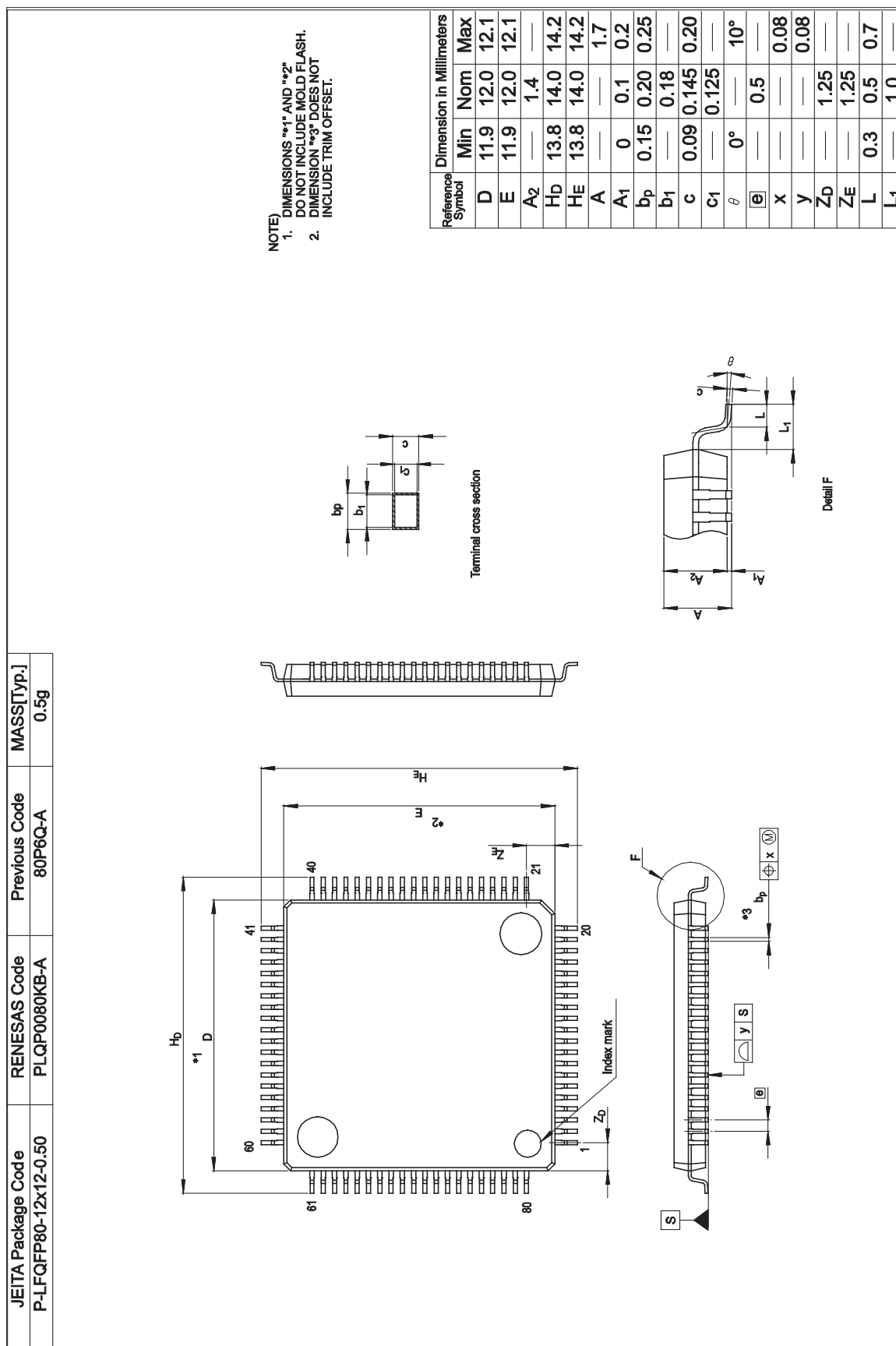


detail of lead end



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.80	14.00	14.20
E	13.80	14.00	14.20
HD	17.00	17.20	17.40
HE	17.00	17.20	17.40
A	—	—	1.70
A1	0.05	0.125	0.20
A2	1.35	1.40	1.45
A3	—	0.25	—
bp	0.26	0.32	0.38
c	0.10	0.145	0.20
L	—	0.80	—
Lp	0.736	0.886	1.036
L1	1.40	1.60	1.80
	0°	3°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
ZD	—	0.825	—
ZE	—	0.825	—

R5F10WMAAFB, R5F10WMCAFB, R5F10WMDAFB, R5F10WMEAFB, R5F10WMFAFB, R5F10WMGAFB,
R5F10WMAGFB, R5F10WMCGB, R5F10WMDGB, R5F10WMEGB, R5F10WMFGB, R5F10WMGGB



Revision History	RL78/L13 Data Sheet
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Rev.	Date	Description	
		Page	Summary
0.01	Apr 13, 2012	-	First Edition issued
0.02	Oct 31, 2012	-	Change of the number of segment pins • 64-pin products: 36 pins • 80-pin products: 51 pins
2.10	Aug 12, 2016	1	Modification of features of 16-bit timer and 16-bit timer KB20 (IH) in 1.1 Features
		5	Addition of product name (RL78/L13) and description (Top View) in 1.3.1 64-pin products
		6	Addition of product name (RL78/L13) and description (Top View) in 1.3.2 80-pin products
		10	Modification of functional overview of main system clock in 1.6 Outline of Functions
		15	Modification of description in Absolute Maximum Ratings (3/3)
		17, 18	Modification of description in 2.3.1 Pin characteristics
		38	Modification of remark 3 in 2.5.1 (4) During communication at same potential (simplified I ² C mode)
		68	Modification of the title and note, and addition of caution in 2.8 RAM Data Retention Characteristics
		70	Addition of Remark
		74	Modification of description in Absolute Maximum Ratings (T _A = 25 °C) (3/3)
		76	Modification of description in 3.3.1 Pin characteristics
		95	Modification of remark 3 in 3.5.1 (4) During communication at same potential (simplified I ² C mode)
		118	Modification of the title and note, and addition of caution in 3.8 RAM Data Retention Characteristics

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- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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