

PIN-CONTROLLED 1–711 MHz JITTER CLEANING CLOCK

Features

- Provides jitter attenuation for any clock frequency
- One clock input / two clock outputs
- Input/output frequency range: 1–711 MHz
- Ultra low jitter: 300 fs (12 kHz–20 MHz) typical
- Simple pin control interface
- Selectable loop bandwidth for jitter attenuation: 60 Hz–8.4 kHz
- Meets OC-192 GR-253-CORE jitter specifications
- Selectable output clock signal format: LVPECL, LVDS, CML or CMOS
- Single supply: 1.8, 2.5, or 3.3 V
- Loss of lock and loss of signal alarms
- VCO freeze during LOS/LOL
- On-chip voltage regulator with high PSRR
- Small size: 6 x 6 mm, 36-QFN
- Wide temperature range: –40 to +85 °C

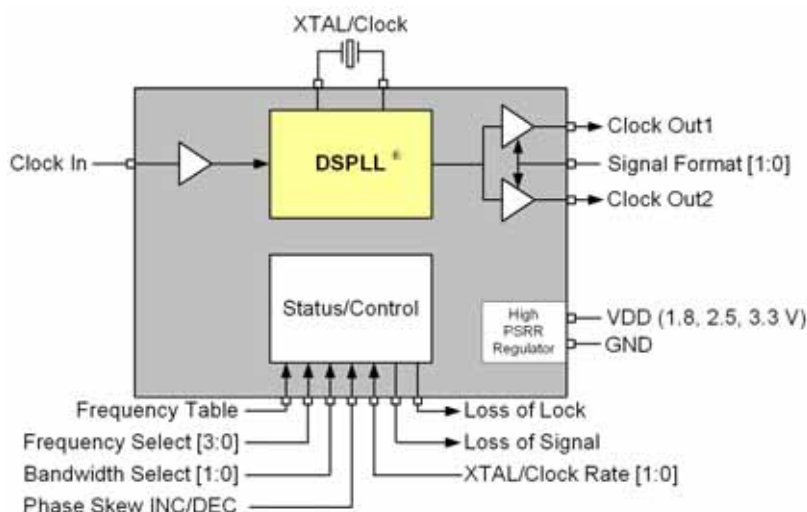
Applications

- Data converter clocking
- Wireless infrastructure
- Networking, SONET/SDH
- Switches and routers
- Medical instrumentation
- Test and measurement

Description

The Si5317 is a flexible 1:1 jitter cleaning clock for high-performance applications that require jitter attenuation without clock multiplication. The Si5317 accepts a single clock input ranging from 1 to 711 MHz and generates two low jitter clock outputs at the same frequency. The clock frequency range and loop bandwidth are selectable from a simple look-up table. The Si5317 is based on Silicon Laboratories' 3rd-generation DSPLL[®] technology, which provides jitter attenuation on any frequency in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is user selectable, providing jitter performance optimization at the application level.

Functional Block Diagram



Ordering Information:

See page 40.

Pin Assignments

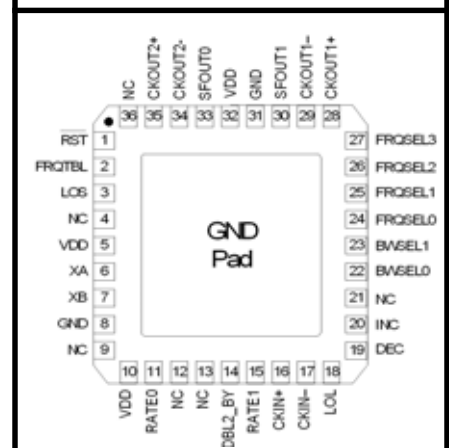


TABLE OF CONTENTS

| <u>Section</u> | <u>Page</u> |
|---|--------------------|
| 1. Electrical Specifications | 4 |
| 1.1. Three-Level (3L) Input Pins (No External Resistors) | 9 |
| 1.2. Three-Level Input Pins (Example with External Resistors) | 9 |
| 2. Functional Description | 14 |
| 2.1. Overview | 14 |
| 3. Frequency Plan Tables | 15 |
| 3.1. Frequency Range Plan | 15 |
| 3.2. Output Skew Adjustment | 15 |
| 3.3. PLL Self-Calibration | 22 |
| 3.4. Alarms | 23 |
| 3.5. VCO Freeze | 23 |
| 3.6. PLL Bypass Mode | 24 |
| 4. High-Speed I/O | 25 |
| 4.1. Input Clock Buffer | 25 |
| 4.2. Output Clock Driver | 27 |
| 5. Crystal/Reference Clock Input | 29 |
| 5.1. Crystal/Reference Clock Selection | 30 |
| 6. Power Supply Filtering | 33 |
| 7. Typical Phase Noise Plots | 34 |
| 7.1. Example: SONET OC-192 | 34 |
| 8. Typical Application Circuit | 35 |
| 9. Pin Descriptions: Si5317 | 36 |
| 10. Ordering Guide | 40 |
| 11. Package Outline: 36-Pin QFN | 41 |
| 12. Recommended PCB Layout | 42 |
| 13. Si5317 Device Top Mark | 44 |
| Document Change List | 45 |
| Contact Information | 46 |

1. Electrical Specifications

Table 1. Recommended Operating Conditions
 $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------|----------|----------------|------|-----|------|------------------|
| Temperature Range | T_A | | -40 | 25 | 85 | $^\circ\text{C}$ |
| Supply Voltage | V_{DD} | 3.3 V nominal | 2.97 | 3.3 | 3.63 | V |
| | | 2.5 V nominal | 2.25 | 2.5 | 2.75 | V |
| | | 1.8 V nominal | 1.71 | 1.8 | 1.89 | V |

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 $^\circ\text{C}$ unless otherwise noted.

Table 2. DC Characteristics
 $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|----------|--|-----|-----|-----|-------|
| Supply Current (Supply current is independent of V_{DD}) | I_{DD} | LVPECL Format 622.08 MHz Out All CKOUTs Enabled ¹ | — | 251 | 279 | mA |
| | | LVPECL Format 622.08 MHz Out Only 1 CKOUT Enabled ¹ | — | 217 | 243 | mA |
| | | CMOS Format 19.44 MHz Out All CKOUTs Enabled ² | — | 204 | 234 | mA |
| | | CMOS Format 19.44 MHz Out Only CKOUT1 Enabled ² | — | 194 | 220 | mA |

CKIN Input Pin

| | | | | | | |
|--|-------------|--|------|----|----------|-----------|
| Input Common Mode Voltage (Input Threshold Voltage) | V_{ICM} | 1.8 V \pm 5% | 0.9 | — | 1.4 | V |
| | | 2.5 V \pm 10% | 1.0 | — | 1.7 | V |
| | | 3.3 V \pm 10% | 1.1 | — | 1.95 | V |
| Input Resistance | CKN_{RIN} | Single-ended | 20 | 40 | 60 | $k\Omega$ |
| Input Voltage Level Limits | CKN_{VIN} | See note ³ | 0 | — | V_{DD} | V |
| Single-ended Input Voltage Swing | V_{ISE} | $f_{CKIN} \leq 212.5 \text{ MHz}$ See Figure 2. | 0.2 | — | — | V_{PP} |
| | | $f_{CKIN} > 212.5 \text{ MHz}$ See Figure 2. | 0.25 | — | — | V_{PP} |

Notes:

- LVPECL outputs require $V_{DD} \geq 2.25 \text{ V}$.
- This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended.
- No overshoot or undershoot.

Table 2. DC Characteristics (Continued) $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---------------|---|---------------------|-----------------|-----------------|-----------|
| Differential Input Voltage Swing | V_{ID} | $f_{CKIN} \leq 212.5 \text{ MHz}$ See Figure 2. | 0.2 | — | — | V_{PP} |
| | | $f_{CKIN} > 212.5 \text{ MHz}$ See Figure 2. | 0.25 | — | — | V_{PP} |
| CKOUT Output Clock¹ | | | | | | |
| Common Mode | V_{OCM} | LVPECL 100 Ω load line-to-line | $V_{DD} - 1.42$ | — | $V_{DD} - 1.25$ | V |
| Differential Output Swing | V_{OD} | LVPECL 100 Ω load line-to-line | 1.1 | — | 1.9 | V_{PP} |
| Single-ended Output Swing | V_{SE} | LVPECL 100 Ω load line-to-line | 0.5 | — | 0.93 | V_{PP} |
| Differential Output Voltage | CKO_{VD} | CML 100 Ω load line-to-line | 350 | 425 | 500 | mV_{PP} |
| Common Mode Output Voltage | CKO_{VCM} | CML 100 Ω load line-to-line | — | $V_{DD} - 0.36$ | — | V |
| Differential Output Voltage | CKO_{VD} | LVDS 100 Ω load line-to-line | 500 | 700 | 900 | mV_{PP} |
| | | Low swing LVDS 100 Ω load line-to-line | 350 | 425 | 500 | mV_{PP} |
| Common Mode Output Voltage | CKO_{VCM} | LVDS 100 Ω load line-to-line | 1.125 | 1.2 | 1.275 | V |
| Output Voltage Low | CKO_{VOLLH} | CMOS | — | — | 0.4 | V |
| Output Voltage High | CKO_{VOHLH} | $V_{DD} = 1.71 \text{ V}$ CMOS | $0.8 \times V_{DD}$ | — | — | V |
| Output Drive Current | CKO_{IO} | CMOS Driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally. | | | | |
| | | $V_{DD} = 1.8 \text{ V}$ | — | 7.5 | — | mA |
| | | $V_{DD} = 3.3 \text{ V}$ | — | 32 | — | mA |
| 2-Level LVCMOS Input Pins | | | | | | |
| Input Voltage Low | V_{IL} | $V_{DD} = 1.71 \text{ V}$ | — | — | 0.5 | V |
| | | $V_{DD} = 2.25 \text{ V}$ | — | — | 0.7 | V |
| | | $V_{DD} = 2.97 \text{ V}$ | — | — | 0.8 | V |
| Notes: | | | | | | |
| 1. LVPECL outputs require $V_{DD} \geq 2.25 \text{ V}$. | | | | | | |
| 2. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended. | | | | | | |
| 3. No overshoot or undershoot. | | | | | | |

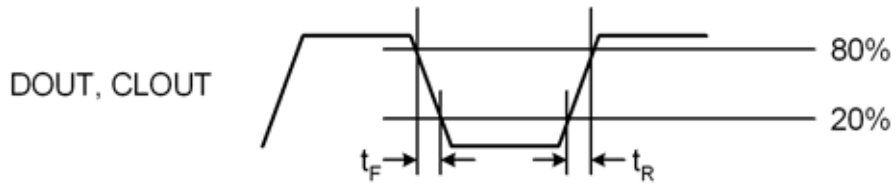
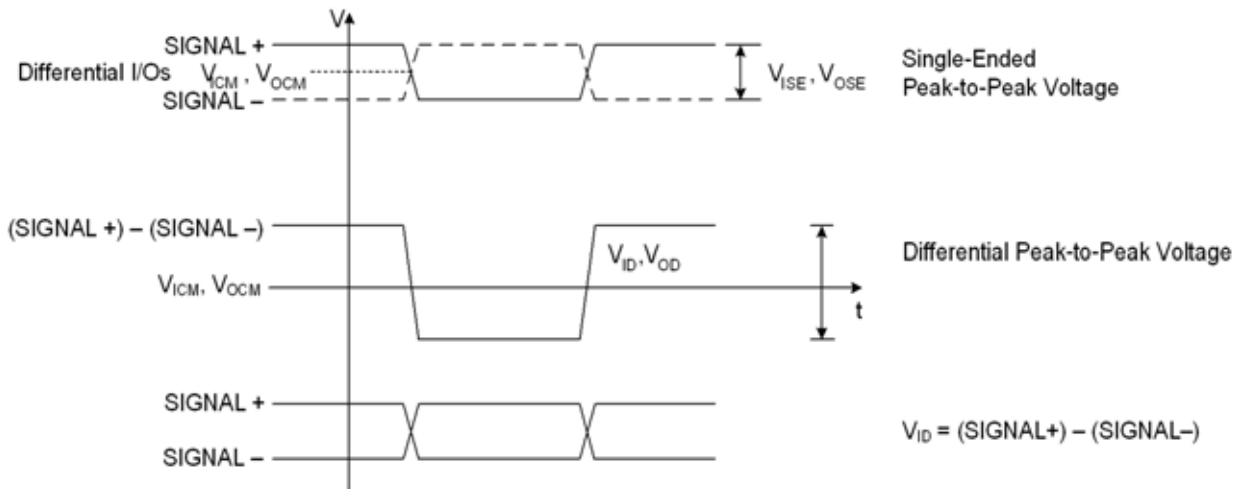
Table 2. DC Characteristics (Continued)

($V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 \text{ V} \pm 10\%$, $T_A = -40$ to $85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|-------------|---------------------------|----------------------|-----|----------------------|------------------|
| Input Voltage High | V_{IH} | $V_{DD} = 1.89 \text{ V}$ | 1.4 | — | — | V |
| | | $V_{DD} = 2.25 \text{ V}$ | 1.8 | — | — | V |
| | | $V_{DD} = 3.63 \text{ V}$ | 2.5 | — | — | V |
| Input Low Current | I_{IL} | | — | — | 50 | μA |
| Input High Current | I_{IH} | | — | — | 50 | μA |
| Weak Internal Input Pull-up Resistor | R_{PUP} | | — | 75 | — | $\text{k}\Omega$ |
| Weak Internal Input Pull-down Resistor | R_{PDN} | | — | 75 | — | $\text{k}\Omega$ |
| 3-Level Input Pins | | | | | | |
| Input Voltage Low | V_{ILL} | | — | — | $0.15 \times V_{DD}$ | V |
| Input Voltage Mid | V_{IMM} | | $0.45 \times V_{DD}$ | — | $0.55 \times V_{DD}$ | V |
| Input Voltage High | V_{IHH} | | $0.85 \times V_{DD}$ | — | — | V |
| Input Low Current | I_{ILL}^2 | | -20 | — | — | μA |
| Input Mid Current | I_{IMM}^2 | | -2 | — | 2 | μA |
| Input High Current | I_{IHH}^2 | | — | — | 20 | μA |
| Notes: | | | | | | |
| 1. LVPECL outputs require $V_{DD} \geq 2.25 \text{ V}$. | | | | | | |
| 2. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended. | | | | | | |
| 3. No overshoot or undershoot. | | | | | | |

Table 2. DC Characteristics (Continued) $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---------------------|--|----------------|-----|-----|------------|
| LVC MOS Output Pins | | | | | | |
| Output Voltage Low | V_{OL} | $I_O = 2 \text{ mA}$ $V_{DD} = 1.62 \text{ V}$ | — | — | 0.4 | V |
| | | $I_O = 2 \text{ mA}$ $V_{DD} = 2.97 \text{ V}$ | — | — | 0.4 | V |
| Output Voltage High | V_{OH} | $I_O = -2 \text{ mA}$ $V_{DD} = 1.62 \text{ V}$ | $V_{DD} - 0.4$ | — | — | V |
| | | $I_O = -2 \text{ mA}$ $V_{DD} = 2.97 \text{ V}$ | $V_{DD} - 0.4$ | — | — | V |
| Single-Ended Reference Clock Input Pin XA (XB with cap to gnd) | | | | | | |
| Input Resistance | XA_{RIN} | XTAL/RefCLK RATE[1:0] = LM, ML, MH, or HM | — | 12 | — | k Ω |
| Input Voltage Level Limits | XA_{VIN} | | 0 | — | 1.2 | V |
| Input Voltage Swing | XA_{VPP} | | 0.5 | — | 1.2 | V_{PP} |
| Differential Reference Clock Input Pins (XA/XB) | | | | | | |
| Input Resistance | XA/XB_{RIN} | XTAL/RefCLK RATE[1:0] = LM, ML, MH, or HM | — | 12 | — | k Ω |
| Differential Input Voltage Level Limits | XA/XB_{VIN} | | 0 | — | 1.2 | V |
| Input Voltage Swing | XA_{VPP}/XB_{VPP} | | 0.5 | — | 2.4 | V_{PP} |
| Notes: | | | | | | |
| 1. LVPECL outputs require $V_{DD} \geq 2.25 \text{ V}$. | | | | | | |
| 2. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended. | | | | | | |
| 3. No overshoot or undershoot. | | | | | | |



1.1. Three-Level (3L) Input Pins (No External Resistors)

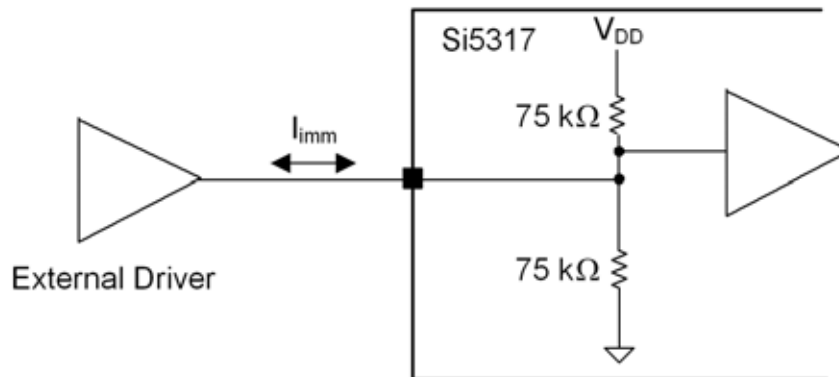
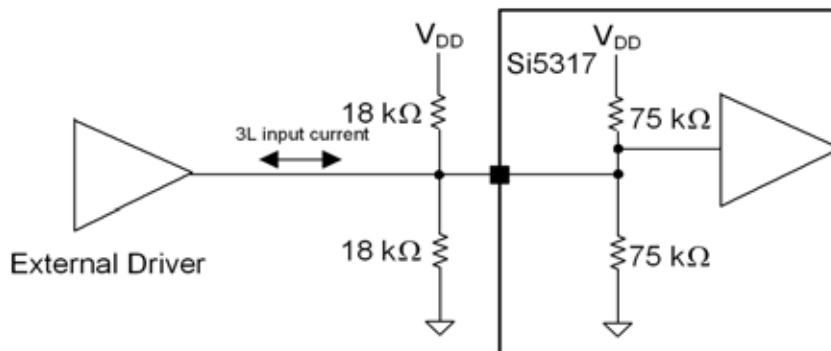


Figure 3. Three-Level Input Pins

1.2. Three-Level Input Pins (Example with External Resistors)



One of eight resistors from a Panasonic EXB-D10C183J
(or similar) resistor pack

Figure 4. Three-Level Input Pins

Table 3. Three-Level Input Pins^{1,2,3,4}

| Parameter | Min | Max |
|--------------------|-------------|-------------|
| Input Low Current | -30 μ A | — |
| Input Mid Current | -11 μ A | -11 μ A |
| Input High Current | — | -30 μ A |

Notes:

1. The current parameters are the amount of leakage that the 3L inputs can tolerate from an external driver using the external resistor values indicated in this example. In most designs, an external resistor voltage divider is recommended.
2. Resistor packs are only needed if the leakage current of the external driver exceeds the current specified in Table 2, I_{lim}. Any resistor pack may be used (e.g. Panasonic EXB-D10C183J). PCB layout is not critical.
3. If a pin is tied to ground or V_{DD}, no resistors are needed.
4. If a pin is left open (no connect), no resistors are needed.

Table 4. AC Characteristics $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|--|-------------|--|-----|-----|----------|-------|
| Input Frequency | CKN_F | | 1 | — | 711 | MHz |
| CKIN Input Pins | | | | | | |
| Input Duty Cycle (Minimum Pulse Width) | CKN_{DC} | Whichever is smaller | 40 | — | 60 | % |
| | | | 2 | — | — | ns |
| Input Capacitance | CKN_{CIN} | | — | — | 3 | pF |
| Input Rise/Fall Time | CKN_{TRF} | 20–80% See Figure 2 | — | — | 11 | ns |
| CKOUT Output Pins | | | | | | |
| Output Frequency (Output not configured for CMOS or disable) | CKO_F | | 1 | — | 711 | MHz |
| Maximum Output Frequency in CMOS Format | CKO_{FMC} | | 1 | — | 212.5 | MHz |
| Single-ended Output Rise/Fall (20–80%) | CKO_{TRF} | CMOS Output $V_{DD} = 1.62$ Load = 5 pF | — | — | 8 | ns |
| | | CMOS Output $V_{DD} = 2.97$ Load = 5 pF | — | — | 2 | ns |
| Differential Output Rise/Fall Time | CKO_{TRF} | 20 to 80 %, $f_{OUT} = 622.08$ | — | 230 | 350 | ps |
| Output Duty Cycle Differential Uncertainty | CKO_{DC} | 100 Ω Load Line to Line Measured at 50% Point (not for CMOS) | — | — | ± 40 | ps |
| LVC MOS Pins | | | | | | |
| Input Capacitance | C_{IN} | | — | — | 3 | pF |

Table 4. AC Characteristics (Continued)

($V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 \text{ V} \pm 10\%$, $T_A = -40$ to $85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---------------------|--|-------------|------|-----|---------------|
| LVC MOS Output Pins | | | | | | |
| Rise/Fall Times | t_{RF} | CLOAD = 20 pf See Figure 2 | — | 25 | — | ns |
| LOS _n Trigger Window | LOS _{TRIG} | From last CKIN \uparrow to LOS \uparrow | — | — | 750 | μs |
| Time to Clear LOL after LOS Cleared | t_{CLRLOL} | f_{in} unchanged and XA/XB stable. \downarrow LOS to \downarrow LOL | — | 10 | — | ms |
| PLL Performance | | | | | | |
| Lock Time | t_{LOCKHW} | Whenever \overline{RST} , FRQTBL, RATE, BWSEL, or FRQSEL are changed, with valid CKIN to \downarrow LOL; BW = 100 Hz | — | — | 1.2 | sec |
| Closed Loop Jitter Peaking | J_{PK} | | — | 0.05 | 0.1 | dB |
| Jitter Tolerance | J_{TOL} | BW determined by BWSEL[1:0] | 5000/ BW | — | — | ns pk-pk |
| Minimum Reset Pulse Width | t_{RSTMIN} | | 1 | — | — | μs |
| Spurious Noise | SP _{SPUR} | Max spur @ $n \times f_3$ ($n \geq 1$, $n \times f_3 < 100 \text{ MHz}$) | — | -93 | -70 | dBc |
| Phase Change due to Temperature Variation | t_{TEMP} | Max phase changes from -40 to +85 $^\circ\text{C}$ | — | 300 | 500 | ps |

Table 5. Performance Specifications^{1, 2, 3, 4, 5}

($V_{DD} = 1.8 \pm 5\%$, $2.5 \pm 10\%$, or $3.3 \text{ V} \pm 10\%$, $T_A = -40$ to $85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------------|----------------|-----|------|------|--------|
| Jitter Generation $f_{IN} = f_{OUT} = 622.08 \text{ MHz}$, LVPECL output format BW = 120 Hz | J_{GEN} | 50 kHz–80 MHz | — | 0.32 | 0.42 | ps rms |
| | | 12 kHz–20 MHz | — | 0.31 | 0.41 | ps rms |
| | | 800 Hz–80 MHz | — | 0.4 | 0.45 | ps rms |
| Phase Noise $f_{IN} = f_{OUT} = 622.08 \text{ MHz}$ LVPECL output format | CKO _{PN} | 1 kHz offset | — | -106 | -87 | dBc/Hz |
| | | 10 kHz offset | — | -121 | -100 | dBc/Hz |
| | | 100 kHz offset | — | -132 | -104 | dBc/Hz |
| | | 1 MHz offset | — | -132 | -119 | dBc/Hz |

Notes:

- BWSEL [1:0] loop bandwidth settings provided in Table 9 on page 22.
- 114.285 MHz 3rd OT crystal used as XA/XB input.
- $V_{DD} = 2.5 \text{ V}$
- $T_A = 85 \text{ }^\circ\text{C}$
- Test condition: $f_{IN} = 622.08 \text{ MHz}$, $f_{OUT} = 622.08 \text{ MHz}$, LVPECL clock input: 1.19 Vppd with 0.5 ns rise/fall time (20-80%), LVPECL clock output.

Table 6. Thermal Characteristics $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, \text{ or } 3.3 \text{ V} \pm 10\%, T_A = -40 \text{ to } 85 \text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------|----------------|-----|-----|-----|--------------------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still Air | — | 32 | — | $^\circ\text{C/W}$ |
| Thermal Resistance Junction to Case | θ_{JC} | | — | 14 | — | $^\circ\text{C/W}$ |

Table 7. Absolute Maximum Limits

| Parameter | Symbol | Value | Unit |
|--|-------------|----------------------------|------|
| DC Supply Voltage | V_{DD} | -0.5 to 3.8 | V |
| LVC MOS Input Voltage | V_{DIG} | -0.3 to ($V_{DD} + 0.3$) | V |
| CKINn Voltage Level Limits | CKN_{VIN} | 0 to V_{DD} | V |
| XA/XB Voltage Level Limits | XA_{VIN} | 0 to 1.2 | V |
| Operating Junction Temperature | T_{JCT} | -55 to 150 | C |
| Storage Temperature Range | T_{STG} | -55 to 150 | C |
| ESD HBM Tolerance (100 pF, 1.5 k Ω); All pins except CKIN+/CKIN- | | 2 | kV |
| ESD MM Tolerance; All pins except CKIN+/CKIN- | | 150 | V |
| ESD HBM Tolerance (100 pF, 1.5 k Ω); CKIN+/CKIN- | | 750 | V |
| ESD MM Tolerance; CKIN+/CKIN- | | 100 | V |
| Latch-Up Tolerance | | JESD78 Compliant | |
| Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. | | | |

2. Functional Description

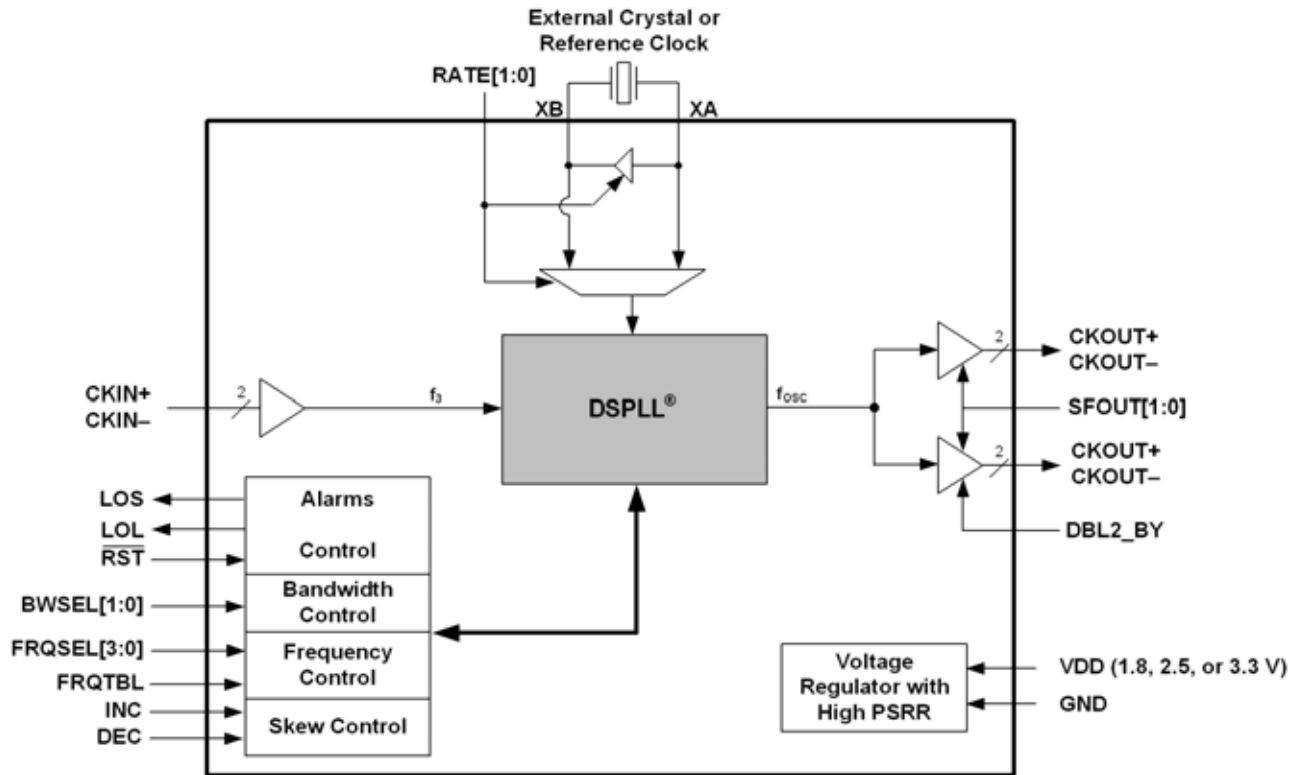


Figure 5. Detailed Block Diagram

2.1. Overview

The Si5317 is a 1:1 jitter-attenuating precision clock for applications requiring sub 1 ps jitter performance. The Si5317 accepts one clock input ranging from 1 to 711 MHz and generates two clock outputs at the same frequency ranging from 1 to 711 MHz. The Si5317 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides jitter attenuation on any frequency in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The nominal operating frequency is selectable from a look-up table. The Si5317 PLL loop bandwidth (BW) is selectable via the BWSEL[1:0] pins and supports a range from 60 Hz to 8.4 kHz.

The Si5317 monitors the input clock for loss-of-signal (LOS) and provides a LOS alarm when it detects missing pulses on the input clock. The device monitors the lock status of the DSPLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock.

The Si5317 provides a VCO freeze capability that allows the device to continue generation of a stable output clock when the selected input clock is lost. During VCO freeze, the DSPLL latches its VCO settings and uses its XA/XB clock as its frequency reference.

The Si5317 has two output clock drivers and can be configured as four single-ended or two differential outputs. The signal format of the clock output is selectable to support LVPECL, LVDS, CML, or CMOS loads. The device operates from a single 1.8, 2.5, or 3.3 V supply. The use of LVPECL requires a $VDD \geq 2.25$ V.

3. Frequency Plan Tables

For ease of use, the Si5317 is pin-controlled to enable simple device configuration of the frequency range plan and PLL loop bandwidth via a predefined look-up table. The DSPLL has been optimized for jitter performance and tunability for each frequency range and PLL loop bandwidth provided in Table 9 on page 22.

Many of the control inputs are three levels: High, Low, and Medium. High and Low are standard voltage levels determined by the supply pins: V_{DD} and Ground. If the input pin is left floating, it is driven to nominally half of V_{DD} . Effectively, this creates three logic levels for these controls. See section 6. "Power Supply Filtering" on page 33 and section 1.2. "Three-Level Input Pins (Example with External Resistors)" on page 9 for additional information.

3.1. Frequency Range Plan

The input to output clock frequency range is set by the 3-level FRQSEL[3:0] and FRQTBL pins. The CKIN and CKOUT is the same frequency range as specified in Table 8. Due to the wide tunability of the Si5317, each frequency plan provides overlap between adjacent settings. To select a frequency plan, the desired frequency should be selected as close to the defined center frequency. In certain cases where the desired frequency is exactly between two overlapping plans, either FRQTBL and FRQSEL setting can be used.

3.1.1. PLL Loop Bandwidth Plan

The Si5317's loop bandwidth ranges from 60 Hz to 8.4 kHz. For each frequency range, the corresponding loop bandwidth is provided in a simple look-up table (see Table 9 on page 22). The loop bandwidth is digitally programmable using the three-level BWSEL [1:0] input pins.

3.2. Output Skew Adjustment

The overall device skew (CKIN to CKOUTn phase delay) is adjustable via the INC and DEC input pins. A positive edge triggered pulse applied to the INC pin increases the device skew defined by Table 8, INC/DEC step size, for each given frequency plan. The identical operation on the DEC pin decreases the skew by the same amount. Using the INC and DEC pins, there is no limit to the range of skew adjustment that can be made. Following a powerup or reset, the overall device skew will revert to the reset value, although the input-to-output skew is effectively random. The rate of change for each INC/DEC operation is defined by the selected loop bandwidth, BWSEL[1:0].

Table 8. Look-up Tables for Fin = Fout Frequency Range and Loop Bandwidth Settings

| Plan No | FRQTBL | FRQSEL [3:0] | Frequency Range (MHz) | | | BWSEL [1:0] (BW in Hz) | | | | | | INC/DEC Phase Change (ns) |
|---------|--------|--------------|-----------------------|--------|------|------------------------|------|------|-----|-----|-----|---------------------------|
| | | | Min | Center | Max | LH | ML | MM | MH | HL | HM | |
| 0 | L | LLLL | .95 | 1.00 | 1.05 | — | 3814 | 927 | 230 | 114 | 57 | 0.21 |
| 1 | L | LLLM | 1.00 | 1.05 | 1.10 | — | 3814 | 927 | 230 | 114 | 57 | 0.21 |
| 2 | L | LLLH | 1.05 | 1.10 | 1.15 | — | 3834 | 931 | 231 | 115 | 57 | 0.21 |
| 3 | L | LLML | 1.10 | 1.15 | 1.20 | — | 4052 | 983 | 244 | 121 | 60 | 0.21 |
| 4 | L | LLMM | 1.15 | 1.20 | 1.25 | — | 4251 | 1030 | 255 | 127 | 63 | 0.21 |
| 5 | L | LLMH | 1.20 | 1.25 | 1.30 | — | 4451 | 1078 | 267 | 133 | 66 | 0.21 |
| 6 | L | LLHL | 1.25 | 1.30 | 1.35 | — | 4652 | 1125 | 279 | 139 | 69 | 0.21 |
| 7 | L | LLHM | 1.30 | 1.35 | 1.40 | — | 4852 | 1172 | 290 | 145 | 72 | 0.21 |
| 8 | L | LLHH | 1.35 | 1.40 | 1.45 | — | 5054 | 1219 | 302 | 150 | 75 | 0.21 |
| 9 | L | LMLL | 1.40 | 1.45 | 1.50 | — | 5256 | 1267 | 314 | 156 | 78 | 0.21 |
| 10 | L | LMLM | 1.45 | 1.50 | 1.55 | — | 5256 | 1267 | 314 | 156 | 78 | 0.21 |
| 11 | L | LMLH | 1.50 | 1.55 | 1.60 | — | 5459 | 1314 | 325 | 162 | 81 | 0.21 |
| 12 | L | LMML | 1.55 | 1.60 | 1.65 | — | 5866 | 1409 | 349 | 174 | 87 | 0.21 |
| 13 | L | LMMM | 1.60 | 1.65 | 1.70 | — | 5866 | 1409 | 349 | 174 | 87 | 0.21 |
| 14 | L | LMMH | 1.65 | 1.70 | 1.75 | — | 6071 | 1457 | 360 | 180 | 89 | 0.21 |
| 15 | L | LMHL | 1.70 | 1.75 | 1.80 | — | 6276 | 1504 | 372 | 185 | 92 | 0.21 |
| 16 | L | LMHM | 1.75 | 1.80 | 1.85 | — | 6483 | 1552 | 384 | 191 | 95 | 0.21 |
| 17 | L | LMHH | 1.80 | 1.85 | 1.90 | — | 6688 | 1599 | 395 | 197 | 98 | 0.21 |
| 18 | L | LHLL | 1.85 | 1.90 | 1.95 | — | 6895 | 1647 | 407 | 203 | 101 | 0.21 |
| 19 | L | LHLM | 1.90 | 1.95 | 2.00 | 4696 | 2285 | 560 | 139 | 69 | — | 0.21 |
| 20 | L | LHLH | 1.95 | 2.00 | 2.10 | 4832 | 2350 | 575 | 143 | 71 | — | 0.21 |
| 21 | L | LHML | 2.00 | 2.10 | 2.20 | 4967 | 2415 | 591 | 147 | 73 | — | 0.21 |
| 22 | L | LHMM | 2.10 | 2.20 | 2.30 | 5239 | 2544 | 622 | 154 | 77 | — | 0.21 |
| 23 | L | LHMH | 2.20 | 2.30 | 2.40 | — | 4052 | 983 | 244 | 121 | 60 | 0.21 |
| 24 | L | LHHL | 2.30 | 2.40 | 2.50 | — | 4251 | 1030 | 255 | 127 | 63 | 0.21 |
| 25 | L | LHHM | 2.40 | 2.50 | 2.60 | — | 4451 | 1078 | 267 | 133 | 66 | 0.21 |
| 26 | L | LHHH | 2.50 | 2.60 | 2.70 | — | 4651 | 1125 | 279 | 139 | 69 | 0.21 |
| 27 | L | MLLL | 2.60 | 2.70 | 2.80 | — | 4852 | 1172 | 290 | 145 | 72 | 0.20 |
| 28 | L | MLLM | 2.70 | 2.80 | 2.90 | — | 5054 | 1219 | 302 | 150 | 75 | 0.21 |
| 29 | L | MLLH | 2.80 | 2.90 | 3.00 | — | 5255 | 1267 | 314 | 156 | 78 | 0.20 |
| 30 | L | MLML | 2.90 | 3.00 | 3.10 | — | 5458 | 1314 | 325 | 162 | 81 | 0.20 |
| 31 | L | MLMM | 3.00 | 3.10 | 3.20 | — | 5859 | 1409 | 349 | 174 | 87 | 0.20 |
| 32 | L | MLMH | 3.10 | 3.20 | 3.30 | — | 5859 | 1409 | 349 | 174 | 87 | 0.20 |

Note: For BWSEL[1:0] settings LL, LM, HH are reserved.

Table 8. Look-up Tables for Fin = Fout Frequency Range and Loop Bandwidth Settings (Continued)

| Plan No | FRQTBL | FRQSEL [3:0] | Frequency Range (MHz) | | | BWSEL [1:0] (BW in Hz) | | | | | | INC/DEC Phase Change (ns) |
|---------|--------|--------------|-----------------------|--------|-------|------------------------|------|------|-----|-----|-----|---------------------------|
| | | | Min | Center | Max | LH | ML | MM | MH | HL | HM | |
| 33 | L | MLHL | 3.20 | 3.30 | 3.40 | — | 6071 | 1457 | 360 | 180 | 89 | 0.21 |
| 34 | L | MLHM | 3.30 | 3.40 | 3.50 | — | 6071 | 1457 | 360 | 180 | 89 | 0.21 |
| 35 | L | MLHH | 3.40 | 3.50 | 3.60 | — | 6276 | 1504 | 372 | 185 | 92 | 0.21 |
| 36 | L | MMLL | 3.50 | 3.60 | 3.70 | — | 6483 | 1552 | 384 | 191 | 95 | 0.21 |
| 37 | L | MMLM | 3.60 | 3.70 | 3.80 | — | 6895 | 1647 | 407 | 203 | 101 | 0.21 |
| 38 | L | MMLH | 3.70 | 3.80 | 3.90 | — | 6895 | 1647 | 407 | 203 | 101 | 0.21 |
| 39 | L | MMML | 3.80 | 3.90 | 4.00 | — | 4650 | 1125 | 279 | 139 | 69 | 0.20 |
| 40 | L | MMMM | 3.90 | 4.00 | 4.20 | — | 4786 | 1156 | 286 | 143 | 71 | 0.21 |
| 41 | L | MMMh | 4.00 | 4.20 | 4.40 | — | 4919 | 1188 | 294 | 147 | 73 | 0.21 |
| 42 | L | MMHL | 4.20 | 4.40 | 4.60 | — | 5457 | 1314 | 325 | 162 | 81 | 0.20 |
| 43 | L | MMHM | 4.40 | 4.60 | 4.80 | — | 5457 | 1314 | 325 | 162 | 81 | 0.20 |
| 44 | L | MMHH | 4.60 | 4.80 | 5.00 | — | 5730 | 1378 | 341 | 170 | 85 | 0.21 |
| 45 | L | MHLL | 4.80 | 5.00 | 5.20 | — | 6268 | 1504 | 372 | 185 | 92 | 0.20 |
| 46 | L | MHLM | 5.00 | 5.20 | 5.40 | — | 6273 | 1504 | 372 | 185 | 92 | 0.20 |
| 47 | L | MHLH | 5.20 | 5.40 | 5.60 | — | 6550 | 1568 | 387 | 193 | 96 | 0.20 |
| 48 | L | MHML | 5.40 | 5.60 | 5.80 | — | 6823 | 1631 | 403 | 201 | 100 | 0.20 |
| 49 | L | MHMM | 5.60 | 5.80 | 6.00 | — | 6823 | 1631 | 403 | 201 | 100 | 0.20 |
| 50 | L | MHMh | 5.80 | 6.00 | 6.20 | — | 6333 | 3064 | 748 | 185 | 92 | 0.20 |
| 51 | L | MHHL | 6.00 | 6.20 | 6.40 | — | 6571 | 3176 | 774 | 192 | 96 | 0.20 |
| 52 | L | MHHM | 6.20 | 6.40 | 6.60 | — | 6811 | 3289 | 801 | 199 | 99 | 0.20 |
| 53 | L | MHHH | 6.40 | 6.60 | 6.80 | — | 6071 | 1457 | 360 | 180 | 89 | 0.21 |
| 54 | L | HLLL | 6.60 | 6.80 | 7.00 | — | 6534 | 1567 | 387 | 193 | 96 | 0.20 |
| 55 | L | HLLM | 6.80 | 7.00 | 7.20 | — | 6534 | 1567 | 387 | 193 | 96 | 0.20 |
| 56 | L | HLLH | 7.00 | 7.20 | 7.40 | — | 6483 | 1552 | 384 | 191 | 95 | 0.21 |
| 57 | L | HLML | 7.20 | 7.40 | 7.60 | — | 6686 | 1599 | 395 | 197 | 98 | 0.20 |
| 58 | L | HLMM | 7.40 | 7.60 | 7.80 | — | 6891 | 1647 | 407 | 203 | 101 | 0.20 |
| 59 | L | HLMH | 7.60 | 7.80 | 8.00 | — | 4648 | 1125 | 279 | 139 | 69 | 0.20 |
| 60 | L | HLHL | 7.80 | 8.00 | 8.40 | — | 4786 | 1156 | 286 | 143 | 71 | 0.21 |
| 61 | L | HLHM | 8.00 | 8.40 | 8.80 | — | 4919 | 1188 | 294 | 147 | 73 | 0.21 |
| 62 | L | HLHH | 8.40 | 8.80 | 9.00 | — | 6599 | 1580 | 391 | 195 | 97 | 0.20 |
| 63 | L | HMLL | 8.80 | 9.00 | 9.20 | — | 7080 | 1693 | 418 | 209 | 104 | 0.19 |
| 64 | L | HMLM | 9.00 | 9.20 | 9.60 | — | 7080 | 1693 | 418 | 209 | 104 | 0.19 |
| 65 | L | HMLH | 9.20 | 9.60 | 10.00 | — | 5727 | 1377 | 341 | 170 | 85 | 0.20 |
| 66 | L | HMML | 9.60 | 10.00 | 10.50 | — | 6003 | 1441 | 356 | 178 | 88 | 0.21 |

Note: For BWSEL[1:0] settings LL, LM, HH are reserved.

Table 8. Look-up Tables for Fin = Fout Frequency Range and Loop Bandwidth Settings (Continued)

| Plan No | FRQTBL | FRQSEL [3:0] | Frequency Range (MHz) | | | BWSEL [1:0] (BW in Hz) | | | | | | INC/DEC Phase Change (ns) |
|---------|--------|--------------|-----------------------|--------|-------|------------------------|------|------|-----|-----|-----|---------------------------|
| | | | Min | Center | Max | LH | ML | MM | MH | HL | HM | |
| 67 | L | HMMM | 10.00 | 10.50 | 11.00 | — | 6273 | 1504 | 372 | 185 | 92 | 0.20 |
| 68 | L | HMMH | 10.50 | 11.00 | 11.50 | — | 6992 | 1672 | 413 | 206 | 103 | 0.20 |
| 69 | L | HMHL | 11.00 | 11.50 | 12.00 | — | 5866 | 1409 | 349 | 174 | 87 | 0.21 |
| 70 | L | HMHM | 11.50 | 12.00 | 12.50 | — | 6155 | 1477 | 365 | 182 | 91 | 0.20 |
| 71 | L | HMHH | 12.00 | 12.50 | 13.00 | — | 6446 | 1545 | 382 | 190 | 95 | 0.20 |
| 72 | L | HHLL | 12.50 | 13.00 | 13.50 | — | 7034 | 1680 | 415 | 207 | 103 | 0.20 |
| 73 | L | HHLM | 13.00 | 13.50 | 14.00 | — | 5408 | 1303 | 323 | 161 | 80 | 0.20 |
| 74 | L | HHLH | 13.50 | 14.00 | 14.50 | — | 5633 | 1356 | 336 | 167 | 83 | 0.20 |
| 75 | L | HHML | 14.00 | 14.50 | 15.00 | — | 5861 | 1409 | 349 | 174 | 87 | 0.20 |
| 76 | L | HHMM | 14.50 | 15.00 | 15.50 | — | 7383 | 1764 | 436 | 217 | 108 | 0.19 |
| 77 | L | HHMH | 15.00 | 15.50 | 16.00 | — | 6321 | 1515 | 374 | 187 | 93 | 0.21 |
| 78 | L | HHHL | 15.50 | 16.00 | 16.50 | — | 6321 | 1515 | 374 | 187 | 93 | 0.21 |
| 79 | L | HHHM | 16.00 | 16.50 | 17.00 | — | 6774 | 1620 | 400 | 200 | 99 | 0.20 |
| 80 | L | HHHH | 16.50 | 17.00 | 17.50 | — | 7230 | 1726 | 426 | 213 | 106 | 0.20 |
| 81 | M | LLLL | 17.00 | 17.50 | 18.00 | — | 4422 | 1071 | 265 | 132 | 66 | 0.21 |
| 82 | M | LLLM | 17.50 | 18.00 | 18.50 | — | 7342 | 1756 | 434 | 216 | 108 | 0.19 |
| 83 | M | LLLH | 18.00 | 18.50 | 19.00 | — | 7342 | 1756 | 434 | 216 | 108 | 0.19 |
| 84 | M | LLML | 18.50 | 19.00 | 19.50 | — | 7298 | 1742 | 430 | 214 | 107 | 0.20 |
| 85 | M | LLMM | 19.00 | 19.50 | 20.00 | — | 4995 | 1206 | 299 | 149 | 74 | 0.20 |
| 86 | M | LLMH | 19.50 | 20.00 | 21.00 | — | 7518 | 1796 | 444 | 221 | 110 | 0.19 |
| 87 | M | LLHL | 20.00 | 21.00 | 22.00 | — | 6208 | 1488 | 368 | 183 | 91 | 0.21 |
| 88 | M | LLHM | 21.00 | 22.00 | 23.00 | — | 7429 | 1777 | 439 | 219 | 109 | 0.18 |
| 89 | M | LLHH | 22.00 | 23.00 | 24.00 | — | 6155 | 1477 | 365 | 182 | 91 | 0.20 |
| 90 | M | LMLL | 23.00 | 24.00 | 25.00 | — | 6155 | 1477 | 365 | 182 | 91 | 0.20 |
| 91 | M | LMLM | 24.00 | 25.00 | 26.00 | — | 6739 | 1612 | 399 | 199 | 99 | 0.20 |
| 92 | M | LMLH | 25.26 | 26.00 | 27.00 | — | 7613 | 1816 | 449 | 224 | 111 | 0.19 |
| 93 | M | LMML | 26.00 | 27.00 | 28.00 | — | 6817 | 1631 | 403 | 201 | 100 | 0.20 |
| 94 | M | LMMM | 27.00 | 28.00 | 29.00 | — | 6817 | 1631 | 403 | 201 | 100 | 0.20 |
| 95 | M | LMMH | 28.00 | 29.00 | 30.00 | — | 7640 | 1821 | 450 | 224 | 112 | 0.20 |
| 96 | M | LMHL | 29.00 | 30.00 | 31.00 | — | 4941 | 1194 | 296 | 147 | 73 | 0.20 |
| 97 | M | LMHM | 30.31 | 31.00 | 32.00 | — | 7658 | 1827 | 451 | 225 | 112 | 0.19 |
| 98 | M | LMHH | 31.00 | 32.00 | 33.00 | — | 7658 | 1827 | 451 | 225 | 112 | 0.19 |
| 99 | M | LHLL | 32.00 | 33.00 | 34.00 | — | 6774 | 1620 | 400 | 200 | 99 | 0.20 |
| 100 | M | LHLM | 33.00 | 34.00 | 35.00 | — | 6774 | 1620 | 400 | 200 | 99 | 0.20 |

Note: For BWSEL[1:0] settings LL, LM, HH are reserved.

Table 8. Look-up Tables for Fin = Fout Frequency Range and Loop Bandwidth Settings (Continued)

| Plan No | FRQTBL | FRQSEL [3:0] | Frequency Range (MHz) | | | BWSEL [1:0] (BW in Hz) | | | | | | INC/DEC Phase Change (ns) |
|---------|--------|--------------|-----------------------|--------|--------|------------------------|------|------|-----|-----|-----|---------------------------|
| | | | Min | Center | Max | LH | ML | MM | MH | HL | HM | |
| 101 | M | LHLH | 34.00 | 35.00 | 36.00 | — | 7692 | 1832 | 452 | 225 | 112 | 0.20 |
| 102 | M | LHML | 35.00 | 36.00 | 37.00 | — | 7680 | 1833 | 453 | 226 | 113 | 0.19 |
| 103 | M | LHMM | 36.00 | 37.00 | 38.00 | — | 7539 | 1803 | 446 | 222 | 111 | 0.18 |
| 104 | M | LHMH | 37.00 | 38.00 | 39.00 | — | 7658 | 1827 | 451 | 225 | 112 | 0.19 |
| 105 | M | LHHL | 38.00 | 39.00 | 40.00 | — | 7607 | 1818 | 449 | 224 | 112 | 0.18 |
| 106 | M | LHHM | 39.00 | 40.00 | 42.00 | — | 7607 | 1818 | 449 | 224 | 112 | 0.18 |
| 107 | M | LHHH | 40.00 | 42.00 | 44.00 | — | 5709 | 1373 | 340 | 169 | 84 | 0.21 |
| 108 | M | MLLL | 43.30 | 44.00 | 46.00 | — | 7653 | 1828 | 452 | 225 | 112 | 0.18 |
| 109 | M | MLLM | 44.00 | 46.00 | 48.00 | — | 7653 | 1828 | 452 | 225 | 112 | 0.18 |
| 110 | M | MLLH | 46.00 | 48.00 | 50.00 | — | 6155 | 1477 | 365 | 182 | 91 | 0.20 |
| 111 | M | MLML | 48.00 | 50.00 | 52.00 | — | 7630 | 1823 | 450 | 225 | 112 | 0.18 |
| 112 | M | MLMM | 50.52 | 52.00 | 54.00 | — | 7692 | 1832 | 452 | 225 | 112 | 0.20 |
| 113 | M | MLMH | 52.00 | 54.00 | 56.00 | — | 7880 | 1882 | 465 | 232 | 116 | 0.18 |
| 114 | M | MLHL | 54.00 | 56.00 | 58.00 | — | 6169 | 1481 | 366 | 183 | 91 | 0.20 |
| 115 | M | MLHM | 56.00 | 58.00 | 60.00 | — | 7664 | 1826 | 451 | 225 | 112 | 0.20 |
| 116 | M | MLHH | 58.00 | 60.00 | 60.00 | — | 7664 | 1826 | 451 | 225 | 112 | 0.20 |
| 117 | M | MMLL | 60.00 | 62.00 | 64.00 | — | 7882 | 1882 | 465 | 232 | 116 | 0.18 |
| 118 | M | MMLM | 62.00 | 64.00 | 66.00 | — | 7890 | 1883 | 465 | 232 | 116 | 0.18 |
| 119 | M | MMLH | 64.00 | 66.00 | 68.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 120 | M | MMML | 66.00 | 68.00 | 70.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 121 | M | MMMM | 68.00 | 70.00 | 70.88 | — | 6228 | 1494 | 369 | 184 | 92 | 0.20 |
| 122 | M | MMMh | 70.00 | 72.00 | 74.00 | — | 7888 | 1883 | 465 | 232 | 116 | 0.18 |
| 123 | M | MMHL | 72.00 | 74.00 | 76.00 | — | 7889 | 1883 | 465 | 232 | 116 | 0.18 |
| 124 | M | MMHM | 75.78 | 76.00 | 78.00 | — | 7917 | 1884 | 465 | 232 | 116 | 0.20 |
| 125 | M | MMHH | 76.00 | 78.00 | 80.00 | — | 7895 | 1883 | 465 | 232 | 116 | 0.19 |
| 126 | M | MHLL | 78.00 | 80.00 | 84.00 | — | 7895 | 1883 | 465 | 232 | 116 | 0.19 |
| 127 | M | MHLM | 80.00 | 84.00 | 88.00 | — | 6010 | 1445 | 357 | 178 | 89 | 0.20 |
| 128 | M | MHLH | 84.00 | 88.00 | 88.59 | — | 6010 | 1445 | 357 | 178 | 89 | 0.20 |
| 129 | M | MHML | 88.00 | 90.00 | 92.00 | — | 6329 | 1518 | 375 | 187 | 93 | 0.20 |
| 130 | M | MHMM | 90.00 | 92.00 | 96.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 131 | M | MHMH | 92.00 | 96.00 | 100.00 | — | 7795 | 1864 | 461 | 230 | 114 | 0.18 |
| 132 | M | MHHL | 96.00 | 100.00 | 105.00 | — | 7795 | 1864 | 461 | 230 | 114 | 0.18 |
| 133 | M | MHHM | 101.04 | 105.00 | 110.00 | — | 7903 | 1884 | 465 | 232 | 116 | 0.19 |
| 134 | M | MHHH | 105.00 | 110.00 | 115.00 | — | 7812 | 1866 | 461 | 230 | 115 | 0.18 |

Note: For BWSEL[1:0] settings LL, LM, HH are reserved.

Table 8. Look-up Tables for Fin = Fout Frequency Range and Loop Bandwidth Settings (Continued)

| Plan No | FRQTBL | FRQSEL [3:0] | Frequency Range (MHz) | | | BWSEL [1:0] (BW in Hz) | | | | | | INC/DEC Phase Change (ns) |
|---------|--------|--------------|-----------------------|--------|--------|------------------------|------|------|-----|-----|-----|---------------------------|
| | | | Min | Center | Max | LH | ML | MM | MH | HL | HM | |
| 135 | M | HLLL | 110.00 | 115.00 | 118.13 | — | 6329 | 1518 | 375 | 187 | 93 | 0.20 |
| 136 | M | HLLM | 115.00 | 120.00 | 125.00 | — | 7820 | 1867 | 461 | 230 | 115 | 0.18 |
| 137 | M | HLLH | 120.00 | 125.00 | 130.00 | — | 7812 | 1868 | 462 | 230 | 115 | 0.18 |
| 138 | M | HLML | 125.00 | 130.00 | 135.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 139 | M | HLMM | 130.00 | 135.00 | 140.00 | — | 6873 | 1648 | 408 | 203 | 101 | 0.19 |
| 140 | M | HLMH | 135.00 | 140.00 | 145.00 | — | 7851 | 1871 | 462 | 230 | 115 | 0.19 |
| 141 | M | HLHL | 140.00 | 145.00 | 150.00 | — | 7826 | 1870 | 462 | 230 | 115 | 0.18 |
| 142 | M | HLHM | 145.00 | 150.00 | 155.00 | — | 7240 | 1735 | 429 | 214 | 107 | 0.18 |
| 143 | M | HLHH | 151.56 | 155.00 | 160.00 | — | 7853 | 1872 | 462 | 230 | 115 | 0.19 |
| 144 | M | HMLL | 155.00 | 160.00 | 165.00 | — | 7890 | 1883 | 465 | 232 | 116 | 0.18 |
| 145 | M | HMLM | 160.00 | 165.00 | 170.00 | — | 7831 | 1871 | 462 | 231 | 115 | 0.18 |
| 146 | M | HMLH | 165.00 | 170.00 | 175.00 | — | 7831 | 1871 | 462 | 231 | 115 | 0.18 |
| 147 | M | HMML | 170.00 | 175.00 | 177.19 | — | 6912 | 1654 | 409 | 204 | 102 | 0.20 |
| 148 | M | HMMM | 175.00 | 180.00 | 185.00 | — | 7140 | 1710 | 423 | 211 | 105 | 0.19 |
| 149 | M | HMMH | 180.00 | 185.00 | 190.00 | — | 7846 | 1873 | 463 | 231 | 115 | 0.18 |
| 150 | M | HMHL | 185.00 | 190.00 | 195.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 151 | M | HMHM | 190.00 | 195.00 | 200.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 152 | M | HMHM | 195.00 | 200.00 | 202.50 | — | 6993 | 1673 | 414 | 206 | 103 | 0.19 |
| 153 | M | HHLL | 202.08 | 210.00 | 220.00 | — | 7903 | 1884 | 465 | 232 | 116 | 0.19 |
| 154 | M | HHLM | 210.00 | 220.00 | 230.00 | — | 7069 | 1689 | 417 | 208 | 104 | 0.20 |
| 155 | M | HHLH | 220.45 | 230.00 | 240.00 | — | 7903 | 1884 | 465 | 232 | 116 | 0.19 |
| 156 | M | HHML | 230.00 | 240.00 | 250.00 | — | 7507 | 1793 | 443 | 221 | 110 | 0.19 |
| 157 | M | HHMM | 242.50 | 250.00 | 260.00 | — | 7910 | 1884 | 465 | 232 | 116 | 0.19 |
| 158 | M | HHMH | 250.00 | 260.00 | 270.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 159 | M | HHHL | 260.00 | 270.00 | 280.00 | — | 7429 | 1776 | 439 | 219 | 109 | 0.19 |
| 160 | M | HHHM | 270.00 | 280.00 | 290.00 | — | 7908 | 1884 | 465 | 232 | 116 | 0.19 |
| 161 | M | HHHH | 280.00 | 290.00 | 300.00 | — | 7879 | 1882 | 465 | 232 | 116 | 0.18 |
| 162 | H | LLLL | 290.00 | 300.00 | 310.00 | — | 7571 | 1811 | 448 | 223 | 111 | 0.18 |
| 163 | H | LLLM | 303.13 | 310.00 | 320.00 | — | 7903 | 1884 | 465 | 232 | 116 | 0.19 |
| 164 | H | LLLH | 310.00 | 320.00 | 330.00 | — | 7890 | 1883 | 465 | 232 | 116 | 0.18 |
| 165 | H | LLML | 320.00 | 330.00 | 340.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 166 | H | LLMM | 330.00 | 340.00 | 350.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 167 | H | LLMH | 340.00 | 350.00 | 354.38 | — | 7344 | 1757 | 434 | 217 | 108 | 0.18 |

Note: For BWSEL[1:0] settings LL, LM, HH are reserved.

Table 8. Look-up Tables for Fin = Fout Frequency Range and Loop Bandwidth Settings (Continued)

| Plan No | FRQTBL | FRQSEL [3:0] | Frequency Range (MHz) | | | BWSEL [1:0] (BW in Hz) | | | | | | INC/DEC Phase Change (ns) |
|---------|--------|--------------|-----------------------|--------|--------|------------------------|------|------|-----|-----|-----|---------------------------|
| | | | Min | Center | Max | LH | ML | MM | MH | HL | HM | |
| 168 | H | LLHL | 350.00 | 360.00 | 370.00 | — | 7900 | 1883 | 465 | 232 | 116 | 0.19 |
| 169 | H | LLHM | 360.00 | 370.00 | 380.00 | — | 7889 | 1883 | 465 | 232 | 116 | 0.18 |
| 170 | H | LLHH | 370.00 | 380.00 | 390.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 171 | H | LMLL | 380.00 | 390.00 | 400.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 172 | H | LMLM | 390.00 | 400.00 | 405.00 | — | 7755 | 1854 | 458 | 228 | 114 | 0.18 |
| 173 | H | LMLH | 404.17 | 420.00 | 440.00 | — | 7903 | 1884 | 465 | 232 | 116 | 0.19 |
| 174 | H | LMML | 420.00 | 440.00 | 460.00 | — | 7848 | 1874 | 463 | 231 | 115 | 0.18 |
| 175 | H | LMMM | 440.91 | 460.00 | 480.00 | — | 7903 | 1884 | 465 | 232 | 116 | 0.19 |
| 176 | H | LMMH | 460.00 | 480.00 | 500.00 | — | 7507 | 1793 | 443 | 221 | 110 | 0.19 |
| 177 | H | LMHL | 485.00 | 500.00 | 520.00 | — | 7910 | 1884 | 465 | 232 | 116 | 0.19 |
| 178 | H | LMHM | 500.00 | 520.00 | 540.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 179 | H | LMHH | 520.00 | 540.00 | 560.00 | — | 7704 | 1842 | 455 | 227 | 113 | 0.18 |
| 180 | H | LHLL | 540.00 | 560.00 | 580.00 | — | 7908 | 1884 | 465 | 232 | 116 | 0.19 |
| 181 | H | LHLM | 560.00 | 580.00 | 600.00 | — | 7879 | 1882 | 465 | 232 | 116 | 0.18 |
| 182 | H | LHLH | 580.00 | 600.00 | 620.00 | — | 7571 | 1811 | 448 | 223 | 111 | 0.18 |
| 183 | H | LHML | 606.25 | 620.00 | 640.00 | — | 7903 | 1884 | 465 | 232 | 116 | 0.19 |
| 184 | H | LHMM | 620.00 | 640.00 | 660.00 | — | 7890 | 1883 | 465 | 232 | 116 | 0.18 |
| 185 | H | LHMH | 640.00 | 660.00 | 680.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 186 | H | LHHL | 660.00 | 680.00 | 700.00 | — | 7878 | 1882 | 465 | 232 | 116 | 0.18 |
| 187 | H | LHHM | 680.00 | 700.00 | 704.00 | — | 7831 | 1871 | 462 | 231 | 115 | 0.18 |
| 188 | H | LHHH | 700.00 | 7.05 | 711.00 | — | 7908 | 1880 | 464 | 231 | 115 | 0.20 |

Note: For BWSEL[1:0] settings LL, LM, HH are reserved.

3.3. PLL Self-Calibration

An internal self-calibration (ICAL) is performed before operation to optimize loop parameters and jitter performance. While the self-calibration is being performed, the DSPLL is being internally controlled by the self-calibration state machine. The LOL alarm will be active during ICAL. The self-calibration time t_{LOCKHW} is given in Table 4, "AC Characteristics".

Any of the following events will trigger a self-calibration:

- Power-on-reset (POR)
- Release of the external reset pin \overline{RST} (transition of \overline{RST} from 0 to 1)
- Change in FRQSEL, FRQTBL, BWSEL, or RATE[1:0] pins
- Internal DSPLL registers out-of-range, indicating the need to relock the DSPLL

In any of the above cases, an ICAL will be initiated if a valid input clock exists with no input alarm. The external crystal or reference clock must also be present for the self-calibration to begin. If no valid input clock is present, the self-calibration state machine will wait until it appears, at which time the calibration will start.

After a successful ICAL has been performed with a valid input clock, no subsequent self-calibrations are performed unless one of the above conditions are met. If the input clock is lost following self-calibration, the device enters VCO freeze mode. When the input clock returns, the device relocks to the input clock without performing a self-calibration.

3.3.1. Input Clock Stability during Internal Self-Calibration

An exit from reset must occur when the selected CKIN clock is stable in frequency with a frequency value that is within the device operating range.

3.3.2. Self-Calibration caused by Changes in Input Frequency

If the selected CKIN frequency varies by 500 ppm or more within the frequency range defined by FRQSEL and FRQTBL since the last calibration, the device may initiate a self-calibration.

3.3.3. Device Reset

Upon powerup, the device internally executes a power-on-reset (POR) which resets the internal device logic. The pin \overline{RST} can also be used to initiate a reset. The device stays in this state until a valid CKINn is present, when it then performs a PLL self-calibration (refer to section 3.3. "PLL Self-Calibration").

3.3.4. Recommended Reset Guidelines

Follow the recommended RESET guidelines in Table 9 that describe when reset should be applied to a device.

Table 9. Si5317 Pins and Reset

| Pin # | Si5317 Pin Name | Must Reset after Changing |
|-------|-----------------|---------------------------|
| 2 | FRQTBL | Yes |
| 11 | RATE0 | Yes |
| 15 | RATE1 | Yes |
| 22 | BWSEL0 | Yes |
| 23 | BWSEL1 | Yes |
| 24 | FRQSEL0 | Yes |
| 25 | FRQSEL1 | Yes |
| 26 | FRQSEL2 | Yes |
| 27 | FRQSEL3 | Yes |

3.4. Alarms

Summary alarms are available to indicate the overall status of the input signals. Alarm outputs stay high until all the alarm conditions for that alarm output are cleared.

3.4.1. Loss-of-Signal

The device has loss-of-signal circuitry that continuously monitors CKIN for missing pulses.

An LOS condition on CKIN causes the LOS alarm to become active. Once a LOS alarm is asserted, it remains asserted until the input clock is validated over a designated time period. The time to clear LOS after a valid input clock appears is listed in Table 4, “AC Characteristics”. If another error condition on the same input clock is detected during the validation time, then the alarm remains asserted and the validation time starts over.

3.4.1.1. LOS Algorithm

The LOS circuitry divides down each input clock to produce an 8 kHz to 2 MHz signal. The LOS circuitry oversamples this divided down input clock using a 40 MHz clock to search for extended periods of time without input clock transitions. If the LOS monitor detects twice the normal number of samples without a clock edge, a LOS alarm is declared. Table 4, “AC Characteristics” gives the minimum and maximum amount of time for the LOS monitor to trigger.

3.4.1.2. Lock Detect

The PLL lock detection algorithm indicates the lock status on the LOL output pin. The algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. If the time between two consecutive phase cycle slips is greater than the retrigger time, the PLL is in lock. The LOL output has a guaranteed minimum pulse width as shown in Table 4, “AC Characteristics”. The LOL pin is also held in the active state during an internal PLL calibration. The retrigger time is automatically set based on the PLL closed loop bandwidth (see Table 10).

Table 10. Lock Detect Retrigger Time

| PLL Bandwidth Setting (BW) | Retrigger Time (ms) |
|----------------------------|---------------------|
| 60–120 Hz | 53 |
| 120–240 Hz | 26.5 |
| 240–480 Hz | 13.3 |
| 480–960 Hz | 6.6 |
| 960–1920 Hz | 3.3 |
| 1920–3840 Hz | 1.66 |
| 3840–7680 Hz | 0.833 |

3.5. VCO Freeze

The Si5317 device features a VCO freeze mode whereby the DSPLL is locked to a frequency value.

If an LOS condition exists on the selected input clock, the device freezes the VCO. In this mode, the device provides a stable output frequency until the input clock returns and is validated. When the device enters VCO freeze, the internal oscillator is initially held to its last frequency value.

3.5.1. Recovery from VCO Freeze

When the input clock signal returns, the device transitions from VCO freeze to the selected input clock.

3.6. PLL Bypass Mode

The Si5317 supports a PLL bypass mode in which the selected input clock is fed directly to both enabled output buffers, bypassing the DSPLL. Internally, the bypass path is implemented with high-speed signaling; however, this path is not a low jitter path and will result in significantly higher jitter on CKOUT. In PLL bypass mode, the input and output clocks will be at the same frequency. PLL bypass mode is useful as a debug tool. The DSBL2_BY pin is used to select the PLL Bypass Mode according to Table 11. Bypass mode is not supported for CMOS clock outputs.

Table 11. DSBL2/BYPASS Pin Settings

| DSBL2/BYPASS | Function |
|--------------|-----------------------------------|
| L | CKOUT2 Enabled |
| M | CKOUT2 Disabled |
| H | PLL Bypass Mode w/ CKOUT2 Enabled |

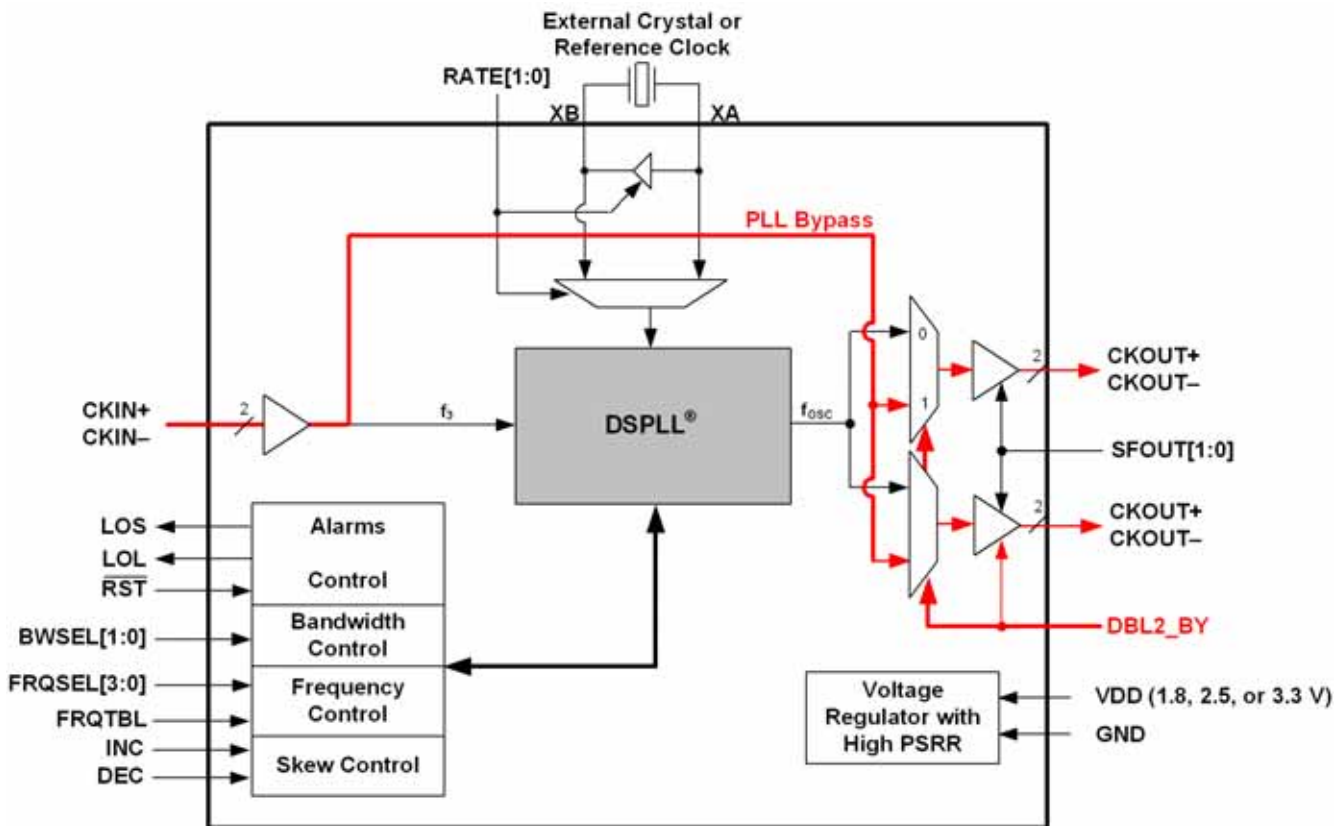


Figure 6. Bypass Signal

4. High-Speed I/O

4.1. Input Clock Buffer

The Si5317 provides differential inputs for the CKIN clock input. This input is internally biased to a common mode voltage (see Table 2, “DC Characteristics”) and can be driven by either a single-ended or differential source. No additional external bias is required. Figure 7 through Figure 10 show typical interface circuits for LVPECL, CML, LVDS, or CMOS input clocks. Note that the jitter generation improves for higher levels on CKINn within the limits in Table 4, “AC Characteristics”.

AC coupling the input clocks is recommended because it removes any issue with common mode input voltages. DC coupling is acceptable if the device driving the Si5317 meets all of the input clock requirements, including the input common mode range and the peak-to-peak swing specifications. Figure 7 and Figure 8 shows various examples of different input termination arrangements. Unused inputs can be left unconnected.

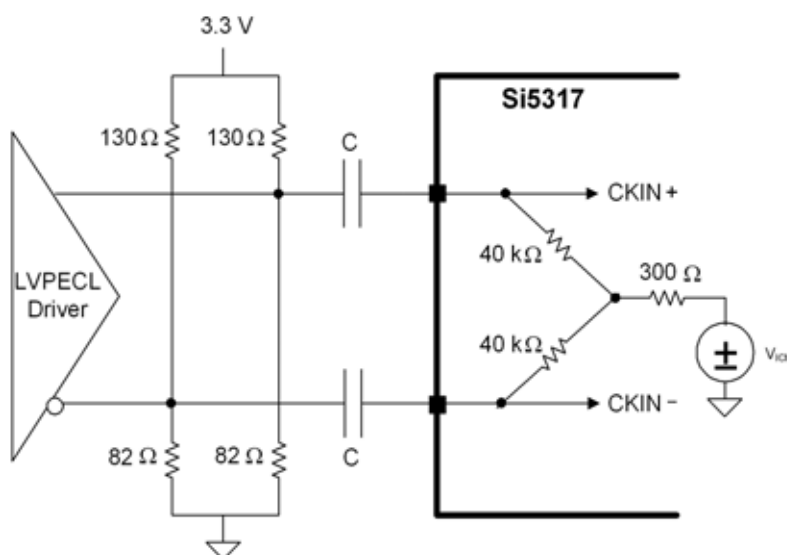


Figure 7. Differential LVPECL Termination

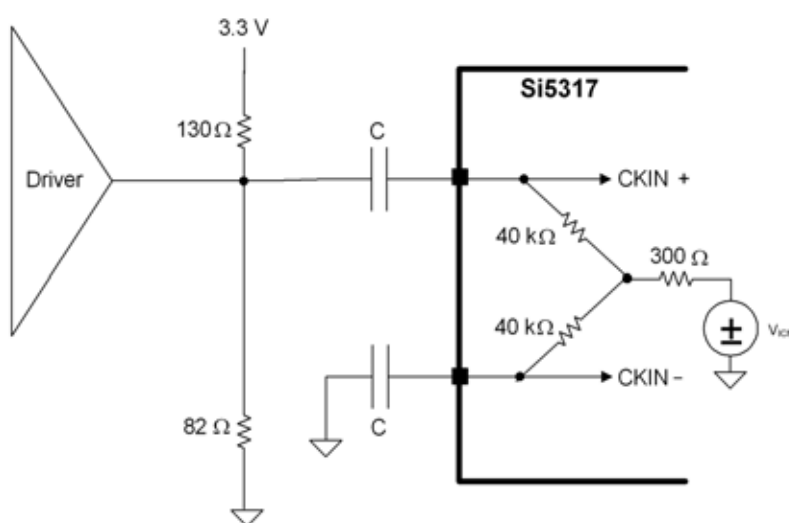


Figure 8. Single-ended LVPECL Termination

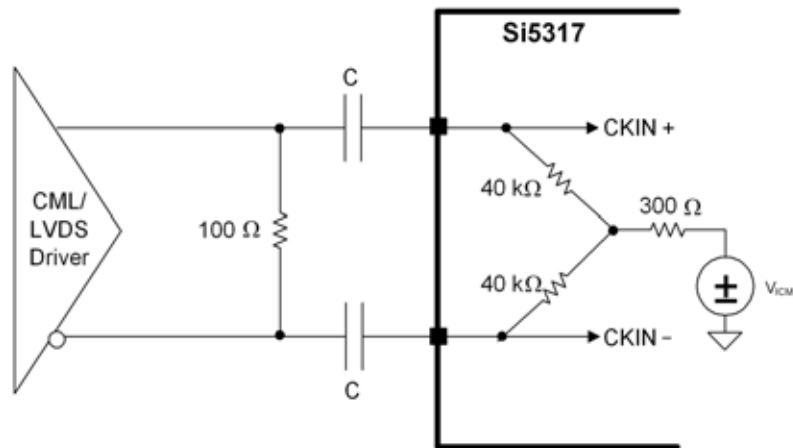
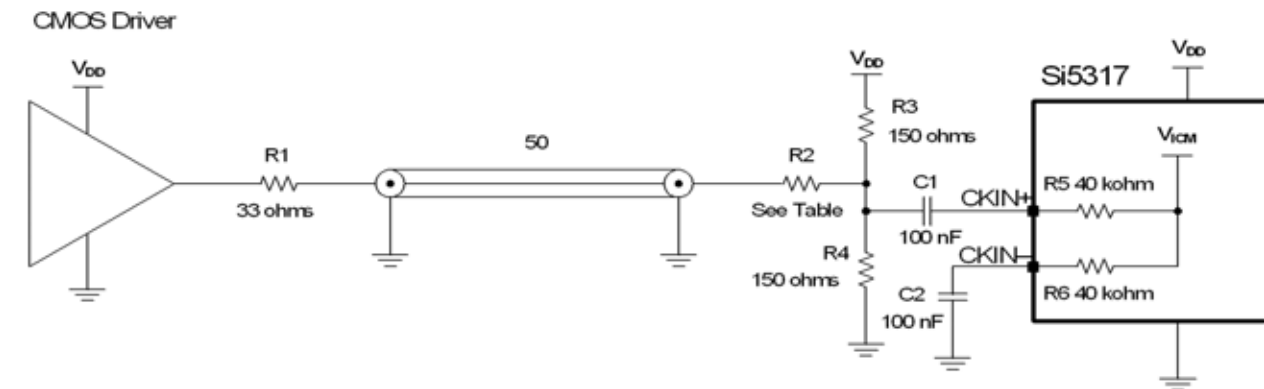


Figure 9. CML/LVDS Termination (1.8, 2.5, 3.3 V)



| V _{DD} | R2 | Notes |
|-----------------|----------|---|
| 3.3 V | 100 ohm | Locate R1 near CMOS driver |
| 2.5 V | 49.9 ohm | Locate other components near Si5317 |
| 1.8 V | 14.7 ohm | Recalculate resistor values for other drive strengths |

- Additional Notes:**
1. Attenuation circuit limits overshoot and undershoot.
 2. Not to be used with non-square wave input clocks.

Figure 10. CMOS Termination with Attenuation and AC-Coupling (1.8, 2.5, 3.3 V)

4.2. Output Clock Driver

The Si5317 has a flexible output driver structure that can drive a variety of loads, including LVPECL, LVDS, CML, and CMOS formats. The signal format is selected for CKOUT output using the SFOUT [1:0] pins. This modifies the output common mode and differential signal swing. See Table 2, “DC Characteristics” for output driver specifications. The SFOUT [1:0] pins are three-level input pins with the states designated as L (ground), M ($V_{DD}/2$), and H (V_{DD}). Table 12 shows the signal formats based on the supply voltage and the type of load being driven. When SFOUT = LH for CMOS, bypass mode is not supported.

Table 12. Output Signal Format Selection (SFOUT)

| SFOUT[1:0] | Signal Format |
|------------|----------------|
| HL | CML |
| HM | LVDS |
| LH | CMOS |
| LM | Disabled |
| MH | LVPECL |
| ML | Low-swing LVDS |
| All Others | Reserved |

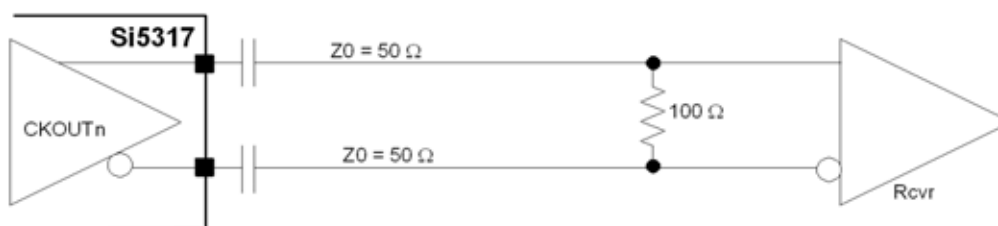


Figure 11. Typical Differential Output Circuit

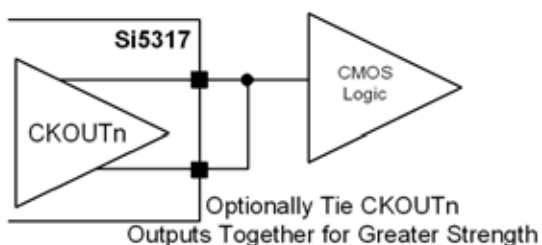


Figure 12. Typical CMOS Output Circuit (Tie CKOUTn+ and CKOUTn- Together)

For the CMOS setting (SFOUT = LH), both output pins drive single-ended in-phase signals and should be externally shorted together to obtain the drive strength specified in Table 2, “DC Characteristics”.

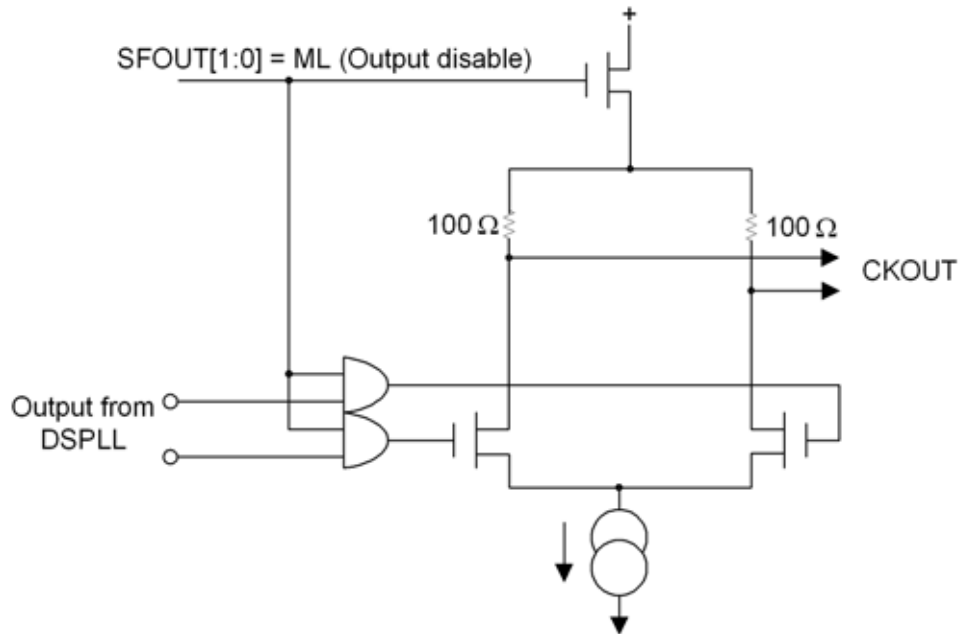
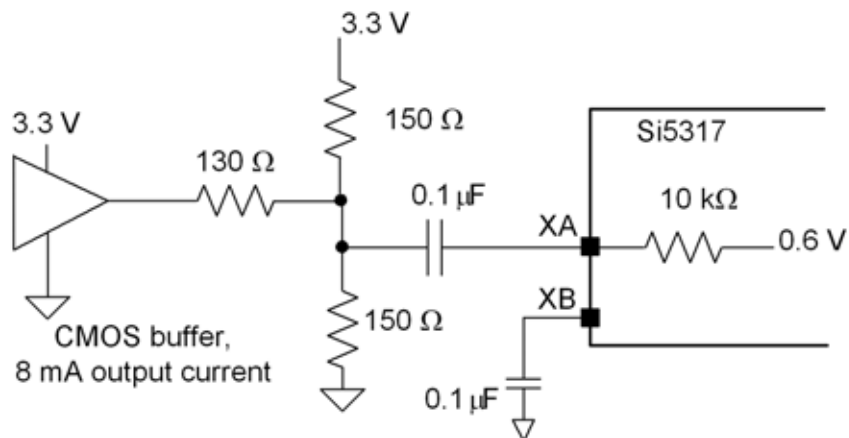


Figure 13. Disable CKOUT Structure

The SFOUT [1:0] pins can also be used to disable both outputs. Disabling the output puts the CKOUT+ and CKOUT- pins in a high-impedance state relative to V_{DD} (common mode tri-state) while the two outputs remain connected to each other through a $200\ \Omega$ on-chip resistance (differential impedance of $200\ \Omega$). The maximum amount of internal circuitry is powered down, minimizing power consumption and noise generation (see Figure 13). Recovery from the disable mode requires additional time as specified in Table 4, “AC Characteristics”.

5. Crystal/Reference Clock Input

The device can use an external crystal or external clock as a reference. If an external clock is used, it must be ac coupled. With appropriate buffers, the same external reference clock can be applied to CKIN. Although the reference clock input can be driven single ended (See Figure 14), the best performance is with a crystal or differential clock source.



For 2.5 V operation, change 130 Ω to 82 Ω .

Figure 14. CMOS External Reference Circuit

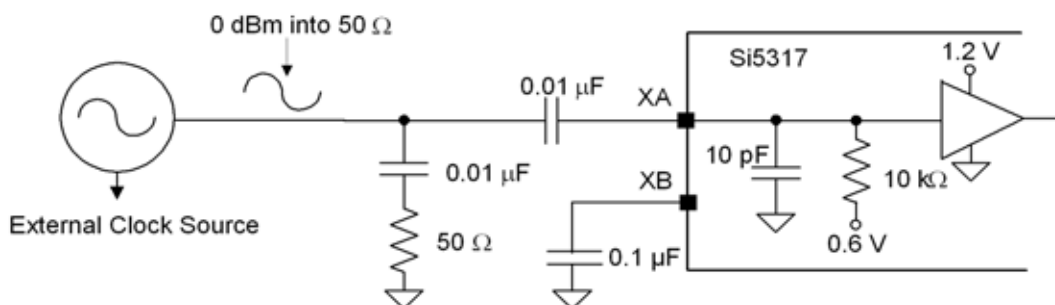


Figure 15. Sinewave External Reference Clock Input Example

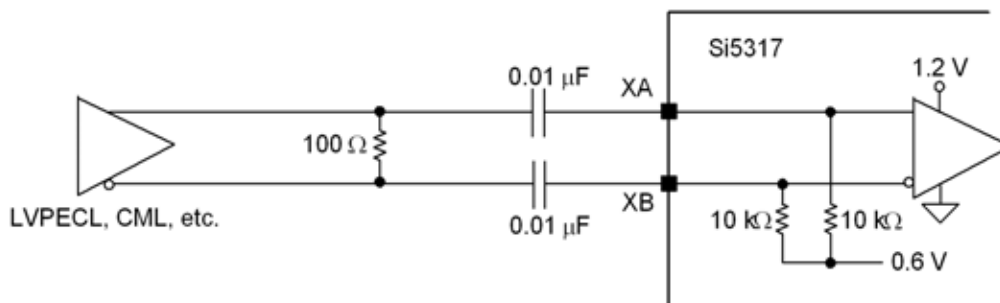


Figure 16. Differential External Reference Clock Input Example

5.1. Crystal/Reference Clock Selection

An external low-jitter clock or a low-cost crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external clock is required for the device to perform jitter attenuation. Silicon Laboratories recommends using a high-quality crystal.

In VCO freeze, the DSPLL remains locked to this external clock. Any changes in the frequency of this clock when the DSPLL is in VCO freeze will be tracked by the output of the device. Note that crystals can have temperature sensitivities. See “AN591: Crystal Selection for the Si5315 and Si5317” for a list of approved crystals for the Si5317 and guidance in their selection. AN591 can be downloaded from the Silicon Labs web site: www.silabs.com.

Table 13. XA/XB Reference Sources and Frequencies

| RATE[1:0] | Type | Recommended | Lower limit | Upper limit |
|-----------|---------------------------|-------------|-------------|-------------|
| HH | Reserved | — | — | — |
| HM | Reserved | — | — | — |
| HL | Reserved | — | — | — |
| MH | External clock | 114.285 MHz | 109 MHz | 125.5 MHz |
| MM | 3rd overtone crystal* | 114.285 MHz | — | — |
| ML | Reserved | — | — | — |
| LH | Reserved | — | — | — |
| LM | External clock | 38.88 MHz | 37 MHz | 41 MHz |
| LL | Fundamental mode crystal* | — | — | — |

***Note:** See “AN591: Crystal Selection for the Si5315 and Si5317.”

Because the crystal is used as a jitter reference, rapid changes of the crystal temperature can temporarily disturb the output phase and frequency. For example, it is recommended that the crystal not be placed close to a fan that is being turned off and on. If a situation such as this is unavoidable, the crystal should be thermally isolated with an insulating cover.

5.1.1. XA/XB Clock Drift

During VCO freeze, long-term and temperature-related drift of the XA/XB clock input results in a one-to-one drift of the output frequency. The stability of the any frequency output is identical to the drift of the XA/XB frequency. This means that for the most demanding applications where the drift of a crystal is not acceptable, an external temperature-compensated or ovenized oscillator will be required. Drift is not an issue unless the part is in VCO freeze. Also, the initial accuracy of the XA/XB oscillator (or crystal) is not relevant.

5.1.2. XA/XB Jitter

Jitter on the XA/XB input has a roughly one-to-one transfer function to the output jitter over the bandwidth ranging from 100 Hz up to 30 kHz. If a crystal is used on the XA/XB pins, this will have low jitter if a suitable crystal is in use. If the XA/XB pins are connected to an external oscillator, the jitter of the external oscillator may contribute significantly to the output jitter.

5.1.3. Jitter Attenuation Performance

The internal VCO uses the XA/XB clock on the XA/XB pins as its reference for jitter attenuation. The XA/XB pins support either a crystal input or an input buffer single-ended or differential clock input, such that an external oscillator can become the reference source. In either case, the device accepts a wide margin in absolute frequency of the XA/XB input (refer to section 3.5.1. "Recovery from VCO Freeze" on page 23). In VCO freeze, the Si5317's output clock stability matches the clock supplied on the XA/XB pins. The external crystal or clock must be selected based on the stability requirements of the application if VCO freeze is a key requirement. However, care must be exercised in certain areas for optimum performance. For examples of connections to the XA/XB pins, refer to section 5. Figure 22, "Si5317 Typical Application Circuit," on page 35.

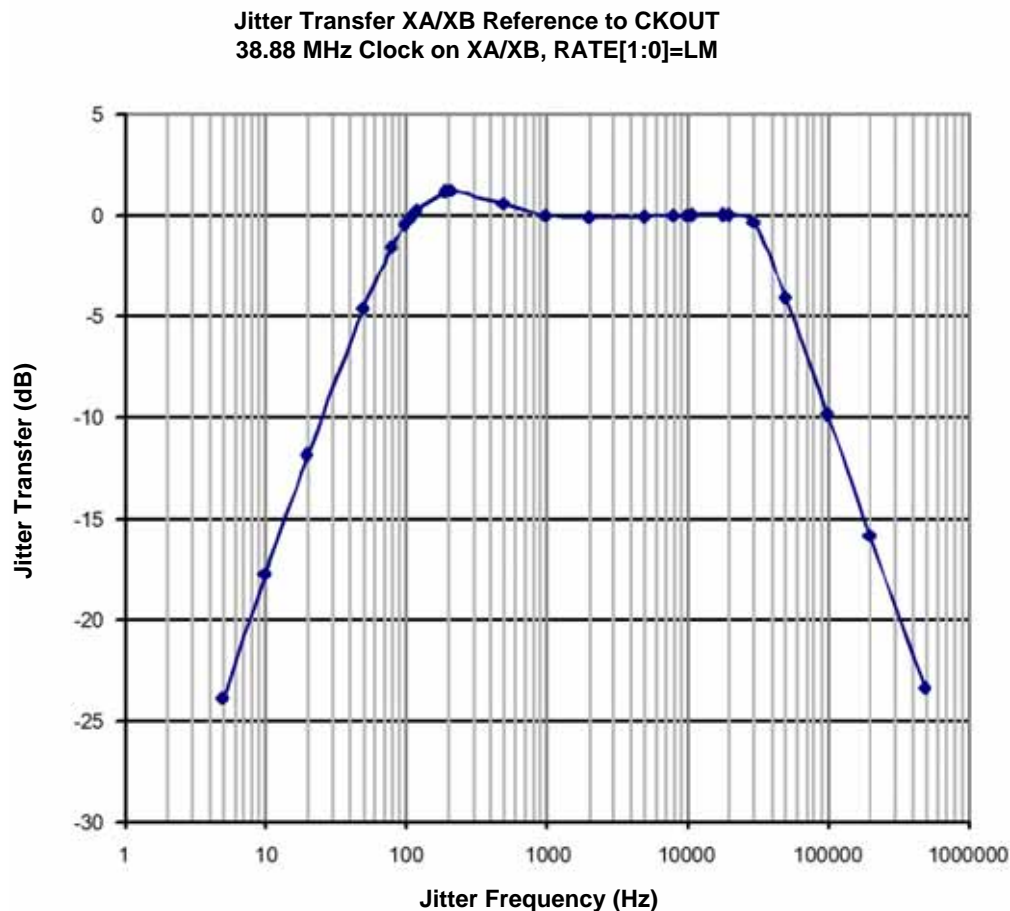


Figure 17. Typical XA-XB Jitter Transfer Function

5.1.4. Reference Clock Frequency

Based on the application and desired output frequency, care should be exercised in selecting the frequency on the reference used for XA/XB. When the CKOUT operating frequency is close to having a simple integer relationship, significant spurs can occur. For example, compare the spurs when the CKOUT operating frequency is 622.08 MHz with a reference of 114.285 MHz (see Figure 21) versus a reference frequency of 38.88 MHz, which is 16 times the XA/XB reference (see Figure 18).

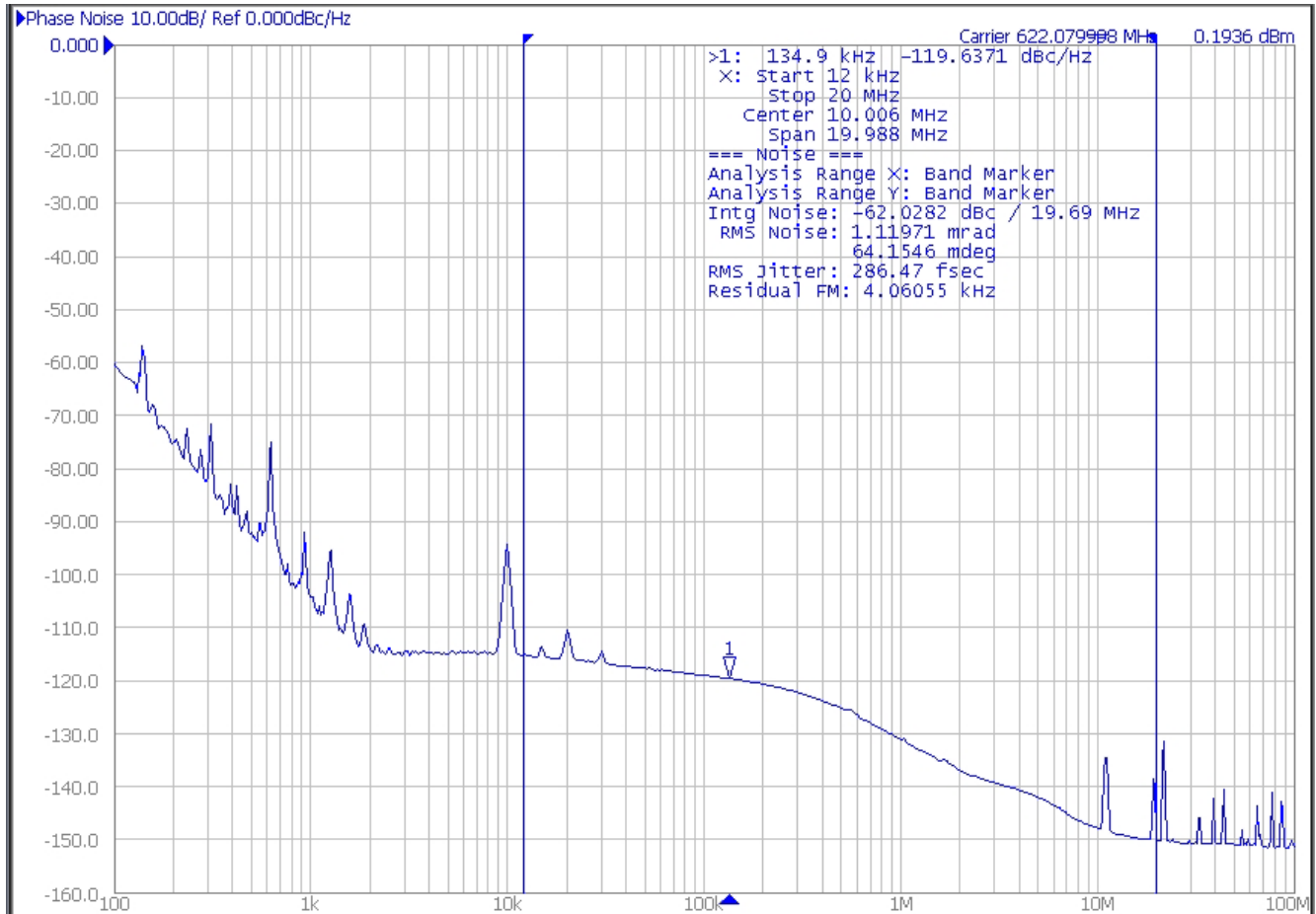


Figure 18. Effect of Reference Frequency on Spurs

6. Power Supply Filtering

This device incorporates an on-chip voltage regulator to power the device from supply voltages of 1.8, 2.5, or 3.3 V. Internal core circuitry is driven from the output of this regulator while I/O circuitry uses the external supply voltage directly. Table 4, "AC Characteristics" gives the sensitivity of the on-chip oscillator to changes in the supply voltage. The center ground pad under the device must be electrically and thermally connected to the ground plane. See Figure 25, "Ground Pad Recommended Layout," on page 42.

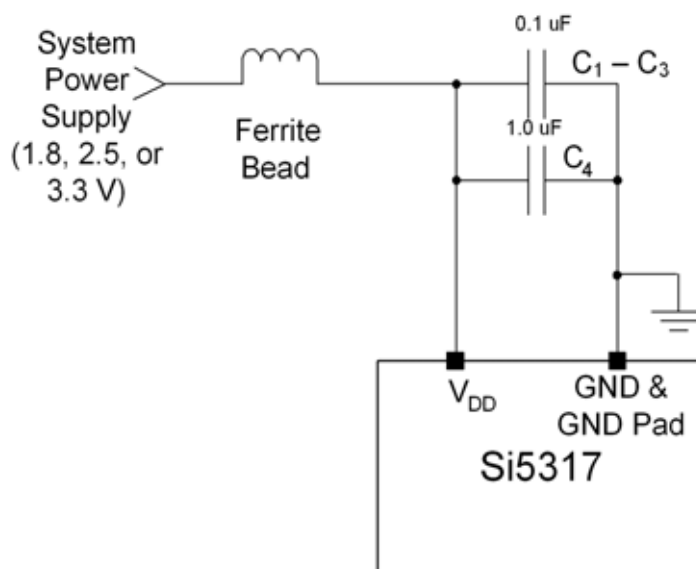


Figure 19. Typical Power Supply Bypass Network

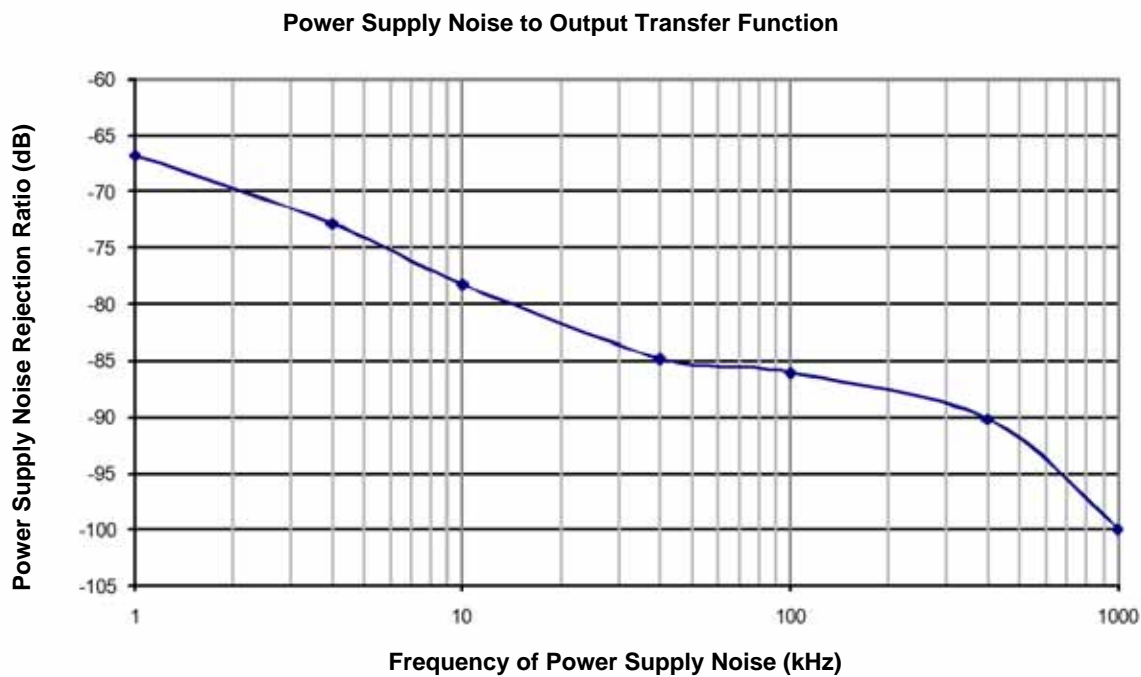


Figure 20. $F_{in} = F_{out} = 155$ MHz with 120 Hz Loop Bandwidth, 100 mV, pk-pk Supply Noise

7. Typical Phase Noise Plots

The following is a typical phase noise plot. The clock input source was a Rohde and Schwarz model SML03 RF Generator. The phase noise analyzer was an Agilent model E5052B. The Si5317 operates at 3.3 V with an ac coupled differential PECL output and an ac coupled differential sine wave input from the RF generator at 0 dBm. Note that, as with any PLL, the output jitter that is below the loop BW is caused by the jitter at the input clock. The loop BW was 120 Hz.

7.1. Example: SONET OC-192

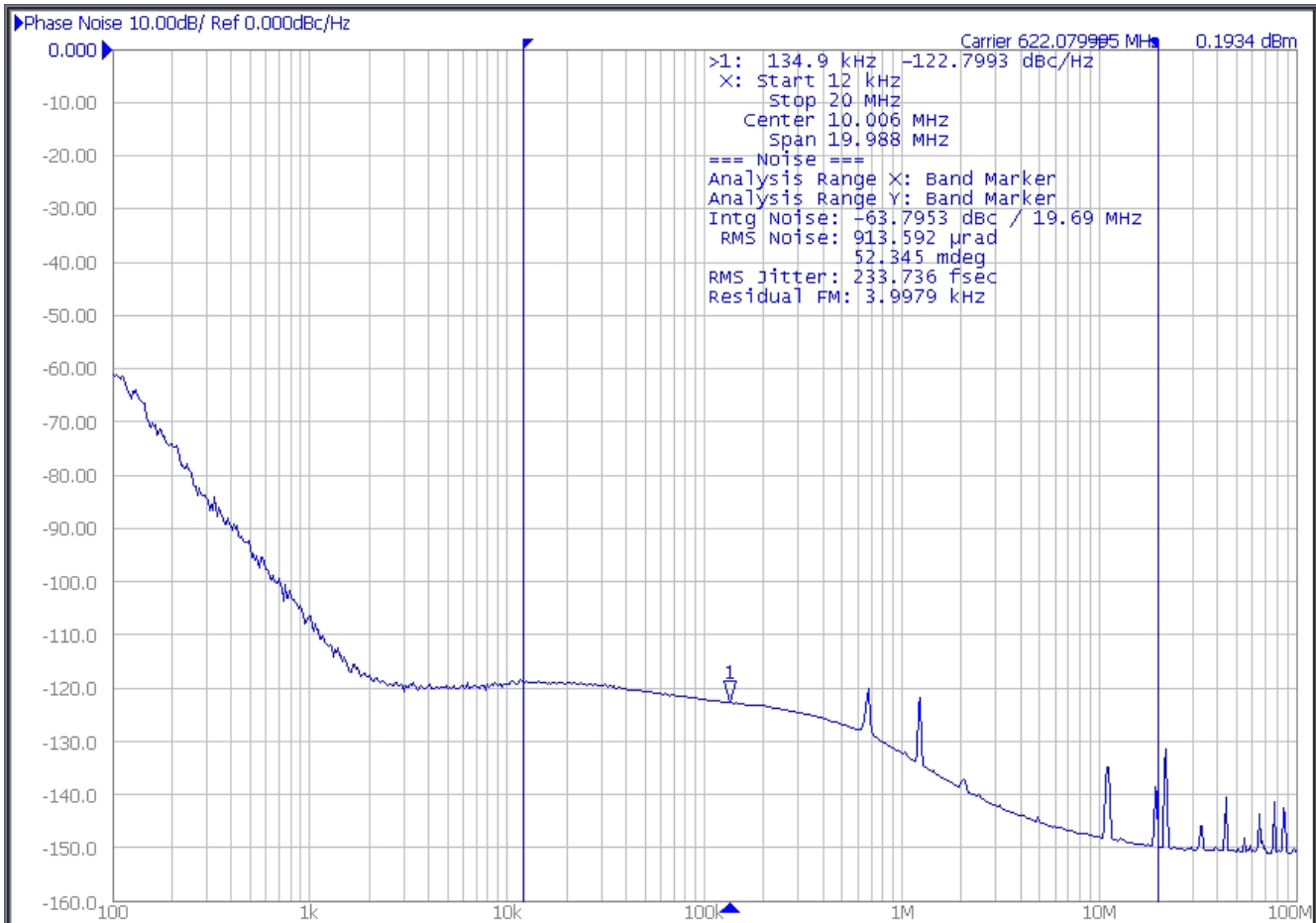


Figure 21. Typical Phase Noise Plot

| Jitter Band | Jitter, RMS |
|---------------------------------|-------------|
| SONET_OC48, 12 kHz to 20 MHz | 250 fs |
| SONET_OC192_A, 20 kHz to 80 MHz | 274 fs |
| SONET_OC192_B, 4 to 80 MHz | 166 fs |
| SONET_OC192_C, 50 kHz to 80 MHz | 267 fs |
| Brick Wall, 800 Hz to 80 MHz | 274 fs |

Note: SONET jitter bands include the SONET skirts. The phase noise plot is brick wall integration.

8. Typical Application Circuit

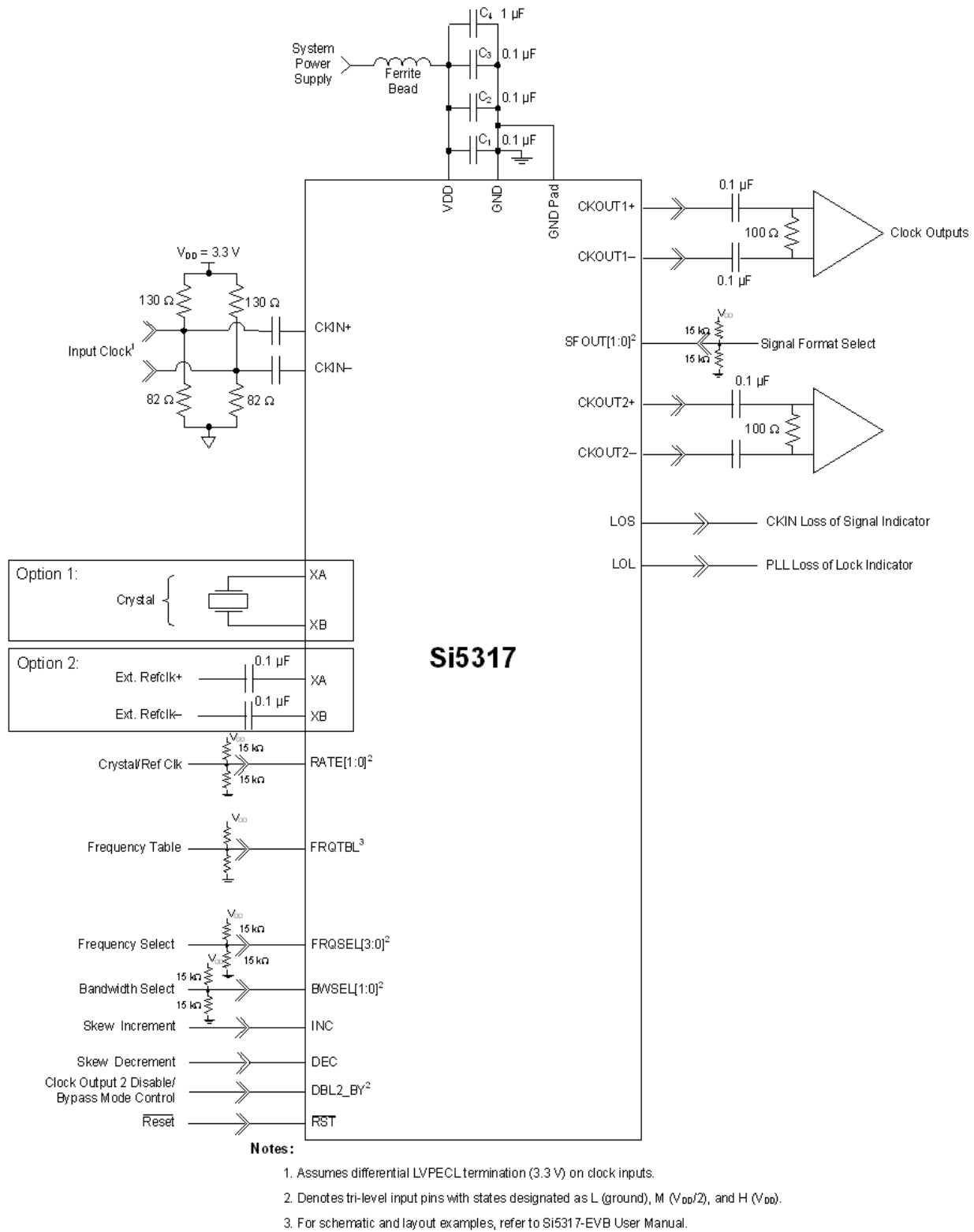
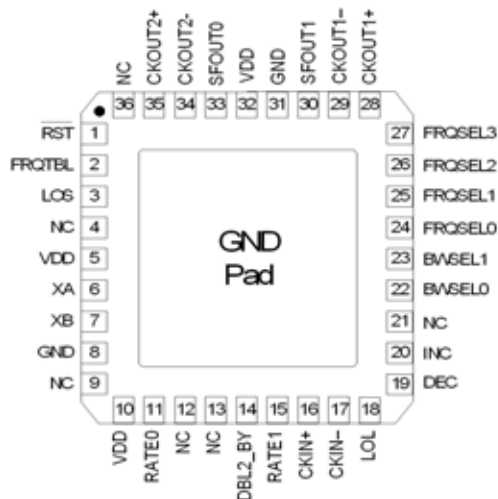


Figure 22. Si5317 Typical Application Circuit

9. Pin Descriptions: Si5317



Note: Pin assignments are preliminary and subject to change.

Table 14. Si5317 Pin Descriptions

| Pin # | Pin Name | I/O | Signal Level | Description |
|-----------|-------------------------|-----------------|--------------|---|
| 1 | $\overline{\text{RST}}$ | I | LVC MOS | External Reset. Active low input that performs external hardware reset of device. Resets all internal logic to a known state. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the Si5317 will perform an internal self-calibration when a valid input signal is present. This pin has a weak pull-up. |
| 2 | FRQTBL | I | 3-level | Frequency Table. Selects frequency table. This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. |
| 3 | LOS | O | LVC MOS | CKIN Loss of Signal. Active high loss-of-signal indicator for CKIN. Once triggered, the alarm will remain active until CKIN is validated. 0 = CKIN present 1 = LOS on CKIN |
| 5, 10, 32 | V _{DD} | V _{DD} | Supply | Supply. The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V _{DD} pins: 5 0.1 μF 10 0.1 μF 32 0.1 μF A 1.0 μF should also be placed as close to device as is practical. |

Table 14. Si5317 Pin Descriptions (Continued)

| Pin # | Pin Name | I/O | Signal Level | Description |
|----------|----------------|-----|--------------|---|
| 7 6 | XB XA | I | Analog | External Crystal or Reference Clock. External crystal should be connected to these pins to use internal oscillator-based reference. Crystal or reference clock selection is set by the XTAL/CLOCK pin. See “AN591: Crystal Selection for the Si5315 and Si5317.” |
| 8,31 | GND | GND | Supply | Ground. Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device. |
| 11 15 | RATE0 RATE1 | I | 3-Level | External Crystal or Reference Clock Rate. Note: See Table 13 for settings. |
| 14 | DBL2_BY | I | 3-Level | Output 2 Disable/Bypass Mode Control. Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode. L = CKOUT2 enabled M = CKOUT2 disabled H = Bypass mode with CKOUT2 enabled This pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. Bypass mode is not supported for CMOS clock outputs. |
| 16 17 | CKIN+ CKIN- | I | Multi | Clock Input. Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from Table 9 on page 22. |
| 18 | LOL | O | LVC MOS | PLL Loss of Lock Indicator. This pin functions as the active high PLL loss of lock indicator. 0 = PLL locked 1 = PLL unlocked |
| 19 | DEC | I | LVC MOS | Skew Decrement. This edge-triggered pin decreases the input to output device skew. There is no limit on the range of skew adjustment by this method. Detailed operations and timing characteristics for this pin are found in Section 3.2, Table 8. This pin has a weak pull-down. |
| 20 | INC | I | LVC MOS | Skew Increment. This edge-triggered pin increases the input to output device skew. There is no limit on the range of skew adjustment by this method. Detailed operations and timing characteristics for this pin are found in Section 3.2, Table 8. This pin has a weak pull-down. |

Table 14. Si5317 Pin Descriptions (Continued)

| Pin # | Pin Name | I/O | Signal Level | Description | | | | | | | | | | | | | | | | | | | | |
|----------------------|--|-----|--------------|---|------------|---------------|----|----------|----|------|----|-----|----|--------|----|----------|----|----------------|----|------|----|---------|----|----------|
| 23 22 | BWSEL1 BWSEL0 | I | 3-Level | <p>Loop Bandwidth Select.</p> <p>Three level inputs that select the DSPLL closed loop bandwidth. See Table 9 on page 22 for available settings. These pins have both weak pull-ups and weak pull-downs and default to M.</p> <p>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.</p> | | | | | | | | | | | | | | | | | | | | |
| 27 26 25 24 | FRQSEL3 FRQSEL2 FRQSEL1 FRQSEL0 | | | <p>Frequency Select.</p> <p>Three level inputs that select the input clock and clock range. See Table 9 on page 22.</p> <p>These pins have both weak pull-ups and weak pull-downs and default to M.</p> <p>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.</p> | | | | | | | | | | | | | | | | | | | | |
| 29 28 | CKOUT1– CKOUT1+ | O | Multi | <p>Clock Output 1.</p> <p>Output signal format is selected by SFOUT pins. Differential formats supported for LVPECL, LVDS, and CML compatible modes. For single-ended CMOS format, both output pins drive identical, in-phase clock outputs.</p> | | | | | | | | | | | | | | | | | | | | |
| 33 30 | SFOUT0 SFOUT1 | I | 3-Level | <p>Signal Format Select.</p> <p>Three-level inputs that select the output signal format (common mode voltage and differential swing) for both CKOUT1 and CKOUT2.</p> <table border="1" data-bbox="891 1077 1382 1528"> <thead> <tr> <th>SFOUT[1:0]</th> <th>Signal Format</th> </tr> </thead> <tbody> <tr> <td>HH</td> <td>Reserved</td> </tr> <tr> <td>HM</td> <td>LVDS</td> </tr> <tr> <td>HL</td> <td>CML</td> </tr> <tr> <td>MH</td> <td>LVPECL</td> </tr> <tr> <td>MM</td> <td>Reserved</td> </tr> <tr> <td>ML</td> <td>LVDS—Low Swing</td> </tr> <tr> <td>LH</td> <td>CMOS</td> </tr> <tr> <td>LM</td> <td>Disable</td> </tr> <tr> <td>LL</td> <td>Reserved</td> </tr> </tbody> </table> <p>These pins have both weak pull-ups and weak pull-downs and default to M.</p> <p>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.* CMOS outputs do not support bypass mode.</p> | SFOUT[1:0] | Signal Format | HH | Reserved | HM | LVDS | HL | CML | MH | LVPECL | MM | Reserved | ML | LVDS—Low Swing | LH | CMOS | LM | Disable | LL | Reserved |
| SFOUT[1:0] | Signal Format | | | | | | | | | | | | | | | | | | | | | | | |
| HH | Reserved | | | | | | | | | | | | | | | | | | | | | | | |
| HM | LVDS | | | | | | | | | | | | | | | | | | | | | | | |
| HL | CML | | | | | | | | | | | | | | | | | | | | | | | |
| MH | LVPECL | | | | | | | | | | | | | | | | | | | | | | | |
| MM | Reserved | | | | | | | | | | | | | | | | | | | | | | | |
| ML | LVDS—Low Swing | | | | | | | | | | | | | | | | | | | | | | | |
| LH | CMOS | | | | | | | | | | | | | | | | | | | | | | | |
| LM | Disable | | | | | | | | | | | | | | | | | | | | | | | |
| LL | Reserved | | | | | | | | | | | | | | | | | | | | | | | |
| 34 35 | CKOUT2– CKOUT2+ | O | Multi | <p>Clock Output 2.</p> <p>Output signal format is selected by SFOUT pins. Differential formats supported for LVPECL, LVDS, and CML compatible modes. For single-ended CMOS format, both output pins drive identical, in-phase clock outputs.</p> | | | | | | | | | | | | | | | | | | | | |

Table 14. Si5317 Pin Descriptions (Continued)

| Pin # | Pin Name | I/O | Signal Level | Description |
|---------------------|----------|-----|--------------|---|
| 4,9,12,13, 21,36 | NC | — | — | No Connect. Leave floating. Make no external connections to this pin for normal operation. |
| GND PAD | GND | GND | Supply | Ground Pad. The ground pad must provide a low thermal and electrical impedance to a ground plane. |

***Note:** LVPECL requires VDD \geq 2.25 V

Table 15. Si5317 Pull-Up/-Down

| Pin # | Si5317 | Pull? |
|-------|-------------------------|-------|
| 1 | $\overline{\text{RST}}$ | U |
| 2 | FRQTBL | U, D |
| 11 | RATE0 | U, D |
| 15 | RATE1 | U, D |
| 19 | DEC | D |
| 20 | INC | D |
| 22 | BWSEL0 | U, D |
| 23 | BWSEL1 | U, D |
| 24 | FRQSEL0 | U, D |
| 25 | FRQSEL1 | U, D |
| 26 | FRQSEL2 | U, D |
| 27 | FRQSEL3 | U, D |
| 30 | SFOUT1 | U, D |
| 33 | SFOUT0 | U, D |

Si5317

10. Ordering Guide

| Ordering Part Number | Output Clock Freq Range | Device Pkg | ROHS6, Pb-Free | Temp Range |
|----------------------|-------------------------|----------------------|----------------|--------------|
| Si5317A-C-GM | 1–711 MHz | 36-Lead 6 x 6 mm QFN | Yes | –40 to 85 °C |
| Si5317B-C-GM | 1–350 MHz | 36-Lead 6 x 6 mm QFN | Yes | –40 to 85 °C |
| Si5317C-C-GM | 1–200 MHz | 36-Lead 6 x 6 mm QFN | Yes | –40 to 85 °C |
| Si5317D-C-GM | 1–100 MHz | 36-Lead 6 x 6 mm QFN | Yes | –40 to 85 °C |
| Si5317-EVB | 1–711 MHz | Evaluation Board | | |

Note: Add an “R” at the end of the device to denote tape and reel options (i.e., Si5317A-C-GMR).

11. Package Outline: 36-Pin QFN

Figure 23 illustrates the package details for the Si5317. Table 16 lists the values for the dimensions shown in the illustration.

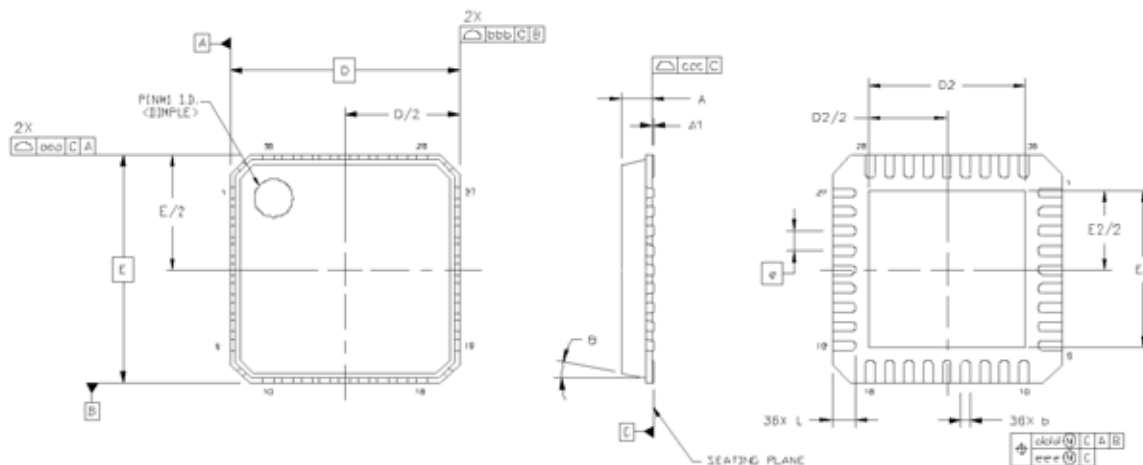


Figure 23. 36-Pin Quad Flat No-Lead (QFN)

Table 16. Package Dimensions

| Symbol | Millimeters | | | Symbol | Millimeters | | |
|--------|-------------|------|------|----------|-------------|------|------|
| | Min | Nom | Max | | Min | Nom | Max |
| A | 0.80 | 0.85 | 0.90 | L | 0.50 | 0.60 | 0.70 |
| A1 | 0.00 | 0.02 | 0.05 | θ | — | — | 12° |
| b | 0.18 | 0.25 | 0.30 | aaa | — | — | 0.10 |
| D | 6.00 BSC | | | bbb | — | — | 0.10 |
| D2 | 3.95 | 4.10 | 4.25 | ccc | — | — | 0.08 |
| e | 0.50 BSC | | | ddd | — | — | 0.10 |
| E | 6.00 BSC | | | eee | — | — | 0.05 |
| E2 | 3.95 | 4.10 | 4.25 | | | | |

Notes:

- All dimensions shown are in millimeters (mm) unless otherwise noted.
- Dimensioning and Tolerancing per ANSI Y14.5M-1994.
- This drawing conforms to JEDEC outline MO-220, variation VJJD.
- Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Recommended PCB Layout

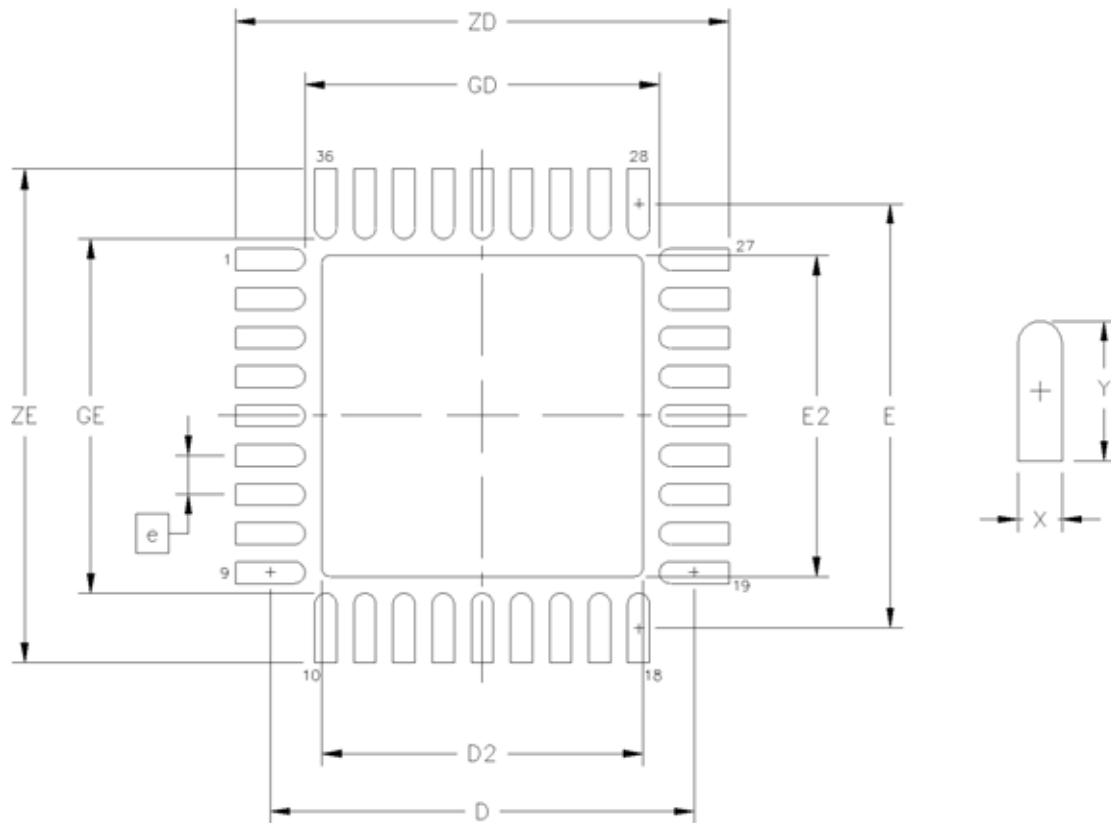


Figure 24. PCB Land Pattern Diagram

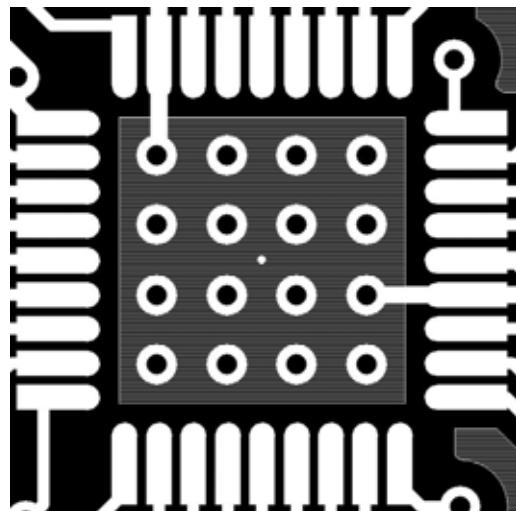


Figure 25. Ground Pad Recommended Layout

Table 17. PCB Land Pattern Dimensions

| Dimension | MIN | MAX |
|-----------|-----------|------|
| e | 0.50 BSC. | |
| E | 5.42 REF. | |
| D | 5.42 REF. | |
| E2 | 4.00 | 4.20 |
| D2 | 4.00 | 4.20 |
| GE | 4.53 | — |
| GD | 4.53 | — |
| X | — | 0.28 |
| Y | 0.89 REF. | |
| ZE | — | 6.31 |
| ZD | — | 6.31 |

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Si5317

13. Si5317 Device Top Mark



| | | |
|------------------------|----------------------------|---|
| Mark Method: | Laser | |
| Font Size: | 0.80 mm Right-Justified | |
| Line 1 Marking: | Si5317Q | Customer Part Number Q = Speed Code: A, B, C, D See Ordering Guide for options. |
| Line 2 Marking: | C-GM | C = Product Revision G = Temperature Range -40 to 85 °C (RoHS6) M = QFN Package |
| Line 3 Marking: | YYWWRF | YY = Year WW = Work Week R = Die Revision F = Internal code Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |
| Line 4 Marking: | Pin 1 Identifier | Circle = 0.75 mm Diameter Lower-Left Justified |
| | XXXX | Internal Code |

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.15

- Updated corresponding sections and pinouts to add CKOUT2, INC/DEC, and DBL2_BY functionality.
- Updated functional block diagram on page 1.
- Updated Table 2 IDD (DD is subscript).
- Added Differential Rise/Fall Time spec to Table 2.
- Updated pin assignment symbol and pin description on page 1 and in section 9 to add CKOUT2, INC/DEC, and DBL2_BY.
- Added section 3.6. "PLL Bypass Mode".
- Updated section 8 diagram to add CKOUT2 and DBL2_BY.
- Added additional CMOS Termination with attenuation figure.
- Corrected pin name assignment (pin28) diagram on page 1 and section 9, page 35 to match pin description name.
- Updated all the frequency plans in Table 8 to provide coverage over the entire frequency range.

Revision 0.15 to Revision 0.2

- Updated bypass mode, ESD specifications and absolute max V_{DD} .
- Corrected INC/DEC pinout.

Revision 0.2 to Revision 1.0

- Removed Output Short to GND on page 5.
- Removed duplicate lock time specification on page 11.
- Removed Time to Clear LOS alarm on page 11.
- Revised spurious noise values.
- Revised phase noise values.

Revision 1.0 to Revision 1.1

- Increased the maximum input/output frequency to 711 MHz
- Added reference to "AN591: Crystal Selection for the Si5315 and Si5317"



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400 West Cesar Chavez
Austin, TX 78701
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Тел: +7 (812) 336 43 04 (многоканальный)

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