74LVC273-Q100

Octal D-type flip-flop with reset; positive-edge trigger

Rev. 1 — 16 September 2013 Product data sheet

1. General description

The 74LVC273-Q100 has eight edge-triggered, D-type flip-flops with individual Dn inputs and Qn outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The state of each Dn input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. All outputs are forced LOW independent of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at +85 °C
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC273D-Q100	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC273PW-Q100	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVC273BQ-Q100	–40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

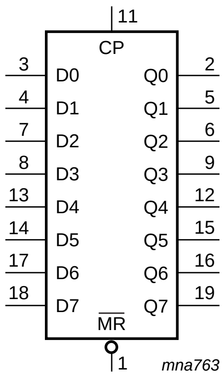


Fig 1. Logic symbol

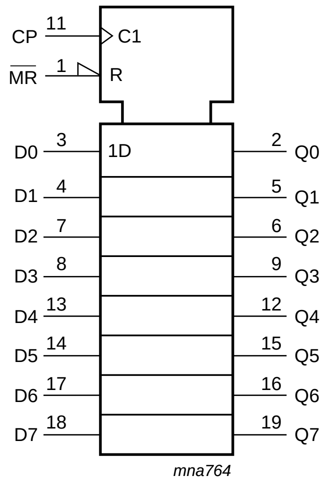


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning

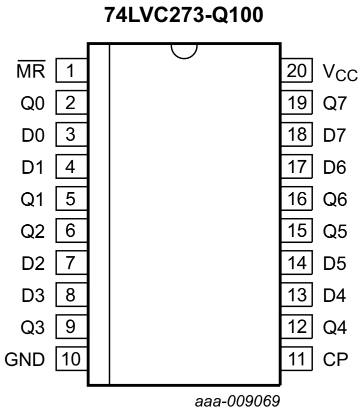
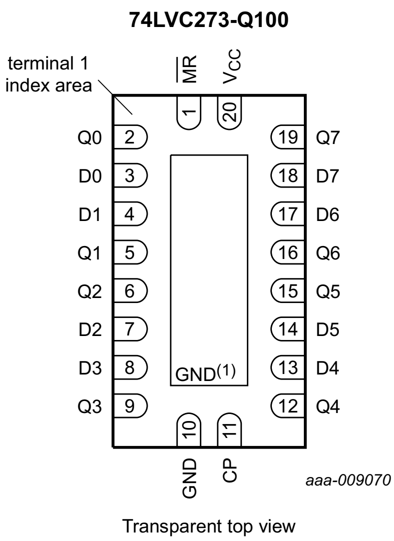


Fig 3. Pin configuration for SO20 and TSSOP20



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 4. Pin configuration for DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{MR}$	1	master reset input (active LOW)
CP	11	clock input (LOW-to-HIGH; edge-triggered)
D[0:7]	3, 4, 7, 8, 13, 14, 17, 18	data input
Q[0:7]	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
GND	10	ground (0 V)
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table[1]

Operating mode	Input			Output
	$\overline{MR}$	CP	Dn	Qn
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH clock transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	50	mA
V_O	output voltage		[2]	–0.5	V_{CC} + 0.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN20 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V

Table 5. Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} – 0.2	-	-	V_{CC} – 0.3	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V; I_O = 0 A	-	5	500	-	5000	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Figure 8.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Figure 5 [2]						
		V_{CC} = 1.2 V	-	18	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.5	9.7	19.2	2.5	22.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.8	4.9	9.9	1.8	11.4	ns
		V_{CC} = 2.7 V	1.5	4.5	8.4	1.5	10.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	4.1	8.2	1.5	10.5	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Figure 6						
		V_{CC} = 1.2 V	-	18	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.4	10.2	20.4	2.4	23.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	5.2	10.5	1.7	12.1	ns
		V_{CC} = 2.7 V	1.5	4.7	8.9	1.5	11.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	4.3	8.7	1.5	11.0	ns
t_W	pulse width	clock HIGH or LOW; see Figure 5						
		V_{CC} = 1.65 V to 1.95 V	6.0	-	-	6.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	-	-	5.0	-	ns
		V_{CC} = 2.7 V	5.0	1.8	-	5.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	4.0	1.2	-	4.0	-	ns
		master reset LOW; see Figure 6						
		V_{CC} = 1.65 V to 1.95 V	6.0	-	-	6.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	-	-	5.0	-	ns
		V_{CC} = 2.7 V	5.0	1.7	-	5.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	4.0	1.2	-	4.0	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 6						
		V_{CC} = 1.65 V to 1.95 V	2.0	-	-	2.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns
		V_{CC} = 2.7 V	2.0	–1.0	-	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	–1.0	-	2.0	-	ns
t_{su}	set-up time	Dn to CP; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	3.5	-	-	3.5	-	ns
		V_{CC} = 2.7 V	3.0	1.0	-	3.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	0.0	-	1.0	-	ns
t_h	hold time	Dn to CP; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V_{CC} = 2.7 V	2.0	–0.2	-	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	0.0	-	1.0	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit, see Figure 8.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
f_{max}	maximum frequency	see Figure 5							
		V_{CC} = 1.65 V to 1.95 V		80	-	-	64	-	MHz
		V_{CC} = 2.3 V to 2.7 V		100	-	-	80	-	MHz
		V_{CC} = 2.7 V		150	-	-	150	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	230	-	150	-	MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	14.0	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	17.7	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	21.0	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

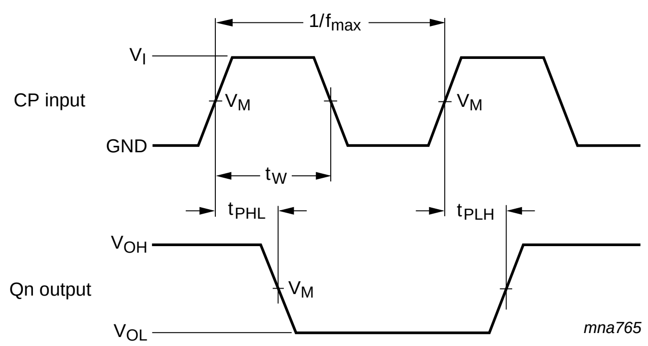
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volt

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

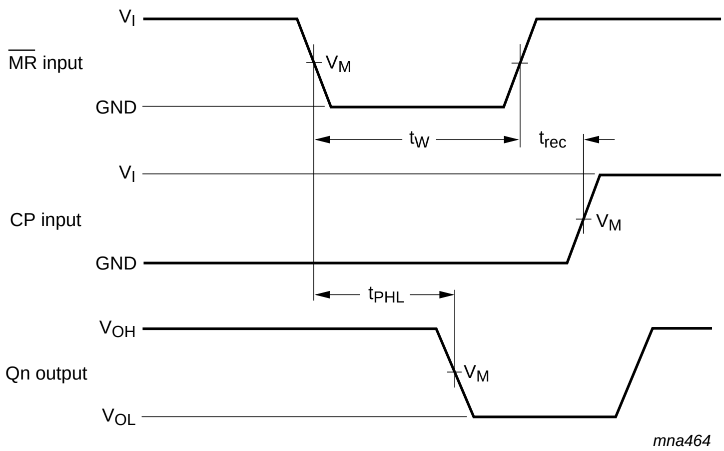
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

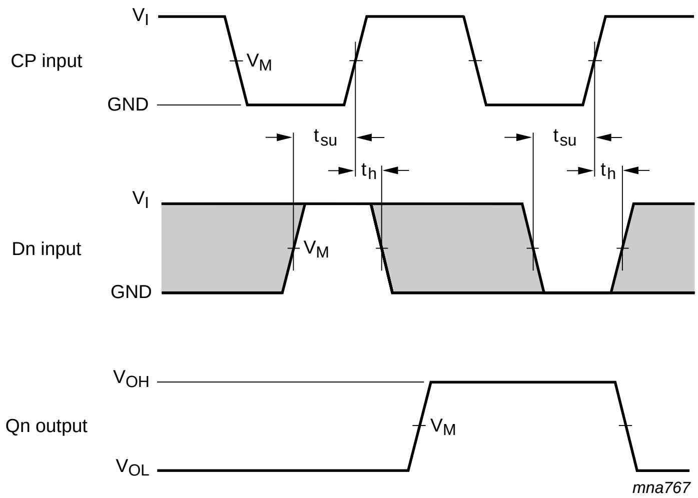
Fig 5. Clock (CP) to output (Qn) propagation delays, the clock pulse width, and the maximum frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. Master reset ($\overline{MR}$) pulse width, the master reset to output (Qn) propagation delays, and the master reset to clock (CP) recovery time



Measurement points are given in Table 8.

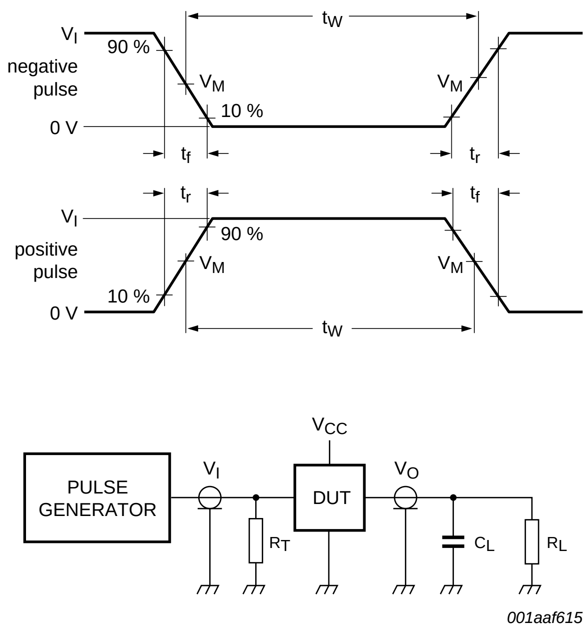
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 7. Data set-up and hold times for the data input (Dn)

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
1.65 V to 1.95 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

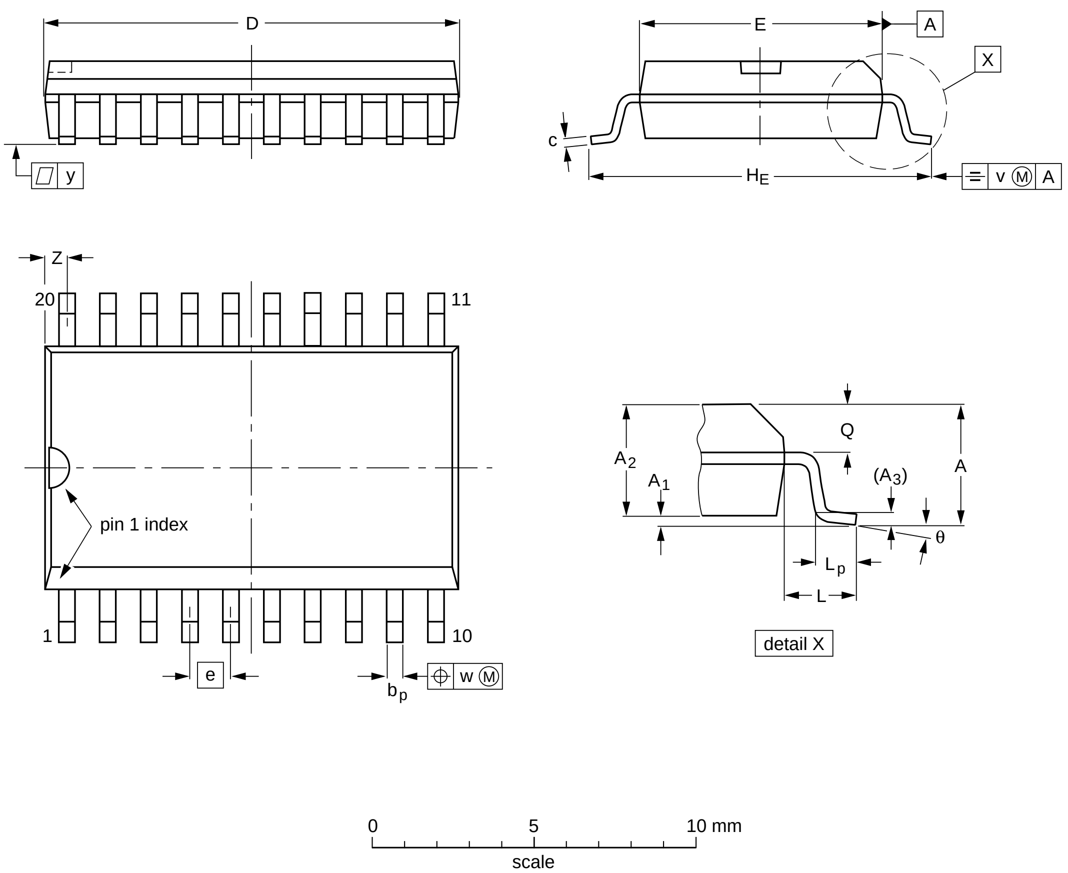
Fig 8. Load circuitry for switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

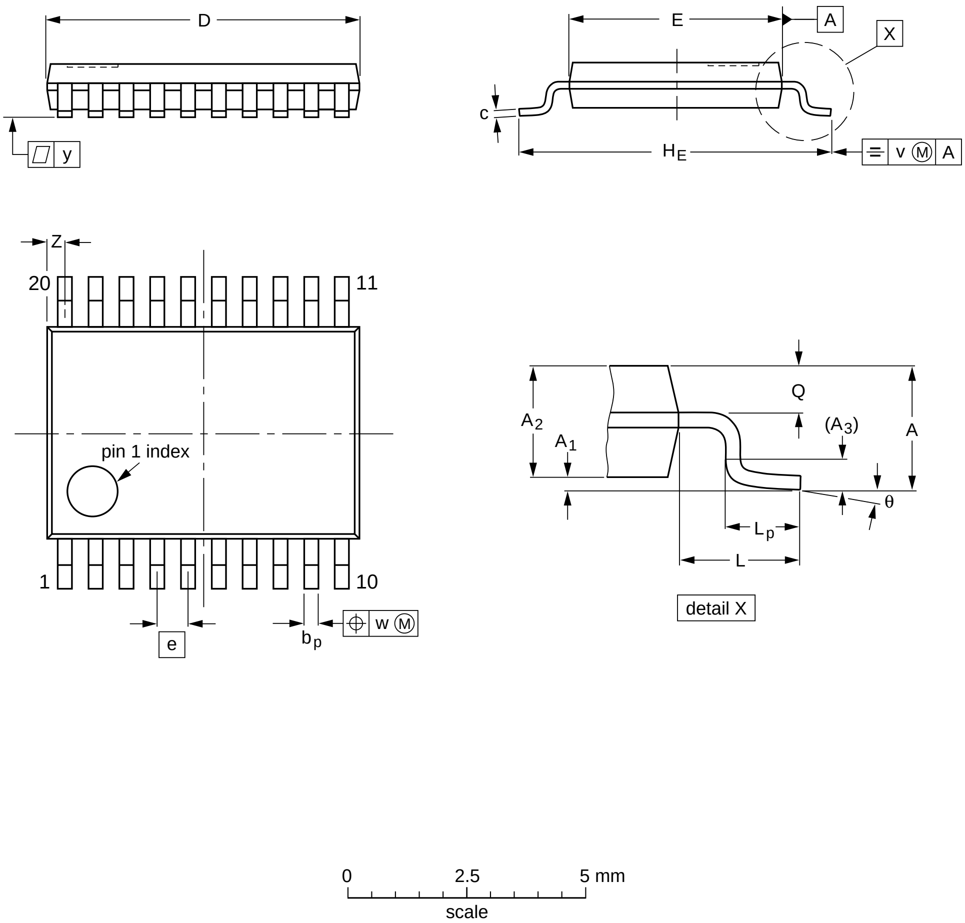
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

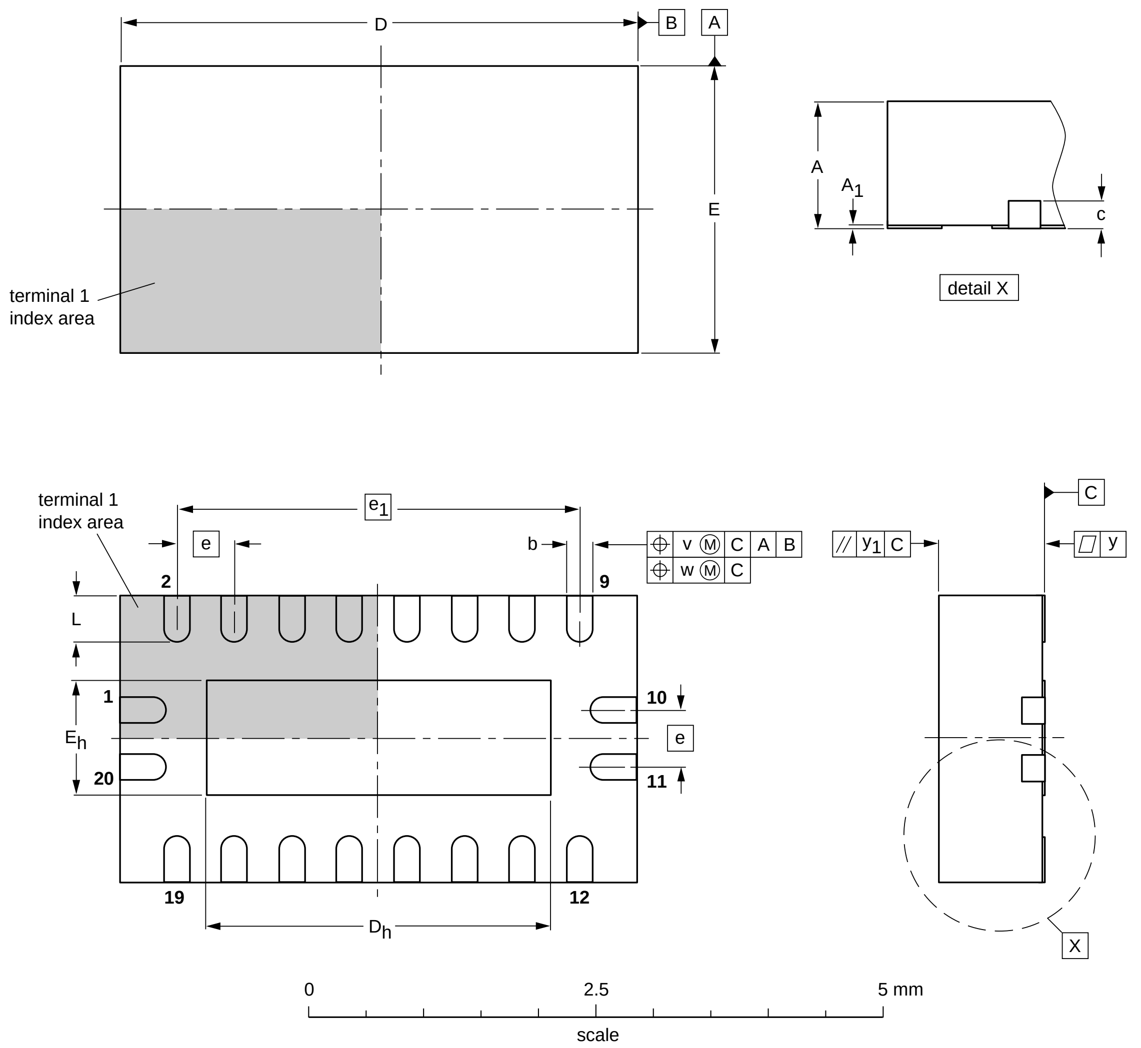
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 11. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC273_Q100 v.1	20130916	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

17. Contents

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Date of release: 16 September 2013