74LVT162374

3.3 V 16-bit edge-triggered D-type flip-flop with 30 Ω termination resistors; 3-state

Rev. 4 — 1 October 2018 Product data sheet

1. General description

The 74LVT162374 is a high performance BiCMOS product designed for V_{CC} operation at 3.3 V.

The 74LVT162374 is designed with 30 Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

This device is a 16-bit edge-triggered D-type flip-flop featuring non-inverting 3-state outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

2. Features and benefits

- 16-bit edge-triggered flip-flop
- 3-state buffers
- Output capability: +12 mA and −12 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Outputs include series resistance of 30 Ω making external resistors unnecessary
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - JESD78B Class II exceeds 500 mA
- ESD protection:
  - HBM: JESD22-A114F exceeds 2000 V
  - MM: JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT162374DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

nexperia

4. Functional diagram

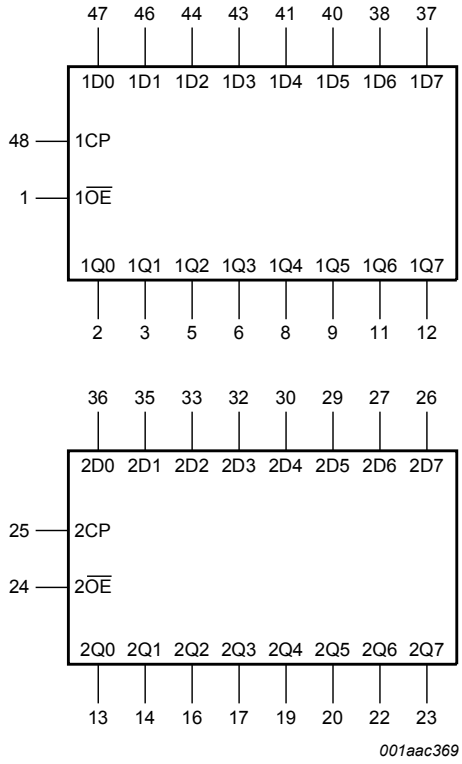


Fig. 1. Logic symbol

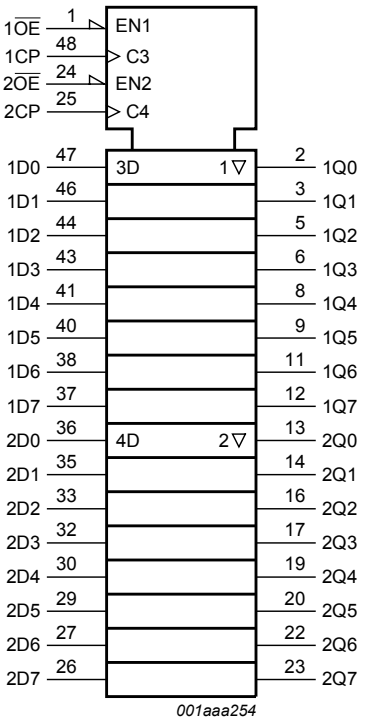


Fig. 2. IEC logic symbol

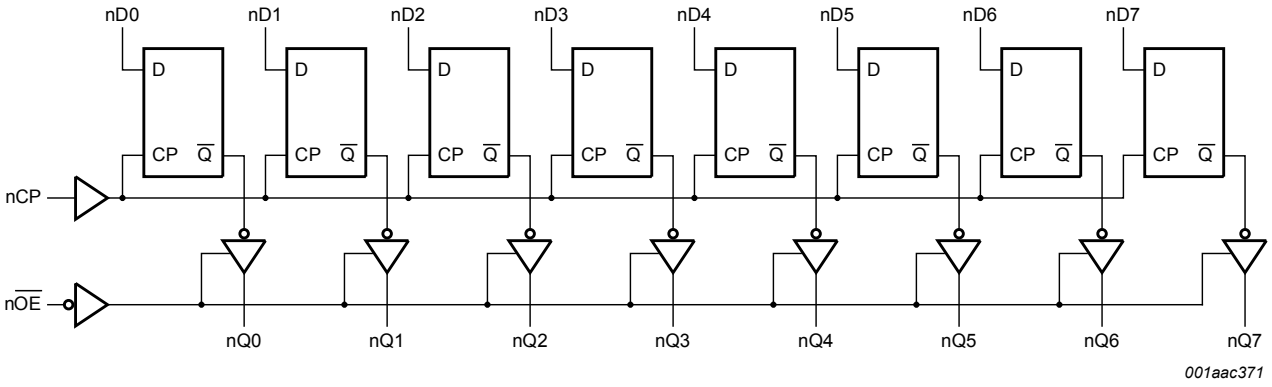


Fig. 3. Logic diagram

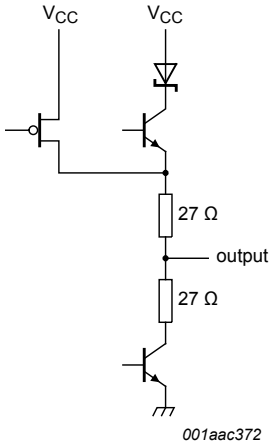


Fig. 4. Schematic of each output

5. Pinning information

5.1. Pinning

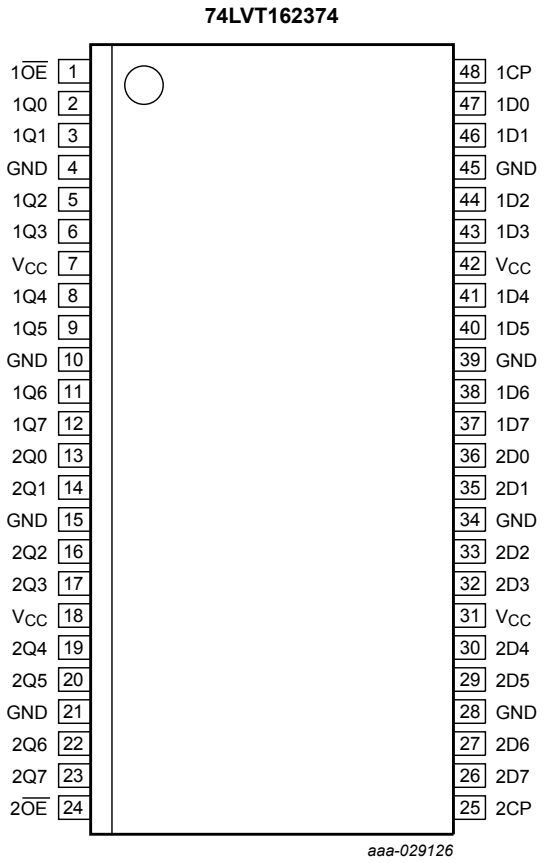


Fig. 5. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	47, 46, 44, 43, 41, 40, 38, 37	data inputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	36, 35, 33, 32, 30, 29, 27, 26	data inputs
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	2, 3, 5, 6, 8, 9, 11, 12	data outputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	13, 14, 16, 17, 19, 20, 22, 23	data outputs
$1\overline{OE}$, $2\overline{OE}$	1, 24	output enable inputs (active LOW)
1CP, 2CP	48, 25	clock pulse inputs (active rising edge)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage

6. Functional description

Table 3. Function table [1]

Operating mode	Input			Internal flip-flops	Output
	$n\overline{OE}$	nCP	nDn		nQn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	NC	X	NC	NC
Disable outputs	H	NC	X	NC	Z
	H	↑	nDn	nDn	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
NC = no change;
X = don't care;
Z = high-impedance OFF-state;
↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T_{stg}	storage temperature		-65	+150	°C

Symbol	Parameter	Conditions	Min	Max	Unit
T_j	junction temperature	[2]		+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature		-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = -18 mA	-	-0.85	-1.2	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC} = 3.0 V; I_{OH} = -12 mA	2.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 3.0 V; I_{OL} = 12 mA	-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	-12	mA
I_{OL}	LOW-level output current		-	-	12	mA
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 3.6 V; I_O = 1 mA; V_I = GND or V_{CC} [2]	-	0.1	0.55	V
I_I	input leakage current	all input pins [3]				
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	0.4	10	µA
		control pins [3]				
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	0.1	±1	µA
		I/O data pins; V_{CC} = 3.6 V [3]				
		V_I = V_{CC}	-	0.1	1	µA
		V_I = 0 V	-	-0.4	-5	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	0.1	±100	µA
I_{BHL}	bus hold LOW current	nDn inputs; V_{CC} = 3 V; V_I = 0.8 V	75	135	-	µA
I_{BHH}	bus hold HIGH current	nDn inputs; V_{CC} = 3 V; V_I = 2.0 V	-75	-135	-	µA
I_{BHLO}	bus hold LOW overdrive current	nDn inputs; V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [4]	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	nDn inputs; V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [4]	-	-	-500	µA
I_{CEX}	output high leakage current	output in HIGH-state when V_O > V_{CC}; V_O = 5.5 V; V_{CC} = 3.0 V	-	50	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} ≤ 1.2 V; V_O = 5.0 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care [5]	-	1	±100	µA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}				
		V_O = 3.0 V	-	0.5	5	µA
		V_O = 0.5 V	-	0.5	-5	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A				
		outputs HIGH	-	0.07	0.12	mA
		outputs LOW	-	4	6	mA
		outputs disabled [6]	-	0.07	0.12	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3 V to 3.6 V; one input at V_{CC} - 0.6 V; other inputs at V_{CC} or GND [7]	-	0.1	0.2	mA
C_I	input capacitance	V_I = 0 V or 3.0 V	-	3	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V	-	9	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
[2] For valid test results, data must not be loaded into the flip-flops after applying power.
[3] Unused pins at V_{CC} or GND.
[4] This is the bus-hold overdrive current required to force the input to the opposite logic state.
[5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.
[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.
[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

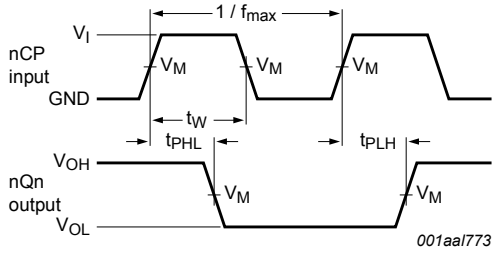
At recommended operating conditions; Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{max}	maximum frequency	nCP; V_{CC} = 3.0 V to 3.6 V; see Fig. 6	150	-	-	MHz
t_{PLH}	LOW to HIGH propagation delay	nCP to nQn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.0	5.3	ns
t_{PHL}	HIGH to LOW propagation delay	nCP to nQn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	5.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.0	4.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nQn; see Fig. 8				
		V_{CC} = 2.7 V	-	-	6.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.5	5.6	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nQn; see Fig. 8				
		V_{CC} = 2.7 V	-	-	6.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.2	4.9	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nQn; see Fig. 8				
		V_{CC} = 2.7 V	-	-	5.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.5	5.4	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nQn; see Fig. 8				
		V_{CC} = 2.7 V	-	-	5.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.2	5.0	ns

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{su}	set-up time	nDn to nCP; see Fig. 7				
		V_{CC} = 2.7 V	2.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	0.7	-	ns
t_h	hold time	nDn to nCP; see Fig. 7				
		V_{CC} = 2.7 V	0.1	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.8	0	-	ns
t_{WH}	pulse width HIGH	nCP; see Fig. 6				
		V_{CC} = 2.7 V	1.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	0.6	-	ns
t_{WL}	pulse width LOW	nCP				
		V_{CC} = 2.7 V	3.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.0	1.6	-	ns

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

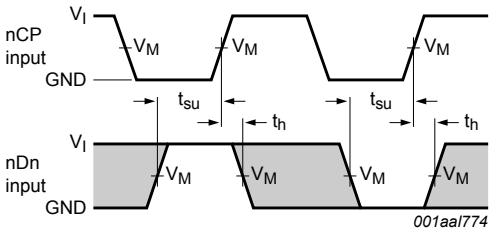
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

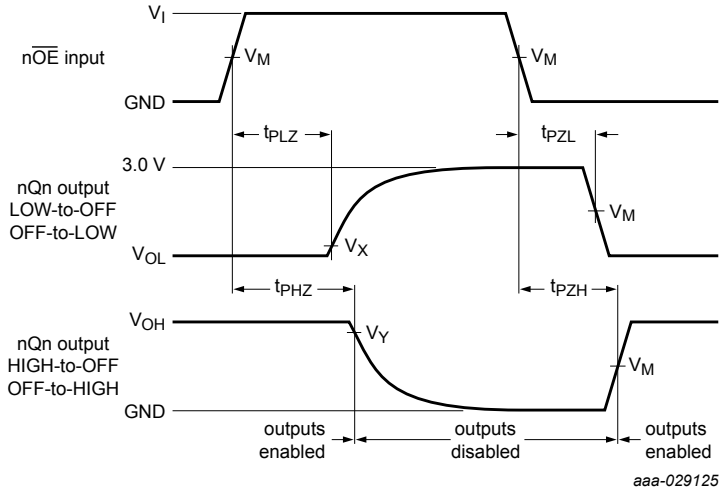
Fig. 6. Clock input (nCP) to output (nQn) propagation delay, clock pulse width and maximum clock frequency



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 7. Data set-up and hold times for input (nDn) to input (nCP)



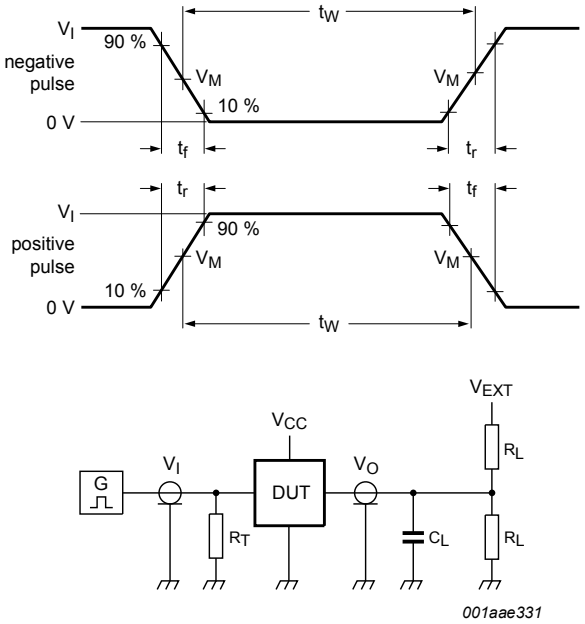
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. 3-state output enable and disable times

Table 8. Measurement points

Input		Output		
V_I	V_M	V_M	V_X	V_Y
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

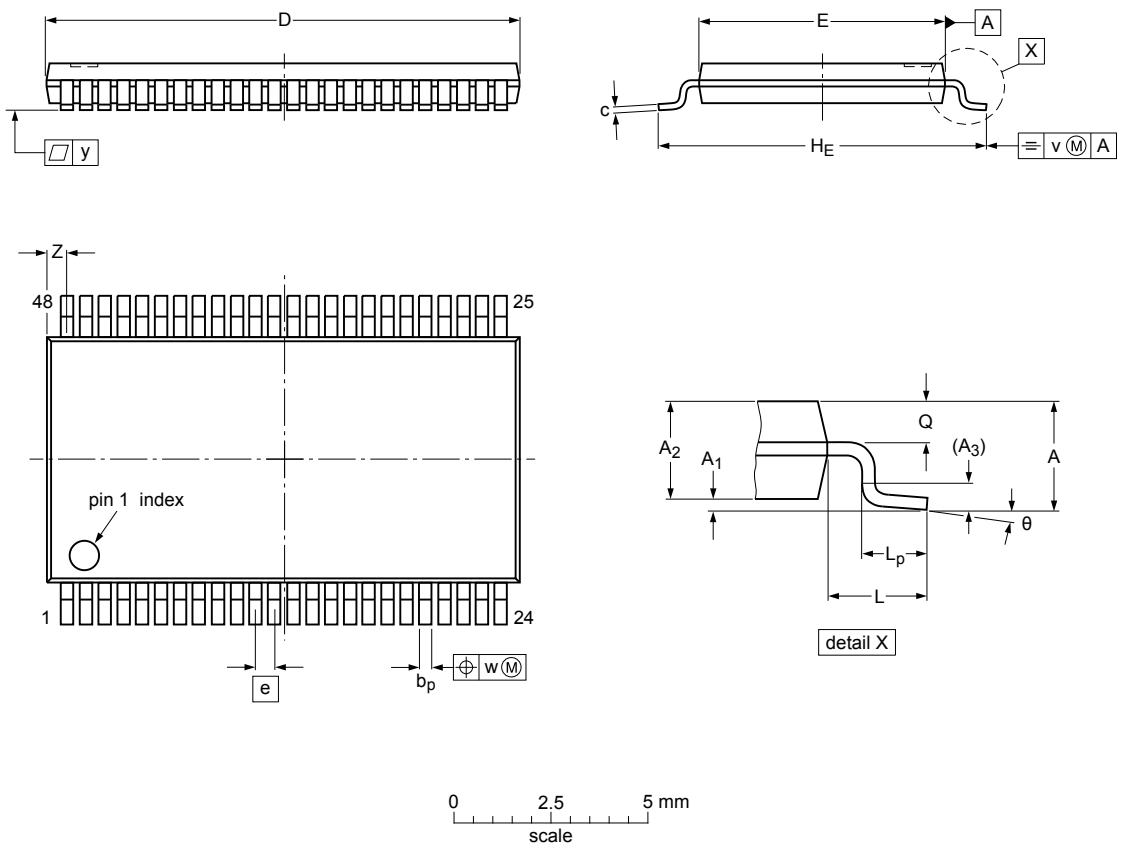
Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
mm nom	1.2			0.25					0.5		1			0.25	0.08	0.1		
min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~03-02-19~~ 13-08-05

Fig. 10. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT162374 v.4	20181001	Product data sheet	-	74LVT162374 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74LVT162374DL (SOT370-1) removed • Section "Quick reference data" removed			
74LVT162374 v.3	20050117	Product data sheet	-	74LVT162374 v.2
Modifications:	• The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Section 2: Changed JEDEC Std 17 into JESD78 • Table 1 "Quick reference data": Changed t_{PLH} and t_{PHL} propagation delays nCP to nQn to 3.0 ns • Table 7: Changed the minimum values of $t_{h(H)}$ and $t_{h(L)}$ hold time nDn to nCP to 0.8 ns			
74LVT162374 v.2	20040922	Product specification	-	74LVT162374 v.1
74LVT162374 v.1	19990923	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 1 October 2018

LifeElectronics
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