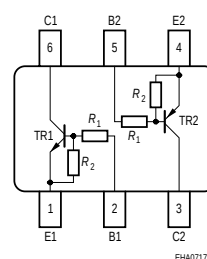
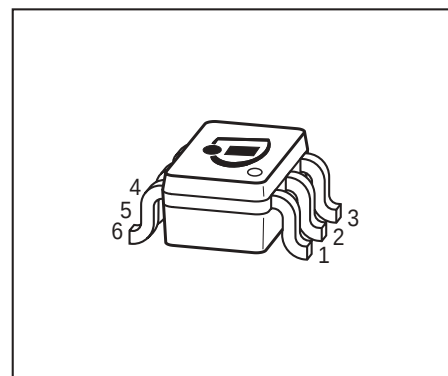
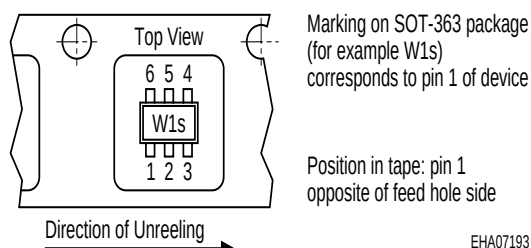


NPN/PNP Silicon Digital Transistor Array

- Switching circuit, inverter, interface circuit, driver circuit
- Two (galvanic) internal isolated NPN/PNP Transistors in one package
- Built in bias resistor NPN and PNP ($R_1=22\text{ k}\Omega$, $R_2=22\text{ k}\Omega$)
- Pb-free (RoHS compliant) package ¹⁾
- Qualified according AEC Q101



EHA07176

Tape loading orientation


EHA07193

Type	Marking	Pin Configuration						Package
BCR22PN	WPs	1=E1	2=B1	3=C2	4=E2	5=B2	6=C1	SOT363

Maximum Ratings for NPN and PNP Types

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Input forward voltage	$V_{i(fwd)}$	60	
Input reverse voltage	$V_{i(rev)}$	10	
DC collector current	I_C	100	mA
Total power dissipation, $T_S = 115\text{ °C}$	P_{tot}	250	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Junction - soldering point ²⁾	R_{thJS}	≤ 140	K/W
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¹Pb-containing package may be available upon special request

²For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at $T_A=25^{\circ}\text{C}$, unless otherwise specified

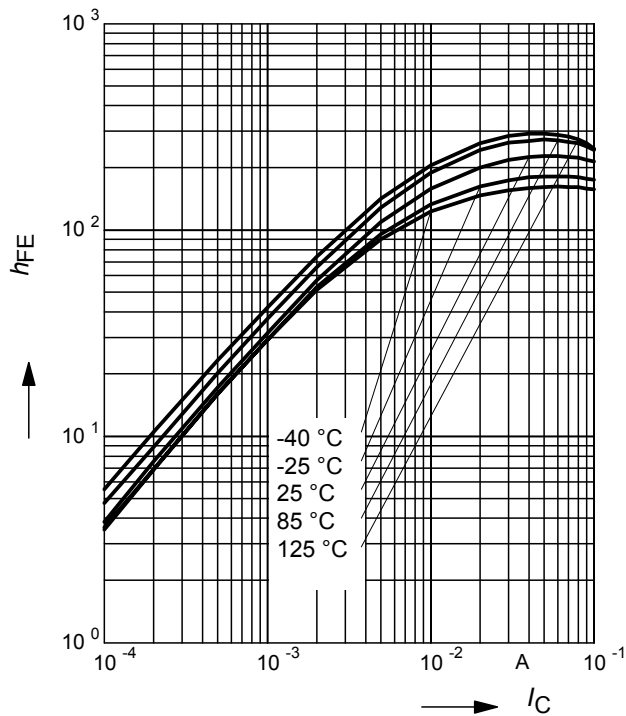
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics for NPN and PNP Types					
Collector-emitter breakdown voltage $I_C = 100\ \mu\text{A}$, $I_B = 0$	$V_{(\text{BR})\text{CEO}}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10\ \mu\text{A}$, $I_E = 0$	$V_{(\text{BR})\text{CBO}}$	50	-	-	
Collector cutoff current $V_{\text{CB}} = 40\ \text{V}$, $I_E = 0$	I_{CBO}	-	-	100	nA
Emitter cutoff current $V_{\text{EB}} = 10\ \text{V}$, $I_C = 0$	I_{EBO}	-	-	350	μA
DC current gain 1) $I_C = 5\ \text{mA}$, $V_{\text{CE}} = 5\ \text{V}$	h_{FE}	50	-	-	-
Collector-emitter saturation voltage1) $I_C = 10\ \text{mA}$, $I_B = 0.5\ \text{mA}$	V_{CEsat}	-	-	0.3	V
Input off voltage $I_C = 100\ \mu\text{A}$, $V_{\text{CE}} = 5\ \text{V}$	$V_{\text{i(off)}}$	0.8	-	1.5	
Input on Voltage $I_C = 2\ \text{mA}$, $V_{\text{CE}} = 0.3\ \text{V}$	$V_{\text{i(on)}}$	1	-	2.5	
Input resistor	R_1	15	22	29	k Ω
Resistor ratio	R_1/R_2	0.9	1	1.1	-
AC Characteristics for NPN and PNP Types					
Transition frequency $I_C = 10\ \text{mA}$, $V_{\text{CE}} = 5\ \text{V}$, $f = 100\ \text{MHz}$	f_{T}	-	130	-	MHz
Collector-base capacitance $V_{\text{CB}} = 10\ \text{V}$, $f = 1\ \text{MHz}$	C_{cb}	-	3	-	pF

1) Pulse test: $t < 300\ \mu\text{s}$; $D < 2\%$

NPN Type

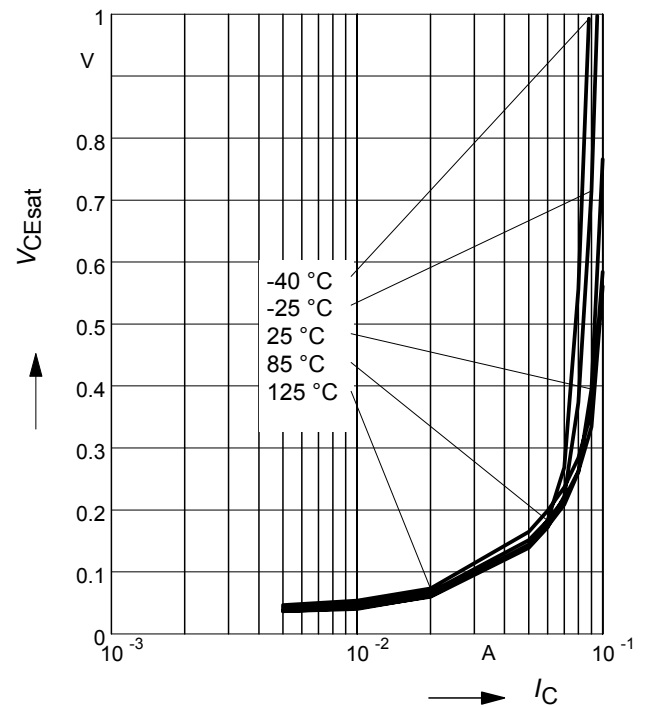
DC Current Gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



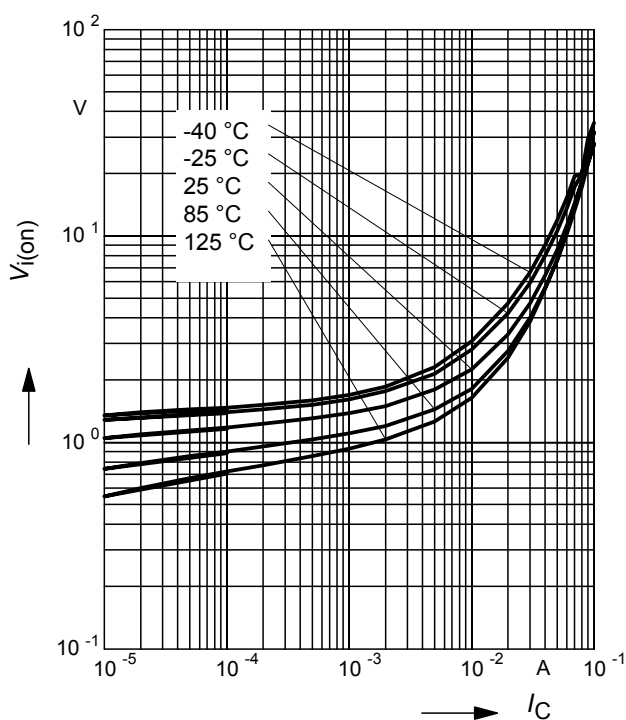
Collector-Emitter Saturation Voltage

$V_{CEsat} = f(I_C), h_{FE} = 20$



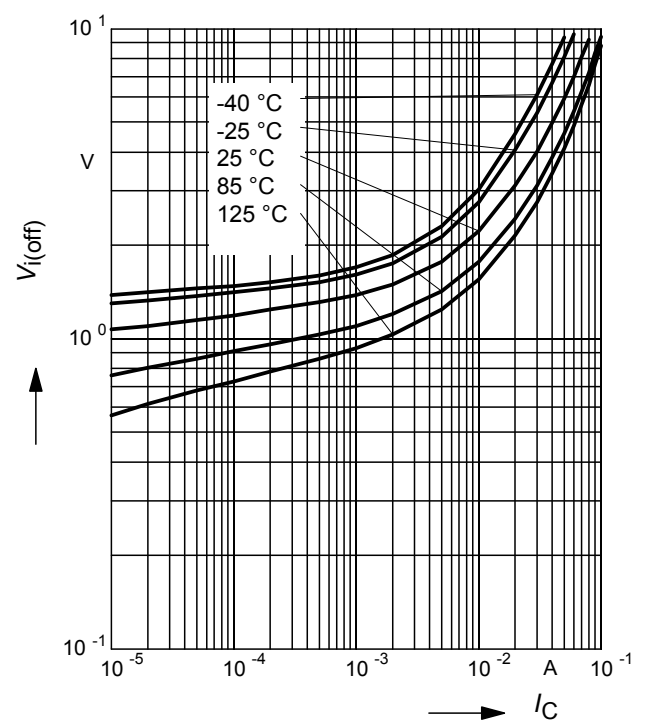
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$ (common emitter configuration)



Input off voltage $V_{i(off)} = f(I_C)$

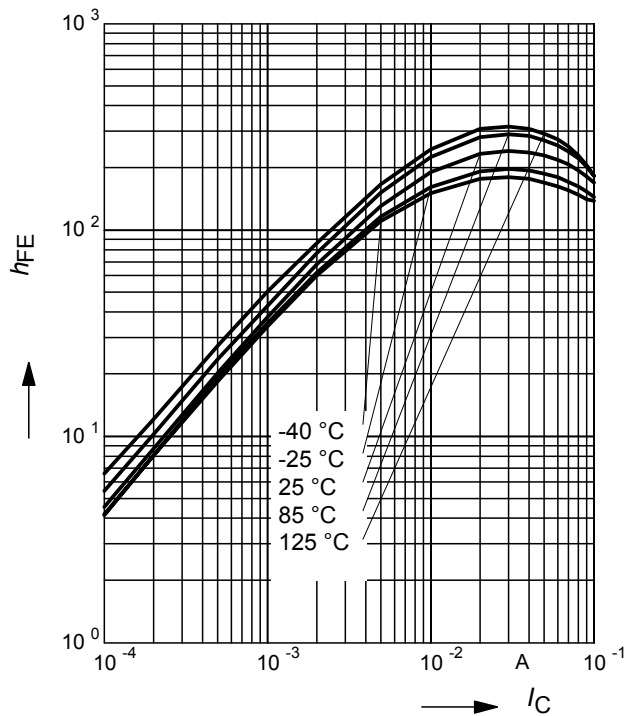
$V_{CE} = 5V$ (common emitter configuration)



PNP Type

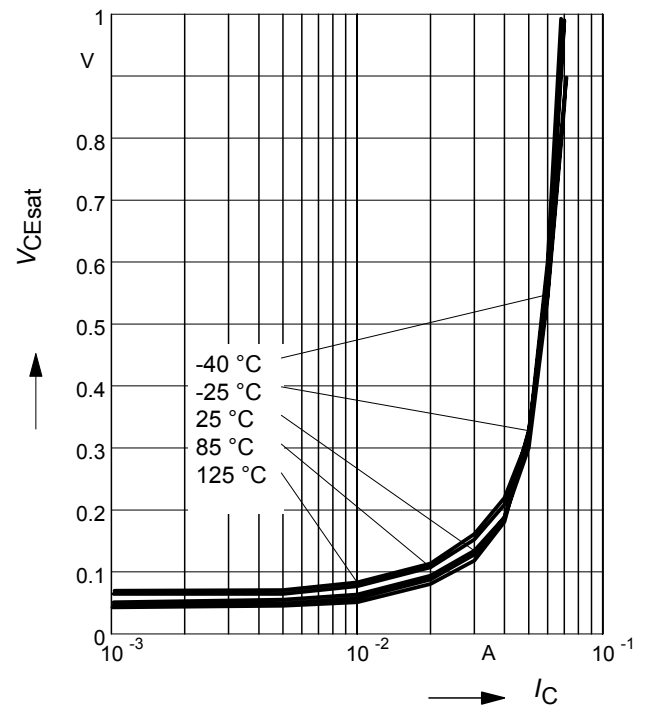
DC Current Gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



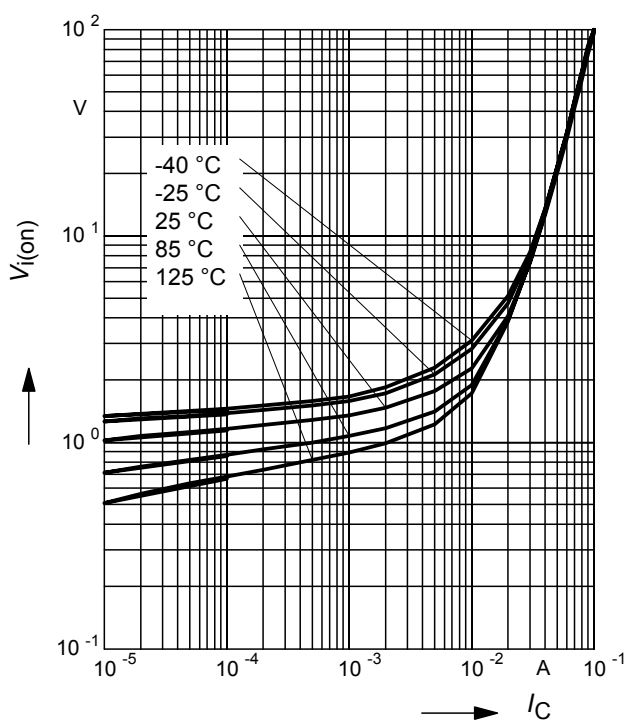
Collector-Emitter Saturation Voltage

$V_{CEsat} = f(I_C), h_{FE} = 20$



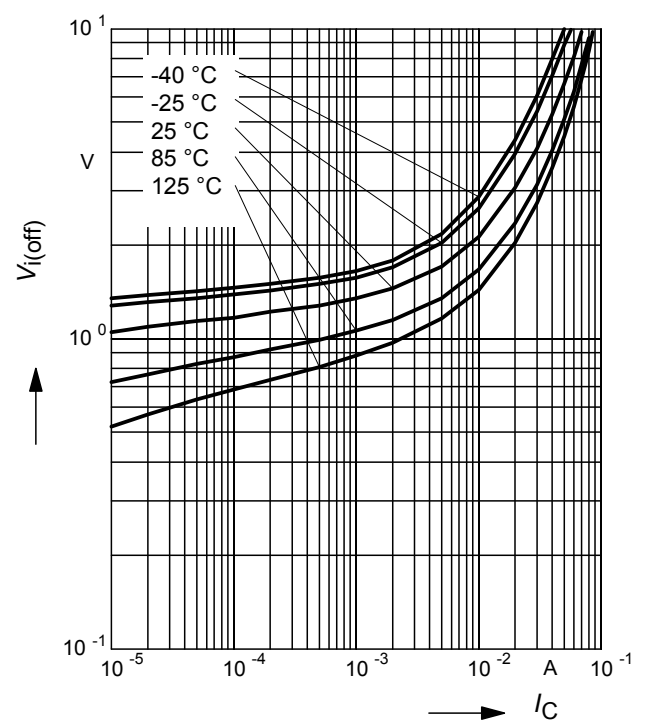
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$ (common emitter configuration)

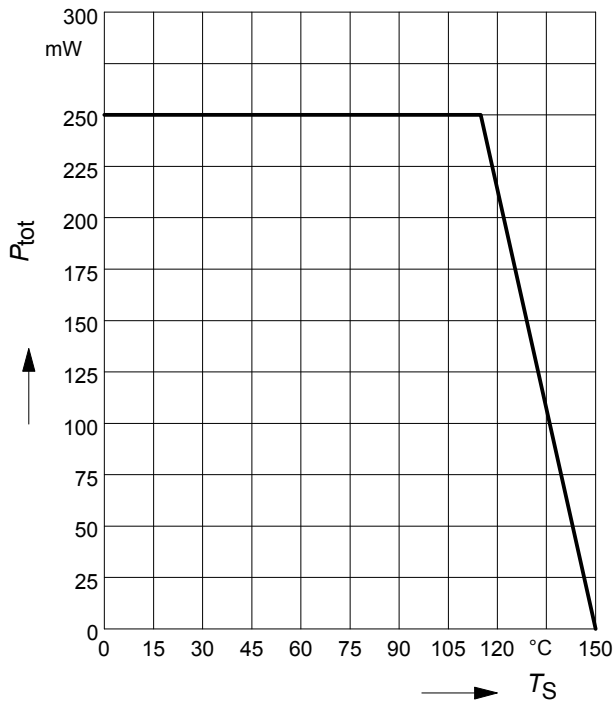


Input off voltage $V_{i(off)} = f(I_C)$

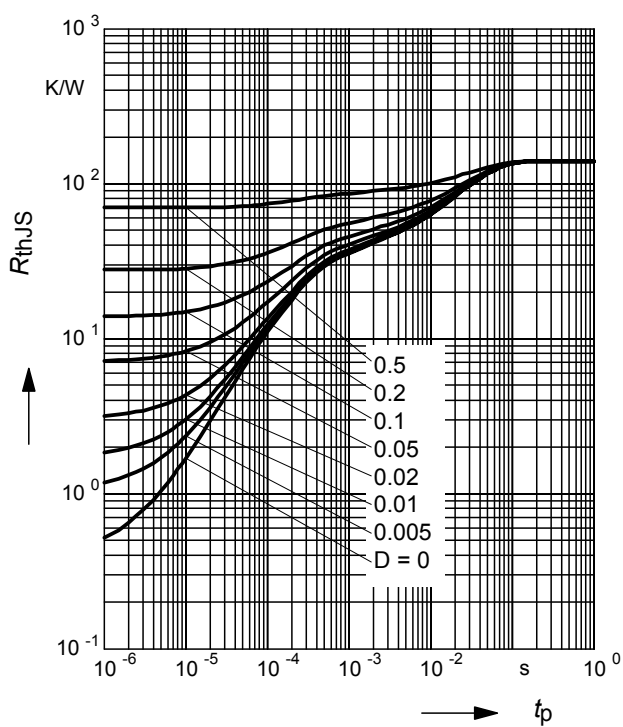
$V_{CE} = 5V$ (common emitter configuration)



Total power dissipation $P_{\text{tot}} = f(T_S)$

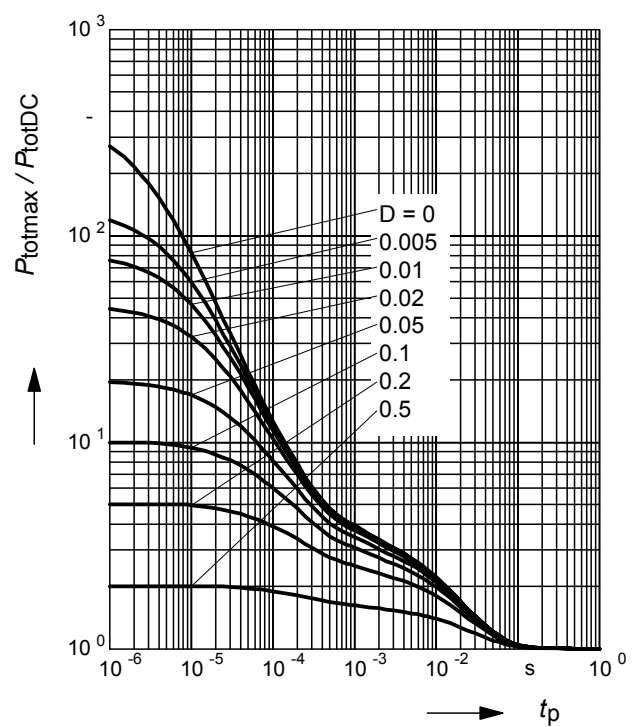


Permissible Pulse Load $R_{\text{thJS}} = f(t_p)$



Permissible Pulse Load

$P_{\text{totmax}} / P_{\text{totDC}} = f(t_p)$



[illegible]

Technical drawing of a 2x3 grid of rectangular features. The top row features are spaced 0.3 units apart. The vertical distance between the top and bottom rows is 0.9 units. The horizontal distance between the left and right columns is 1.6 units. The width of each feature is 0.65 units. The drawing includes dimension lines and arrows indicating the measurements.

Infineon technologies

Manufacturer

2005, June

Date code (Year/Month)

Pin 1 marking

Laser marking

BCR108S

Type code

Technical drawing of a PCB layout for a 3-pin connector. The top view shows a rectangular board with dimensions 4 (width) and 8 (height). Three circular pin holes are spaced 2.15 apart. A 2.3 wide rectangular area is marked. A side view shows a 0.2 thick board with a 1.1 high component.

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Тел: +7 (812) 336 43 04 (многоканальный)

Email: org@lifeelectronics.ru

www.lifeelectronics.ru