Datasheet

Multiple Input Switch Monitor LSI for Automotive

BD3375KV-C

General Description

BD3375KV-C is a 22-channel Multiple Input Switch Monitor IC that detects the opening and closing of mechanical switches. Once it senses a change in the status of a switch, it sends an interrupt signal to the MCU via a serial peripheral interface (SPI).
The 22 switch inputs have two types of power supply, VPUB and VPUA. The VPUB and the VPUA power supplies can either be from a battery or from another power supply system. VPUB is the supply for the INB inputs while VPUA is for the INZ and INA inputs.
BD3375KV-C has two modes of operation, Normal and Sleep. In both modes, the internal registers can be set to make the device perform either intermittent or continuous monitoring of the switches.
In intermittent monitoring, the switch status is monitored at regular time intervals, allowing the IC to operate with low power consumption. Also, operation with reduced noise can be achieved by enabling uniform sequential monitoring of all switches or sequential monitoring by power supply system.

Specifications

- AEC-Q100 Qualified (Note 1)
- Operational Voltage Range: 3.9V to 8V
- Uses 3.3/5.0V SPI protocol in communicating with the MCU
- Serial communication error checking through 8bit-CRC
- Thermal Shutdown Protection (TSD)
- Power on Reset (POR)
- Selectable source/sink current levels through register settings
- Wetting current timer capability
- 8 source or sink input terminals
- 14 source input terminals
- Separable Power Supply
  VPUA: 16ch (INA&INZ), VPUB: 6ch (INB)
- Interrupt notification upon switch status change
- 1 to 6 times matched LPF that eliminates input terminal noise
- Low current consumption (Intermittent monitoring)
- Status display of selected terminal at DMUX terminal

(Note 1) Grade 1

Application

- Engine Control Module

Key Specifications

- Fully Functional Voltage Range: 8V to 26V
- Switch Input Voltage Range: -14V to +40V
- Selectable Wetting Current (Min): 1mA, 3mA, 5mA, 10mA, 15mA

Package

Package	W(Typ) x D(Typ) x H(Max)
VQFP48C (48 pin QFP)	9.00mm x 9.00mm x 1.60mm

Typical Application Circuit

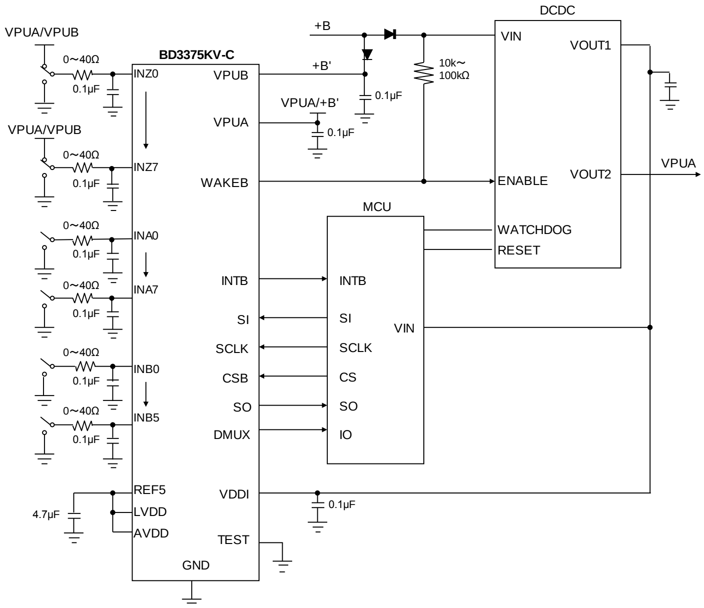


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

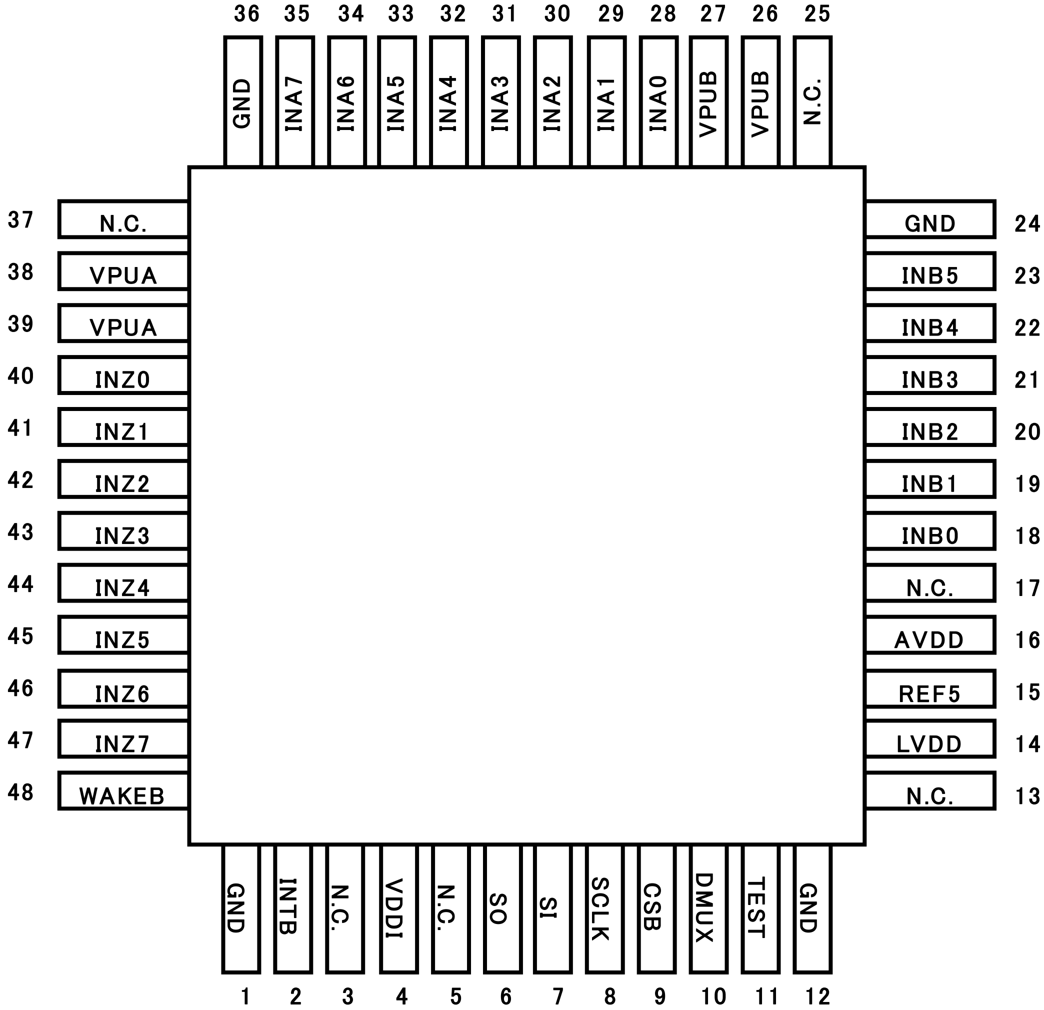


Figure 2. Pin Configuration (Top View)

Pin Description

Table 1. Pin Description (1)

Pin No.	Pin Name	Function	Description	Equivalent Circuit Diagram (Note 2)
1	GND	Ground	Ground pin	--
2	INTB	Output	Open-drain interrupt output pin to the MCU (with an internal pull-down resistor)	C
3	N.C.	-	No Connection	--
4	VDDI	Input	Power supply pin for CSB, SI, SCLK, SO, INTB and DMUX	--
5	N.C.	-	No Connection	--
6	SO	Output	SPI data output pin to the MCU	H
7	SI	Input	SPI control data input pin from the MCU (with an internal pull-down resistor)	A
8	SCLK	Input	SPI control clock input pin from the MCU (with an internal pull-down resistor)	A
9	CSB	Input	SPI control chip select input pin from the MCU (with internal pull-up current source)	B
10	DMUX	Output	Digital multiplexer for switch input output pin	G
11	TEST	Input	Test mode control pin (Note 3)	J
12	GND	Ground	Ground	--
13	N.C.	-	No Connection	--
14	LVDD	Input	Power supply input pin for the logic block (Note 4)	--
15	REF5	Output	5V power supply output pin (Note 4)	I
16	AVDD	Input	Power supply input pin for the analog block (Note 4)	--
17	N.C.	-	No Connection	--
18	INB0	Input	Switch input pin 0 under VPUB power supply system (with an internal pull-up current source)	F
19	INB1	Input	Switch input pin 1 under VPUB power supply system (with an internal pull-up current source)	F
20	INB2	Input	Switch input pin 2 under VPUB power supply system (with an internal pull-up current source)	F
21	INB3	Input	Switch input pin 3 under VPUB power supply system (with an internal pull-up current source)	F
22	INB4	Input	Switch input pin 4 under VPUB power supply system (with an internal pull-up current source)	F
23	INB5	Input	Switch input pin 5 under VPUB power supply system (with an internal pull-up current source)	F
24	GND	Ground	Ground	--

(Note 2) Ref. Page 65 IO Equivalent Circuit.
(Note 3) Short TEST pin to ground when mounted.
(Note 4) Short REF5 pin to AVDD pin and LVDD pin, and connect a 4.7µF capacitor between it and ground. Do not use it as voltage source to another IC.

Table 2. Pin Description (2)

Pin No.	Pin Name	Function	Description	Equivalent Circuit Diagram (Note 2)
25	GND	-	No Connection	--
26	VPUB	Input	Power supply input pin for the main system and INB switches	--
27	VPUB	Input	Power supply input pin for the main system and INB switches	--
28	INA0	Input	Switch input pin 0 under VPUA power supply system (with an internal pull-up current source)	F
29	INA1	Input	Switch input pin 1 under VPUA power supply system (with an internal pull-up current source)	F
30	INA2	Input	Switch input pin 2 under VPUA power supply system (with an internal pull-up current source)	F
31	INA3	Input	Switch input pin 3 under VPUA power supply system (with an internal pull-up current source)	F
32	INA4	Input	Switch input pin 4 under VPUA power supply system (with an internal pull-up current source)	F
33	INA5	Input	Switch input pin 5 under VPUA power supply system (with an internal pull-up current source)	F
34	INA6	Input	Switch input pin 6 under VPUA power supply system (with an internal pull-up current source)	F
35	INA7	Input	Switch input pin 7 under VPUA power supply system (with an internal pull-up current source)	F
36	GND	Ground	Ground	--
37	N.C.	-	No Connection	--
38	VPUA	Input	Power supply input pin for INA and INZ switches	--
39	VPUA	Input	Power supply input pin for INA and INZ switches	--
40	INZ0	Input	Switch input pin 0 under VPUA power supply system (with an internal pull-up/down current source)	E
41	INZ1	Input	Switch input pin 1 under VPUA power supply system (with an internal pull-up/down current source)	E
42	INZ2	Input	Switch input pin 2under VPUA power supply system (with an internal pull-up/down current source)	E
43	INZ3	Input	Switch input pin 3 under VPUA power supply system (with an internal pull-up/down current source)	E
44	INZ4	Input	Switch input pin 4 under VPUA power supply system (with an internal pull-up/down current source)	E
45	INZ5	Input	Switch input pin 5 under VPUA power supply system (with an internal pull-up/down current source)	E
46	INZ6	Input	Switch input pin 6 under VPUA power supply system (with an internal pull-up/down current source)	E
47	INZ7	Input	Switch input pin 7 under VPUA power supply system (with an internal pull-up/down current source)	E
48	WAKEB	Output	Open-drain output pin to monitor the mode of operation (Note 5)	D

(Note 5) In the application circuit, WAKEB should be pulled-up by an external resistor.

Block Diagram

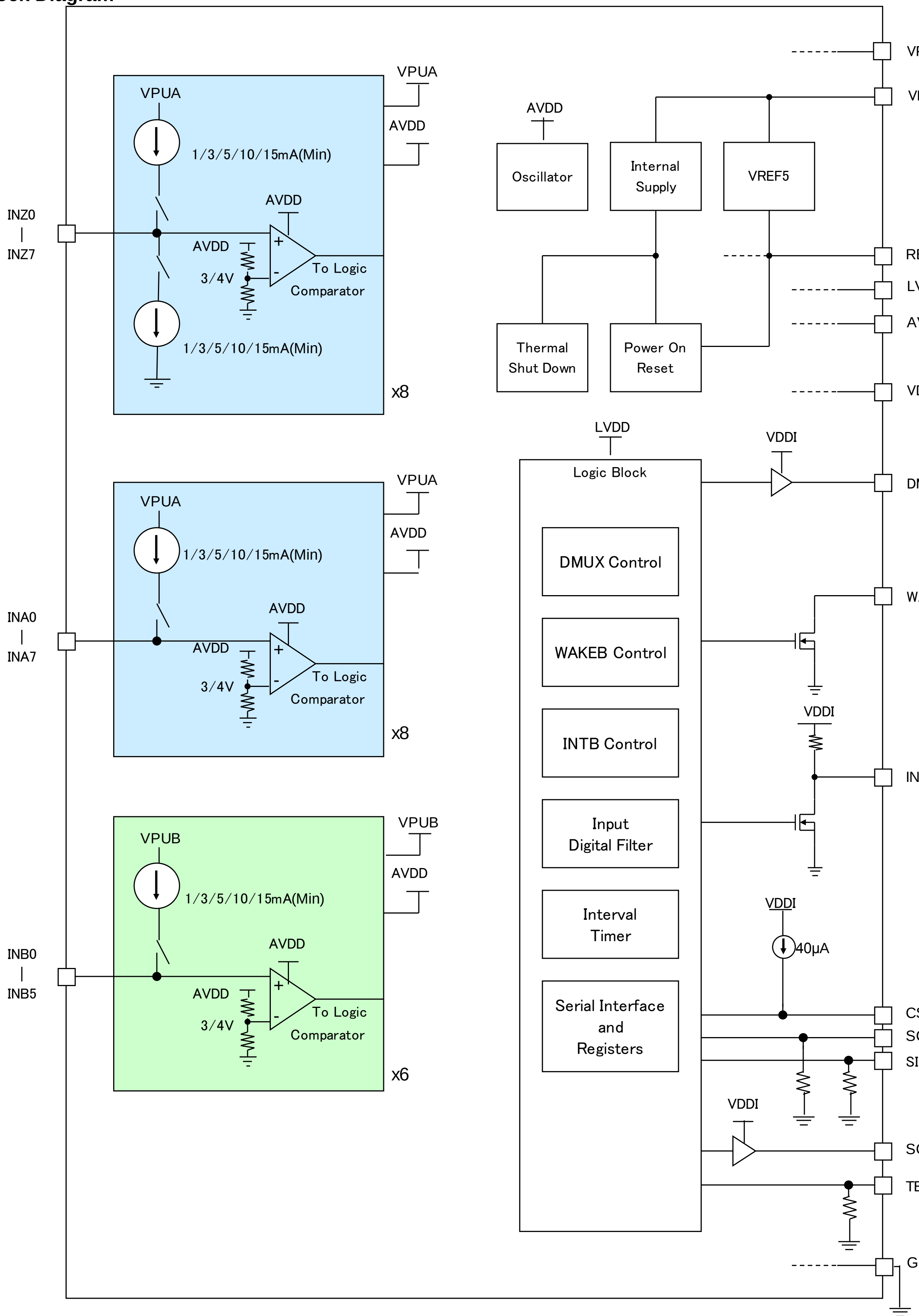


Figure 3. Block Diagram

Absolute Maximum Ratings

Table 3. Pin Description

Parameter	Symbol	Ratings	Unit
Supply Voltage Range on Pin VDDI, AVDD, LVDD Input Voltage Range on Pin CSB, SI, SCLK, TEST Output Voltage Range at Pin SO, INTB, DMUX, REF5	-	-0.3 to +7.0	V
Supply Voltage Range on Pin VPUA, VPUB Voltage Range on Pin WAKEB	-	-0.3 to +40	V
Input Current at Pin WAKEB	-	10	mA
Input Voltage on Switch Pin (INB0-INB5, INA0-INA7,INZ0-INZ7)	-	-14 to +40	V
Operating Temperature Range	T_{OPR}	-40 to +125	°C
Storage Temperature Range	T_{STR}	-55 to +150	°C
Maximum Junction Temperature	Tj	-40 to +150	°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance (Note 6)

Table 4. Thermal Resistance

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 8)	2s2p (Note 9)	
VQFP48C				
Junction to Ambient	θ_{JA}	93.7	53.3	°C/W
Junction to Top Characterization Parameter (Note 7)	Ψ_{JT}	4	4	°C/W

(Note 6) Based on JESD51-2A(Still-Air)
(Note 7) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 8) Using a PCB board based on JESD51-3 (Table 5).
(Note 9) Using a PCB board based on JESD51-5, 7 (Table 6).

Table 5. 1s

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

Table 6. 2s2p

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Parameter	Symbol	Ratings		Unit
		Min	Max	
Operating Temperature	T_{OPR}	-40	+125	°C
VPUA/VPUB Supply Voltage	V_{VPUX}	8.0	26	V
VDDI Supply Voltage	V_{VDDI}	3.1	5.25	V
Capacitance for REF5 (Note 11)	C_{REF}	4.7	-	μF

(Note 10) Recommend a ceramic capacitance. Please consider variation of capacitance.

Electrical Characteristics

Spec conditions: 8.0V≤VPUA/VPUB≤26V, 3.1V≤VDDI≤5.25V, -40°C≤T_{OPR}≤+125°C
VPUA/VPUB/INZ/INA/INB terminal: resistors and capacitors are not connected
REF5 terminal: 4.7µF
Unless otherwise specified, the typical condition is VPUA/VPUB=13V, VDDI=5.00V, T_{OPR}=25°C.

Table 8. Recommended Operating Conditions

Parameter	Symbol/Name	Min	Typ	Max	Unit
VPUA/VPUB Supply Voltage Low -voltage Operating Range (Note 11) Fully Operational Voltage Range High-voltage Operating Range (Note 12)	$V_{VPUX(QFL)}$ $V_{VPUX(FO)}$ $V_{VPUX(QFH)}$	3.9 8.0 26	- - -	8.0 26 40	V
POR(Power on Reset) Activation Voltage (Note 13)	$V_{POR(LOW)}$	3.9	4.2	4.5	V
POR(Power on Reset) Deactivation Voltage (Note 13)	$V_{POR(HIGH)}$	4.0	4.3	4.6	V
VPUA/VPUB Operating Current Continuous Monitoring Current source is invalid, “Hi-Z” Status	$I_{VPUX(OFF)}$	-	-	600	µA
VPUA/VPUB Average Operating Current Intermittent Monitoring Source/Sink Current Setting=1mA Monitoring Period=50ms, Strobe Time=125µs	$I_{VPUX(SS)}$	-	75	100	µA
VDDI Operating Current INTB=“L”, CSB=“H”	I_{VDDI}	-	5	10	µA
REF5 Output Voltage	V_{REF5}	4.75	5.00	5.25	V

(Note 11) Electrical characteristics are not guaranteed though functions are operating. POR is active between 3.9V and 4.5V.
(Note 12) Electrical characteristics are not guaranteed though functions are operating.
(Note 13) The POR circuit monitors the REF5 voltage.

Table 9. Electrical Characteristics (Switch Input)

Parameter	Symbol/Name	Min	Typ	Max	Unit
Source Current 1 (Internal Pull-up Current Source) 0V external supply, VPUA/VPUB system (1mA Setting)	$I_{SOURCE1}$	1.0	1.4	1.8	mA
Sink Current 1 (Internal Pull-down Current Source) 8V external supply, VPUA system (1mA Setting)	I_{SINK1}	1.0	1.4	1.8	mA
Source Current 2 (Internal Pull-up Current Source) 0V external supply, VPUA/VPUB system (3mA Setting)	$I_{SOURCE3}$	3.0	4.2	5.4	mA
Sink Current 2 (Internal Pull-down Current Source) 8V external supply, VPUA system (3mA Setting)	I_{SINK3}	3.0	4.2	5.4	mA
Source Current 3 (Internal Pull-up Current Source) 0V external supply, VPUA/VPUB system (5mA Setting)	$I_{SOURCE5}$	5.0	7.0	9.0	mA
Sink Current 3 (Internal Pull-down Current Source) 8V external supply, VPUA system (5mA Setting)	I_{SINK5}	5.0	7.0	9.0	mA
Source Current 4 (Internal Pull-up Current Source) 0V external supply, VPUA/VPUB system (10mA Setting)	$I_{SOURCE10}$	10.0	14.0	18.0	mA
Sink Current 4 (Internal Pull-down Current Source) 8V external supply, VPUA system (10mA Setting)	I_{SINK10}	10.0	14.0	18.0	mA
Source Current 5 (Internal Pull-up Current Source) 0V external supply, VPUA/VPUB system (15mA Setting)	$I_{SOURCE15}$	15.0	21.0	27.0	mA
Sink Current 5 (Internal Pull-down Current Source) 8V external supply, VPUA system (15mA Setting)	I_{SINK15}	15.0	21.0	27.0	mA
Low to High Switch Detection Threshold Voltage (3.0V Setting)	$V_{TH3(HIGH)}$	2.7	3.0	3.3	V
High to Low Switch Detection Threshold Voltage (3.0V Setting)	$V_{TH3(LOW)}$	2.6	2.9	3.2	V
Low to High Switch Detection Threshold Voltage (4.0V Setting)	$V_{TH4(HIGH)}$	3.7	4.0	4.3	V
High to Low Switch Detection Threshold Voltage (4.0V Setting)	$V_{TH4(LOW)}$	3.6	3.9	4.2	V

Table 10. Electrical Characteristics (Static Electrical Characteristics)

Parameter	Symbol/Name	Min	Typ	Max	Unit
Serial Interface Threshold Voltage (Note 14)	$V_{INLOGIC}$	0.8	-	2.2	V
CSB Input Current CSB=VDDI	$I_{CS(HIGH)}$	-10	-	+10	µA
CSB Pull-up Current CSB=0V	$I_{CS(LOW)}$	30	-	85	µA
SI, SCLK Pull-down Resistor	R_{SI}, R_{SCLK}	50	100	150	kΩ
SI, SCLK Input Current SI, SCLK=0V	$I_{SI(LOW)}$, $I_{SCLK(LOW)}$	-10	-	+10	µA
SO “H” Level Output Voltage I_{SOURCE}=200µA	$V_{SC(HIGH)}$	V_{VDDI}-0.8	-	V_{VDDI}	V
SO “L” Level Output Voltage I_{SINK}=1.6mA	$V_{SO(LOW)}$	-	-	0.4	V
SO(Set to “Hi-Z”) Input Current 0V to VDDI	$I_{SO(TRI)}$	-10	-	+10	µA
DMUX “H” Level Output Voltage I_{SOURCE}=200µA	$V_{DMUX(HIGH)}$	V_{VDDI}-0.8	-	V_{VDDI}	V
DMUX “L” Level Output Voltage I_{SINK}=1.6mA	$V_{DMUX(LOW)}$	-	-	0.4	V
INTB Internal Pull-up Current (Note 15)	$I_{INTB(PU)}$	15	53	85	µA
INTB “H” Level Output Voltage INTB=OPEN	$V_{INTB(HIGH)}$	V_{VDDI}-0.5	-	V_{VDDI}	V
INTB “L” Level Output Voltage I_{SINK}=1.0mA	$V_{INTB(LOW)}$	-	0.2	0.4	V
WAKEB “L” Level Output Voltage WAKEB=1.0mA	$V_{WAKEB(LOW)}$	-	0.2	0.4	V
WAKEB (Set to “Hi-Z”) Input Current 0V to VPUB	$I_{WAKEB(TRI)}$	-10	-	+10	µA

(Note 14) Applicable to SCLK, SI, CSB
(Note 15) VDDI= 5.0V

Table 11. Electrical Characteristics (Dynamic Electrical Characteristics)

Parameter	Symbol/Name	Min	Typ	Max	Unit
Wetting Current Timer Counting starts after n-times detection of matched LPF	t_{WCT}	13	-	22	ms
Interrupt Delay Time1 Time from switch status change to INTB output change in continuous monitoring	t_{INTB_DLY1}	-	-	1	ms
Interrupt Delay Time 2 Time from switch status change to INTB output change in intermittent monitoring n: Setting time of LPF matched n times	t_{INTB_DLY2}	-	-	[Monitor cycle] x n+1	ms
Interrupt Clear Time Time from CSB rising edge to INTB output change	t_{INTB_CLR}	-	-	150	µs
Command Set Time Time from CSB rising edge to setting of register	t_{REG_EN}	-	-	150	µs
Transition Time to Normal Mode Time from CSB rising edge to WAKEB output change	t_{WAKEB_DLY1}	-	-	1	ms
Transition Time to Sleep Mode Time from CSB rising edge to WAKEB output change	t_{WAKEB_DLY2}	-	-	1	ms
Switch Strobe Time (93.75µs Setting) (Note 16)	t_{SCAN_94}	84.375	93.75	103.125	µs
Switch Strobe Time (125µs Setting) (Note 16)	t_{SCAN_125}	112.5	125	137.5	µs
Switch Strobe Time (187.5µs Setting) (Note 16)	t_{SCAN_188}	168.75	187.5	206.25	µs
Switch Strobe Time (250µs Setting) (Note 16)	t_{SCAN_250}	225	250	275	µs
Source/Sink Current Rise Time FSQ="0", FSQZ/A/B="0", 10mA Setting Load Resistance 100Ω	t_{SR_R}	-	20	-	µs
Source/Sink Current Fall Time FSQ="0", FSQZ/A/B="0", 10mA Setting Load Resistance 100Ω	t_{SR_F}	-	15	-	µs
Internal Clock Accuracy	t_{TIMER}	-10	-	+10	%

(Note 16) "H" width of internal signal (Ref. Page 12 Figure 6).

Table 12. Electrical Characteristics (Digital Interface Characteristics)

Parameter	Symbol/Name	Min	Typ	Max	Unit
SCLK Frequency	f_{SCLK}	-	-	4.4	MHz
Setup Time from CSB Fall to SCLK Rise	t_{LEAD}	100	-	1000	ns
Setup Time from SCLK Fall to CSB Rise	t_{LAG}	50	-	500	ns
Setup Time from SI to SCLK Fall	$t_{SI(SU)}$	16	-	-	ns
Hold Time from SCLK Fall to SI	$t_{SI(HOLD)}$	20	-	-	ns
SI, CSB, SCLK Rise Time	$t_{R(SI)}$	-	5.0	-	ns
SI, CSB, SCLK Fall Time	$t_{F(SI)}$	-	5.0	-	ns
Time from CSB Fall to SO Output Low Impedance	$t_{SO(EN)}$	-	-	55	ns
Time from CSB Rising to SO Output High Impedance	$t_{SO(DIS)}$	-	-	55	ns
SCLK "H" Level Width	t_{SCLKH}	75	-	-	ns
SCLK "L" Level Width	t_{SCLKL}	75	-	-	ns
Time from SCLK Rise to Stable SO Data Output SO CL=20pF	t_{VALID}	-	25	55	ns
CSB "H" Level Time	t_{CSBH}	150	-	-	µs

Timing Chart

・Serial Access Timing

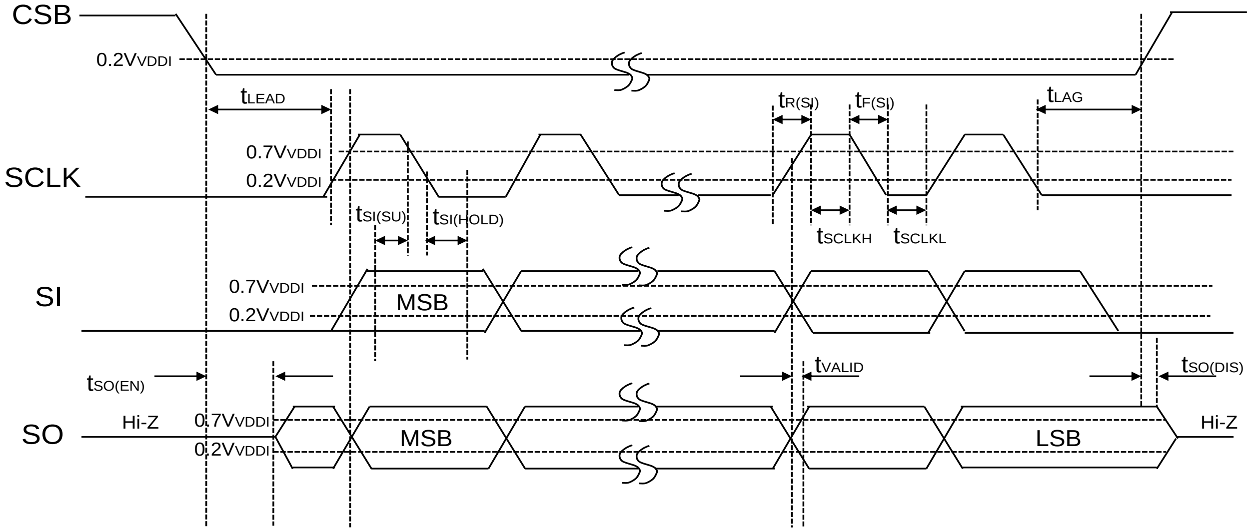


Figure 4. Serial Access Timing

・Power Supply Rising/Falling Sequence

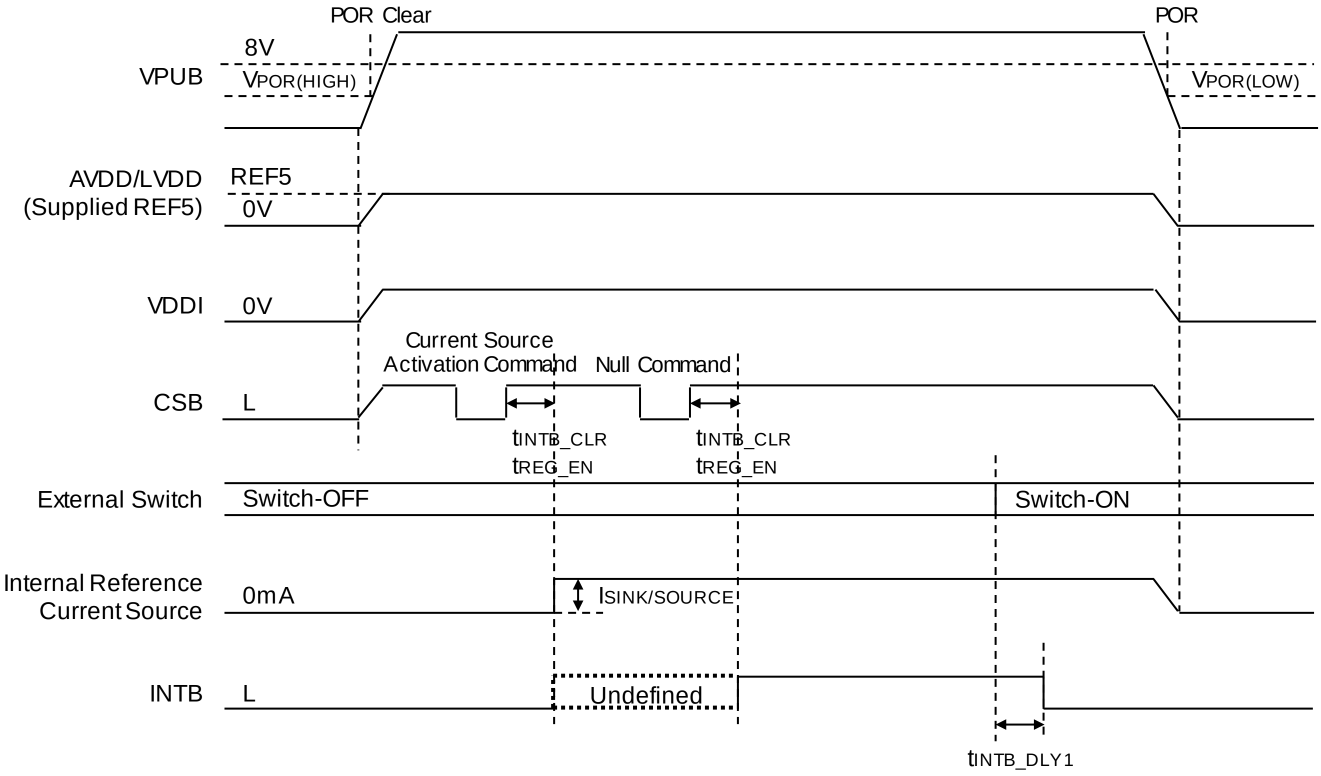


Figure 5. Power Supply Rising/Falling Sequence

・Source/Sink Current Rise and Fall Time

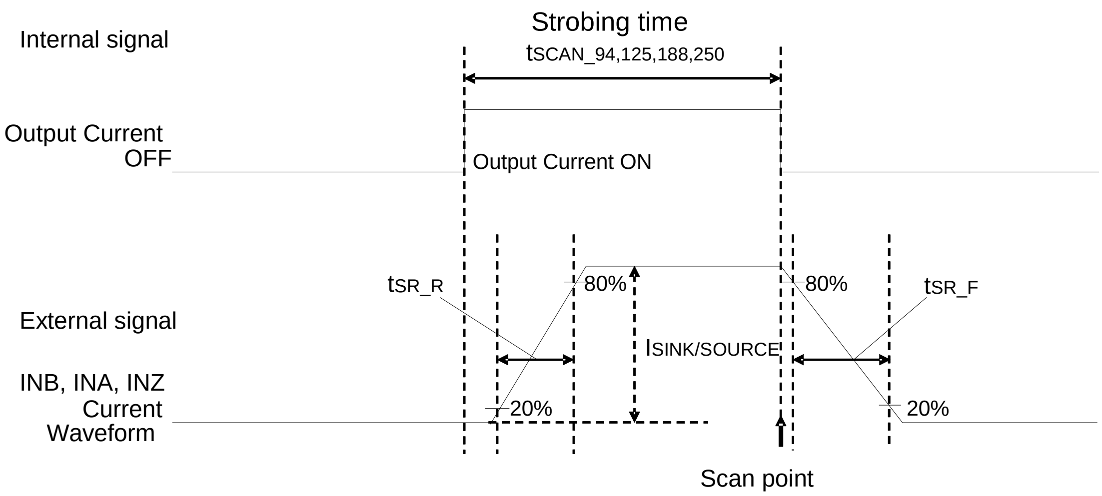


Figure 6. Intermittent Monitoring Enabled (FSQ=0, FSQZ/A/B=0, CMB/A/Z=1), Source/Sink Current Rise and Fall Time

[Basic Operation 1] Detection of Switch Status Change (Continuous Monitoring)

Upon detection of a change in switch status, interrupt (INTB="H"→"L") occurs and the IC requests serial communication with the MCU.

< Example of Recommended Operation Sequence >

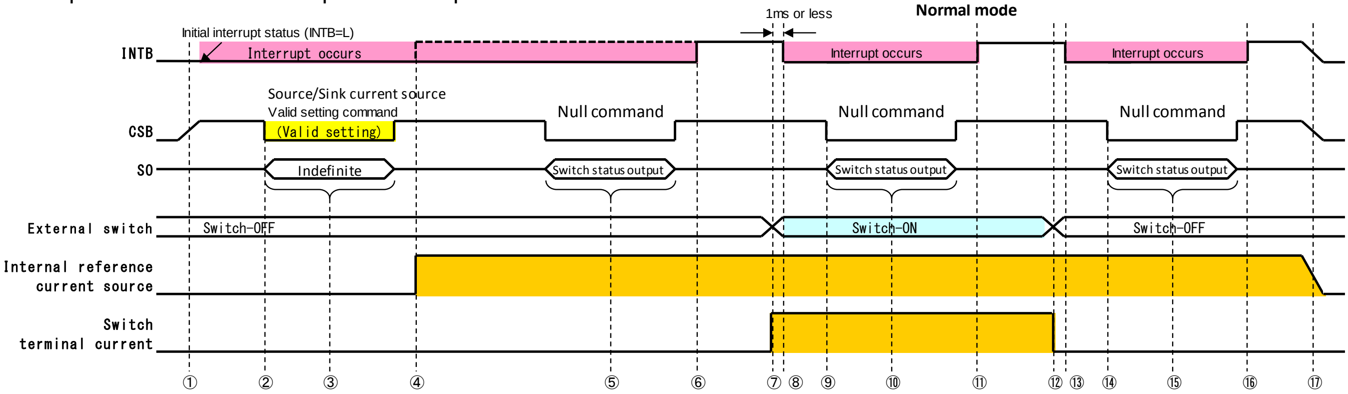


Figure 7. Basic Operation 1

①After power is turned on, interrupt (INTB="L") occurs.
②By serial communication, the switch status is obtained by the MCU at CSB falling edge.
③Since the current source is OFF, the switch terminal is "Hi-Z", and the output of SO is undefined.
④Internal reference current source is activated
⑤Switch status is output by SO.
⑥Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
⑦Switch change occurs (OFF→ON) and IC detects switch status change.
⑧Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested
⑨By serial communication, switch status is obtained by the MCU at CSB falling edge.
⑩Switch status is output by SO.
⑪Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
⑫Switch change occurs (ON→OFF) and IC detects switch status change.
⑬Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested
⑭By serial communication, the switch status is obtained by the MCU at CSB falling edge.
⑮Switch status is output by SO.
⑯Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
⑰Power is turned off.

[Basic Operation 2] Detection of Switch Status Change (Intermittent Monitoring)

When Intermittent Monitoring is enabled, switch status is monitored by periodically turning the current source on and off. Intermittent monitoring allows low power consumption.

< Example of Recommended Operation Sequence >

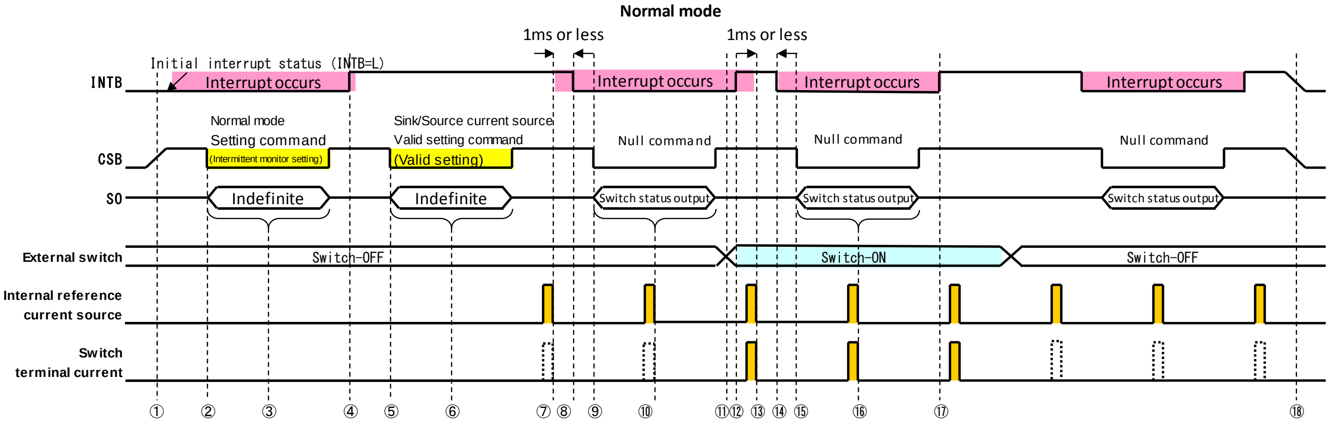


Figure 8. Basic Operation 2

①After power is turned on, interrupt (INTB="L") occurs.
②By serial communication, the switch status is obtained by the MCU at CSB falling edge.
③Since the current source is OFF, the switch terminal is "Hi-Z", and the output of SO is undefined.
④Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
⑤By serial communication, switch status is obtained by the MCU at CSB falling edge.
⑥Since the current source is OFF, the switch terminal is "Hi-Z", and the output of SO is undefined.
⑦IC gets the switch status when the current source is ON.
⑧Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested
⑨By serial communication, switch status is obtained by the MCU at CSB falling edge.
⑩Switch status is output by SO.
⑪IC detects switch status change.
⑫Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
⑬IC detects switch status change.
⑭Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested
⑮By serial communication, switch status is obtained by the MCU at CSB falling edge.
⑯Switch status is output by SO.
⑰Interrupt is cleared (INTB="L"→ "H") by CSB rising edge and prepares for switch change.
⑱Power is turned off.

[Basic Operation 3] Sleep Mode Operation (Manual Transition)

When MDC register of Monitor Mode Transition Command is set to “1”, mode is changed to sleep.
When MDC register of Monitor Mode Transition Command is set to “0”, mode is changed to normal.
During sleep mode, WAKEB is in “Hi-Z” state and its voltage level is the level of the external pull-up.

< Example of Recommended Operation Sequence >

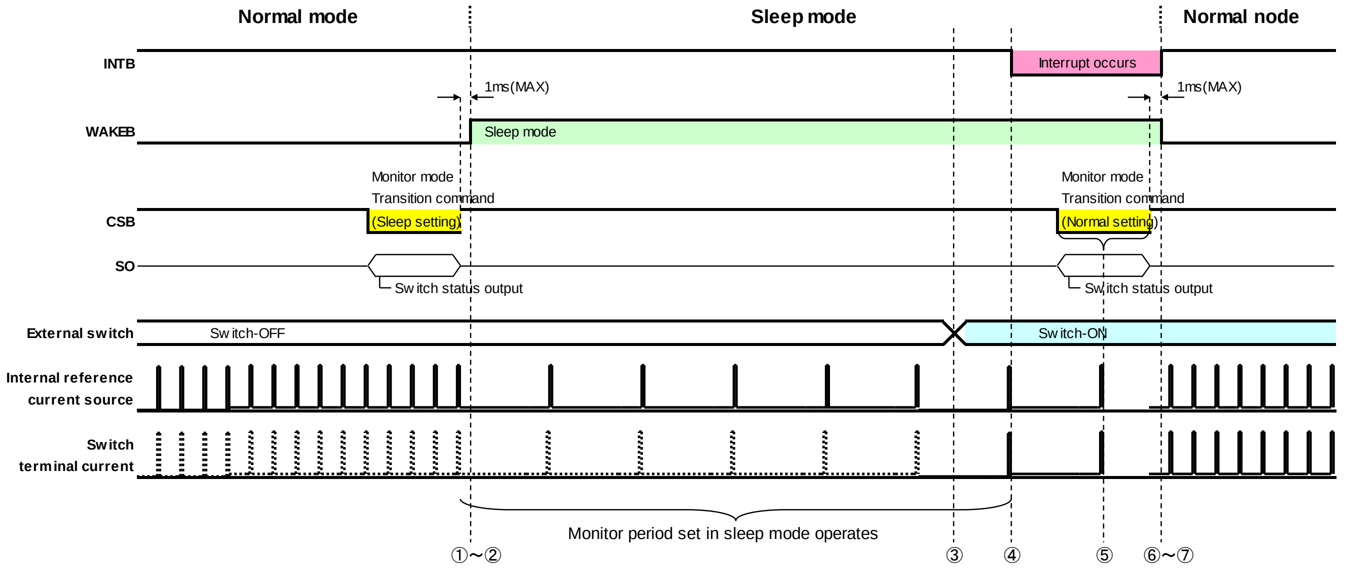


Figure 9. Basic Operation 3

①Monitor mode transition command (Sleep mode setting) is received from MCU.
②Transition to sleep mode.
③Switch change occurs (OFF→ON).
④IC detects switch status change.
⑤IC informs MCU the interrupt (INTB=“H”→“L”) and switch status is output by SO.
⑥Monitor mode transition command (Normal mode setting) is received from MCU.
⑦Transition to normal mode.

[Basic Operation 4] Sleep Mode Operation (Automatic Transition to Normal Mode)

Automatic transition from sleep mode to normal mode when a switch status changes is possible when the automatic mode transition setting is enabled.
During sleep mode, WAKEB is in "Hi-Z" state and its voltage level is the level of the external pull-up.

< Example of Recommended Operation Sequence >

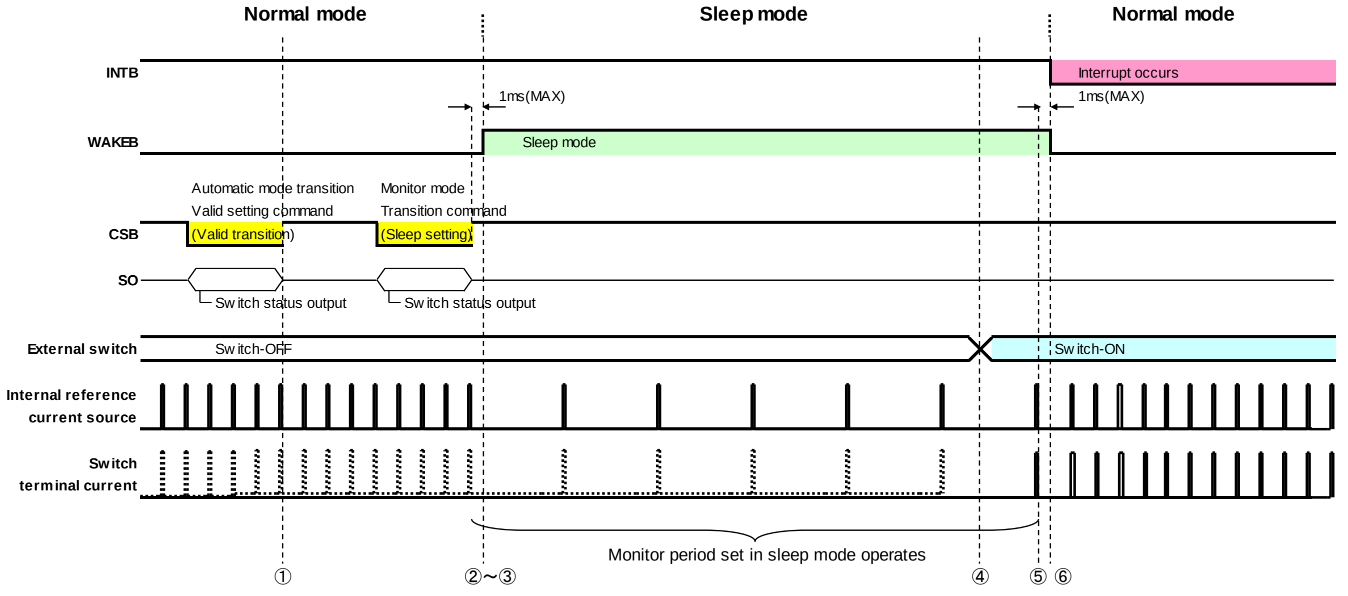


Figure 10. Basic Operation 4

①Automatic transition of mode is enable.
②Monitor mode transition command (sleep mode setting) is received from MCU.
③Transition to sleep mode.
④Switch change occurs (OFF→ON).
⑤IC detects switch status change.
⑥IC informs the interruption to MCU with INTB("H" →"L") and changes to Normal mode automatically.

Description of Functions

1. Power on Reset (POR)

Upon the application of an external voltage to VPUB, REF5 output is generated by the LDO inside the IC.
When REF5 ≤ 4.2(Typ), POR is activated.
When REF5 ≥ 4.3(Typ), POR is deactivated.

2. Serial Interface

Communication between BD3375KV-C and the MCU uses terminals chip select bar input (CSB), serial clock input (SCLK), serial data input (SI), and serial data output (SO).
CSB is internally pulled-up to VDDI. When CSB status is “0”, SCLK and SI inputs are valid, and it is possible to read data from SO. When CSB status is “1”, SCLK and SI inputs are invalid, and SO status is “Hi-Z”.

・Communication Frame

The transmitted frame by the MCU is a 40-bit structure composed of the transmission and reception discrimination (2-bit), the address (6-bit), the data (24-bit), and the CRC (8-bit). The transmission and reception discrimination (2-bit) is intended to differentiate between the transmitted and the received frame. The command (6-bit) sets various settings such as the “valid interrupt setting command”. The CRC (8-bit) outputs the result of a 39 to 8 bit CRC calculation. If a CRC error occurs, either when the structure of the frame is not 40-bit or when the transmission and reception discrimination bit is an error (the 33-bit of the SO frame is “H”), communication error is output and data is not recognized. As for writing, SI data is latched by internal shift register at timing of SCLK falling.

Table 13. Serial Data Input (SI)

Communication frame	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
SI input bit	Register address								Setting data							

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
Setting data																CRC

The received frame by the MCU has two types of bit alignment, “switch status output” and “register value output”.

The switch status output bit alignment is a 40-bit structure composed of transmission and reception discrimination (2-bit), a fixed value (1-bit), interrupt factor output (5-bit), another fixed value (1-bit), mode status output (1-bit), switch status output (22-bit), and CRC (8-bit).
Transmission and reception discrimination (2-bit) is intended to discriminate transmit and receive frame. The interrupt factor is discussed on Page 19. When an interrupt factor occurs, the corresponding bit becomes “1”. Mode status (1-bit) is “0” when set to normal mode, and it is “1” when set to sleep mode. Switch status output (22-bit) is “1” when external switch is ON, and it is “0” when external switch is OFF. The CRC (8-bit) outputs the result of a 39 to 8 bit CRC calculation.
The switch status is latched to the timing of CSB falling edge. The then in order of interrupt factor output, mode status and switch status output are output from SO by SCLK rising.

Table 14. Serial Data Output (SO-Switch Status Output)

Output frame	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
SO output bit	1	0	0	Interrupt factor output					0	Mode	Switch INB5-0 status output					

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
Switch INA7-0 status output								Switch INZ7-0 status output								CRC

The register value output bit alignment is a 40-bit structure composed of transmission and reception discrimination (2-bit), a fixed value (1-bit), interrupt factor output (5-bit), register value output (24-bit), and CRC (8-bit).
The data is output by SO at SCLK's rising edge after the CSB falling edge of the command following the register value output command.
The bit alignment of the register value output is shown on Table 37. The sequence of register value output is shown in Figure 11 and Figure 12.

Table 15. Serial Data Output (SO-Register Value Output)

Output frame	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
SO output bit	1	0	0	Interrupt factor output					Register value output							

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
Register value output																CRC

The register value output command (Table 38 RIER to RMDR) is used to read-back the register value written by register write command (Table 37 IER to MDR).
Figure 11 describes the single read-back sequence. Figure 12 describes the continuous read-back sequence.

<Single Read-back Sequence – Recommended Sequence>

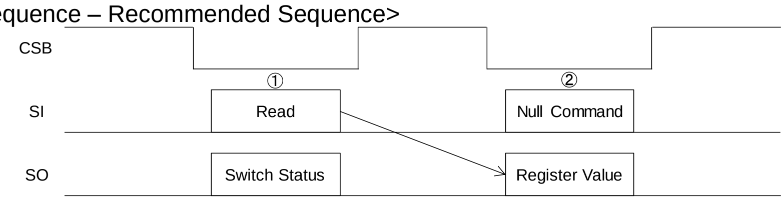


Figure 11. Single Read-back Sequence

① Send the register value output command.
The switch status is output by SO.
② Read the register value by sending the Null command.
The result of the register value output command ① is output by SO.

<Continuous Sequential Read-back Sequence – Recommended Sequence>

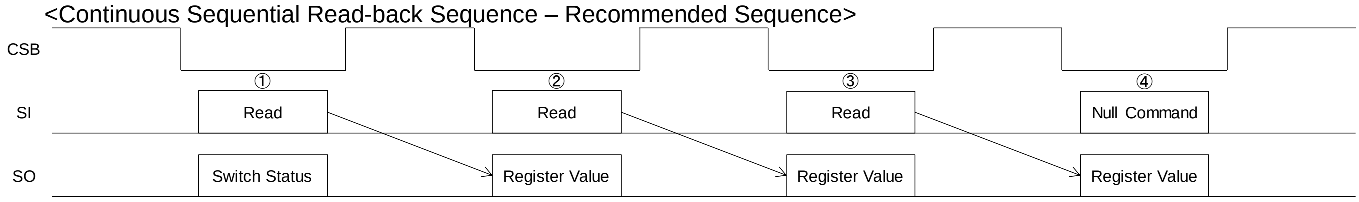


Figure 12. Continuous Read-back Sequence

① Send the register value output command.
The switch status is output by SO.
② Send the register value output command following ①. (The address of the register value output command does not need to be the next address.)
③ Send the register value output command repeatedly as needed.
The SO output at each command is the result of the previous register value output command.
④ Send the Null command in the end.
The register value of the previous register output command is output by SO.

3. Switch Status Output
Switch status can be sent through SO output.

4. Interrupt (INTB operation)

There are five interrupt factors that cause the INTB terminal to output an “L”. The type of interrupt factor that occurred can be checked in the SO output when CSB is “L”.
INTB output will return to “H” once the interrupt factor is cleared by the rising edge of CSB. The INTB terminal is an open-drain output that is internally pulled-up to VDDI.

・Interrupt Factors
The interrupt factors are shown below:

Interrupt Factor	Interrupt flag (SO output)	Flag name
① Test detection	SO output bit [36]	: “test_flg”
② Thermal shutdown detection	SO output bit [35]	: “them_flg”
③ Reset detection	SO output bit [34]	: “rst_flg”
④ Communication error detection (CRC error, 40-bit frame error, or transmission and reception discrimination error)	SO output bit [33]	: “err_flg”
⑤ Switch status change detection	SO output bit [32]	: “sw_flg”

① Test detection
The IC generates an interrupt after a transition to test mode. The TEST terminal should always be connected to ground.

② Thermal shutdown detection
Interrupt occurs when the thermal shutdown circuit detects a temperature higher than the allowable junction temperature inside IC.

③ Reset detection
Interrupt occurs after the activation of Power on Reset (POR) or the transmission of the reset command. Upon POR activation, the SO output interrupt flag “rst_flg” is reflected instantly. With reset command transmission, “rst_flg” is reflected on the next command transmission.

④ Communication error detection
Interrupt occurs due to either a CRC error, a 40-bit frame error, or a command transmission error. The interrupt flag “err_flg” is triggered by the following:

CRC error	: when there is a Cyclic Redundancy Check error
40-bit frame error	: when the command received is not 40-bit
Transmit and receive determination error	: when the first two bits of the command received is not [39:38]=“01”

⑤ Switch status change detection
Interrupt occurs when switch a status changes (switch-ON→OFF or switch-OFF→ON).

・Clearing of INTB output and interrupt factor
The INTB “L” output and the interrupt factor are both cleared by the CSB rising edge during command transmission. In case a new interrupt factor occurs during command transmission, the interrupt factor is not cleared. The new interrupt factor is reflected on the next command transmission.
The interrupt factor is not cleared by the register readout that follows the register value output command.

5. Operating Modes

BD3375KV-C has two types of operating mode, the normal and the sleep mode. Transition between the two modes can be done by sending the correct “Monitor Mode Transition Command”. The current mode of operation can be checked through the WAKEB and the SO terminal outputs.

Monitor Mode Transition register address (0x4F): Bit [31]: 0=Normal mode, 1=Sleep mode)

・Normal Mode

Normal mode operation can be set to continuous monitoring, wherein the switch status is checked by a continuously ON current source, or to intermittent monitoring, wherein the switch status is checked by a regularly ON/OFF current source. The period of intermittent monitoring (Note 17) can be set according to power supply system while strobe time (Note 18) is common for all switch terminals.

At normal mode, WAKEB is “L” and the 30-bit of the SO output is “0”.

・Sleep Mode

Sleep mode operation, like in normal mode, can be set to continuous monitoring or intermittent monitoring.
The monitoring period (Note 17) of intermittent monitoring can be set according to power supply system.
The strobe time (Note 18) is common for all switch terminals and both modes.

The difference with normal mode is that, from sleep mode, it is possible to change to normal mode automatically when interrupt occurs. (Automatic mode transition function)

At sleep mode, WAKEB is in “Hi-Z” state and its voltage level is the level of the external pull-up. The 30-bit of SO output is “1” at sleep mode.

(Note 17) Monitor period
(Note 18) Strobe time

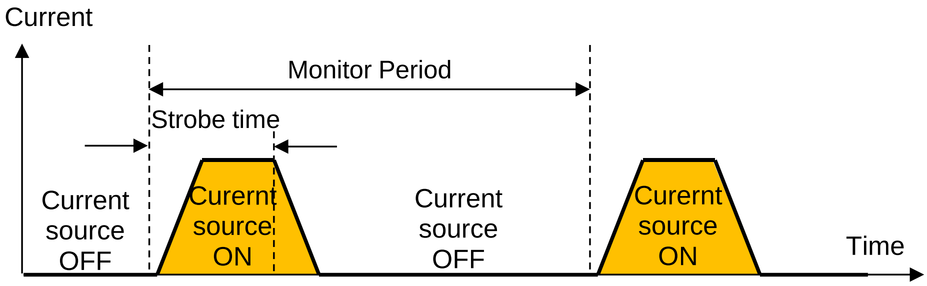


Figure 13. Intermittent Monitoring

6. Automatic Mode Transition Function

By sending the “Automatic Mode Transition Command” through setting the MIR register (0x4E) to “1”, automatic transition from sleep to normal mode is possible. The conditions for a change in mode from sleep to normal to occur for both enabled and disabled “Automatic Mode Transition Function” are shown below:

・Conditions for sleep to normal mode transition when “Automatic Mode Transition Function” is enabled:

1. Normal mode transition command is sent
2. POR occurs or reset command sent (Initialization)
3. A switch status changes (The “Switch Change Interrupt Setting” should be enabled)

・Conditions for sleep to normal mode transition when “Automatic Mode Transition Function” is disabled:

1. Normal mode transition command is sent
2. POR occurs or reset command sent (Initialization)

[Extension Function1: Intermittent Monitoring at the Same Time (with Current Slope)]

In intermittent monitoring, it is possible to detect the status of the all switches at the same time. When all inputs are set to detect the switch status by intermittent monitoring, the wetting current has a rising and falling slope.

Normal Mode Setting Register (0x4B) : 31 to 28 bit is “0000” and intermittent monitoring setting
Sleep Mode Setting Register (0x4C) : 31 to 28 bit is “0000” and intermittent monitoring setting

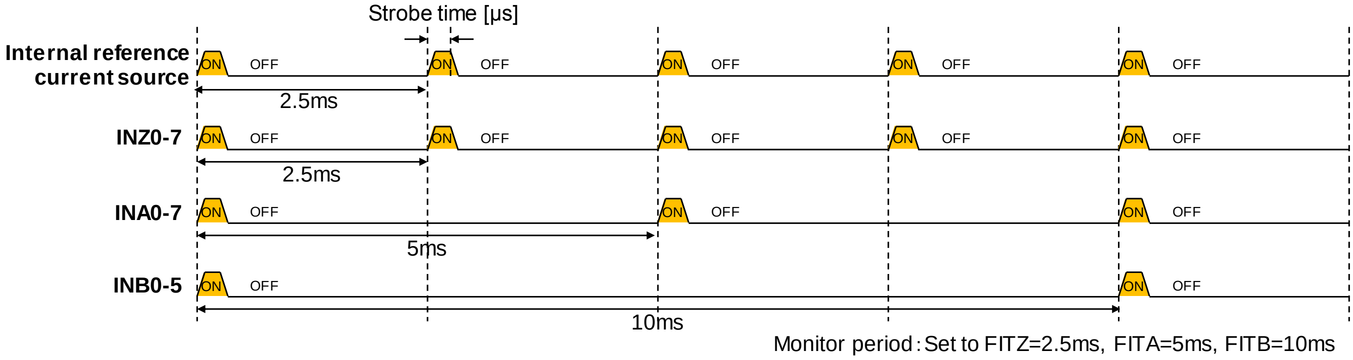


Figure 14. Intermittent Monitoring at the Same Time Example

[Extension Function 2: Sequential Monitoring by Power Supply System]

In this type of sequential monitoring, the status of the switches within a power supply system is monitored one at a time. This type has no slope. Since no two or more current sources in a power supply system are ON at the same time, radiation noise is reduced.

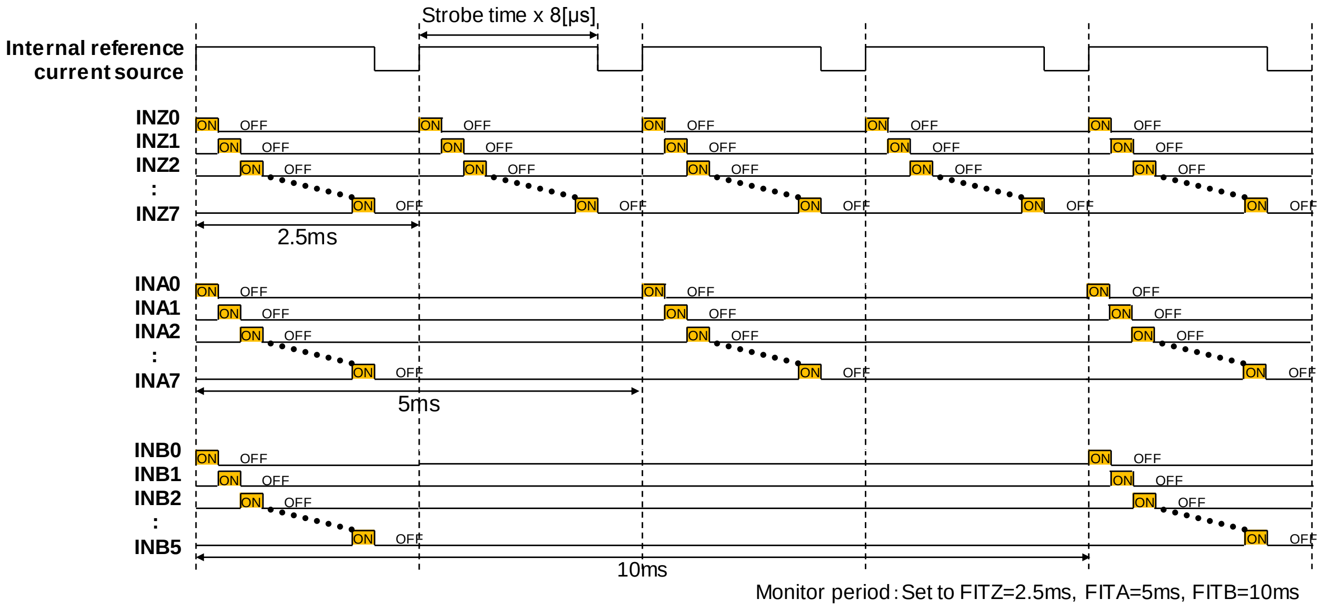


Figure 15. Sequential Monitoring by Power Supply System Example

[Extension Function 3: Sequential Monitoring of All Switch Terminals]

In this type of sequential monitoring, the status of all switches is monitored one at a time.
Since no two or more current sources are ON at the same time, radiation noise is reduced. This type has no slope.

The monitoring period for all switches increases by four times the monitoring period set for the INZ channels as shown in Figure 16. Uniform sequential monitoring and sequential monitoring by power supply should not be enabled at the same time. In case the two sequential monitoring methods are activated simultaneously, the method which prevails is uniform sequential monitoring.

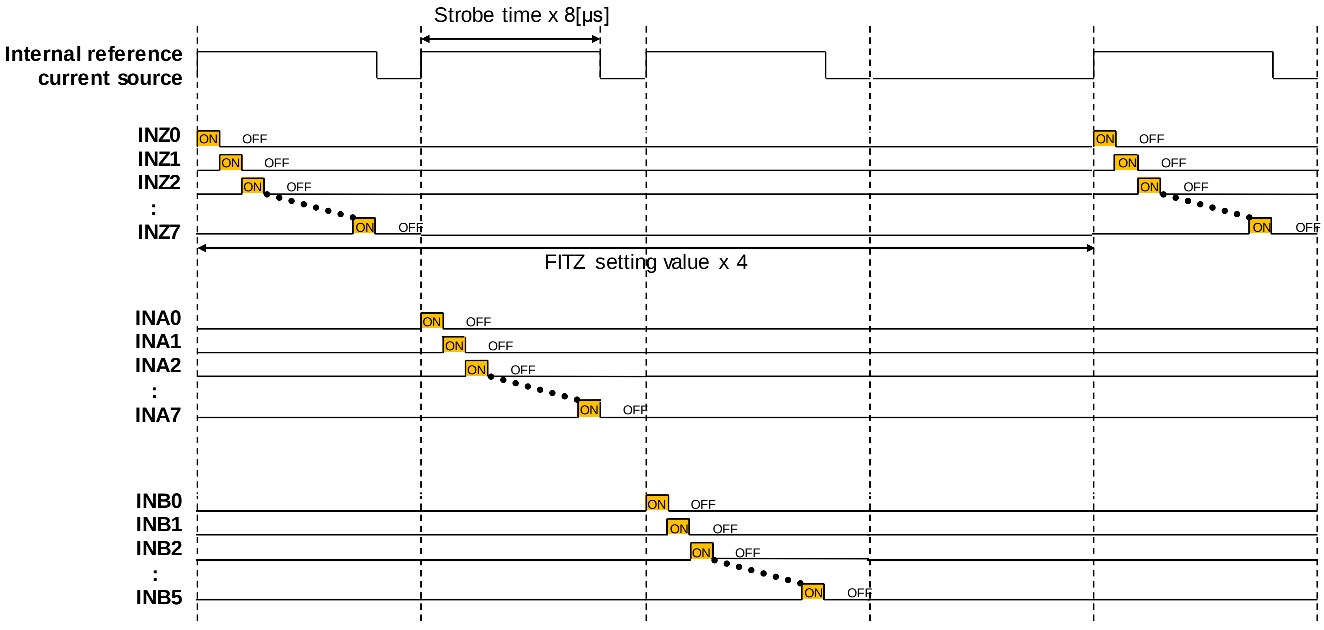


Figure 16. Sequential Monitoring of All Switches Terminals Example

7. WAKEB Terminal

WAKEB is an open drain output pin.
In normal mode, its output is “L”. In sleep mode, its output is “Hi-Z” and its voltage level is the level of the external pull-up.

8. Source/Sink Current Source for Switch Terminal

There are three types of switch terminal inputs with internal current source: INZ, INA, and INB. The current level can be set for each switch terminal.

・Current Source of INZ system (INZ0 – INZ7)
This current source is used to source or sink current to the external switch. The wetting current can be interchanged between pull-up and pull-down. VPUA is the power supply for the pull-up current source.

・Current Source of INA (INA0 – INA7)
This current source is used to source current to the external switch. VPUA is the power supply

・Current Source of INB (INB0 – INB5)
This current source is used to source current to the external switch. VPUB is the power supply.

The current source settings can be fixed by INZ current source/sink selection command, the current source setting command, and the holding current/wetting current value setting command.

9. Wetting Current Timer

The wetting current timer is 13ms to 22ms. This function can be enabled individually for each switch terminal. The timer starts after the switch has been detected as ON. After the 13ms to 22ms timer is finished, the wetting current (10mA/15mA) is switched to holding current (1mA/3mA/5mA). The timer is reset after the switch is turned OFF.

[Function operation1] Wetting Current Timer (Continuous Operation)

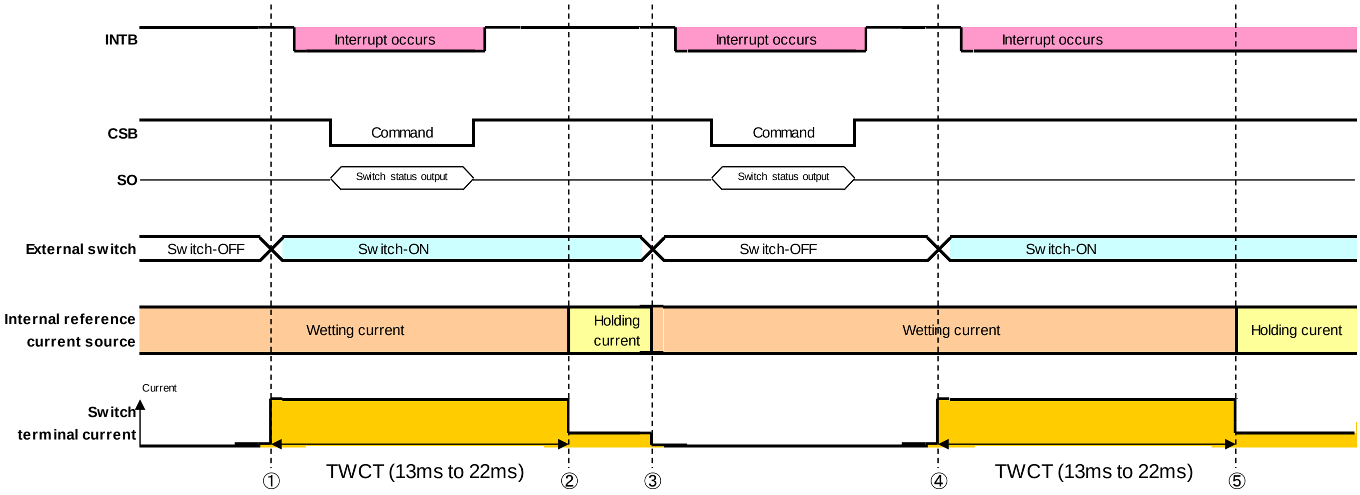


Figure 17. Wetting Current Timer (Continuous Operation)

① Switch change occurs (OFF→ON), IC detects switch status change.
② When ON state of the switch continues for more than 13ms to 22ms, the holding current is output.
③ Switch change occurs (ON→OFF).
④ Switch change occurs (OFF→ON), IC detects switch status change.
⑤ When ON state of the switch continues for more than 13ms to 22ms, the holding current is output.

[Function operation2] Wetting Current Timer (Intermittent Monitoring)

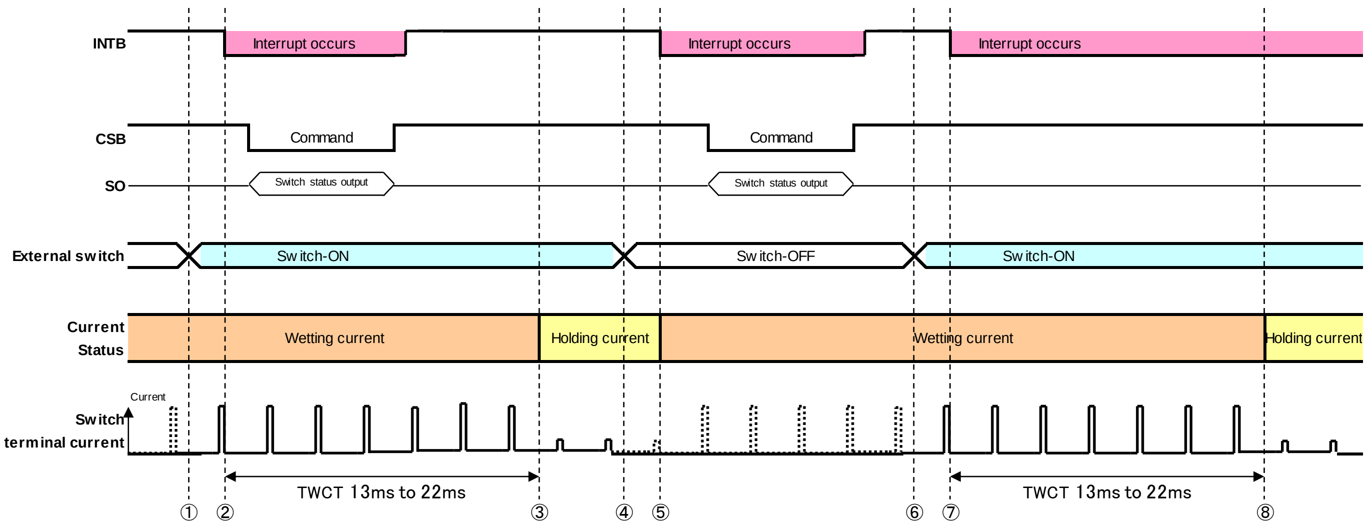


Figure 18. Wetting Current Timer (Intermittent Monitoring)

① Switch change occurs (OFF→ON)
② IC detects switch status change.
③ When ON state of the switch continues for more than 13ms to 22ms, the holding current is output.
④ Switch change occurs (ON→OFF).
⑤ IC detects switch status change, switch current is switched from holding current to wetting current.
⑥ Switch change occurs (OFF→ON).
⑦ IC detects switch status change.
⑧ When ON state of the switch continues for more than 13ms to 22ms, the holding current is output.

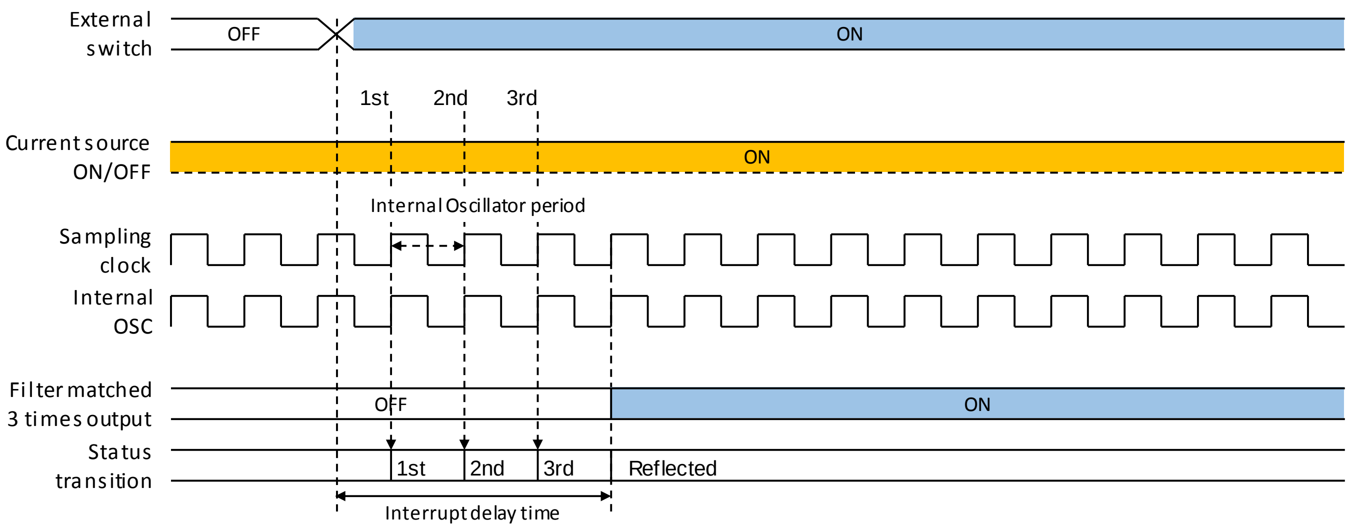
10. n-Times Matched Filter

All switch inputs have built-in "1 to 6 times matched filters". This function can filter the ON/OFF switch status judgment made by the internal comparator. The filter function can be enabled for each power supply system. If the register has been updated during the counting of the filter, the counting is not reset.

If the monitoring method is continuous monitoring, the switch state is filtered n times (n: 1 to 6) multiplied by the period of the internal oscillator (32 kHz).

If the monitoring method is intermittent monitoring, the switch state is filtered n times (n: 1 to 6) multiplied by the monitoring period.

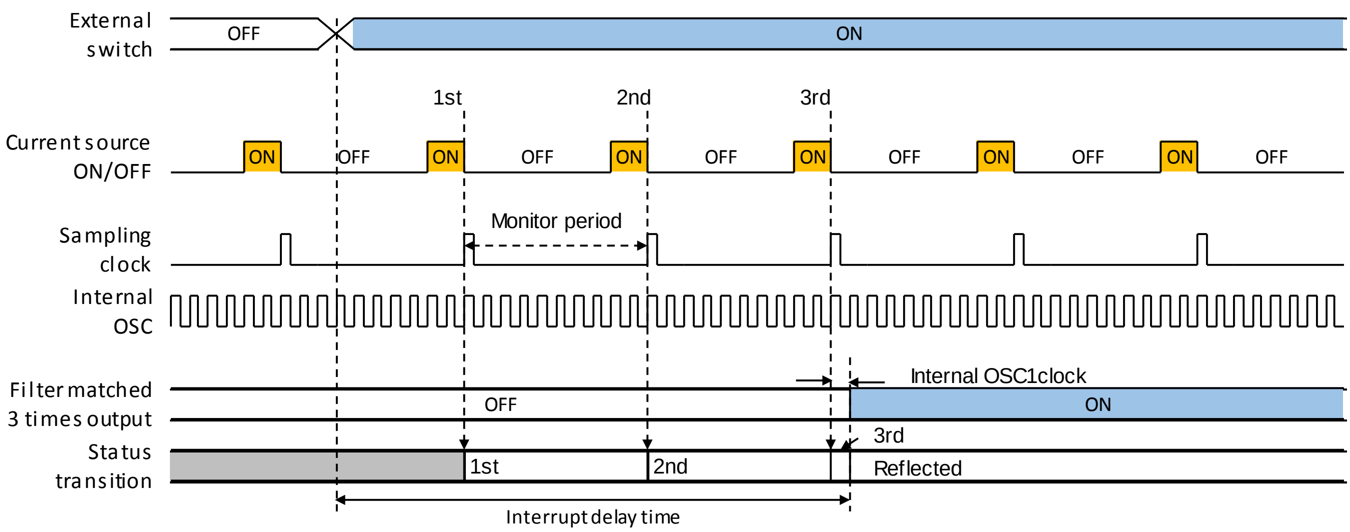
・**Set to full-time monitor :** Sampling period is internal oscillator period : 31.25µs (Typ)



Time from Monitoring to End of Filtering:
{Monitoring Period x (Filter Number of Times -1) + Period of Internal Oscillator}
to {Monitoring Period x (Filter Number of Times) + Period of Internal Oscillator}

Figure 19. 3 Times Matched Filter Operation on Continuous Monitoring

・**Set to intermittent monitor :** Sampling monitor period is common with monitor period.



Time from Monitoring to End of Filtering:
{Monitoring Period x (Filter Number of Times -1) + Period of Internal Oscillator}
to {Monitoring Period x (Filter Number of Times) + Period of Internal Oscillator}

Figure 20. 3 Times Matched Filter Operation on Intermittent Monitoring

11. Digital Multiplexer Output (DMUX)

The status of the selected switch input is reflected by the DMUX terminal. DMUX takes the output of the comparator on a timing determined by the monitoring method.
Only one switch terminal at a time can be selected to be reflected by DMUX.
When no switch is selected, the output of DMUX is “L”.

12. Input Threshold Voltage of Switch Terminal

The switch input threshold voltage is a fraction of the AVDD voltage. It can be set to 3.0V or to 4.0V.

・3.0V Setting：V_{TH3}=AVDDx0.6 (8.0V≤VPUB≤26V)
・4.0V Setting：V_{TH4}=AVDDx0.8 (8.0V≤VPUB≤26V)

Table 16. Relationship between the Switch Input Threshold Voltage and the SO Output

Input type	Source or Sink	Input Voltage	Comparator output	SO serial interface bit
INZ	Source	INZ<Threshold	0	H
	Source	INZ>Threshold	1	L
	Sink	INZ<Threshold	0	L
	Sink	INZ>Threshold	1	H
INA,INB	N/A	INA,INB<Threshold	0	H
	N/A	INA,INB>Threshold	1	L

13. Over-temperature Protection Circuit

When the junction temperature of the IC becomes higher than the thermal limit 160°C (Typ), interrupt (INTB=“L”) occurs and the source/sink current through the switch terminals is switched to 1mA (Min). The MCU is notified by the SO over-temperature detection flag (them_flg) changing to “1” that an irregularity in temperature has occurred. When the junction temperature of the IC has fallen below 140°C (Typ), interrupt is cleared on the next command transmission and the wetting current level returns to what was set on the registers.

Notice: The over-temperature detection value, 155°C to 175°C, and the hysteresis temperature, 10°C to 30°C, were not tested in shipment test. Also, the over-temperature protection circuit operates beyond the absolute maximum temperature ratings so the IC should not be used in a system where activation of the said protection function is expected.

14. Cyclic Redundancy Check (CRC)

The 7-0th bit of both the transmitted and received communication frame of the IC is the cyclic redundancy check (CRC), which is responsible for the detection of a data communication error.
If the IC received a CRC error, asserts interruption (INTB=“L”) and error flag (“err_flg”) to SO output. SO output becomes “H” on the next communication to notify the MCU of the error. A command that has a CRC error is not a valid command.

The CRC generation polynomial is

$$X^8 + X^5 + X^4 + 1.$$

Command Description

Each Command has two types of functions. One is to write a value to a register. The other is to read back the register value which was written by the write command. The function to be used is set by the 37-bit of each command. (The Null and Reset commands don't include the register value output command because they don't write in the registers.)
In the command descriptions below, the Write Command is for writing a value to a register and the read command is for reading back a register value.

1. Null Command
This command is a read only command that allows the user to monitor interruption and switch status.

Table 17. Null Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Null Command (Read Only)	IRC	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

2. Interrupt Notification of Switch Change Setting Command
This command allows the user to configure interrupt sources for the INTB pin.
Specifically, this command allows the user to individually configure which switches trigger an interrupt on INTB by enabling or disabling the IEBn, IEAn, and IEZn setting bits shown below.
The SO output will return the switch status depending on the settings stored at the next CSB falling edge.

Table 18. Interrupt Notification of Switch Change Setting Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Interrupt Notification of Switch Change Setting	IER	0	1	W/R	0	0	0	0	1	x	x	IEB5	IEB4	IEB3	IEB2	IEB1	IEB0

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
IEA7	IEA6	IEA5	IEA4	IEA3	IEA2	IEA1	IEA0	IEZ7	IEZ6	IEZ5	IEZ4	IEZ3	IEZ2	IEZ1	IEZ0	CRC

IEBn (n: 5-0) [Default: 1] Interrupt Notification of Switch Status Change for INB System
0: Disabled 1: Enabled
IEAn (n: 7-0) [Default: 1] Interrupt Notification of Switch Status Change for INA System
0: Disabled 1: Enabled
IEZn (n: 7-0) [Default: 1] Interrupt Notification of Switch Status Change for INZ System
0: Disabled 1: Enabled
W/R Register Write/Read Setting
0: Write 1: Read

3. Comparator Operation Control Command
This command allows the user to individually enable or disable the switch terminal comparator for each switch input.
When a switch input's comparator is disabled through this register, both the corresponding settings available for that switch input within the "Interrupt Notification of Switch Change Setting Command" and the "Source/Sink Current Setting Command" are invalid.
When the comparator is active, the switch status output does not depend on whether the wetting current is set to source or sink. The switch status output is "1" when the switch is ON and "0" when the switch is OFF.
When the comparator is set to disabled, the switch status is undefined.

Table 19. Comparator Operation Control Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Comparator Operation Control	CMR	0	1	W/R	0	0	0	1	0	x	x	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
CMA7	CMA6	CMA5	CMA4	CMA3	CMA2	CMA1	CMA0	CMZ7	CMZ6	CMZ5	CMZ4	CMZ3	CMZ2	CMZ1	CMZ0	CRC

CMBn (n: 5-0) [Default: 1] Comparator Operation for INB System
0: Disabled 1: Enabled
CMAn (n: 7-0) [Default: 1] Comparator Operation for INA System
0: Disabled 1: Enabled
CMZn (n: 7-0) [Default: 1] Comparator Operation for INZ System
0: Disabled 1: Enable
W/R Register Write/Read Setting
0: Write 1: Read

4. Comparator Threshold Selection Command
This command allows the user to set the comparator threshold of the switch terminals.
Switch detection threshold selection is available for each power supply system (See CTB, CTA, CTZ settings shown below).

Table 20. Comparator Threshold Selection Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Comparator Threshold Selection	CTR	0	1	W/R	0	0	0	1	1	CTB	CTA	CTZ	x	x	x	x	x

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

CTB [Default: 0] Comparator Threshold for INB System
0: 3.0V 1: 4.0V
CTA [Default: 0] Comparator Threshold for INA System
0: 3.0V 1: 4.0V
CTZ [Default: 0] Comparator Threshold for INZ System
0: 3.0V 1: 4.0V
W/R Register Write/Read Setting
0: Write 1: Read

5. INZ Current Source/Sink Selection Command
This command allows the user to select the current configuration, whether source (internal pull-up current source) or sink (internal pull-down current source), through the INZ input switch terminals.

Table 21. INZ Current Source/Sink Selection Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
INZ Current Source/Sink Selection	PUDR	0	1	W/R	0	0	1	0	0	x	x	x	x	x	x	x	x

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	PUD7	PUD6	PUD5	PUD4	PUD3	PUD2	PUD1	PUD0	CRC

PUDn (n: 7-0) [Default: 0] Source or Sink Selection for INZ System
0: Source (Internal Pull-up Current Source)
1: Sink (Internal Pull-down Current Source)
W/R Register Write/Read Setting
0: Write 1: Read

6. Current Source Activation Command
This command allows the user to enable or disable the wetting current sources at the switch input terminals. The current sources can be set to ON or OFF per power supply system.
The output current level is determined by the "Holding Current / Wetting Current Value Setting Command" discussed in section 7 below.
If an external current source is used, the comparator should be enabled (see section 3 above) and the internal current source should be disabled using this register.

Table 22. Current Source Activation Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Current Source Activation	CER	0	1	W/R	0	0	1	0	1	CEB	CEA	CEZ	x	x	x	x	x

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

CEB [Default: 0] Current Sources of INB System
0: OFF 1: ON
CEA [Default: 0] Current Sources of INA System
0: OFF 1: ON
CEZ [Default: 0] Current source of INZ System
0: OFF 1: ON
W/R Register Write/Read Setting
0: Write 1: Read

7. Holding Current / Wetting Current Level Selection Command

This command allows the user to select the output level of each current source. This command also has arguments to set both the holding and the wetting current.
The holding current can be set to 1mA, 3mA, or 5mA.
The wetting current can be set to OFF (“Hi-Z”), 1mA, 3mA, 5mA (set to holding current), 10mA, or 15mA.
Unlike holding current, wetting current output levels can be set individually for each switch terminal.

Table 23. Holding Current / Wetting Current Level Selection Command (LSB)

Command 0:“L”, 1:“H”, x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Holding Current / Wetting Current Level Selection (LSB)	LCR	0	1	W/R	0	0	1	1	0	CRH1	CRH0	LCB5	LCB4	LCB3	LCB2	LCB1	LCB0

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
LCA7	LCA6	LCA5	LCA4	LCA3	LCA2	LCA1	LCA0	LCZ7	LCZ6	LCZ5	LCZ4	LCZ3	LCZ2	LCZ1	LCZ0	CRC

Table 24. Holding Current / Wetting Current Level Selection Command (MSB)

Command 0:“L”, 1:“H”, x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Holding Current / Wetting Current Level Selection (MSB)	MCR	0	1	W/R	0	0	1	1	1	x	x	MCB5	MCB4	MCB3	MCB2	MCB1	MCB0

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
MCA7	MCA6	MCA5	MCA4	MCA3	MCA2	MCA1	MCA0	MCZ7	MCZ6	MCZ5	MCZ4	MCZ3	MCZ2	MCZ1	MCZ0	CRC

CRH [1:0] [Default: 00] Holding Current Value
00: 1mA 01: 3mA
10: 5mA 11: 1mA

{MCBn (n: 5-0), LCBn (n: 5-0)} [Default: 01] Wetting Current Value for INB System
00: Invalid(Hi-Z) 01: 1/3/5mA(Holding Current Value)
10: 10mA 11: 15mA

{MCAn (n: 7-0), LCAn (n: 7-0)} [Default: 01] Wetting Current Value for INA System
00: Invalid(Hi-Z) 01: 1/3/5mA(Holding Current Value)
10: 10mA 11: 15mA

{MCZn (n: 7-0), LCZn (n: 7-0)} [Default: 01] Wetting Current Value for INZ System
00: Invalid(Hi-Z) 01: 1/3/5mA(Holding Current Value)
10: 10mA 11: 15mA

W/R Register Write/Read Setting
0: Write 1: Read

8. Wetting Current Operation Control Command

This command allows the user to enable or disable the “wetting current timer”.
This “wetting current timer” counts 13 to 22ms after the switch has been closed and the wetting current changes to holding current (1mA/3mA/5mA). The timer is reset when the switch is turned off.
If the wetting current level is the same as the holding current level, the timer does not operate.
The wetting current timer can be enabled or disabled individually for each switch terminal.

Table 25. Wetting Current Operation Control Command

Command 0:“L”, 1:“H”, x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Wetting Current Operation Control	WTR	0	1	W/R	0	1	0	0	0	x	x	WTB5	WTB4	WTB3	WTB2	WTB1	WTB0

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
WTA7	WTA6	WTA5	WTA4	WTA3	WTA2	WTA1	WTA0	WTZ7	WTZ6	WTZ5	WTZ4	WTZ3	WTZ2	WTZ1	WTZ0	CRC

WTBn (n: 5-0) [Default: 0] Wetting Current Timer for INB System
0: Disabled 1: Enabled

WTAn (n: 7-0) [Default: 0] Wetting Current Timer for INA System
0: Disabled 1: Enabled

WTZn (n: 7-0) [Default: 0] Wetting Current Timer for INZ System
0: Disabled 1: Enabled

W/R Register Write/Read Setting
0: Write 1: Read

9. n-Times Matched Filter Activation Control Command

This command allows the user to enable or disable the n-times matched LPF.

If this function is enabled, the switch output is updated only after the comparator output has been sampled “n” times (where n = 1 to 10) and if all sampled comparator outputs match.

This command allows for each switch terminal to be enabled or disabled individually.

Table 26. n-Times Matched Filter Activation Control Command

Command 0:“L”, 1:“H”, x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
n-Times Matched Filter Activation Control	DFR	0	1	W/R	0	1	0	0	1	DFB2	DFB1	DFB0	DFA2	DFA1	DFA0	DFZ2	DFZ1

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
DFZ0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

DFB [2:0] [Default: 000] n-Times Matched LPF Settings for INB System

000	: Disabled (1 time)	001	: 2 times
010	: 3 times	011	: 4 times
100	: 5 times	101	: 6 times
110	: Disabled (1 time)	111	: Disabled (1 time)

DFA [2:0] [Default: 000] n-Times Matched LPF Settings for INA System

000	: Disabled (1 time)	001	: 2 times
010	: 3 times	011	: 4 times
100	: 5 times	101	: 6 times
110	: Disabled (1 time)	111	: Disabled (1 time)

DFZ [2:0] [Default: 000] n-Times Matched LPF Settings for INZ System

000	: Disabled (1 time)	001	: 2 times
010	: 3 times	011	: 4 times
100	: 5 times	101	: 6 times
110	: Disabled (1 time)	111	: Disabled (1 time)

W/R Register Write/Read Setting

0: Write 1: Read

10. DMUX Setting Command

This command allows the user to enable/disable and configure selected switch output on the DMUX terminal.
The result of the chosen switch terminal's comparator is taken and output to DMUX using timing that depends on the monitoring method used.
Any switch input terminal can be connected to this DMUX pin by adjusting the DMX0 to DMX4 bits shown below.

Table 27. DMUX Setting Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
DMUX Setting	DMR	0	1	W/R	0	1	0	1	0	DMX4	DMX3	DMX2	DMX1	DMX0	x	x	x

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

Table 28. DMUX Channel Selection

31-27 bit	Selected Channel
00000	Disabled (Output is "L")
00001	INZ0
00010	INZ1
00011	INZ2
00100	INZ3
00101	INZ4
00110	INZ5
00111	INZ6
01000	INZ7
01001	INA0
01010	INA1
01011	INA2
01100	INA3
01101	INA4
01110	INA5
01111	INA6
10000	INA7
10001	INB0
10010	INB1
10011	INB2
10100	INB3
10101	INB4
10110	INB5
10111-11111	Disabled (Output is "L")

DMX [4:0] [Default: 00000]	DMUX Terminal Setting	
	00000	: Disabled (DMUX output is "L")
	00001 - 10110	: Selected Channel
	10110 - 11111	: Disabled (DMUX output is "L")
W/R	Register Write/Read Setting	
	0: Write	1: Read

11. Normal Mode Setting Command

This command allows the user to set the monitoring period, strobe time, and monitoring method of normal mode.
The normal mode is set after power on reset or by "Monitor Mode Transition Command".
The monitoring period can be set individually per power supply system but the strobe time is common to all switch terminals.
The monitoring method can be set continuous monitoring, intermittent monitoring at the same time, sequential monitoring by power supply system and sequential monitoring of all switch terminals.

- Continuous Monitoring:
  IC monitors switch status continuously.
  Refer to the "[Basic Operation 1] Detection of switch status change (Continuous Monitoring)" section for additional details.
- Intermittent Monitoring at the Same Time:
  IC monitors switch status per power supply system at the same time.
  Refer to the "[Extension Function1: Intermittent Monitoring at the Same Time (with Current Slope)]" section for additional details.
- Sequential Monitoring by Power Supply System:
  IC monitors switch status per switch by turns on power supply system.
  Refer to the "[Extension Function 2: Sequential Monitoring by Power Supply System]" section for additional details.
- Sequential Monitoring of All Switch Terminals:
  IC monitors switch status per switch by turns.
  Refer to the "[Extension Function 3: Sequential Monitoring of All Switch Terminals]" section for additional details.

If both sequential and continuous monitoring are enabled at the same time, continuous monitoring will be the one implemented.
If both sequential monitoring by power supply system and sequential monitoring of all switch terminals are enabled at the same time, sequential monitoring of all switch terminals will be the one implemented.

Table 29. Normal Mode Setting Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Normal Mode Setting	FMR	0	1	W/R	0	1	0	1	1	FSQ	FSQB	FSQA	FSQZ	FITB2	FITB1	FITB0	FITA2

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
FITA1	FITA0	FITZ2	FITZ1	FITZ0	SVW1	SVW0	FITB3	FITA3	FITZ3	x	x	x	x	x	x	CRC

FSQ [Default: 0] — Sequential Monitoring of All Switch Terminals
0: Disabled 1: Enabled

FSQB [Default: 0] — Sequential Monitoring by Power Supply System for INB System
0: Disabled 1: Enabled

FSQA [Default: 0] — Sequential Monitoring by Power Supply System for INA System
0: Disabled 1: Enabled

FSQZ [Default: 0] — Sequential Monitoring by Power Supply System for INZ System
0: Disabled 1: Enabled

FIT*[3:0] (*: B, A, Z) [Default: 0000] — Monitoring Period for Normal Mode
0000: Continuous Monitoring 0001: 2.5ms
0010: 5ms 0011: 10ms
0100: 20ms 0101: 30ms
0110: 40ms 0111: 50ms
1000: 100ms 1001 – 1111: Setting prohibited

SVW [1:0] [Default: 01] — Strobe Time
00: 93.75µs 01: 125µs
10: 187.5µs 11: 250µs

W/R — Register Write/Read Setting
0: Write 1: Read

12. Sleep Mode Setting Command

This command allows the user to set the monitoring period and monitoring method of sleep mode.
The sleep mode is set by "Monitor Mode Transition Command".
The strobe time of sleep mode is the same as the normal mode.
About the monitoring period and monitoring method, refer to the "Normal Mode Setting Command" discussed in section 11 below.

Table 30. Sleep Mode Setting Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Sleep Mode Setting	SMR	0	1	W/R	0	1	1	0	0	SSQ	SSQB	SSQA	SSQZ	SITB2	SITB1	SITB0	SITA2

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
SITA1	SITA0	SITZ2	SITZ1	SITZ0	x	x	SITB3	SITA3	SITZ3	x	x	x	x	x	x	CRC

SSQ [Default: 0] — Sequential Monitoring of All Switch Terminals
0: Disabled 1: Enabled

SSQB [Default: 0] — Sequential Monitoring by Power Supply System for INB System
0: Disabled 1: Enabled

SSQA [Default: 0] — Sequential Monitoring by Power Supply System for INA System
0: Disabled 1: Enabled

SSQZ [Default: 0] — Sequential Monitoring by Power Supply System for INZ System
0: Disabled 1: Enable

SIT*[3:0] (*: B, A, Z) [Default: 0111] — Monitoring Period for Sleep Mode
0000: Continuous Monitoring 0001: 2.5ms
0010: 5ms 0011: 10ms
0100: 20ms 0101: 30ms
0110: 40ms 0111: 50ms
1000: 100ms 1001 – 1111: Setting prohibited

W/R — Register Write/Read Setting
0: Write 1: Read

13. Detection Edge Selection Command

This command allows the user to configure interrupt trigger of switches for the INTB pin.
The interrupt trigger can be set to only the falling edge (Note 19) or both the rising and falling edges of the switch input voltage per power supply system.
If only the falling edge is selected, the INTB pin not changes by the rising edges of switch input voltage.

(Note 19) If the INZ current "Source Setting" is enabled, the falling edge of the switch input terminal is seen when the external switch is turned on. If the INZ current "Sink Setting" is enabled, the falling edge is seen when the external switch is turned off.

Table 31. Detection Edge Selection Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Detection Edge Selection	ISR	0	1	W/R	0	1	1	0	1	ISB	ISA	ISZ	x	x	x	x	x

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

ISB [Default: 1] Switch edge where interrupt occurs for INB System
0: Only Falling Edge 1: Both Edges

ISA [Default: 1] Switch edge where interrupt occurs for INA System
0: Only Falling Edge 1: Both Edges

ISZ [Default: 1] Switch edge where interrupt occurs for INZ System
0: Only Falling Edge 1: Both Edges

W/R Register Write/Read Setting
0: Write 1: Read

14. Automatic Mode Transition Command

This command allows the user to configure the mode to automatically change by a change in switch status.
If the automatic transition is enabled, the monitoring period and monitoring method are changed to normal mode settings when it detects a change in switch status on sleep.
Refer to the "[Basic Operation 4] Sleep Mode Operation Automatic Transition to Normal Mode" section for additional details on how sleep mode operations works for this IC.

Table 32. Automatic Mode Transition Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Automatic Mode Transition	MIR	0	1	W/R	0	1	1	1	0	MR_IER	x	x	x	x	x	x	x

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

MR_IER [Default: 1] Automatic Mode Transition
0: Disabled 1: Enabled

W/R Register Write/Read Setting
0: Write 1: Read

15. Monitor Mode Transition Command

This command allows the user to change the mode of operation between normal and sleep.
Refer to the "[Basic Operation 3] Sleep Mode Operation (Manual Transition)" section for additional details on how sleep mode operations works for this IC.

Table 33. Monitor Mode Transition Command

Command 0:"L", 1:"H", x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Monitor Mode Transition	MDR	0	1	W/R	0	1	1	1	1	MDC	x	x	x	x	x	x	x

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

MDC [Default: 0] Monitoring mode
0: Normal Mode 1: Sleep Mode

W/R Register Write/Read Setting
0: Write 1: Read

16. Reset Command

This command allows the user to reset the registers to their initial settings. After the reset command has been sent, the physical interrupt pin goes to low (INTB=“L”).

Table 34. Reset Command

Command 0:“L”, 1:“H”, x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Reset	RST	0	1	0	1	1	1	1	1	x	x	x	x	x	x	x	x

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

17. TEST Command

This command is used to enter test mode, which is only possible when the TEST pin is “H”.

Table 35. TEST Command

Command 0:“L”, 1:“H”, x: don't care		Register address								Setting data							
		39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
TEST	TSR	0	1	1	1	1	0	0	1	TSS7	TSS6	TSS5	TSS4	TSS3	TSS2	TSS1	TSS0

Setting data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7-0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

18. Register Map

Table 36. Register Map

Register Name	Symbol	Register Address	Setting Data Name (def*: Default Setting)																								CRC
		39:32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7:0
Null Command	IRC	0x40																									CRC
Interrupt Notification of Switch Change Setting Command [Default: Valid]	IER	0x41			IEB5 (def:1)	IEB4 (def:1)	IEB3 (def:1)	IEB2 (def:1)	IEB1 (def:1)	IEB0 (def:1)	IEA7 (def:1)	IEA6 (def:1)	IEA5 (def:1)	IEA4 (def:1)	IEA3 (def:1)	IEA2 (def:1)	IEA1 (def:1)	IEA0 (def:1)	IEZ7 (def:1)	IEZ6 (def:1)	IEZ5 (def:1)	IEZ4 (def:1)	IEZ3 (def:1)	IEZ2 (def:1)	IEZ1 (def:1)	IEZ0 (def:1)	CRC
Comparator Operation Control Command [Default: Valid]	CMR	0x42			CMB5 (def:1)	CMB4 (def:1)	CMB3 (def:1)	CMB2 (def:1)	CMB1 (def:1)	CMB0 (def:1)	CMA7 (def:1)	CMA6 (def:1)	CMA5 (def:1)	CMA4 (def:1)	CMA3 (def:1)	CMA2 (def:1)	CMA1 (def:1)	CMA0 (def:1)	CMZ7 (def:1)	CMZ6 (def:1)	CMZ5 (def:1)	CMZ4 (def:1)	CMZ3 (def:1)	CMZ2 (def:1)	CMZ1 (def:1)	CMZ0 (def:1)	CRC
Comparator Threshold Selection Command [Default: 3.0V]	CTR	0x43	CTB (def:0)	CTA (def:0)	CTZ (def:0)																						CRC
INZ Current Source/Sink Selection Command [Default: Source]	PUDR	0x44																	PUD7 (def:0)	PUD6 (def:0)	PUD5 (def:0)	PUD4 (def:0)	PUD3 (def:0)	PUD2 (def:0)	PUD1 (def:0)	PUD0 (def:0)	CRC
Current Source Activation Command [Default: OFF (Invalid)]	CER	0x45	CEB (def:0)	CEA (def:0)	CEZ (def:0)																						CRC
Holding Current / Wetting Current Level Selection Command (LSB) [Default: Wetting current =1mA (Holding current)]	LCR	0x46	CRH1 (def:0)	CRH0 (def:0)	LCB5 (def:1)	LCB4 (def:1)	LCB3 (def:1)	LCB2 (def:1)	LCB1 (def:1)	LCB0 (def:1)	LCA7 (def:1)	LCA6 (def:1)	LCA5 (def:1)	LCA4 (def:1)	LCA3 (def:1)	LCA2 (def:1)	LCA1 (def:1)	LCA0 (def:1)	LCZ7 (def:1)	LCZ6 (def:1)	LCZ5 (def:1)	LCZ4 (def:1)	LCZ3 (def:1)	LCZ2 (def:1)	LCZ1 (def:1)	LCZ0 (def:1)	CRC
Holding Current / Wetting Current Level Selection Command (MSB) [Default: Wetting current =1mA (Holding current)]	MCR	0x47			MCB5 (def:0)	MCB4 (def:0)	MCB3 (def:0)	MCB2 (def:0)	MCB1 (def:0)	MCB0 (def:0)	MCA7 (def:0)	MCA6 (def:0)	MCA5 (def:0)	MCA4 (def:0)	MCA3 (def:0)	MCA2 (def:0)	MCA1 (def:0)	MCA0 (def:0)	MCZ7 (def:0)	MCZ6 (def:0)	MCZ5 (def:0)	MCZ4 (def:0)	MCZ3 (def:0)	MCZ2 (def:0)	MCZ1 (def:0)	MCZ0 (def:0)	CRC
Wetting Current Operation Control Command [Default: Invalid]	WTR	0x48			WTB5 (def:0)	WTB4 (def:0)	WTB3 (def:0)	WTB2 (def:0)	WTB1 (def:0)	WTB0 (def:0)	WTA7 (def:0)	WTA6 (def:0)	WTA5 (def:0)	WTA4 (def:0)	WTA3 (def:0)	WTA2 (def:0)	WTA1 (def:0)	WTA0 (def:0)	WTZ7 (def:0)	WTZ6 (def:0)	WTZ5 (def:0)	WTZ4 (def:0)	WTZ3 (def:0)	WTZ2 (def:0)	WTZ1 (def:0)	WTZ0 (def:0)	CRC
n-Times Matched Filter Activation Control Command [Default: Invalid]	DFR	0x49	DFB2 (def:0)	DFB1 (def:0)	DFB0 (def:0)	DFA2 (def:0)	DFA1 (def:0)	DFA0 (def:0)	DFZ2 (def:0)	DFZ1 (def:0)	DFZ0 (def:0)																CRC
DMUX Setting Command [Default: Invalid]	DMR	0x4A	DMX4 (def:0)	DMX3 (def:0)	DMX2 (def:0)	DMX1 (def:0)	DMX0 (def:0)																				CRC
Normal Mode Setting Command [Default: Full-time monitor,Strobe time:125us, Sequential monitor is invalid]	FMR	0x4B	FSQ (def:0)	FSQB (def:0)	FSQA (def:0)	FSQZ (def:0)	FITB2 (def:0)	FITB1 (def:0)	FITB0 (def:0)	FITA2 (def:0)	FITA1 (def:0)	FITA0 (def:0)	FITZ2 (def:0)	FITZ1 (def:0)	FITZ0 (def:0)	SVW1 (def:0)	SVW0 (def:1)	FITB3 (def:0)	FITA3 (def:0)	FITZ3 (def:0)							CRC
Sleep Mode Setting Command [Default: Monitor period:50ms,Sequential monitor is invalid]	SMR	0x4C	SSQ (def:0)	SSQB (def:0)	SSQA (def:0)	SSQZ (def:0)	SITB2 (def:1)	SITB1 (def:1)	SITB0 (def:1)	SITA2 (def:1)	SITA1 (def:1)	SITA0 (def:1)	SITZ2 (def:1)	SITZ1 (def:1)	SITZ0 (def:1)			SITB3 (def:0)	SITA3 (def:0)	SITZ3 (def:0)							CRC
Detection Edge Selection Command [Default: Both edges]	ISR	0x4D	ISB (def:1)	ISA (def:1)	ISZ (def:1)																						CRC
Automatic Mode Transition Command [Default: Automatic transition is valid]	MIR	0x4E	MR_ IER (def:1)																								CRC
Monitor Mode Ttransition Command [Default: Normal mode]	MDR	0x4F	MDC (def:0)																								CRC
Reset Command	RST	0x5F																									CRC
Interrupt Notification of Switch Change Setting Command Read	RIER	0x61																									CRC
Comparator Operation Control Command Read	RCMR	0x62																									CRC
Comparator Threshold Selection Command Read	RCTR	0x63																									CRC
INZ Current Source/Sink Selection Command Read	RPUDR	0x64																									CRC
Current Source Activation Command Read	RCER	0x65																									CRC
Holding Current / Wetting Current Level Selection Command (LSB) Read	RLCR	0x66																									CRC
Holding Current / Wetting Current Level Selection Command (MSB) Read	RMCR	0x67																									CRC
Wetting Current Operation Control Command Read	RWTR	0x68																									CRC
n-Times Matched Filter Activation Control Command Read	RDFR	0x69																									CRC
DMUX Setting Command Read	RDMR	0x6A																									CRC
Normal Mode Setting Command Read	RFMR	0x6B																									CRC
Sleep Mode Setting Command Read	RSMR	0x6C																									CRC
Detection Edge Selection Command Read	RISR	0x6D																									CRC
Automatic Mode Transition Command Read	RMIR	0x6E																									CRC
Monitor Mode Ttransition Command Read	RMDR	0x6F																									CRC
TEST Command [Default: Invalid]	TSR	0x79	TSS7 (def:0)	TSS6 (def:0)	TSS5 (def:0)	TSS4 (def:0)	TSS3 (def:0)	TSS2 (def:0)	TSS1 (def:0)	TSS0 (def:0)																	CRC

Table 37. Register Map (SO Bit Alignment)

Register Name	Symbol	-	Read Data Name																							CRC
		39:32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7:0
Interrupt Notification of Switch Change Setting Command Read	RIER	“100”, Interrupt Factor	0	0	IEB5 (def:1)	IEB4 (def:1)	IEB3 (def:1)	IEB2 (def:1)	IEB1 (def:1)	IEB0 (def:1)	IEA7 (def:1)	IEA6 (def:1)	IEA5 (def:1)	IEA4 (def:1)	IEA3 (def:1)	IEA2 (def:1)	IEA1 (def:1)	IEA0 (def:1)	IEZ7 (def:1)	IEZ6 (def:1)	IEZ5 (def:1)	IEZ4 (def:1)	IEZ3 (def:1)	IEZ2 (def:1)	IEZ1 (def:1)	IEZ0 (def:1)	CRC
Comparator Operation Control Command Read	RCMR	“100”, Interrupt Factor	0	0	CMB5 (def:1)	CMB4 (def:1)	CMB3 (def:1)	CMB2 (def:1)	CMB1 (def:1)	CMB0 (def:1)	CMA7 (def:1)	CMA6 (def:1)	CMA5 (def:1)	CMA4 (def:1)	CMA3 (def:1)	CMA2 (def:1)	CMA1 (def:1)	CMA0 (def:1)	CMZ7 (def:1)	CMZ6 (def:1)	CMZ5 (def:1)	CMZ4 (def:1)	CMZ3 (def:1)	CMZ2 (def:1)	CMZ1 (def:1)	CMZ0 (def:1)	CRC
Comparator Threshold Selection Command Read	RCTR	“100”, Interrupt Factor	CTB (def:0)	CTA (def:0)	CTZ (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
INZ Current Source/Sink Selection Command Read	RPUDR	“100”, Interrupt Factor	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUD7 (def:0)	PUD6 (def:0)	PUD5 (def:0)	PUD4 (def:0)	PUD3 (def:0)	PUD2 (def:0)	PUD1 (def:0)	PUD0 (def:0)	CRC
Wetting Current Operation Control Command Read	RCER	“100”, Interrupt Factor	CEB (def:0)	CEA (def:0)	CEZ (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Holding Current / Wetting Current Level Selection Command (LSB) Read	RLCR	“100”, Interrupt Factor	CRH1 (def:0)	CRH0 (def:0)	LCB5 (def:1)	LCB4 (def:1)	LCB3 (def:1)	LCB2 (def:1)	LCB1 (def:1)	LCB0 (def:1)	LCA7 (def:1)	LCA6 (def:1)	LCA5 (def:1)	LCA4 (def:1)	LCA3 (def:1)	LCA2 (def:1)	LCA1 (def:1)	LCA0 (def:1)	LCZ7 (def:1)	LCZ6 (def:1)	LCZ5 (def:1)	LCZ4 (def:1)	LCZ3 (def:1)	LCZ2 (def:1)	LCZ1 (def:1)	LCZ0 (def:1)	CRC
Holding Current / Wetting Current Level Selection Command (MSB) Read	RMCR	“100”, Interrupt Factor	0	0	MCB5 (def:0)	MCB4 (def:0)	MCB3 (def:0)	MCB2 (def:0)	MCB1 (def:0)	MCB0 (def:0)	MCA7 (def:0)	MCA6 (def:0)	MCA5 (def:0)	MCA4 (def:0)	MCA3 (def:0)	MCA2 (def:0)	MCA1 (def:0)	MCA0 (def:0)	MCZ7 (def:0)	MCZ6 (def:0)	MCZ5 (def:0)	MCZ4 (def:0)	MCZ3 (def:0)	MCZ2 (def:0)	MCZ1 (def:0)	MCZ0 (def:0)	CRC
Wetting Current Operation Control Command Read	RWTR	“100”, Interrupt Factor	0	0	WTB5 (def:0)	WTB4 (def:0)	WTB3 (def:0)	WTB2 (def:0)	WTB1 (def:0)	WTB0 (def:0)	WTA7 (def:0)	WTA6 (def:0)	WTA5 (def:0)	WTA4 (def:0)	WTA3 (def:0)	WTA2 (def:0)	WTA1 (def:0)	WTA0 (def:0)	WTZ7 (def:0)	WTZ6 (def:0)	WTZ5 (def:0)	WTZ4 (def:0)	WTZ3 (def:0)	WTZ2 (def:0)	WTZ1 (def:0)	WTZ0 (def:0)	CRC
n-Times Matched Filter Activation Control Command Read	RDFR	“100”, Interrupt Factor	DFB2 (def:0)	DFB1 (def:0)	DFB0 (def:0)	DFA2 (def:0)	DFA1 (def:0)	DFA0 (def:0)	DFZ2 (def:0)	DFZ1 (def:0)	DFZ0 (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
DMUX Setting Command Read	RDMR	“100”, Interrupt Factor	DMX4 (def:0)	DMX3 (def:0)	DMX2 (def:0)	DMX1 (def:0)	DMX0 (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Normal Mode Setting Command Read	RFMR	“100”, Interrupt Factor	FSQ (def:0)	FSQB (def:0)	FSQA (def:0)	FSQZ (def:0)	FITB2 (def:0)	FITB1 (def:0)	FITB0 (def:0)	FITA2 (def:0)	FITA1 (def:0)	FITA0 (def:0)	FITZ2 (def:0)	FITZ1 (def:0)	FITZ0 (def:0)	SVW1 (def:0)	SVW0 (def:1)	FITB3 (def:0)	FITA3 (def:0)	FITZ3 (def:0)	0	0	0	0	0	0	CRC
Sleep Mode Setting Command Read	RSMR	“100”, Interrupt Factor	SSQ (def:0)	SSQB (def:0)	SSQA (def:0)	SSQZ (def:0)	SITB2 (def:1)	SITB1 (def:1)	SITB0 (def:1)	SITA2 (def:1)	SITA1 (def:1)	SITA0 (def:1)	SITZ2 (def:1)	SITZ1 (def:1)	SITZ0 (def:1)	0	0	SITB3 (def:0)	SITA3 (def:0)	SITZ3 (def:0)	0	0	0	0	0	0	CRC
Detection Edge Selection Command Read	RISR	“100”, Interrupt Factor	ISB (def:1)	ISA (def:1)	ISZ (def:1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Automatic Mode Transition Command Read	RMIR	“100”, Interrupt Factor	MR_ IER (def:1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Monitor Mode Ttransition Command Read	RMDR	“100”, Interrupt Factor	MDC (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC

Typical Performance Curves

Unless otherwise specified, VPUA=VPUB=13V, VDDI=5V, LVDD=AVDD=REF5
Series products (BD3375MUV-M/BD3375KV-C) use the same data.

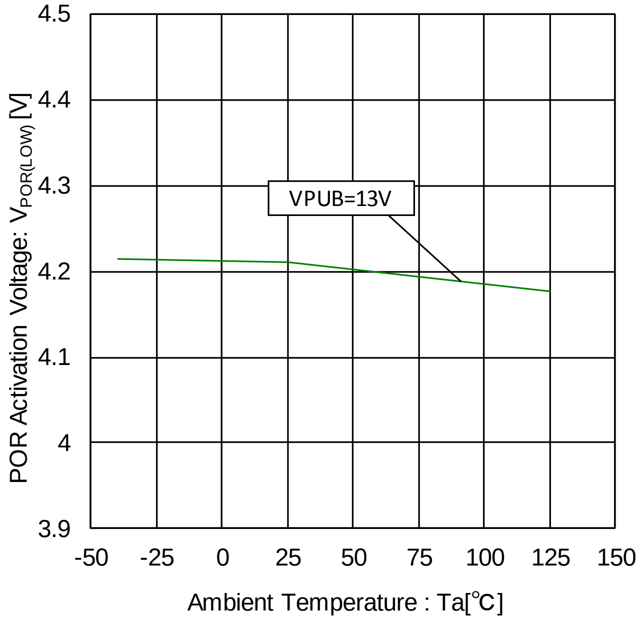


Figure 21. POR (Power on Reset) Activation Voltage - Temperature Characteristic

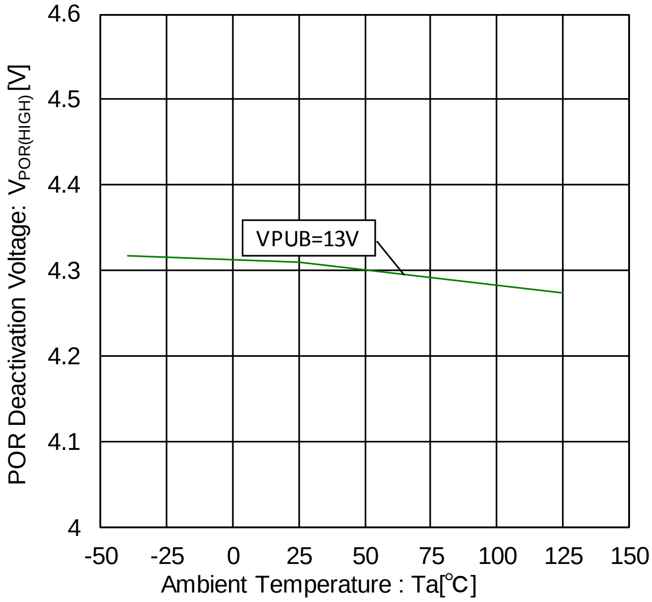


Figure 22. POR (Power on Reset) Deactivation Voltage -Temperature Characteristic

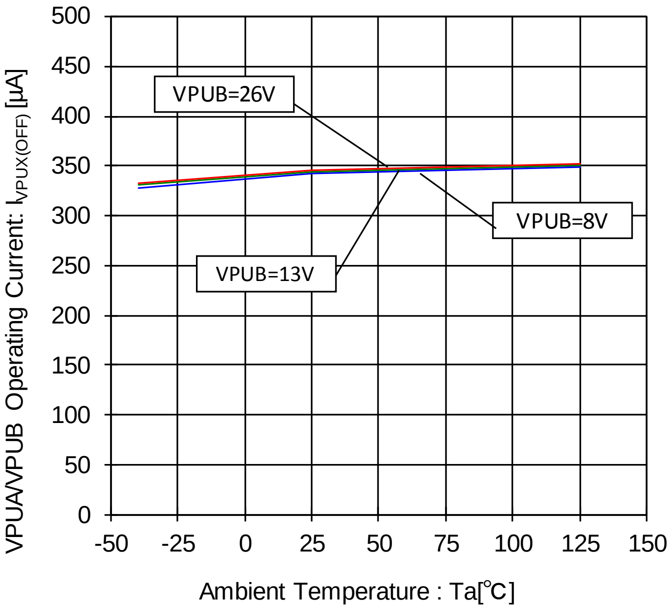


Figure 23. VPUA/VPUB Operating Current - Temperature Characteristic (Continuous monitor setting, Current source is invalid, "Hi-Z" Status)

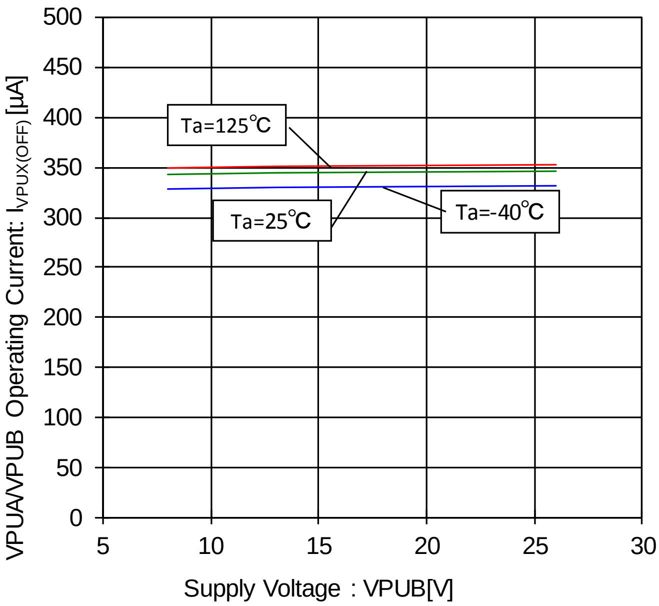


Figure 24. VPUA/VPUB Operating Current - Voltage Characteristic (Continuous monitor setting, Current source is invalid, "Hi-Z" Status)

Typical Performance Curves - continued

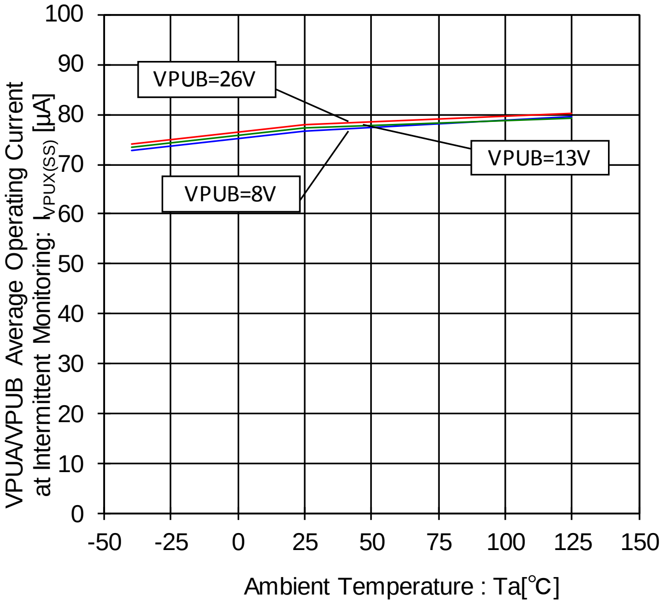


Figure 25. VPUA/VPUB Average Operating Current at Intermittent Monitoring - Temperature Characteristic (Monitoring Period: 50ms, Strobe Time: 125µs, Source/Sink Current Setting: 1mA)

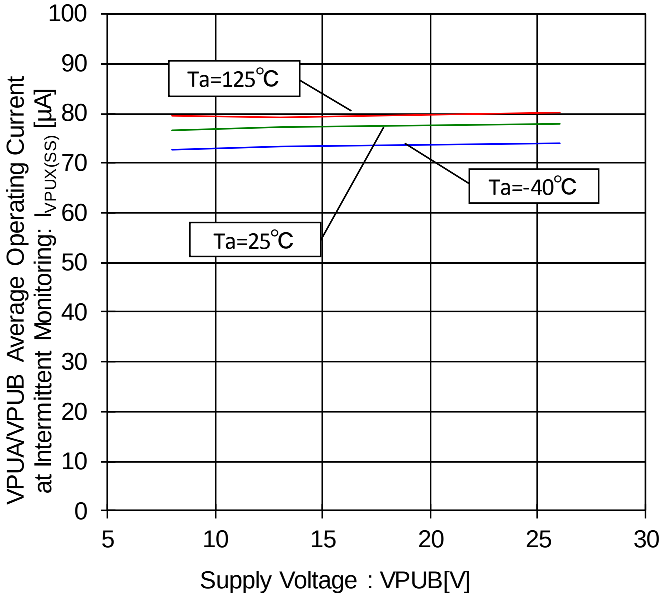


Figure 26. VPUA/VPUB Average Operating Current at Intermittent Monitoring - Voltage Characteristic (Monitoring Period: 50ms, Strobe Time: 125µs, Source/Sink Current Setting: 1mA)

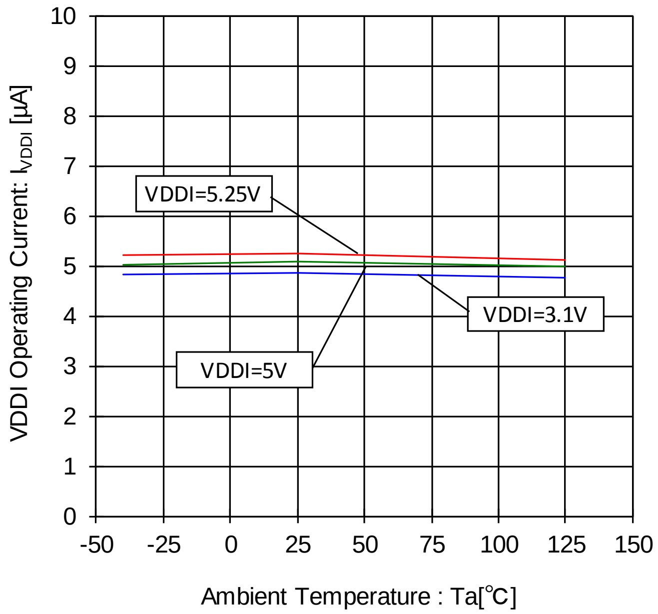


Figure 27. VDDI Operating Current- Temperature Characteristic (INTB="H", CSB="H")

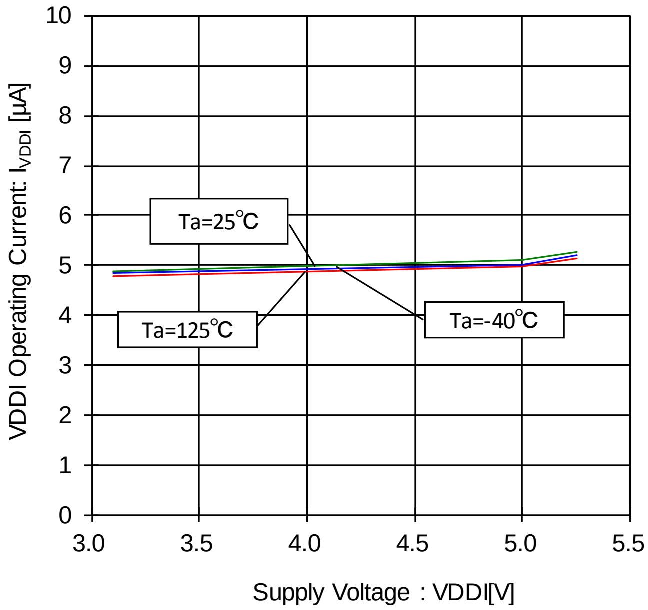


Figure 28. VDDI Operating Current- Voltage Characteristic (INTB="H", CSB="H")

Typical Performance Curves - continued

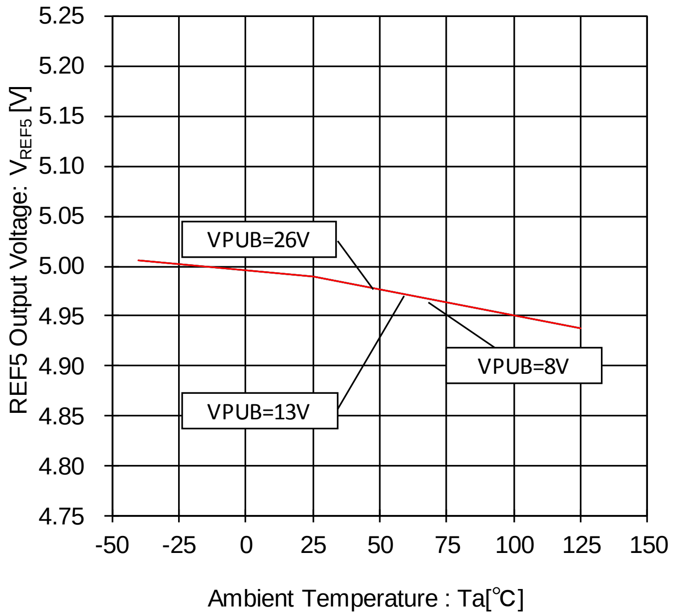


Figure 29. REF5 Output Voltage- Temperature Characteristic

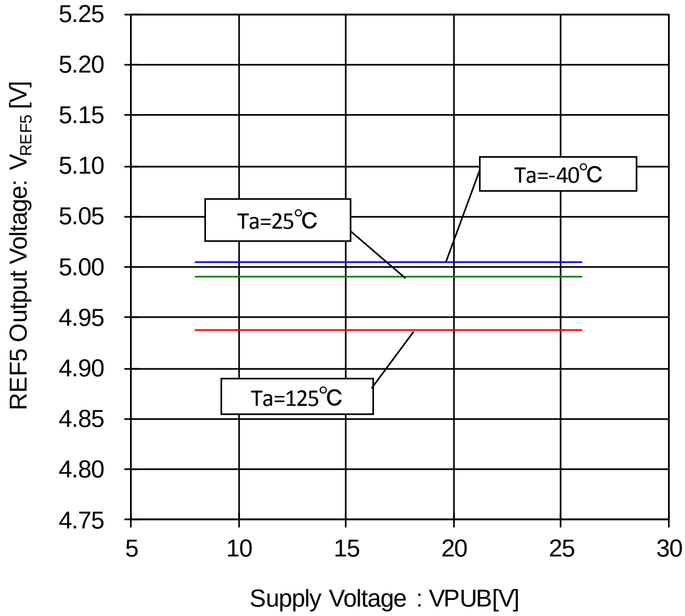


Figure 30. REF5 Output Voltage- Voltage Characteristic

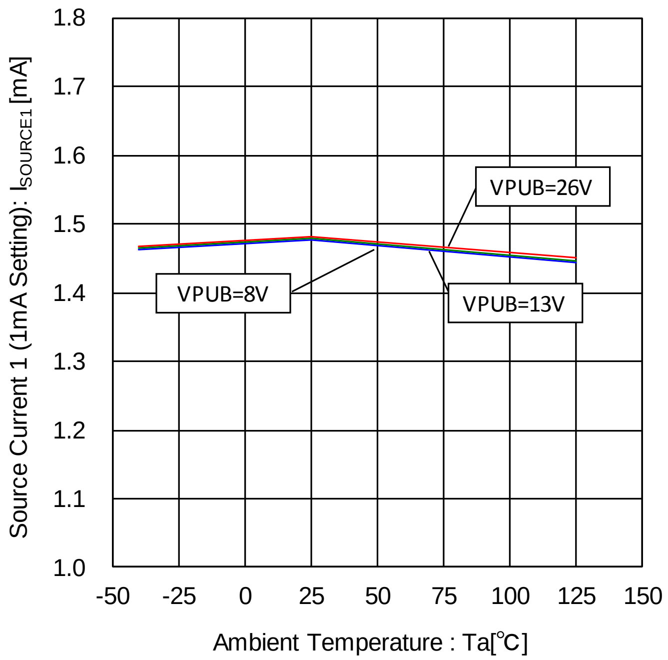


Figure 31. Source Current 1- Temperature Characteristic (1mA Setting, 0V external supply)

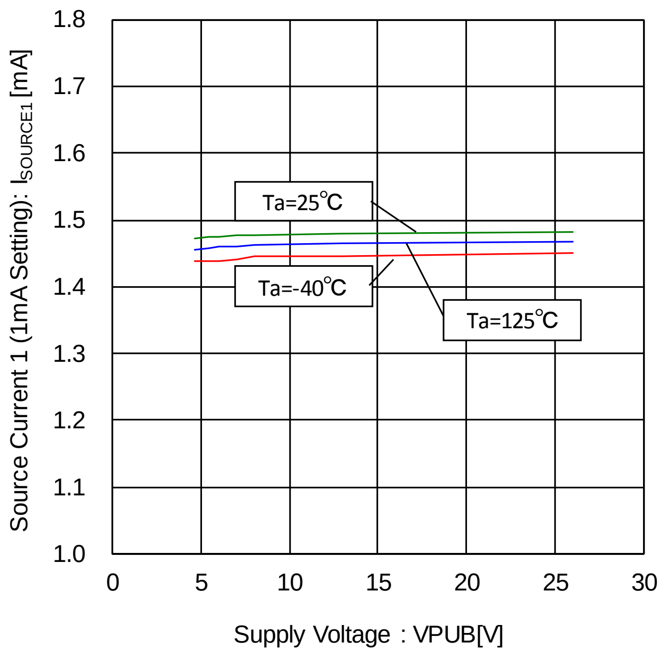


Figure 32. Source Current 1- Voltage Characteristic (1mA Setting, 0V external supply)

Typical Performance Curves - continued

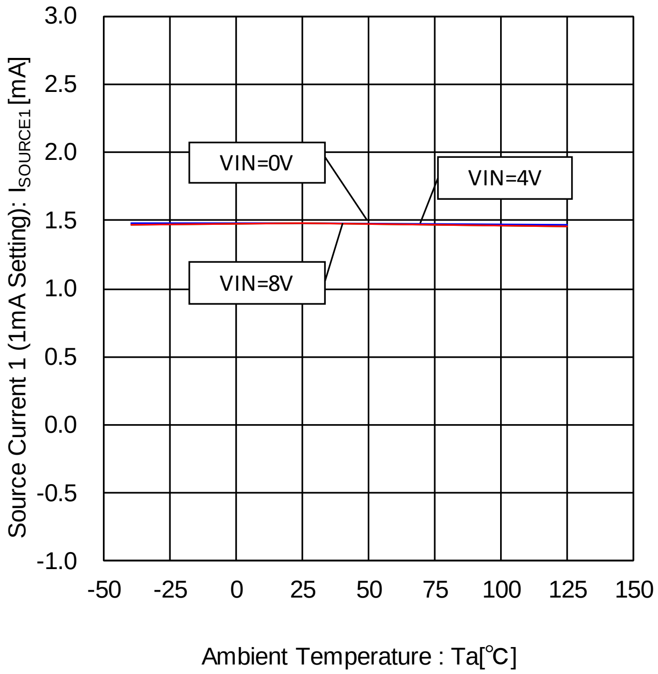


Figure 33. Source Current 1- Temperature Characteristic (1mA Setting)

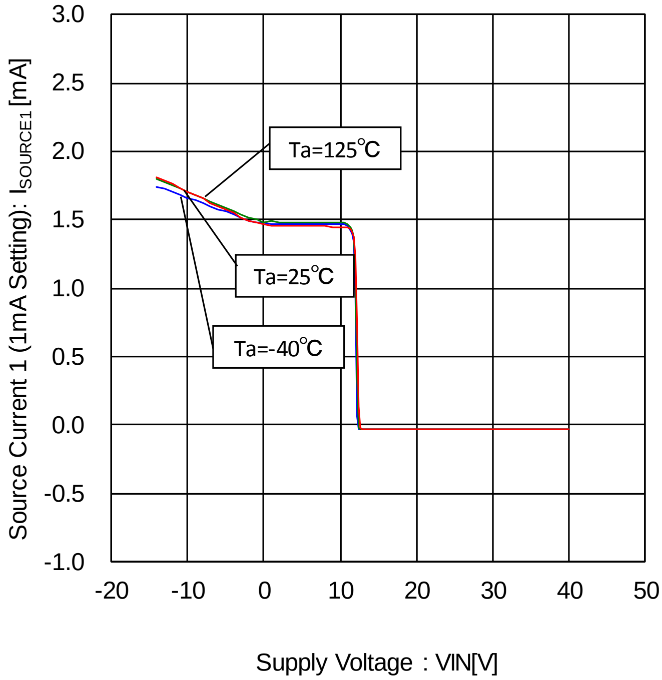


Figure 34. Source Current 1- Voltage Characteristic (1mA Setting)

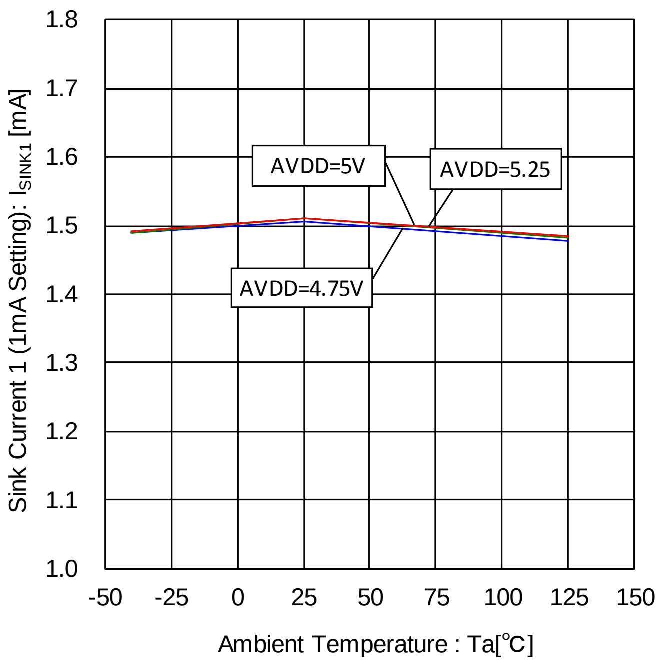


Figure 35. Sink Current 1- Temperature Characteristic (1mA Setting, 8V external supply)

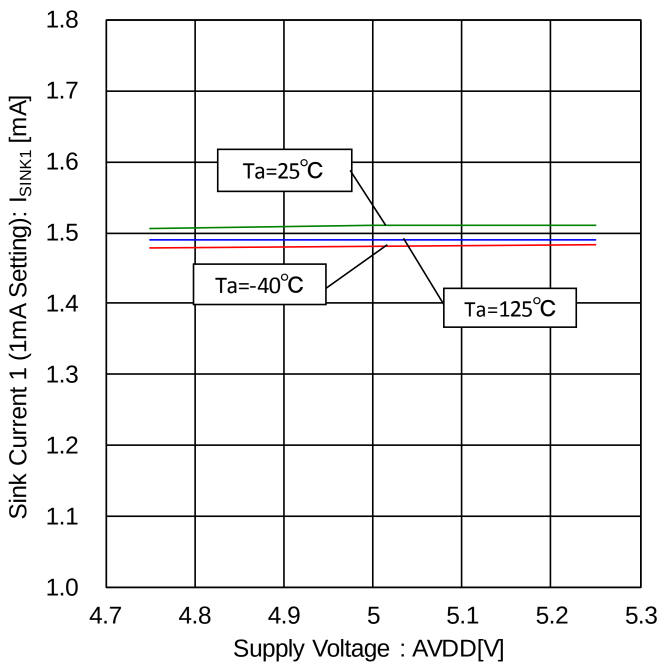


Figure 36. Sink Current 1- Voltage Characteristic (1mA Setting, 8V external supply)

Typical Performance Curves - continued

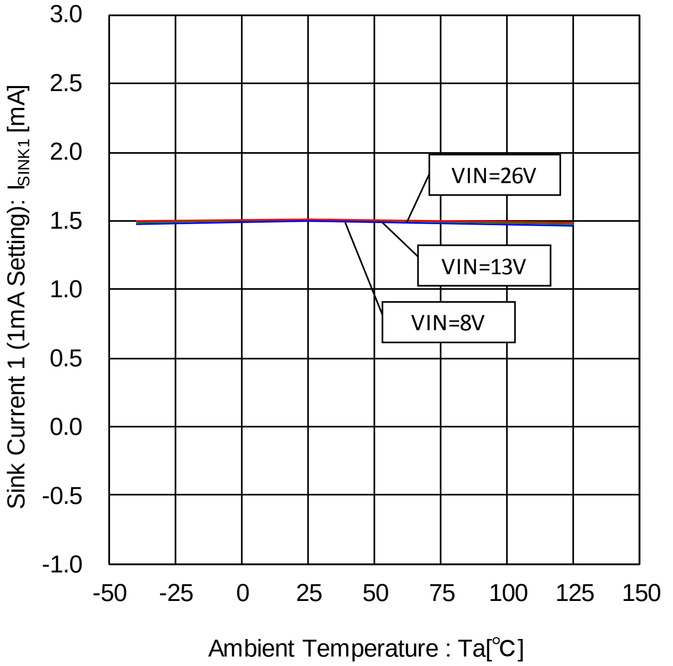


Figure 37. Sink Current 1- Temperature Characteristic (1mA Setting)

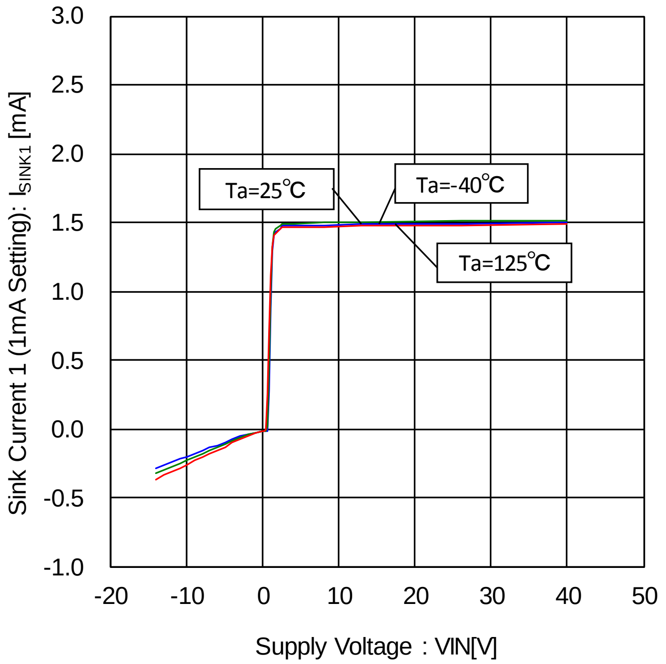


Figure 38. Sink Current 1- Voltage Characteristic (1mA Setting)

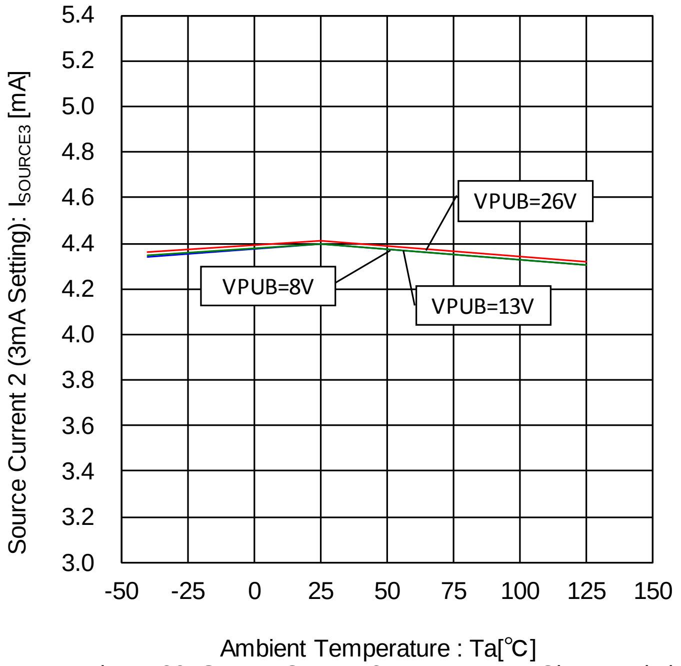


Figure 39. Source Current 2- Temperature Characteristic (3mA Setting, 0V external supply)

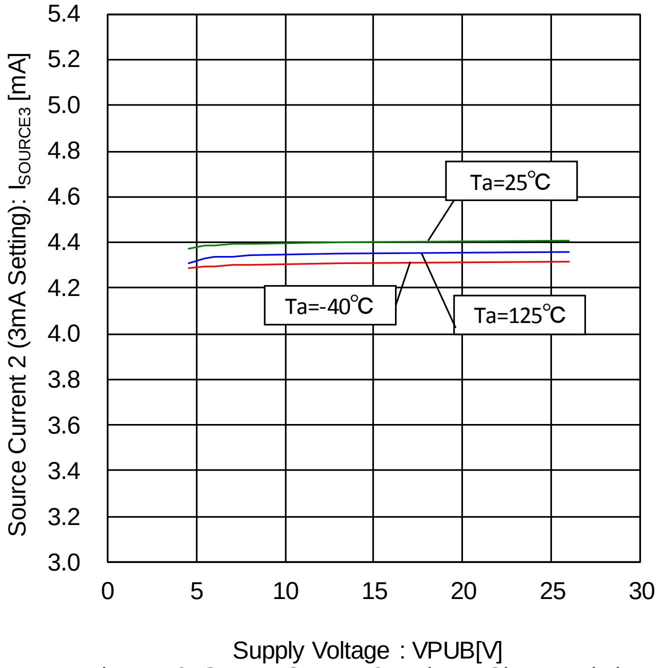


Figure 40. Source Current 2- Voltage Characteristic (3mA Setting, 0V external supply)

Typical Performance Curves - continued

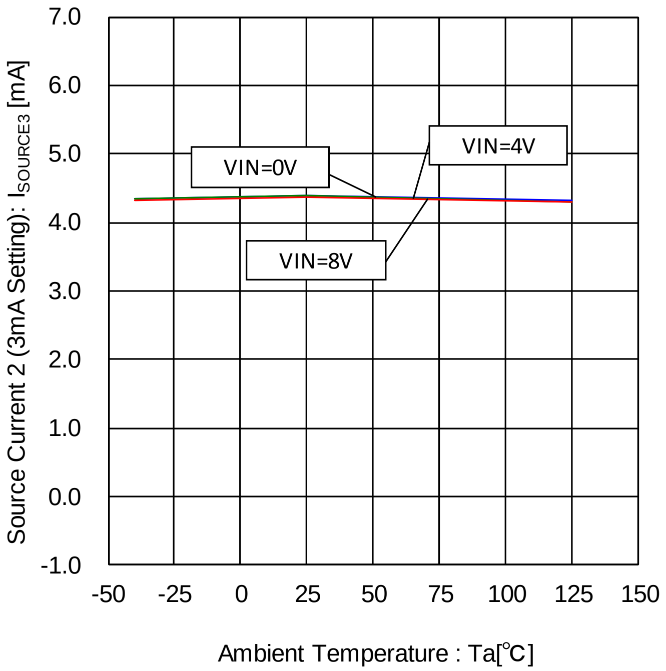


Figure 41. Source Current 2- Temperature Characteristic (3mA Setting)

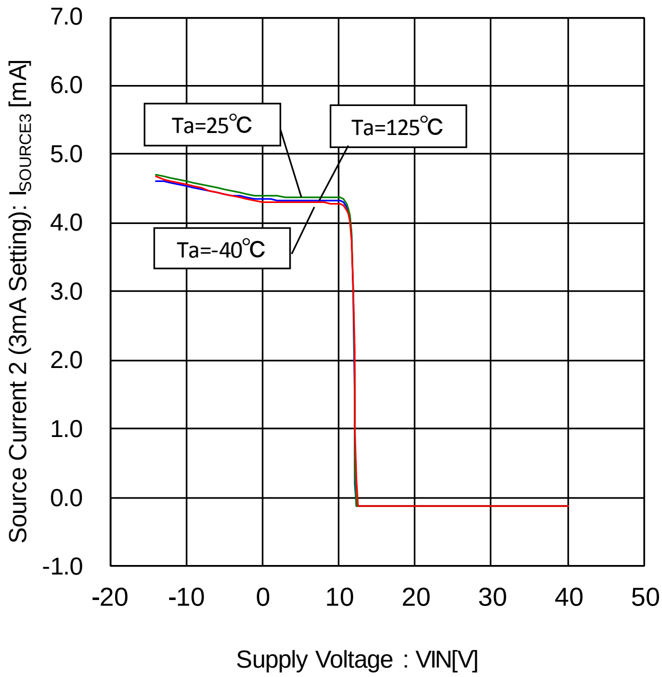


Figure 42. Source Current 2- Voltage Characteristic (3mA Setting)

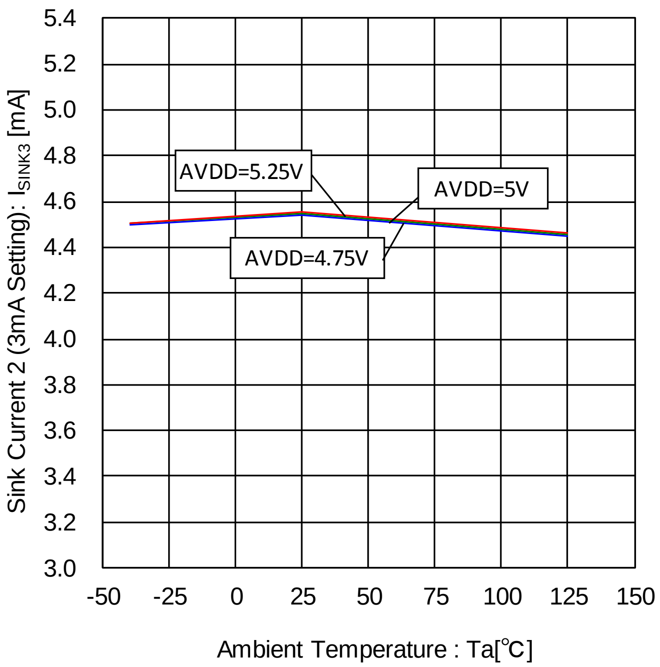


Figure 43. Sink Current 2- Temperature Characteristic (3mA Setting, 8V external supply)

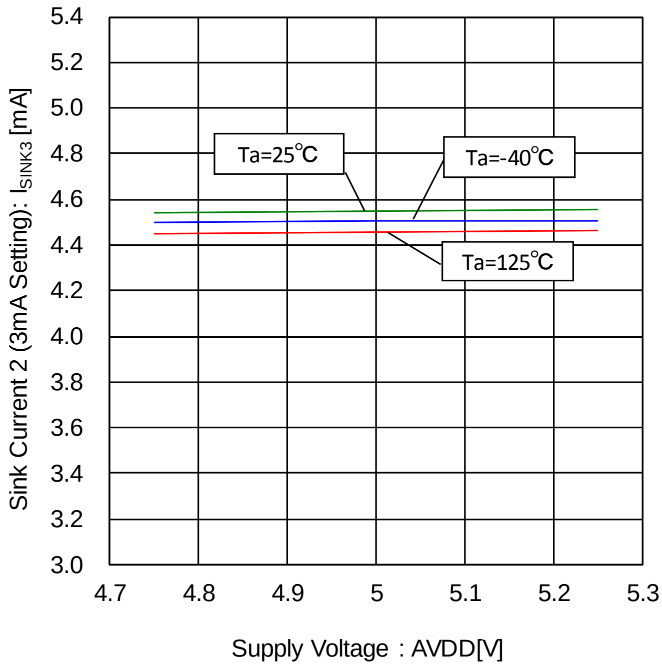


Figure 44. Sink Current 2- Voltage Characteristic (3mA Setting, 8V external supply)

Typical Performance Curves - continued

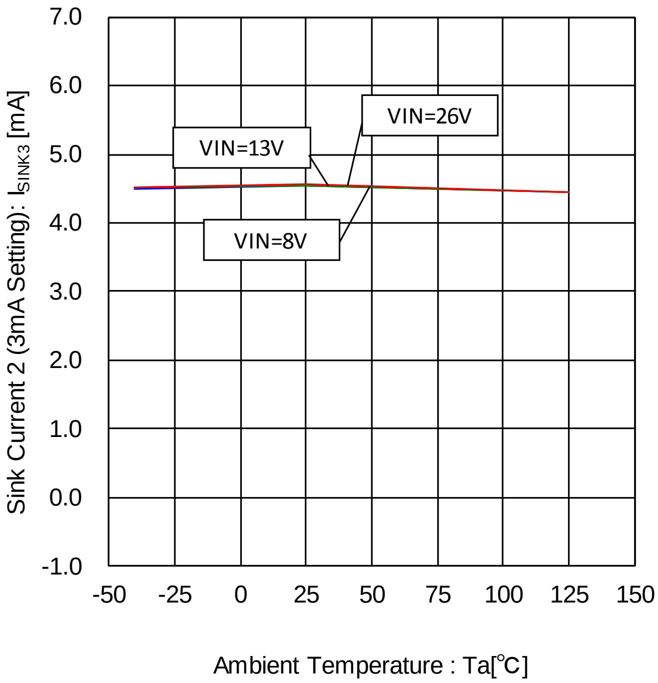


Figure 45. Sink Current 2- Temperature Characteristic (3mA Setting)

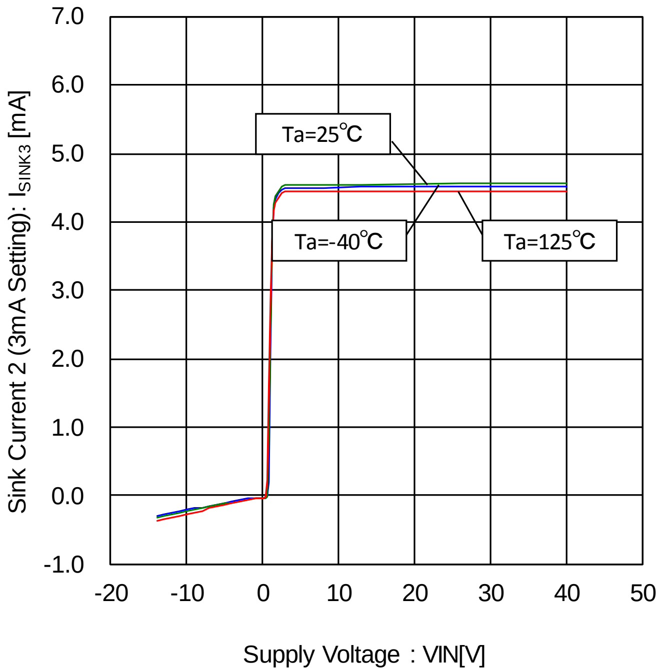


Figure 46. Sink Current 2- Voltage Characteristic (3mA Setting)

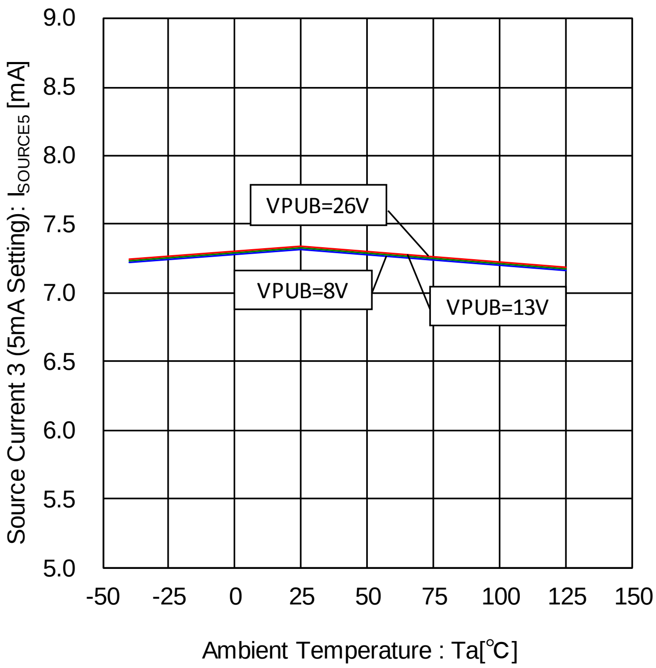


Figure 47. Source Current 3- Temperature Characteristic (5mA Setting, 0V external supply)

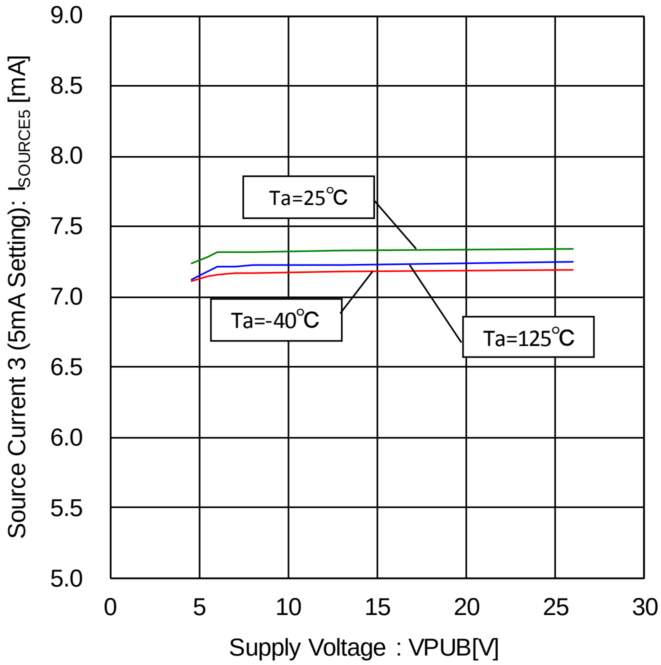


Figure 48. Source Current 3- Voltage Characteristic (5mA Setting, 0V external supply)

Typical Performance Curves - continued

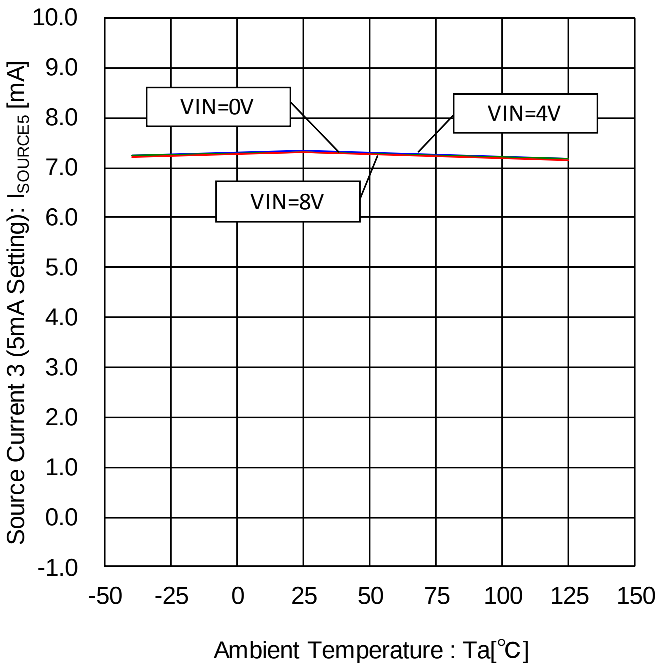


Figure 49. Source Current 3- Temperature Characteristic (5mA Setting)

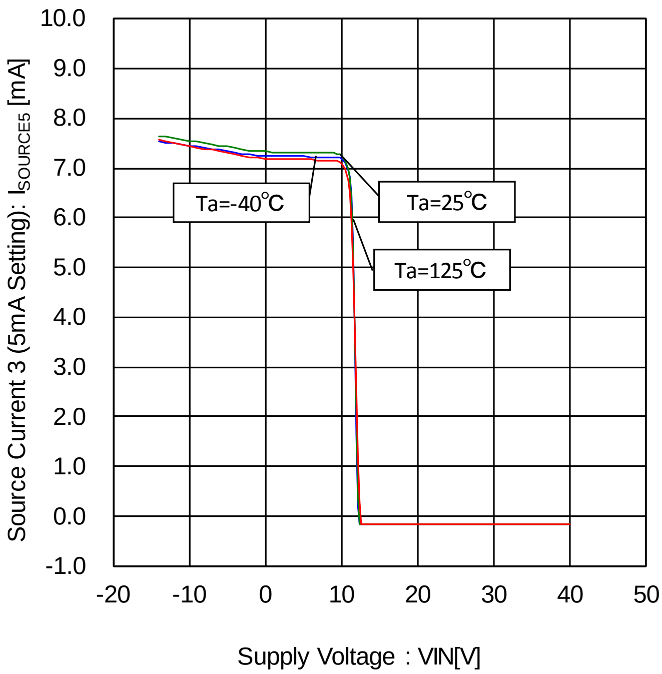


Figure 50. Source Current 3- Voltage Characteristic (5mA Setting)

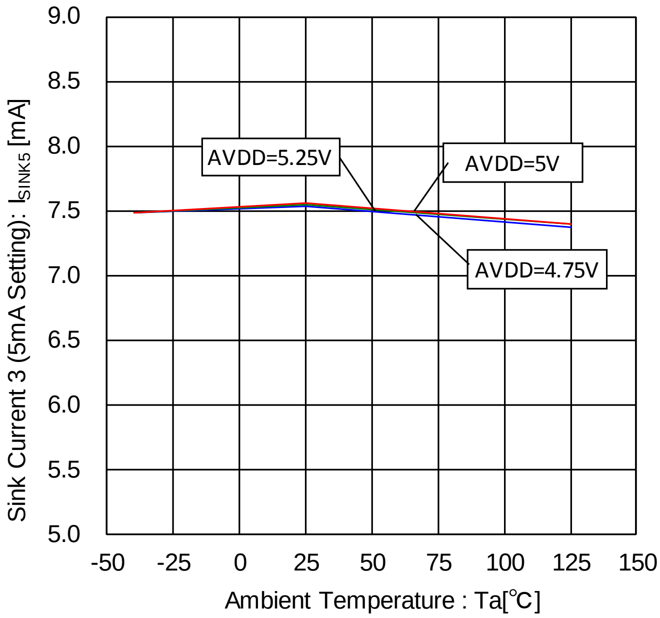


Figure 51. Sink Current 3- Temperature Characteristic (5mA Setting, 8V external supply)

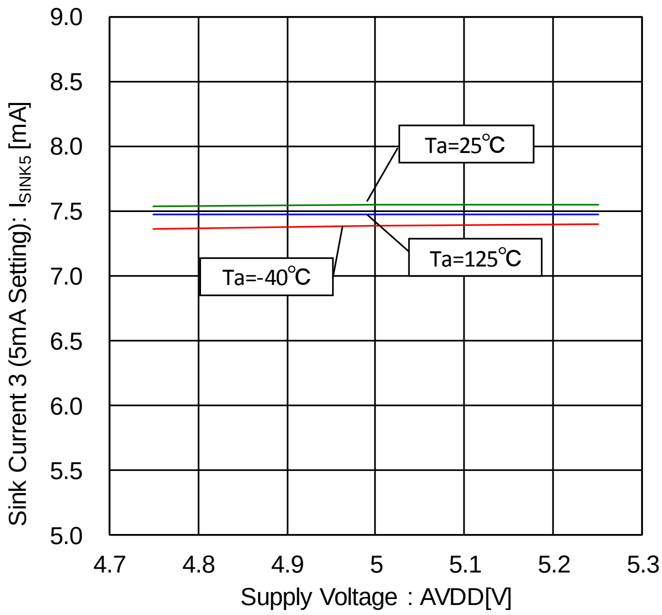


Figure 52. Sink Current 3- Voltage Characteristic (5mA Setting, 8V external supply)

Typical Performance Curves - continued

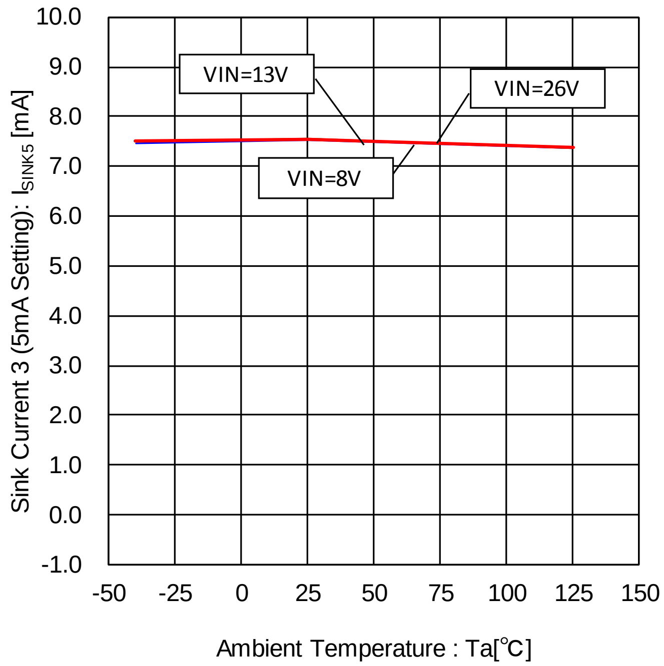


Figure 53. Sink Current 3- Temperature Characteristic (5mA Setting)

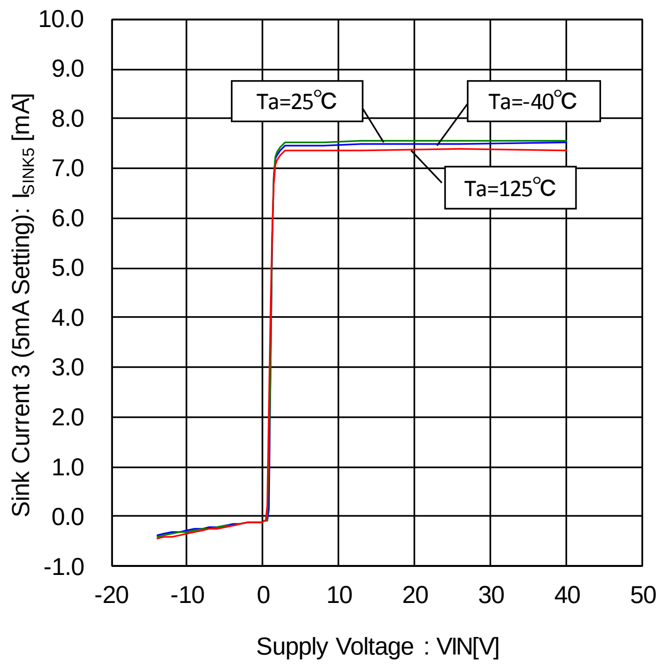


Figure 54. Sink Current 3- Voltage Characteristic (5mA Setting)

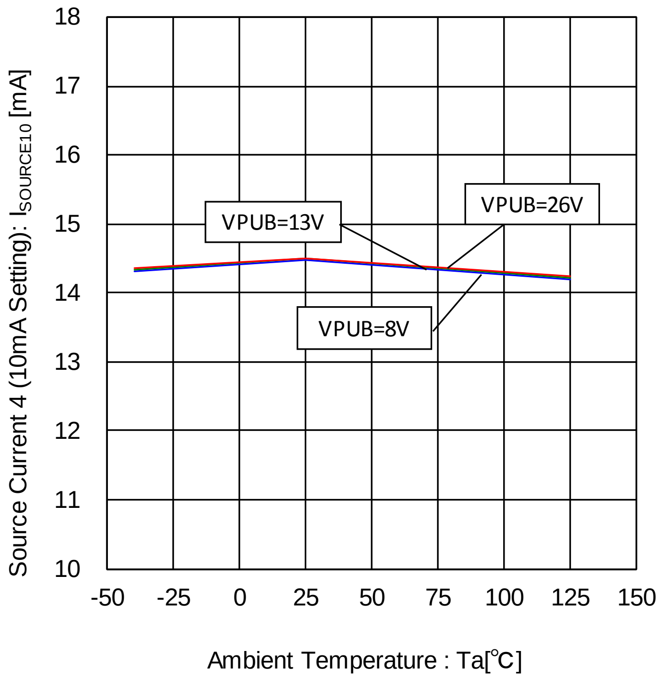


Figure 55. Source Current 4- Temperature Characteristic (10mA Setting, 0V external supply)

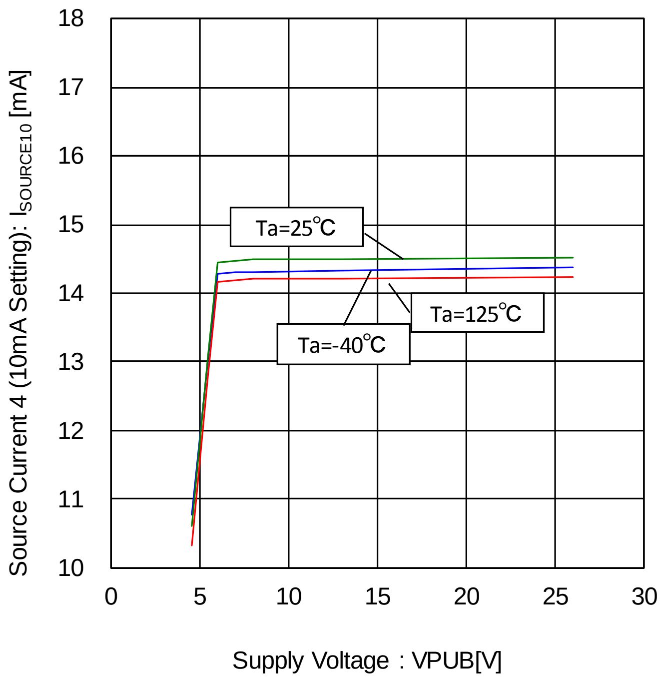


Figure 56. Source Current 4- Voltage Characteristic (10mA Setting, 0V external supply)

Typical Performance Curves - continued

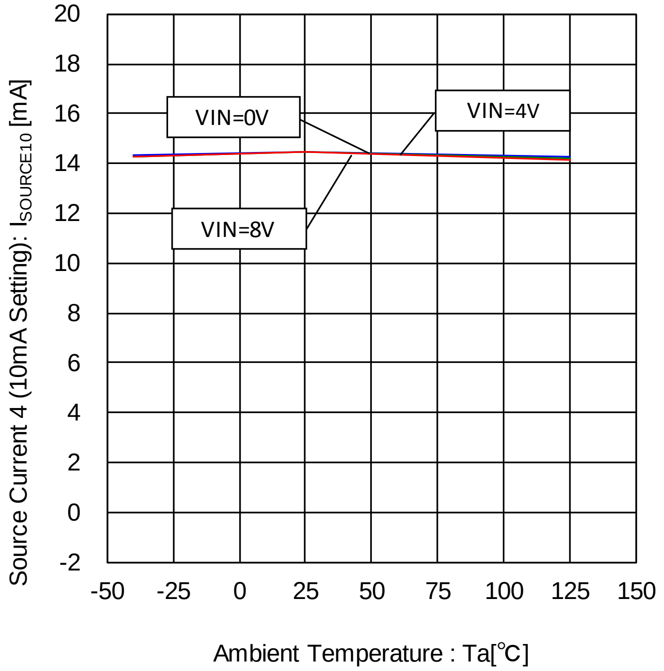


Figure 57. Source Current 4- Temperature Characteristic (10mA Setting)

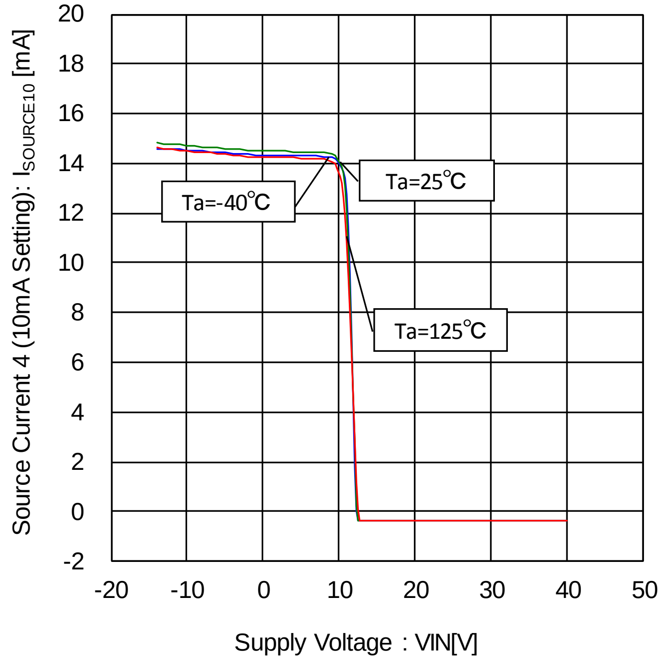


Figure 58. Source Current 4- Voltage Characteristic (10mA Setting)

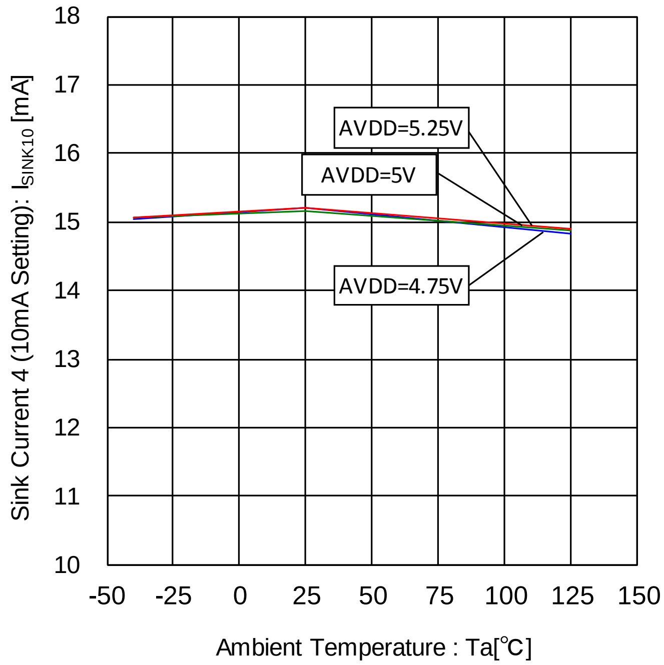


Figure 59. Sink Current 4- Temperature Characteristic (10mA Setting, 8V external supply)

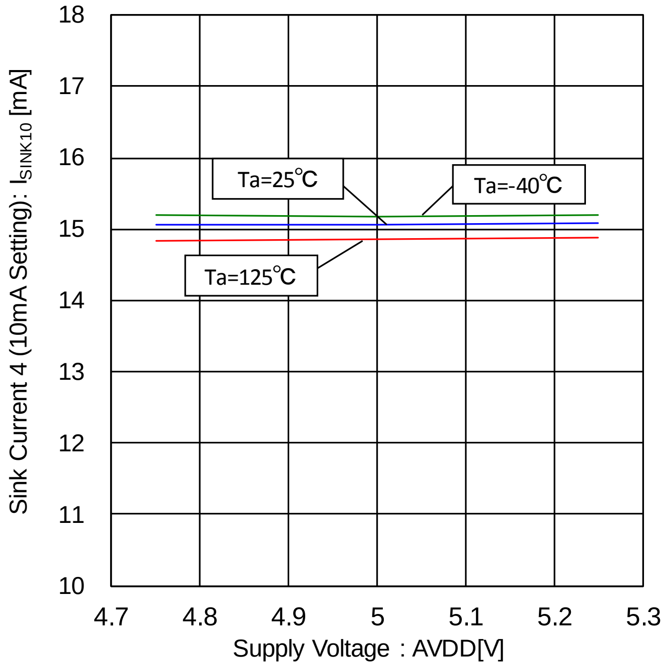


Figure 60. Sink Current 4- Voltage Characteristic (10mA Setting, 8V external supply)

Typical Performance Curves - continued

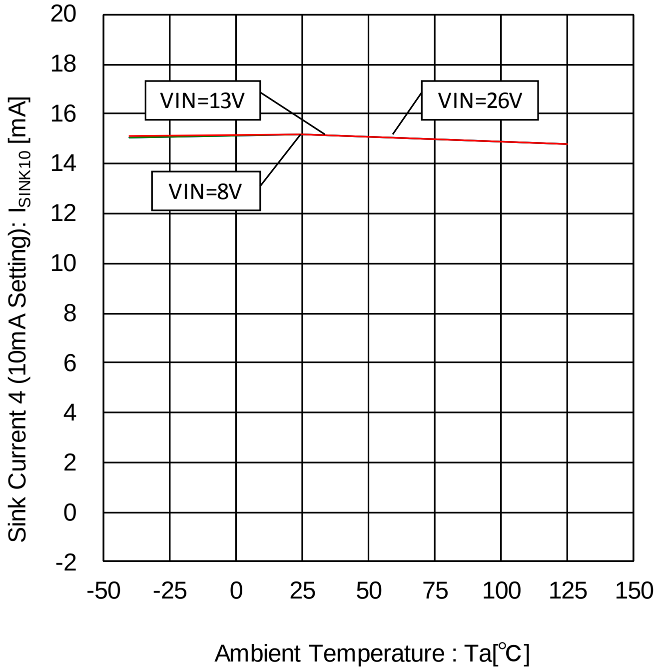


Figure 61. Sink Current 4- Temperature Characteristic (10mA Setting)

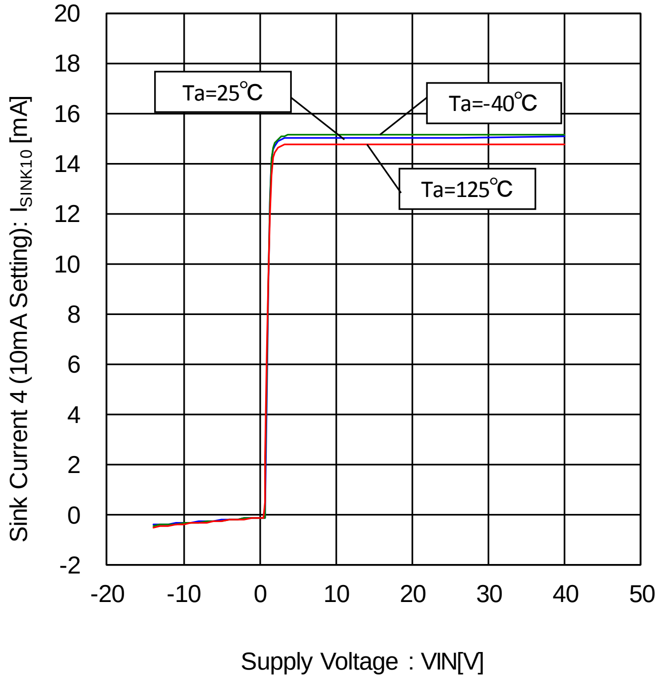


Figure 62. Sink Current 4- Voltage Characteristic (10mA Setting)

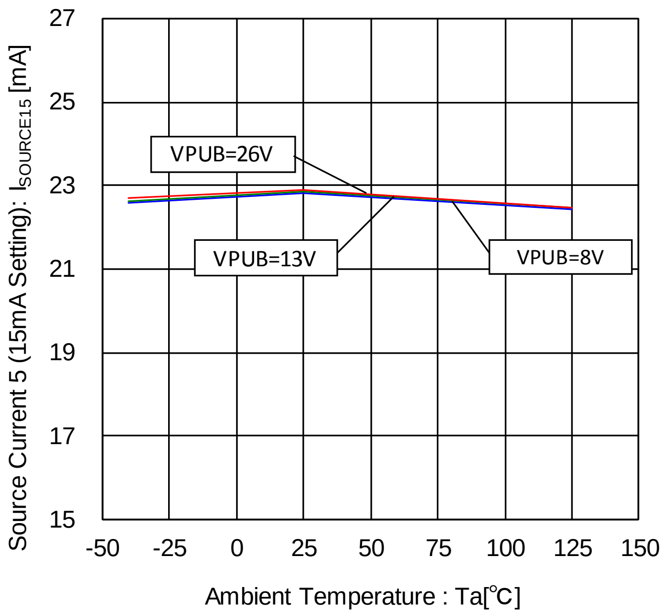


Figure 63. Source Current 5- Temperature Characteristic (15mA Setting, 0V external supply)

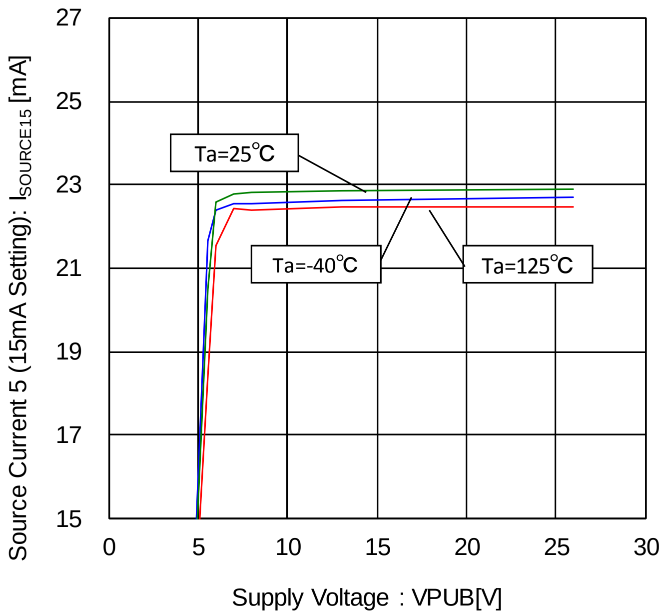


Figure 64. Source Current 5- Voltage Characteristic (15mA Setting, 0V external supply)

Typical Performance Curves - continued

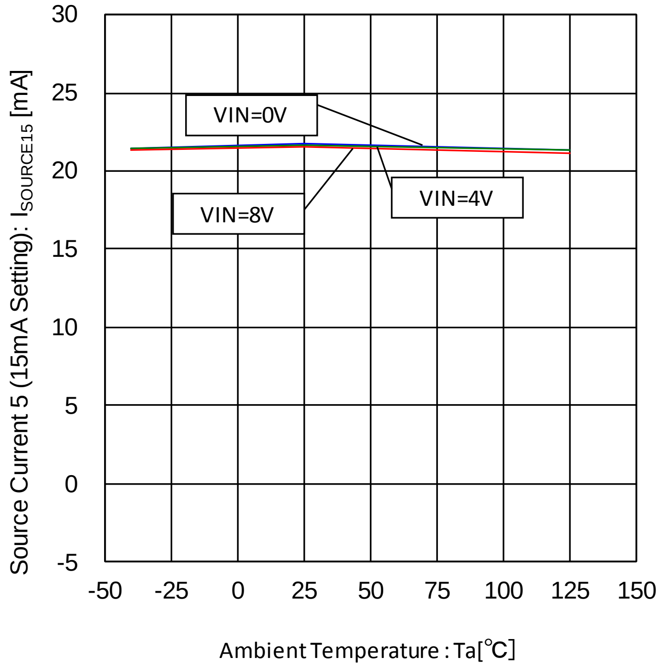


Figure 65. Source Current 5- Temperature Characteristic (15mA Setting)

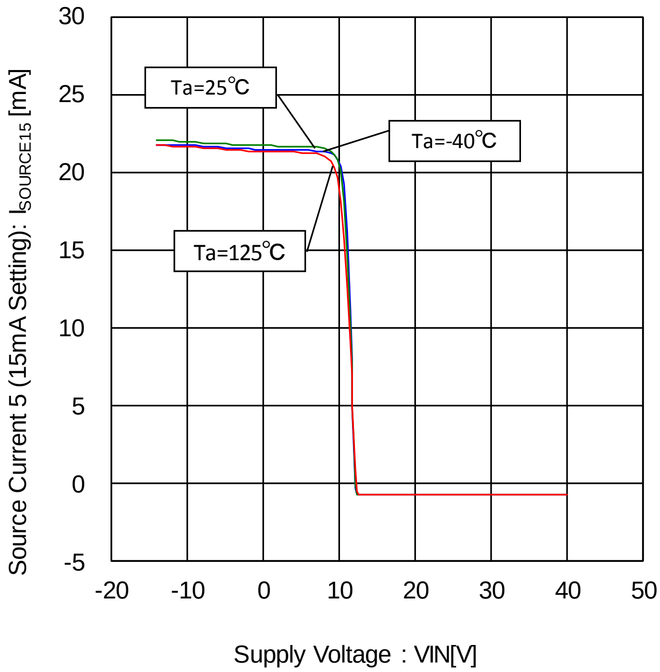


Figure 66. Source Current 5- Voltage Characteristic (15mA Setting)

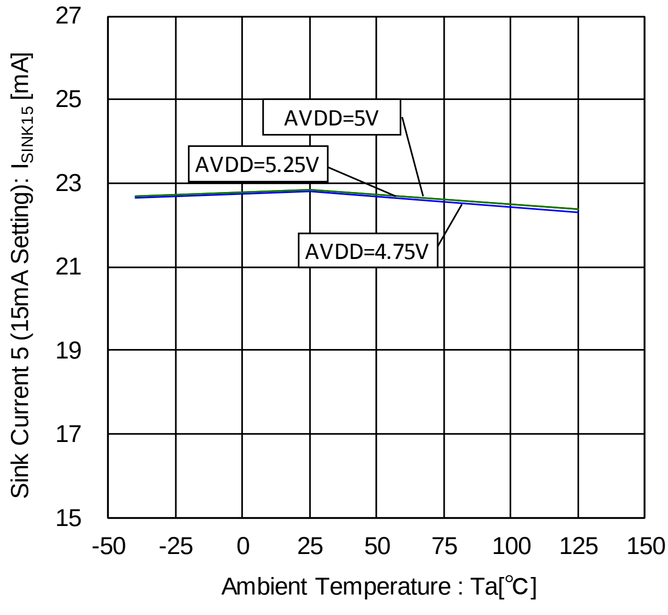


Figure 67. Sink Current 5- Temperature Characteristic (15mA Setting, 8V external supply)

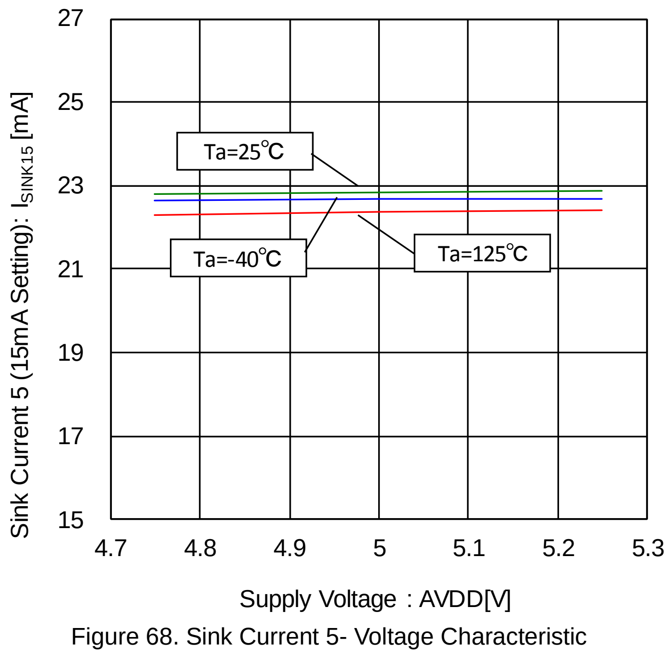


Figure 68. Sink Current 5- Voltage Characteristic (15mA Setting, 8V external supply)

Typical Performance Curves - continued

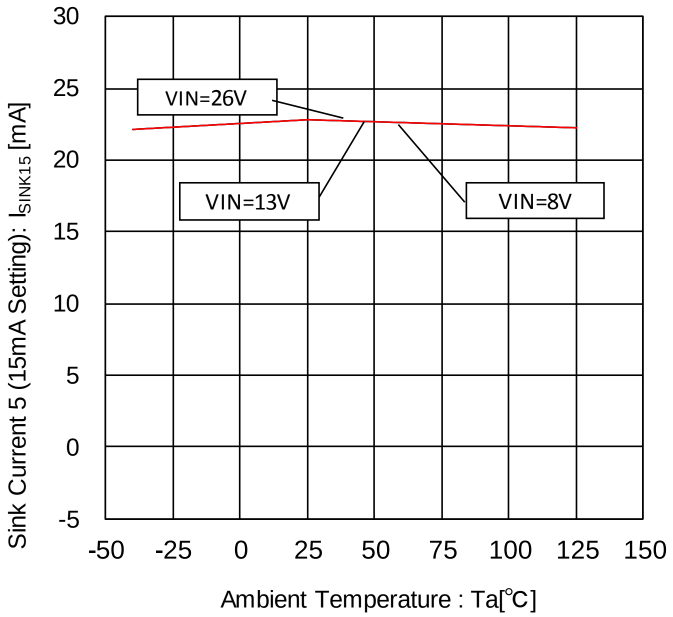


Figure 69. Sink Current 5- Temperature Characteristic (15mA Setting)

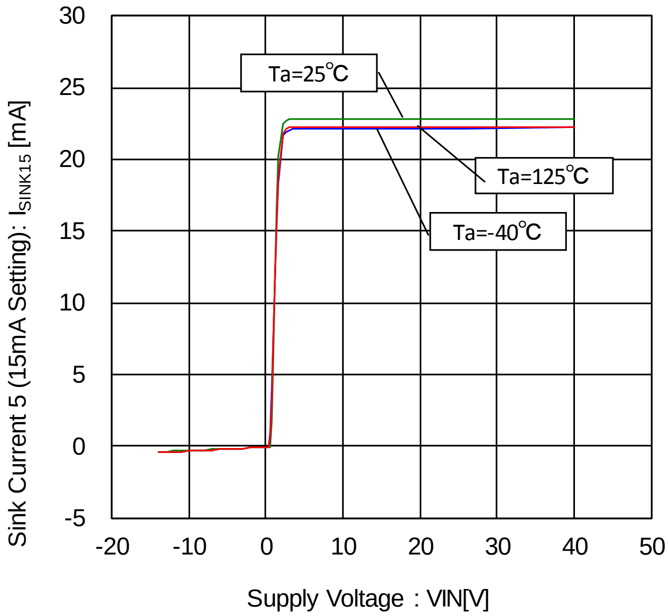


Figure 70. Sink Current 5- Voltage Characteristic (15mA Setting)

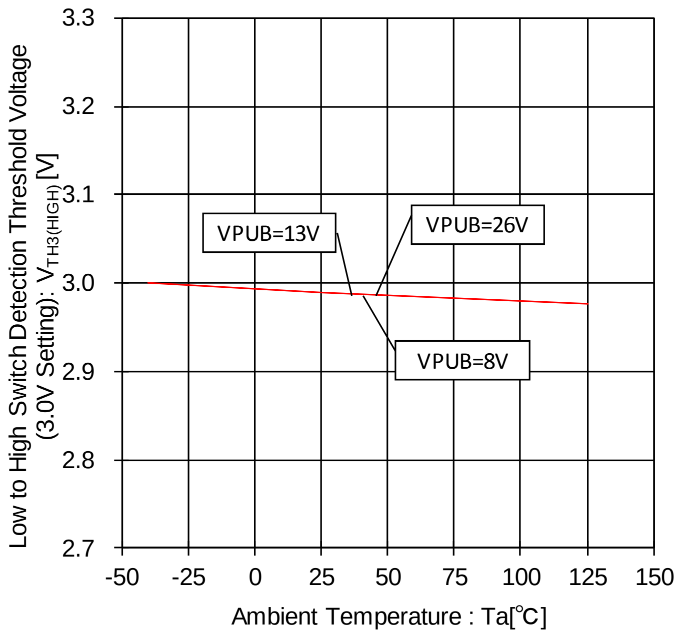


Figure 71. Low to High Switch Detection Threshold Voltage - Temperature Characteristic (3.0V Setting)

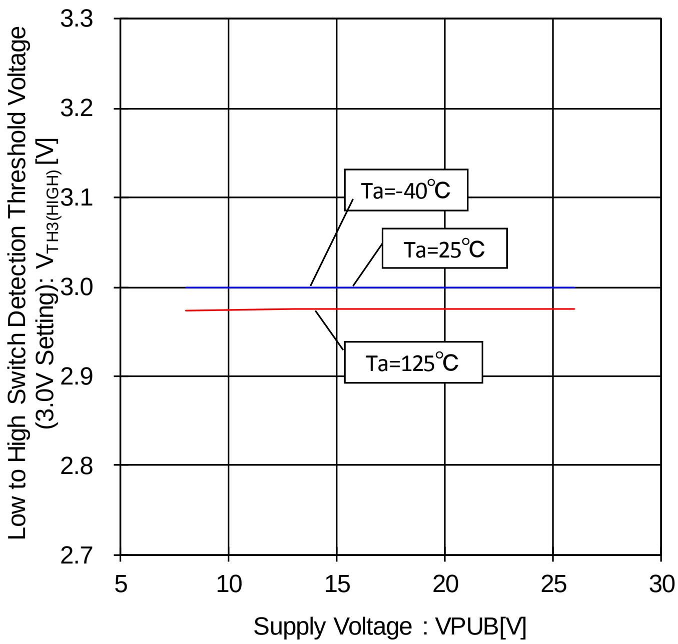


Figure 72. Low to High Switch Detection Threshold Voltage - Voltage Characteristic (3.0V Setting)

Typical Performance Curves - continued

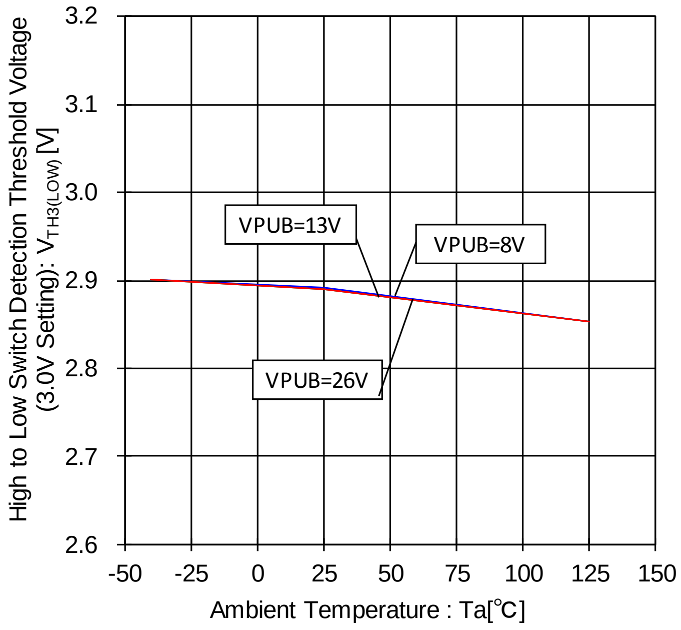


Figure 73. High to Low Switch Detection Threshold Voltage - Temperature Characteristic (3.0V Setting)

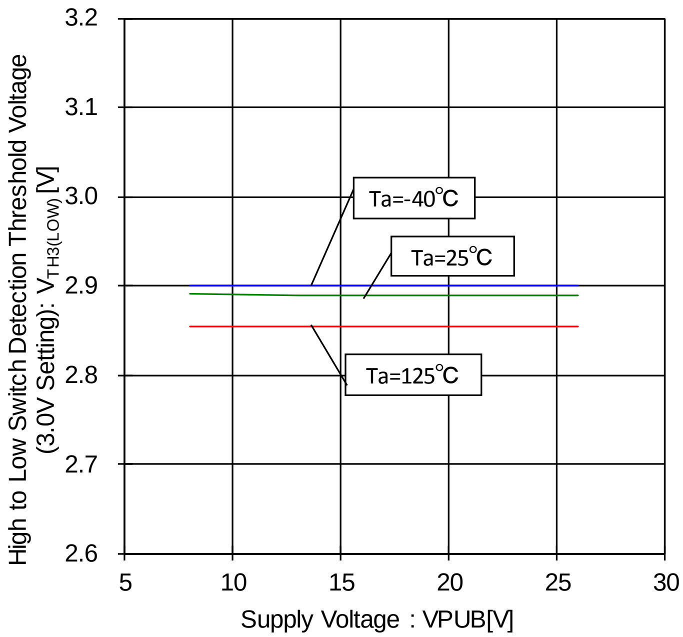


Figure 74. High to Low Switch Detection Threshold Voltage - Voltage Characteristic (3.0V Setting)

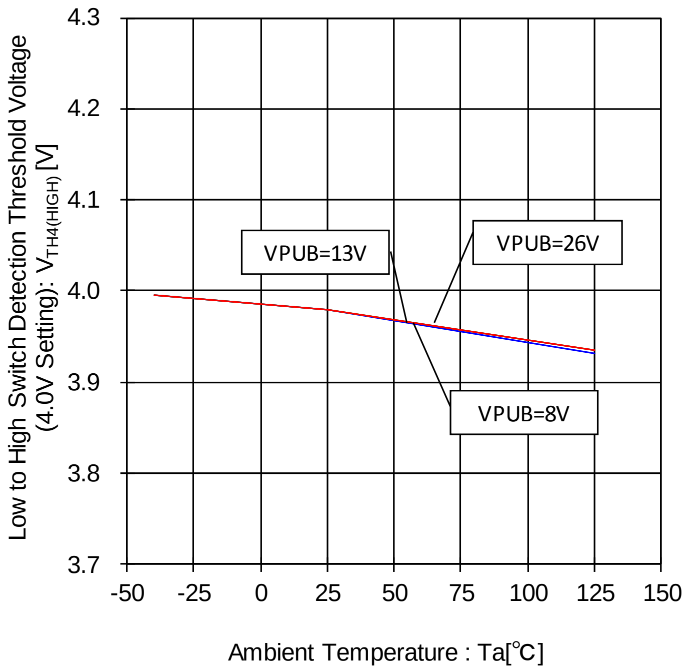


Figure 75. Low to High Switch Detection Threshold Voltage - Temperature Characteristic (4.0V Setting)

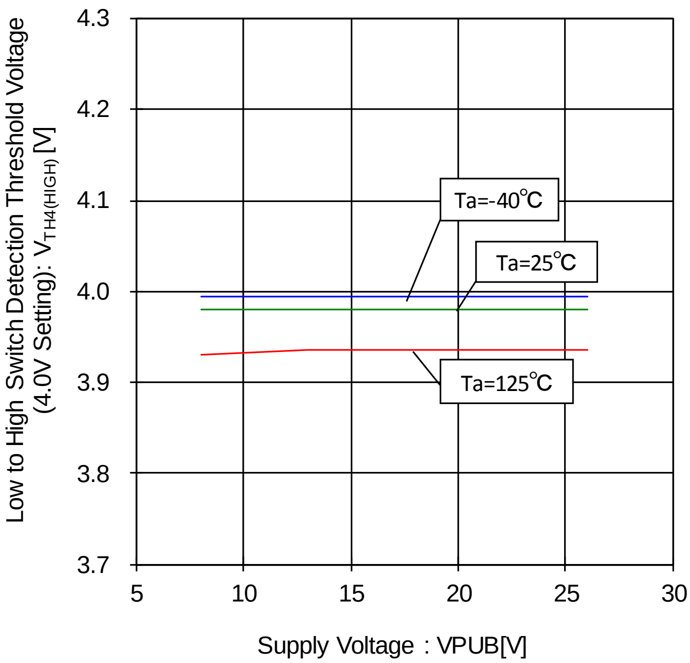


Figure 76. Low to High Switch Detection Threshold Voltage - Voltage Characteristic (4.0V Setting)

Typical Performance Curves - continued

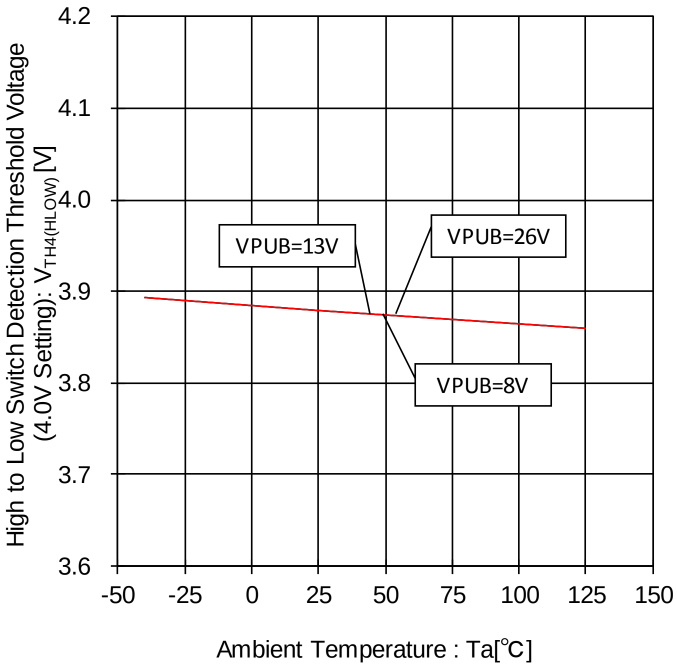


Figure 77. High to Low Switch Detection Threshold Voltage - Temperature Characteristic (4.0V Setting)

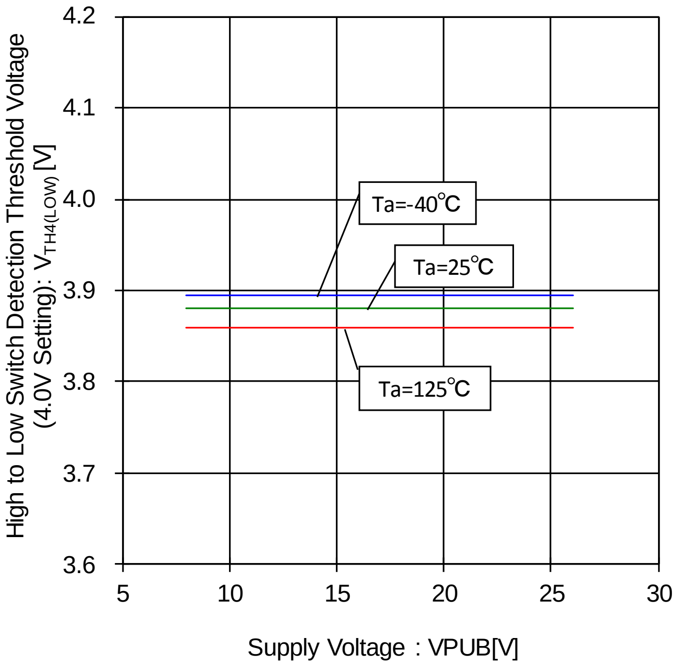


Figure 78. High to Low Switch Detection Threshold Voltage - Voltage Characteristic (4.0V Setting)

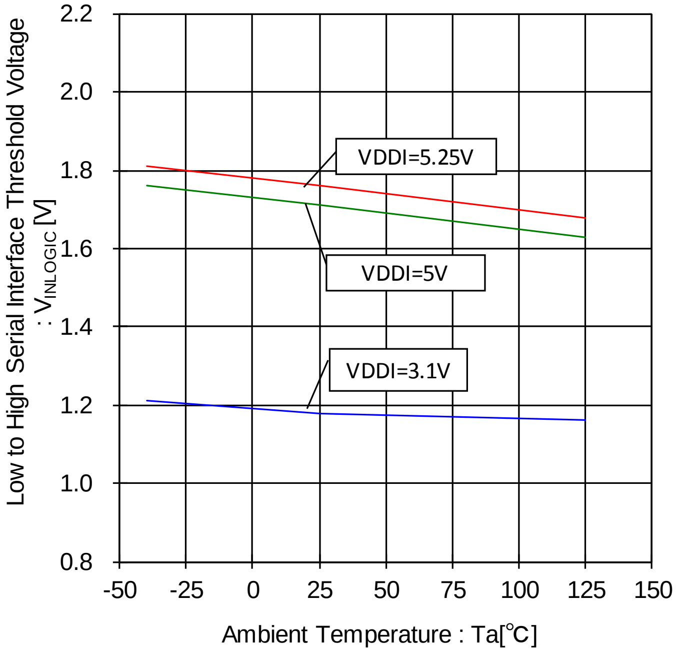


Figure 79. Low to High Serial Interface Threshold Voltage - Temperature Characteristic

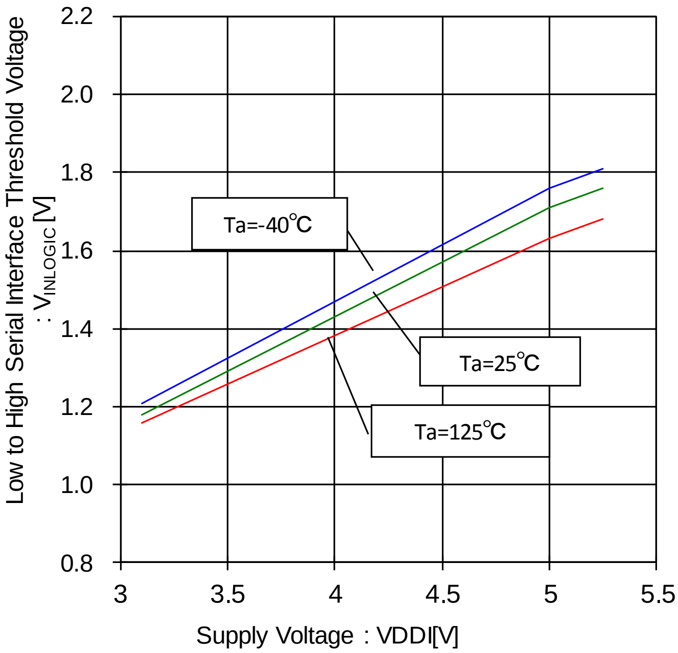


Figure 80. Low to High Serial Interface Threshold Voltage - Voltage Characteristic

Typical Performance Curves - continued

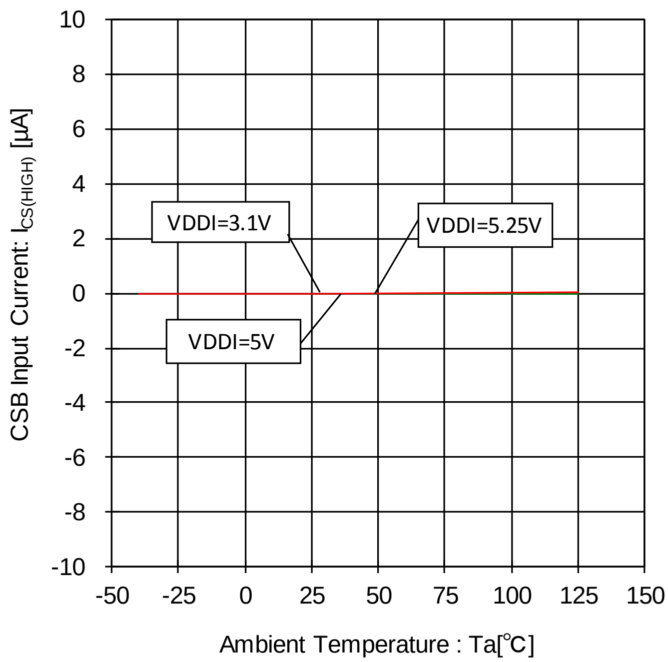


Figure 81. CSB Input Current- Temperature Characteristic (CSB=VDDI)

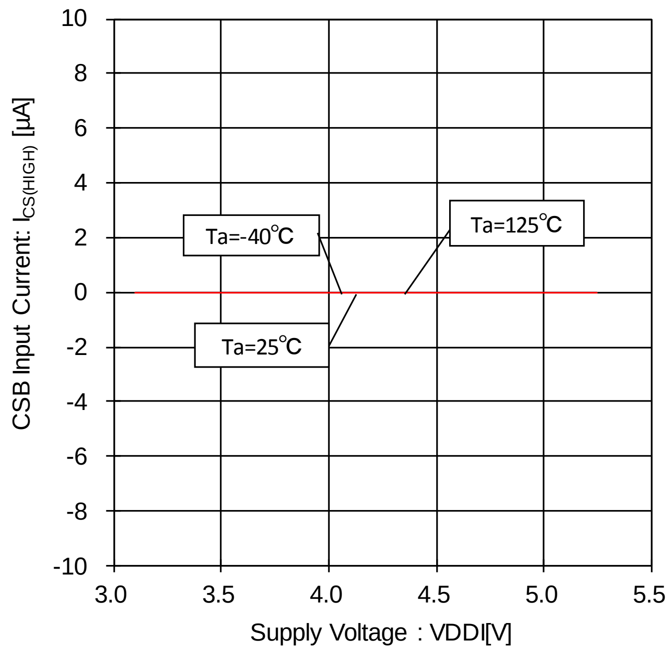


Figure 82. CSB Input Current- Voltage Characteristic (CSB=VDDI)

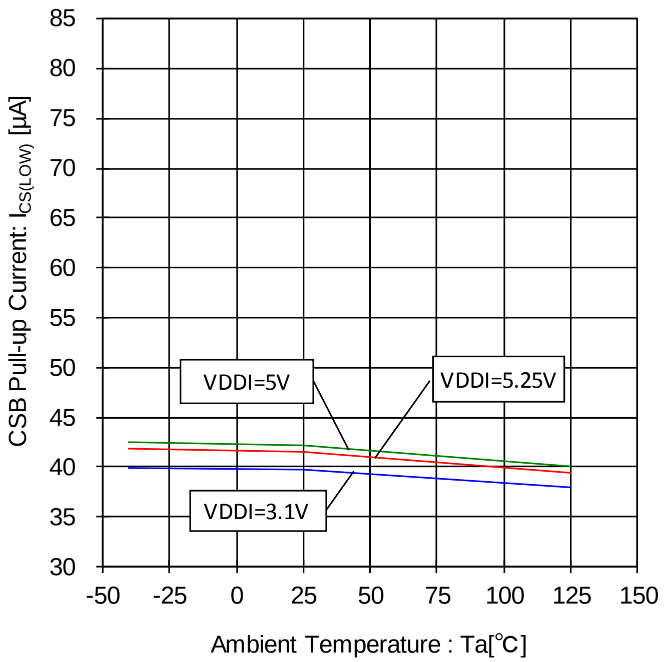


Figure 83. CSB Pull-up Current- Temperature Characteristic (CSB=0V)

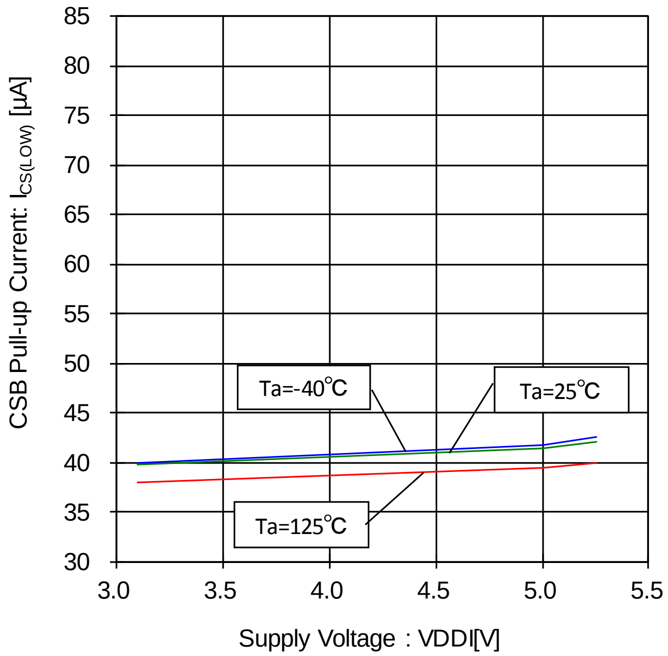


Figure 84. CSB Pull-up Current- Voltage Characteristic (CSB=0V)

Typical Performance Curves - continued

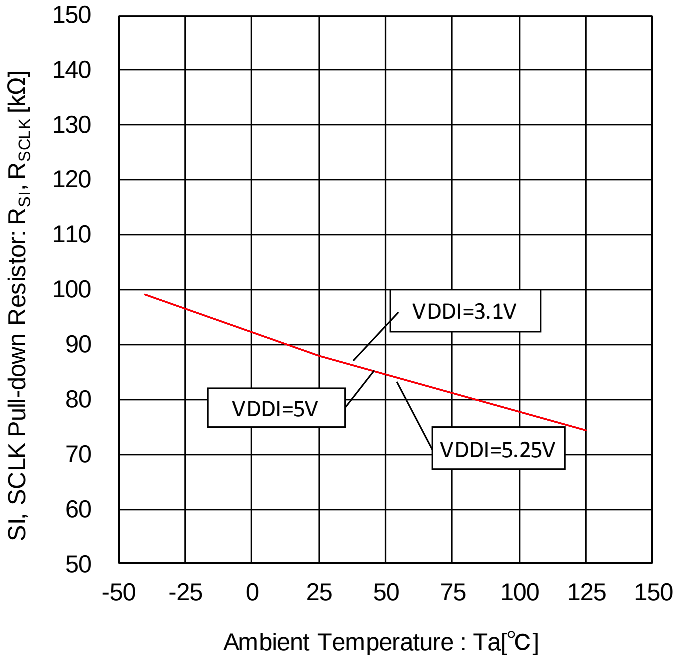


Figure 85. SI, SCLK Pull-down Resistor- Temperature Characteristic

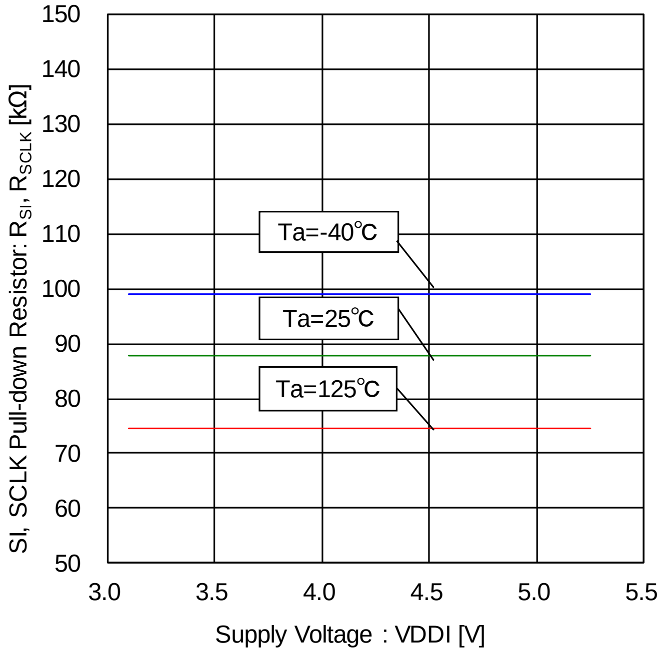


Figure 86. SI, SCLK Pull-down Resistor- Voltage Characteristic

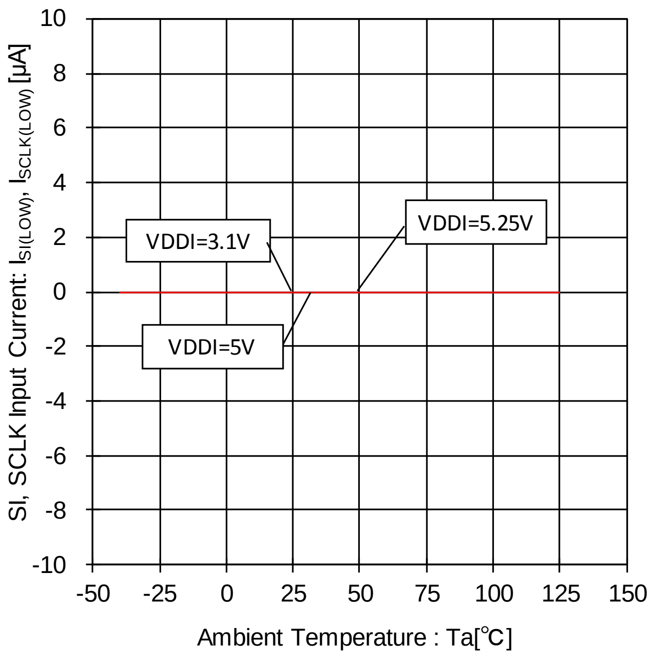


Figure 87. SI, SCLK Input Current- Temperature Characteristic
(SI, SCLK=0V)

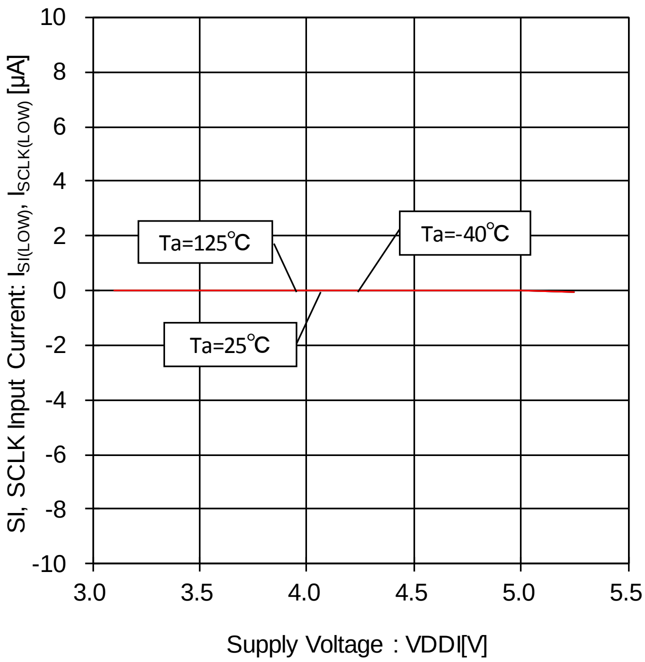


Figure 88. SI, SCLK Input Current- Voltage Characteristic
(SI, SCLK=0V)

Typical Performance Curves - continued

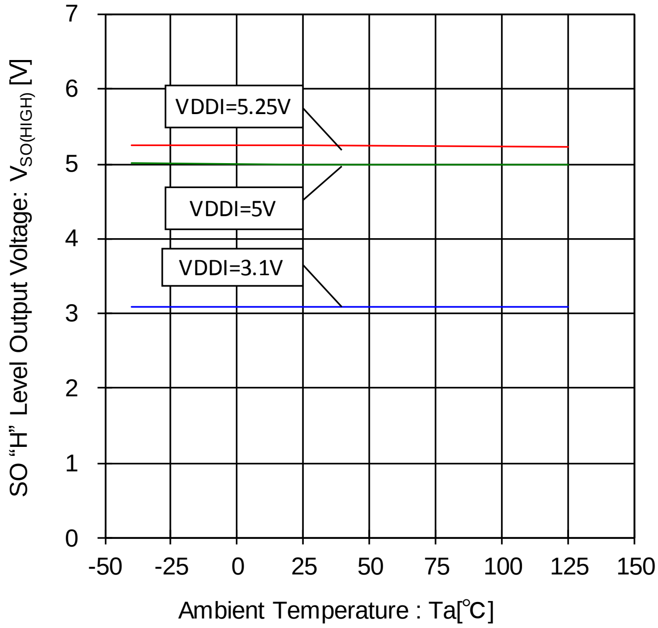


Figure 89. SO "H" Level Output Voltage- Temperature Characteristic (I_{SOURCE}=200µA)

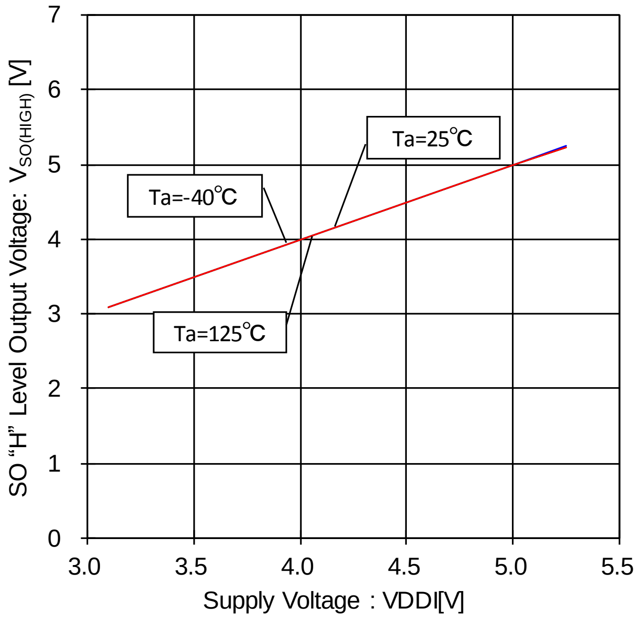


Figure 90. SO "H" Level Output Voltage- Voltage Characteristic (I_{SOURCE}=200µA)

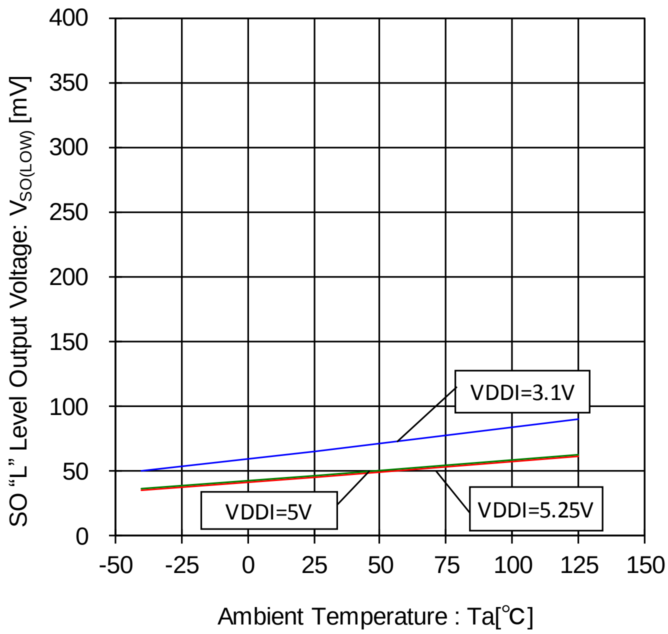


Figure 91. SO "L" Level Output Voltage- Temperature Characteristic (I_{SINK}=1.6mA)

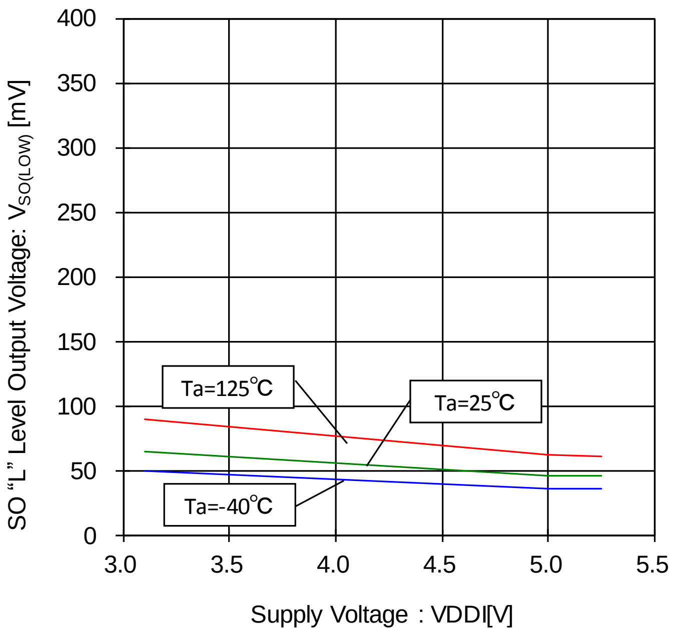


Figure 92. SO "L" Level Output Voltage- Voltage Characteristic (I_{SINK} =1.6mA)

Typical Performance Curves - continued

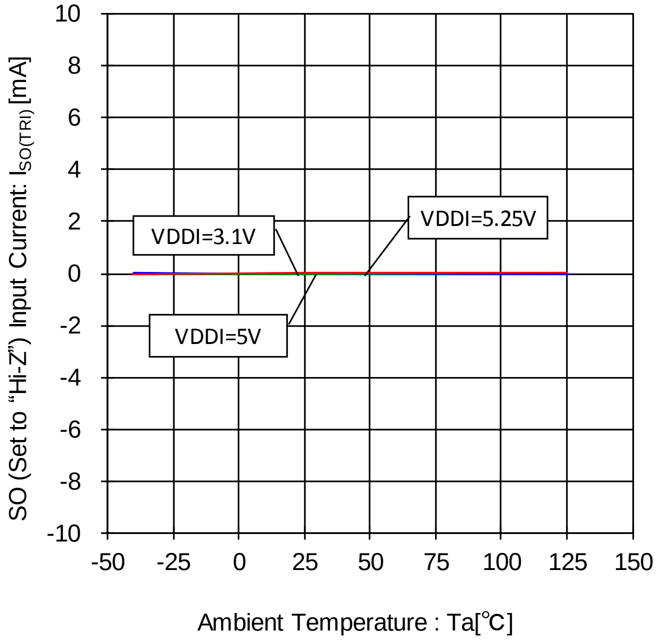


Figure 93. SO (Set to "Hi-Z") Input Current- Temperature Characteristic

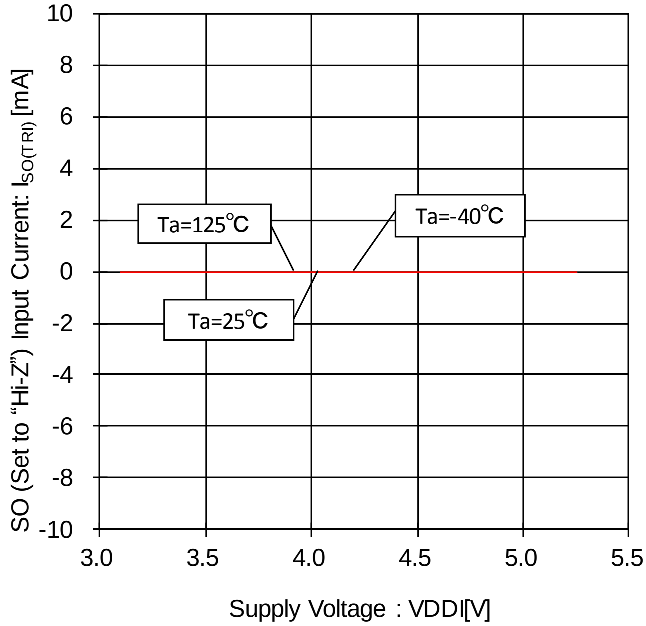


Figure 94. SO (Set to "Hi-Z") Input Current- Voltage Characteristic

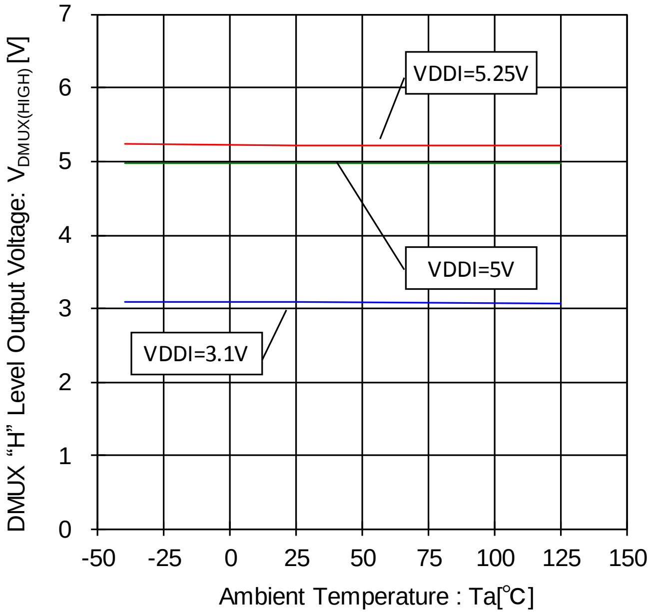


Figure 95. DMUX "H" Level Output Voltage- Temperature Characteristic (I_{SOURCE}=200µA)

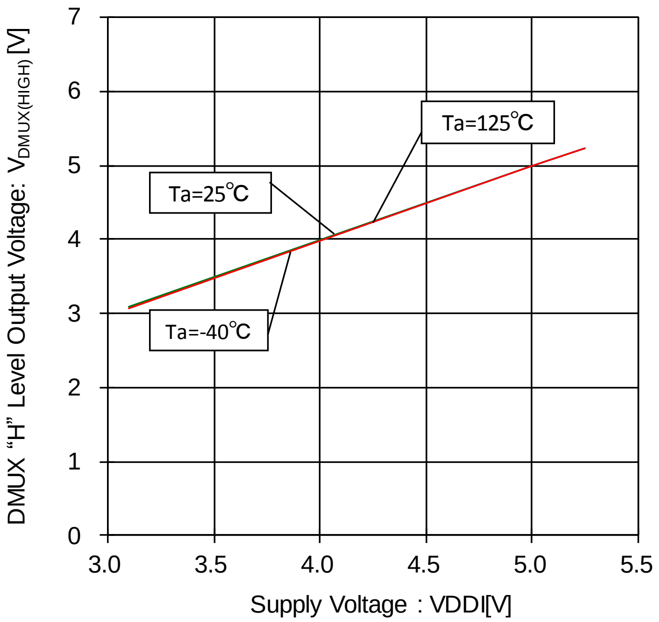


Figure 96. DMUX "H" Level Output Voltage- Voltage Characteristic (I_{SOURCE}=200µA)

Typical Performance Curves - continued

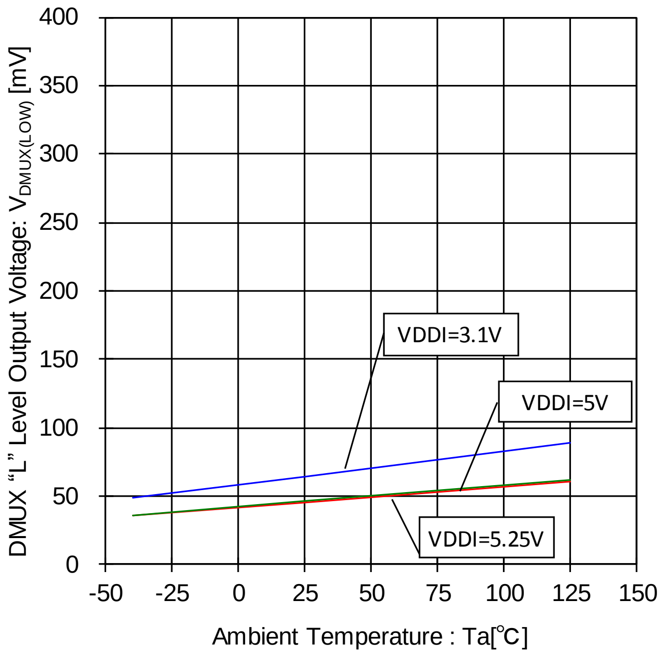


Figure 97. DMUX "L" Level Output Voltage- Temperature Characteristic (I_{SINK}=1.6mA)

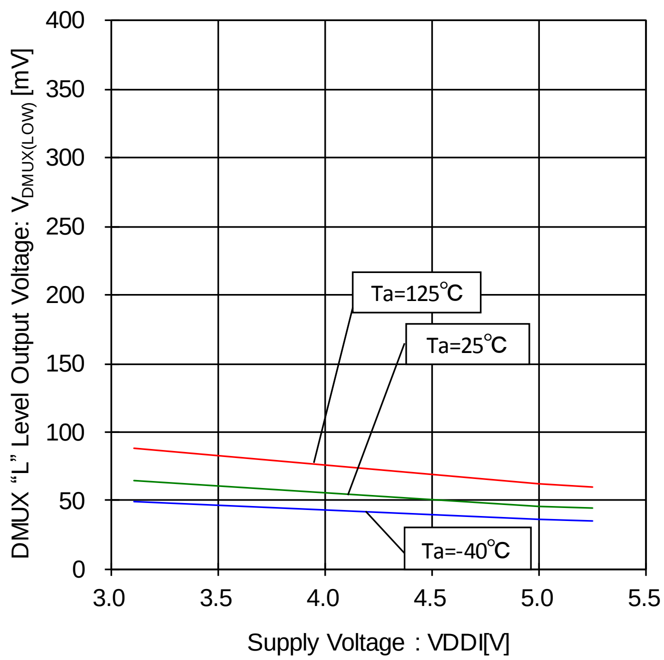


Figure 98. DMUX "L" Level Output Voltage- Voltage Characteristic (I_{SINK}=1.6mA)

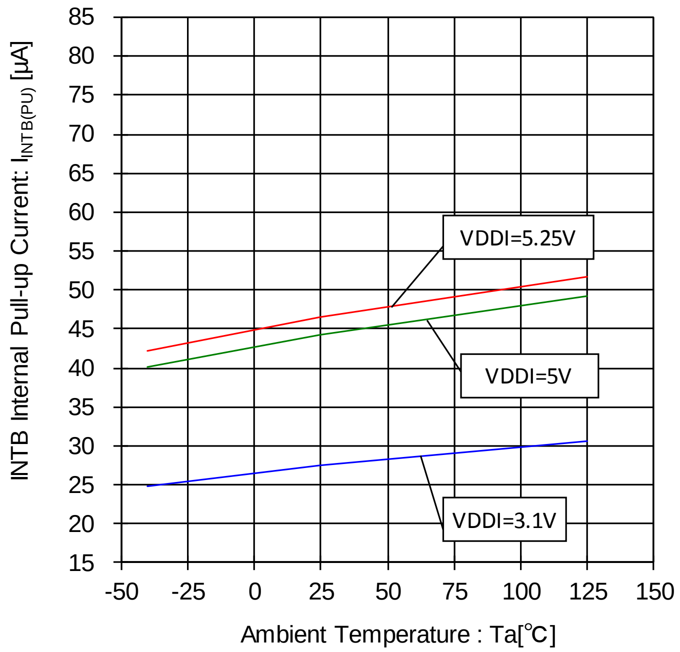


Figure 99. INTB Internal Pull-up Current- Temperature Characteristic

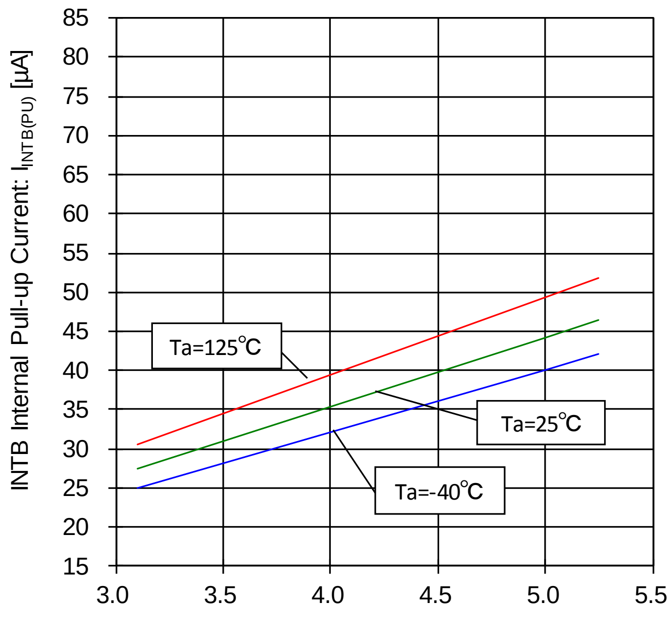


Figure 100. INTB Internal Pull-up Current- Voltage Characteristic

Typical Performance Curves - continued

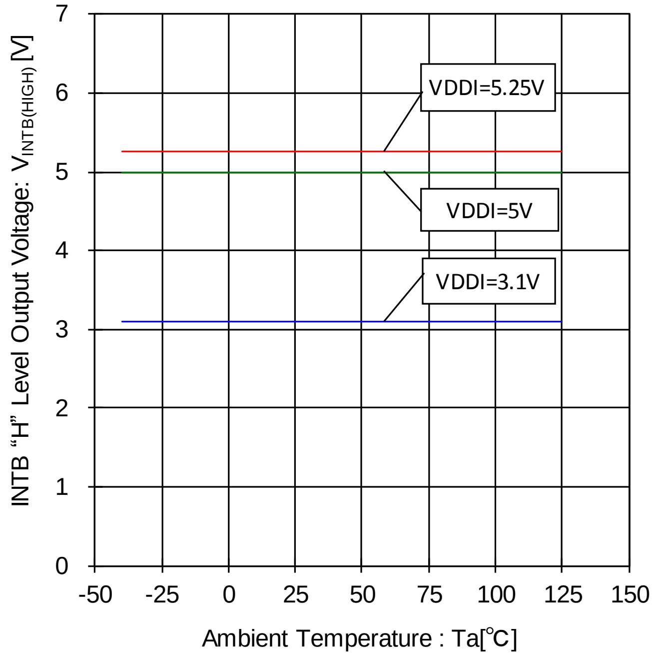


Figure 101. INTB "H" Level Output Voltage- Temperature Characteristic (INTB=OPEN)

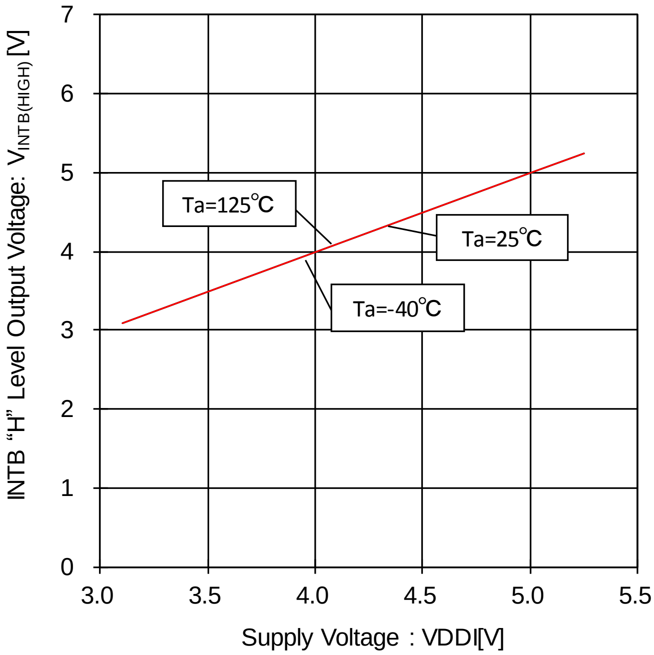


Figure 102. INTB "H" Level Output Voltage- Voltage Characteristic (INTB=OPEN)

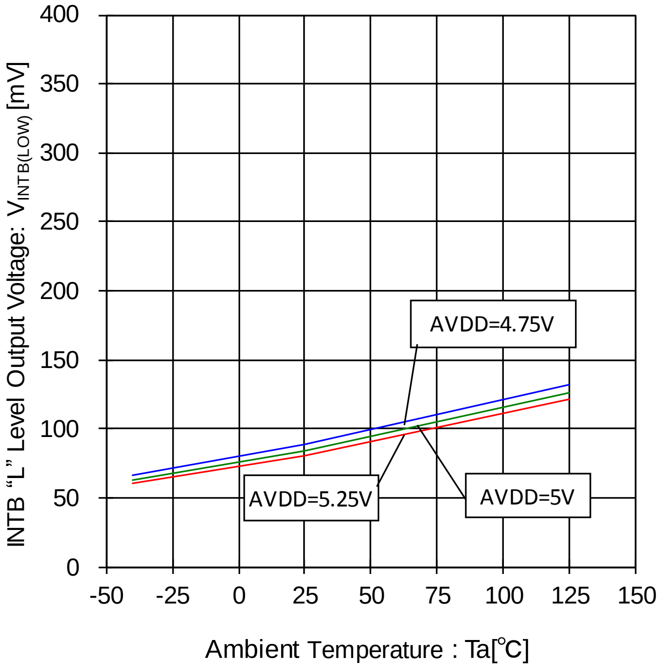


Figure 103. INTB "L" Level Output Voltage- Temperature Characteristic (I_{SINK}=1.0mA)

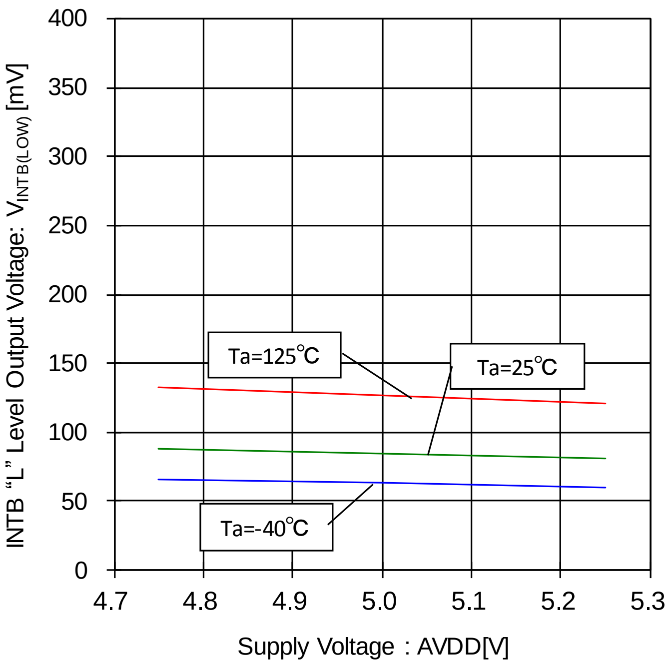


Figure 104. INTB "L" Level Output Voltage- Voltage Characteristic (I_{SINK}=1.0mA)

Typical Performance Curves - continued

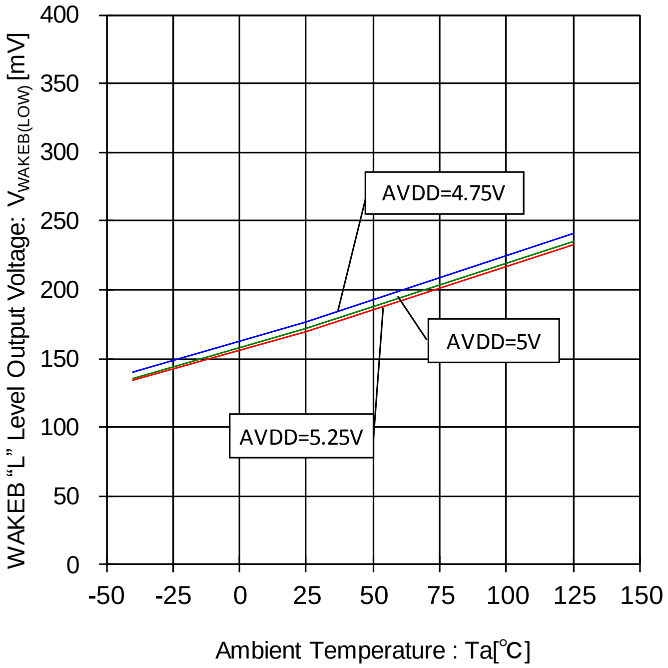


Figure 105. WAKEB "L" Level Output Voltage- Temperature Characteristic (WAKEB=1.0mA)

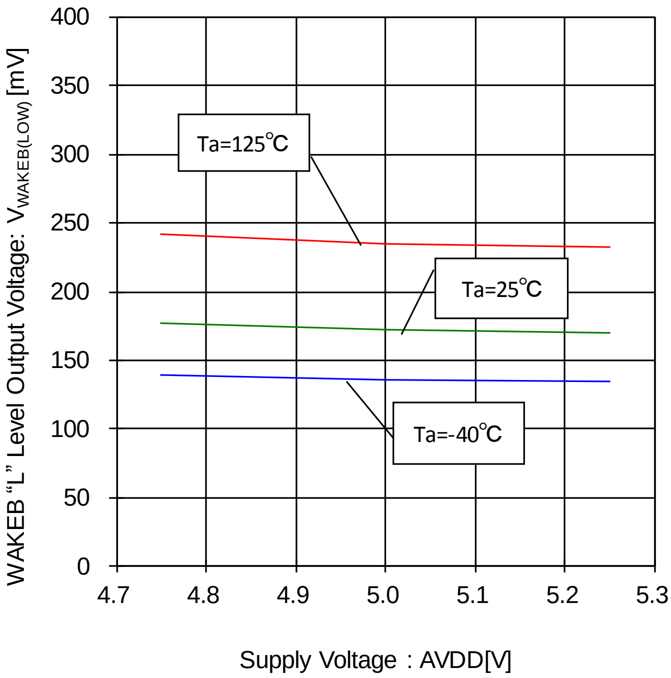


Figure 106. WAKEB "L" Level Output Voltage- Voltage Characteristic (WAKEB=1.0mA)

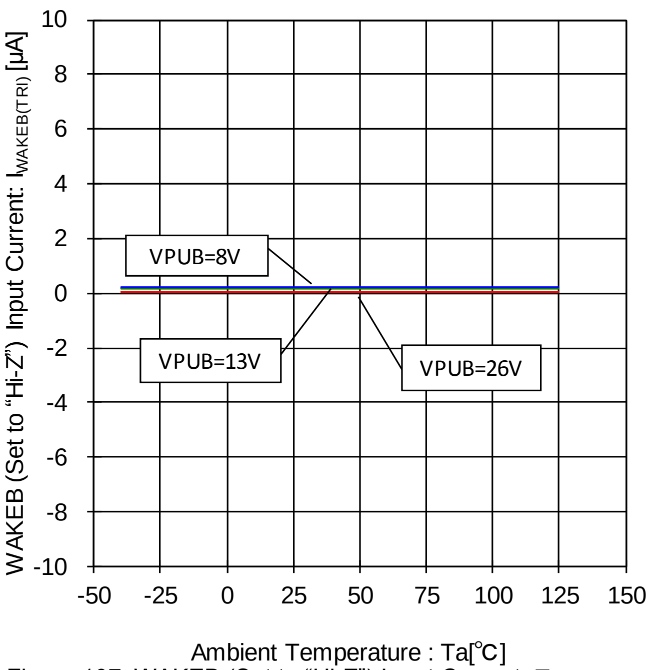


Figure 107. WAKEB (Set to "Hi-Z") Input Current- Temperature Characteristic

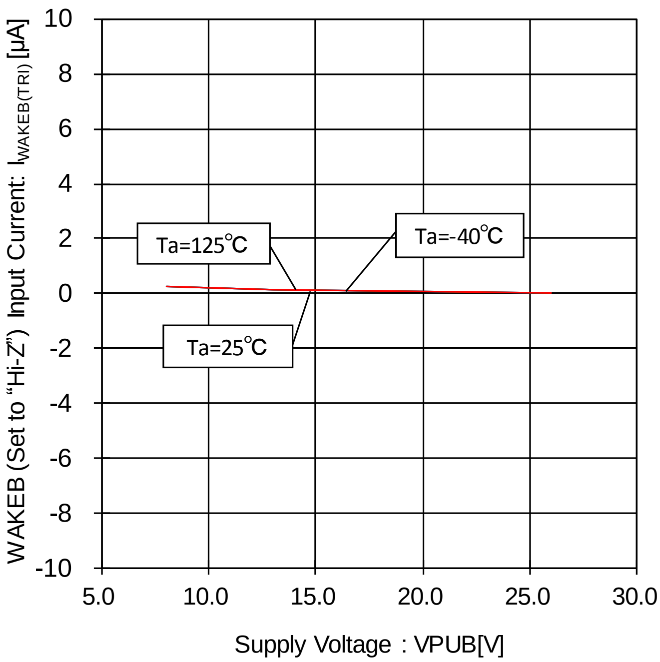


Figure 108. WAKEB (Set to "Hi-Z") Input Current- Voltage Characteristic

Typical Performance Curves - continued

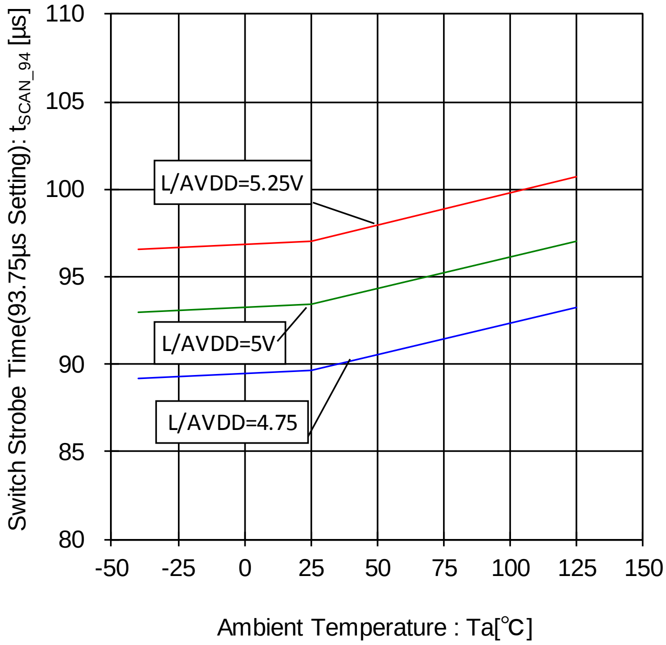


Figure 109. Switch Strobe Time- Temperature Characteristic (93.75µs Setting)

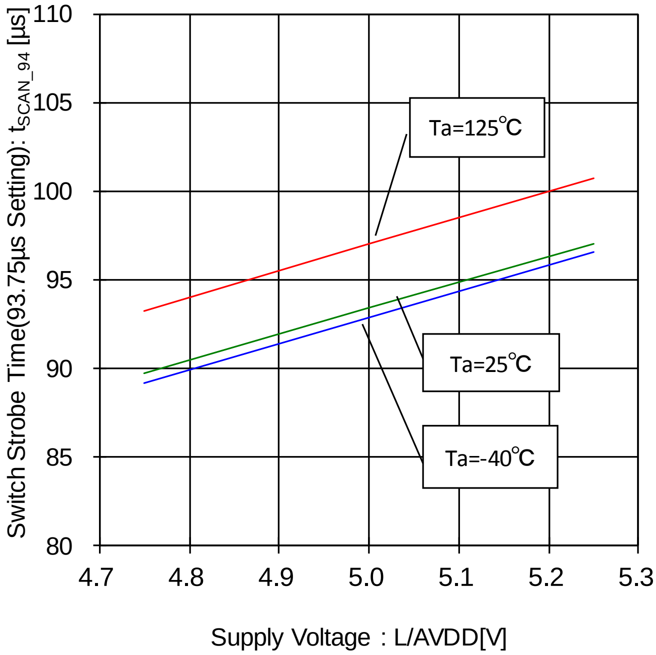


Figure 110. Switch Strobe Time- Voltage Characteristic (93.75µs Setting)

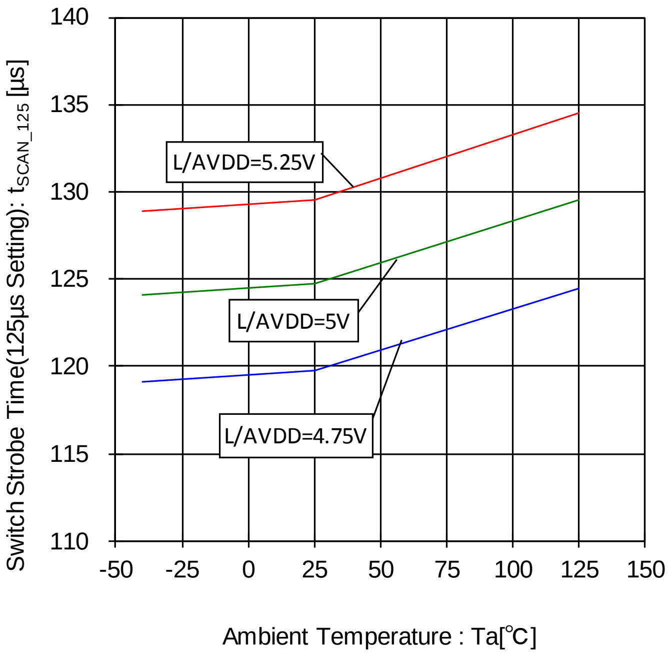


Figure 111. Switch Strobe Time- Temperature Characteristic (125µs Setting)

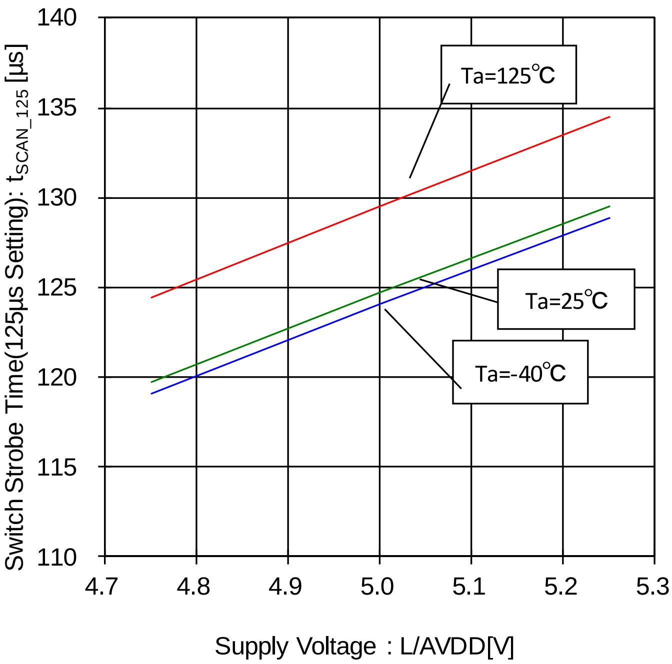


Figure 112. Switch Strobe Time- Voltage Characteristic (125µs Setting)

Typical Performance Curves - continued

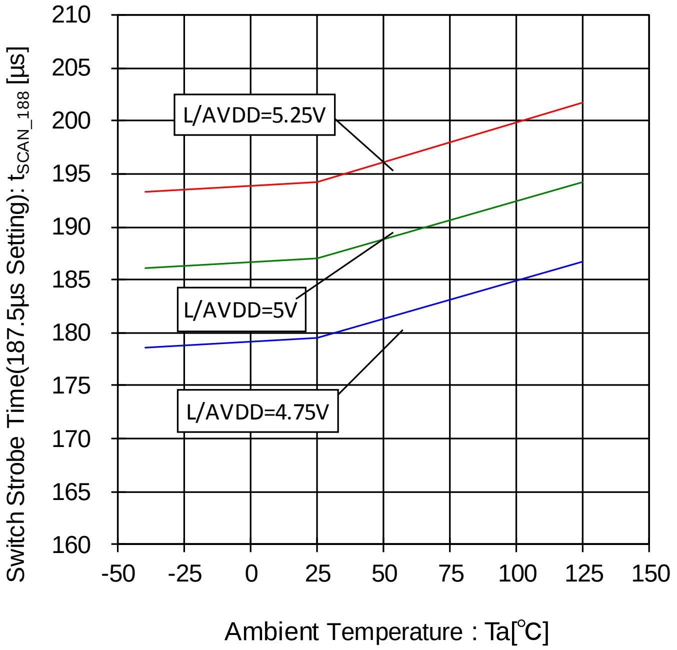


Figure 113. Switch Strobe Time- Temperature Characteristic (187.5µsSetting)

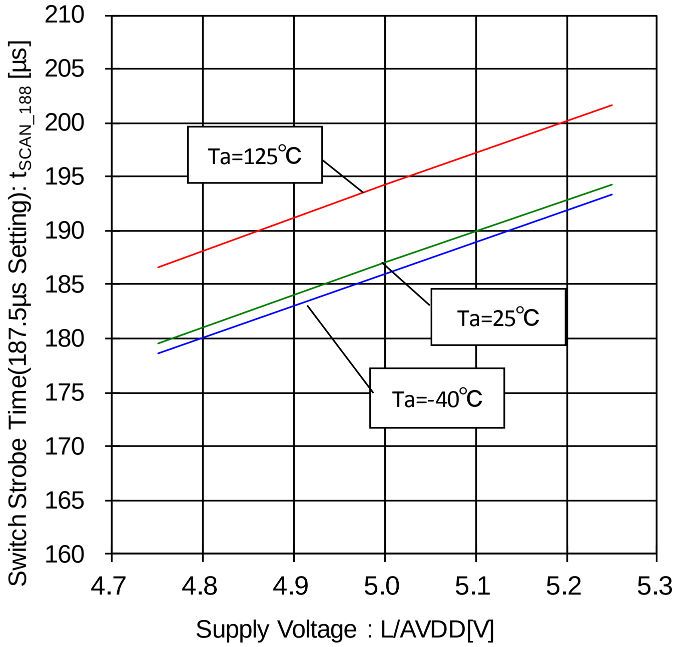


Figure 114. Switch Strobe Time- Voltage Characteristic (187.5µsSetting)

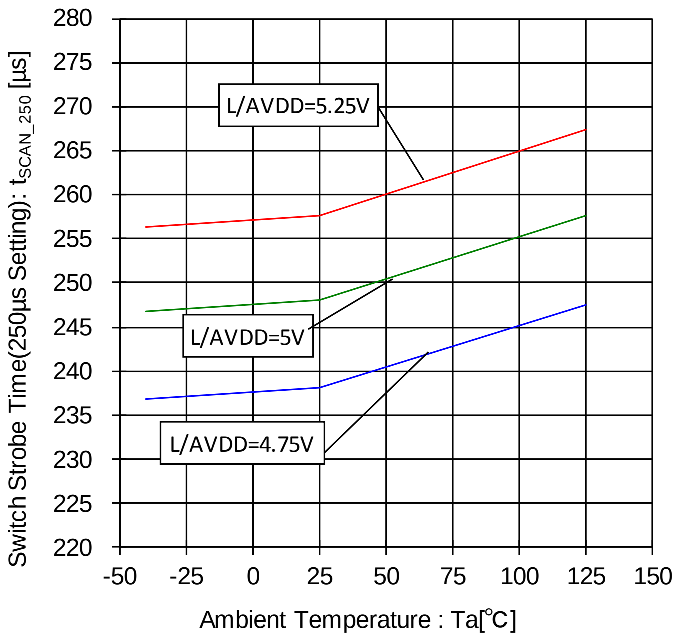


Figure 115. Switch Strobe Time- Temperature Characteristic (250µs Setting)

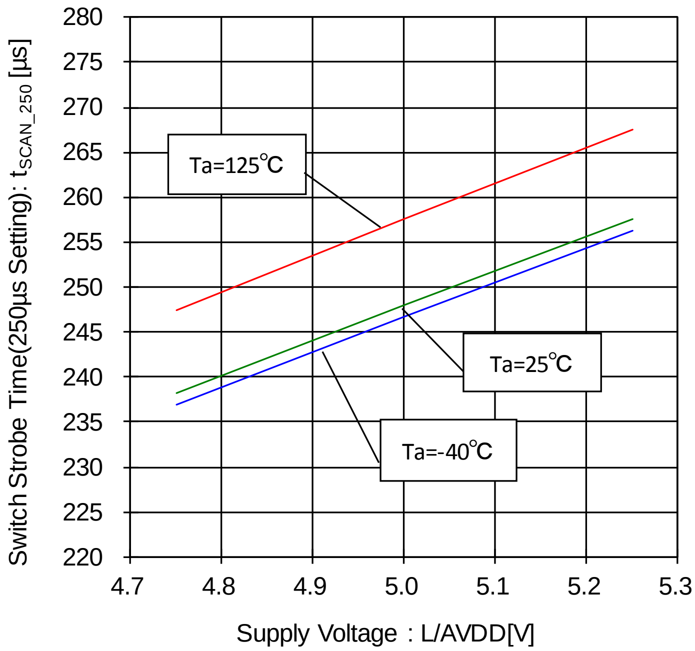


Figure 116. Switch Strobe Time- Voltage Characteristic (250µs Setting)

Typical Performance Curves　- continued

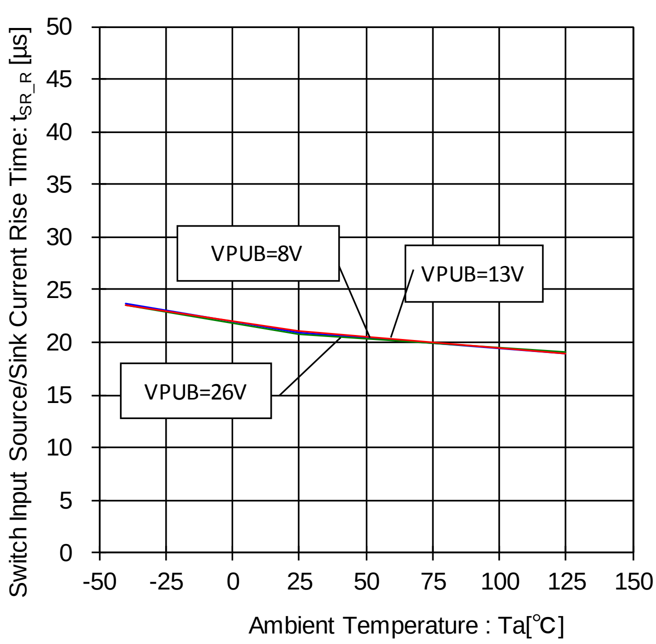


Figure 117. Switch Input Source/Sink Current Rise Time-Temperature Characteristic
(FSQ="0", FSQZ/A/B="0", 10mA Setting,
Load Resistance=100Ω)

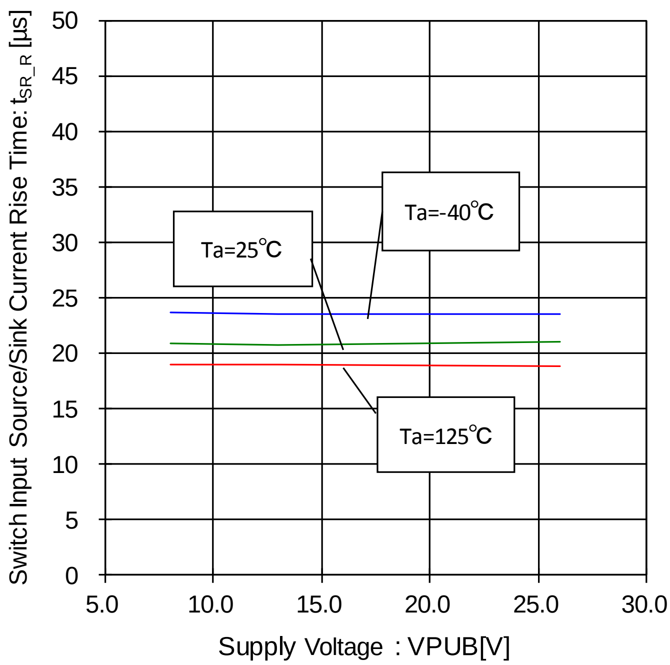


Figure 118. Switch Input Source/Sink Current Rise Time-Voltage Characteristic
(FSQ="0", FSQZ/A/B="0", 10mA Setting,
Load Resistance=100Ω)

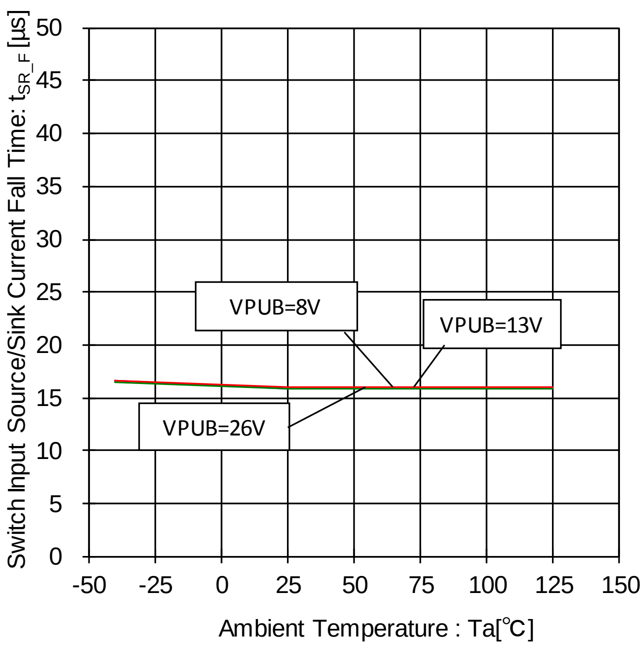


Figure 119. Switch Input Source/Sink Current Fall Time-Temperature Characteristic
(FSQ="0", FSQZ/A/B="0", 10mA Setting,
Load Resistance=100Ω)

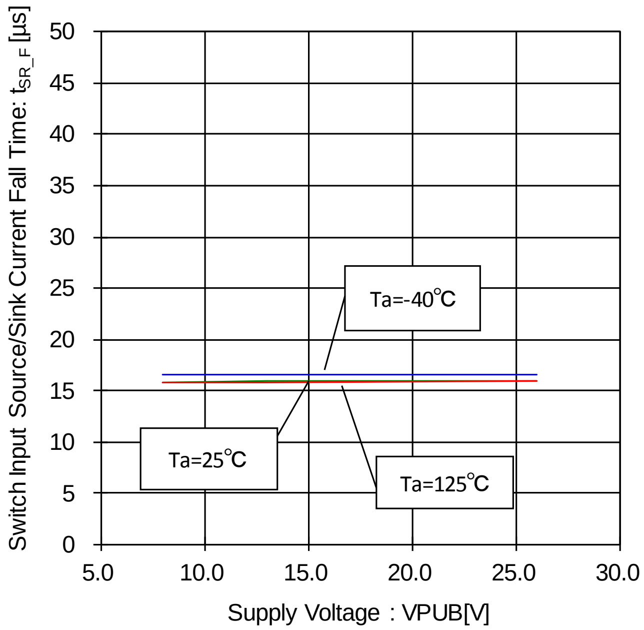


Figure 120. Switch Input Source/Sink Current Fall Time-Voltage Characteristic
(FSQ="0", FSQZ/A/B="0", 10mA Setting,
Load Resistance=100Ω)

Application Circuit Examples

1. Example of Application Circuit and its External Components

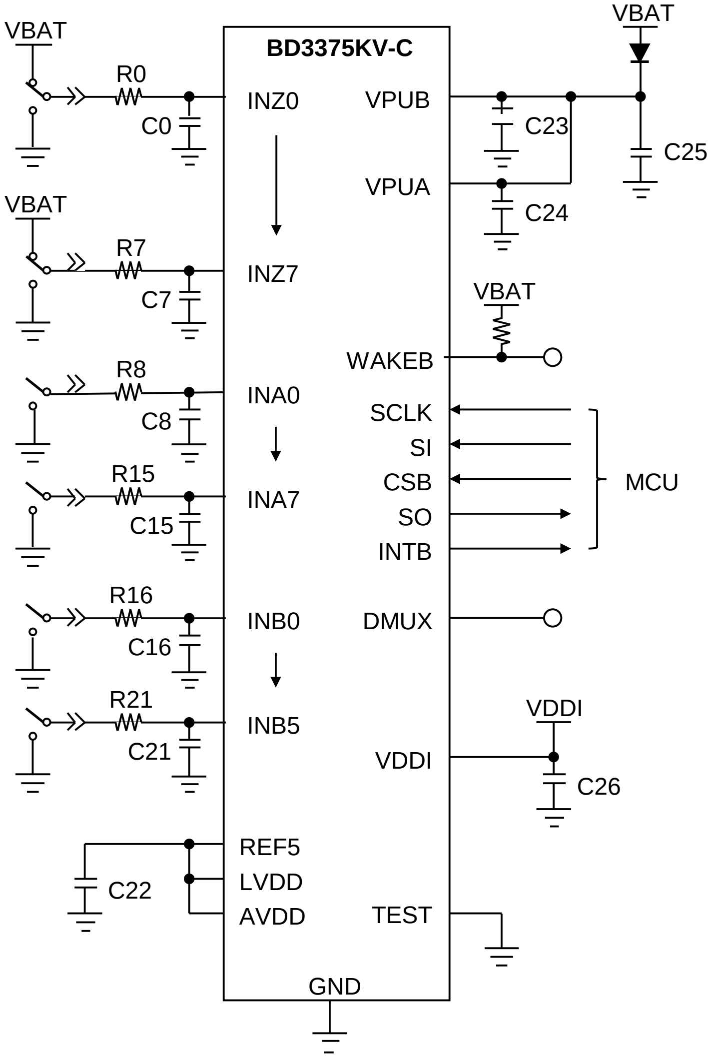


Figure 121. Example of Application Circuit and its External Components

・Capacitor (C23, C24, C26) at Power Supply Pins (VPUA, VPUB, VDDI)
Insert a 0.1µF capacitor between each power supply pin (VPUA, VPUB, and VDDI) and ground. Make sure to design the external components with sufficient margin for the intended application. It is recommended to use capacitors with excellent voltage and temperature characteristics.

・Capacitor (C22) at REF5
In order to prevent oscillation, a capacitor needs to be placed between the REF5 output pin and ground. It is recommended to use a capacitor (electrolytic, tantalum, or ceramic of at least 4.7µF). Make sure that capacitance of 4.7µF or higher is maintained at the intended operating supply voltage and temperature range. Temperature change can cause fluctuation in capacitance, which may lead to oscillation. If a ceramic capacitor is chosen, it is recommended to use X5R, X7R, or any others with better temperature and DC biasing characteristics and higher voltage tolerance.

・Capacitor(C0 to C21) at Switch Pin (INZ, INA, INB)
It is recommended to use at least 0.1µF capacitors as protection against ESD. Make sure to design the external circuit with sufficient margin for the intended application. Use capacitors with application specific voltage and temperature characteristics.

・Resistor (R0 to R21) at Switch Pin (INZ, INA, INB)
Choose the appropriate resistor to reduce EMI noise. Design the circuit so the pin voltage does not fall below the threshold voltage defined by ground float of [Load Resistance] x [Wetting Current] (when wetting current is set to source) or voltage drop (when wetting current is set to sink) may occur.

2. Example of Parallel Connection Circuit

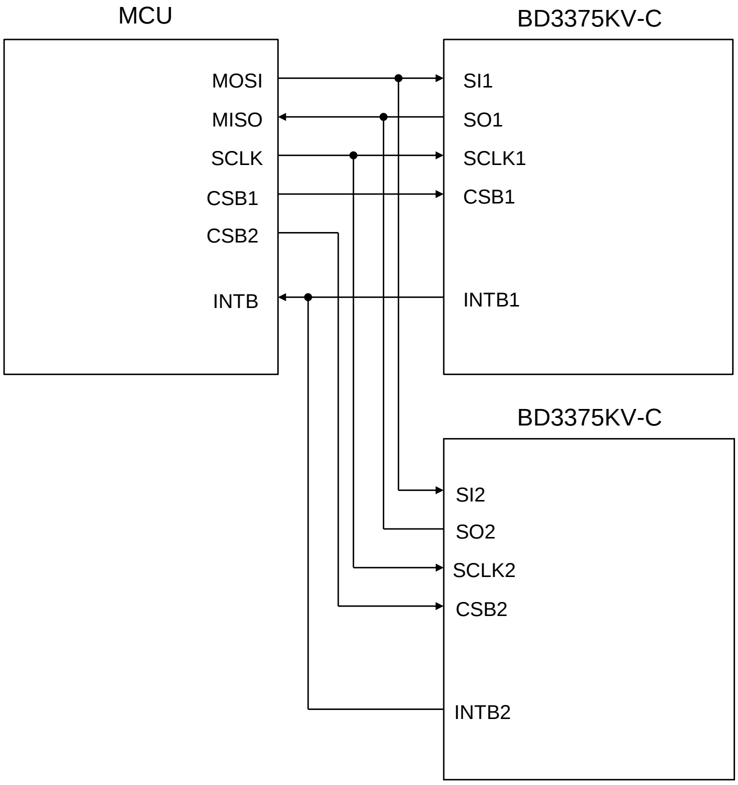
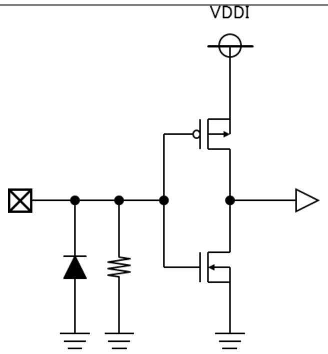
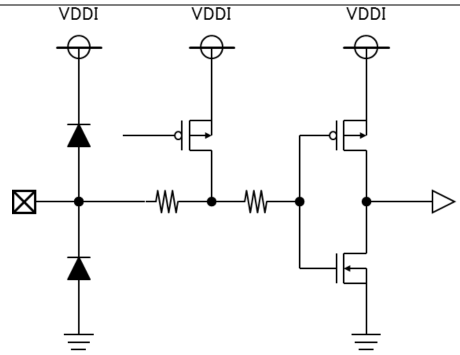
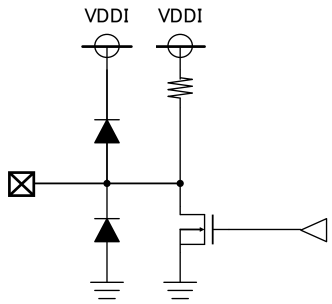
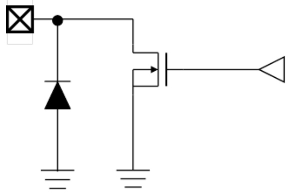
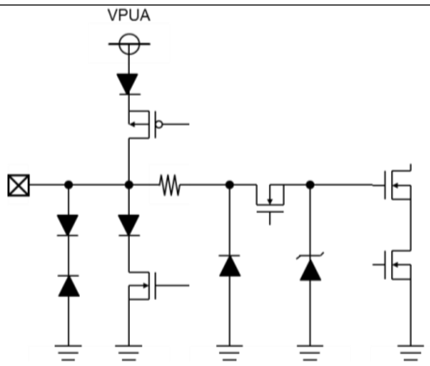
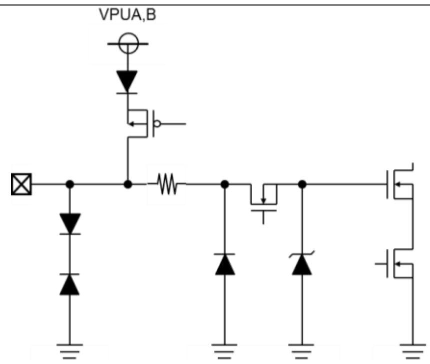
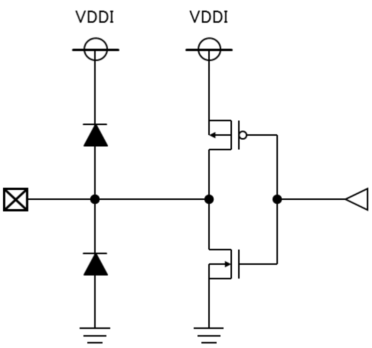
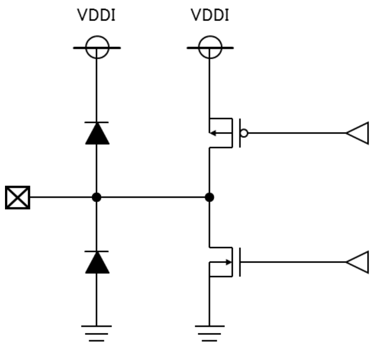


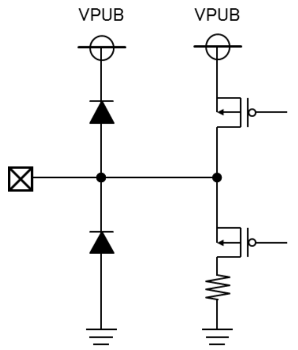
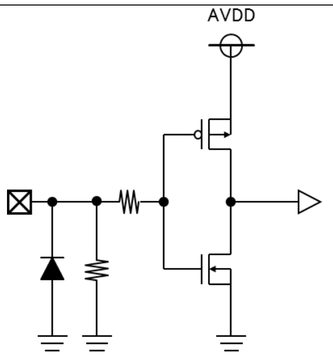
Figure 122. Example of Application Circuit and its External Components

・Parallel Connection
Please prepare CSB terminals respectively.

I / O Equivalence Circuit

Type	Equivalence circuit	Type	Equivalence circuit
A	 Input: SI, SCLK (with an Internal Pull-down Resistor)	B	 Input: CSB (with an Internal Pull-up Current source)
C	 Open-drain Output: INTB (with an Internal Pull-up Resistor)	D	 Open-drain Output: WAKEB
E	 Switch Input: INZ (with an Internal Pull-up/down Current Source)	F	 Switch Input: INA, INB (with an Internal Pull-up Current Source)
G	 Output: DMUX	H	 Output: SO

I / O Equivalence Circuit

Type	Equivalence circuit	Type	Equivalence circuit
I	 Output: REF5	J	 Input: TEST (with an Internal Pull-down Resistor)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

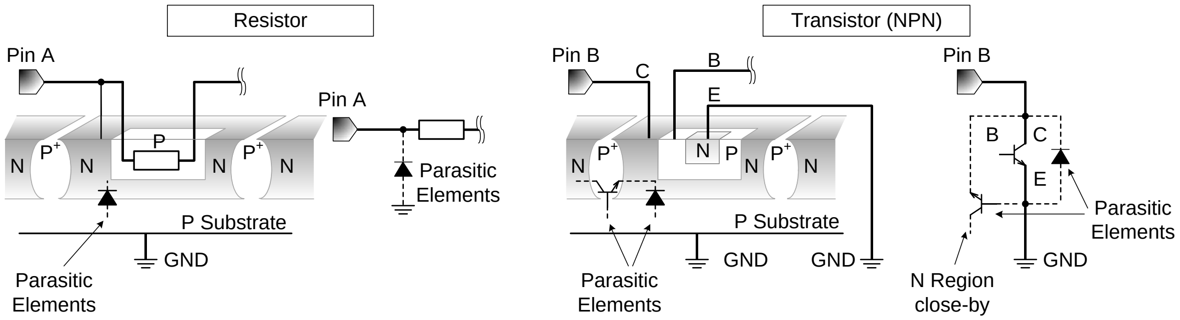


Figure 123. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

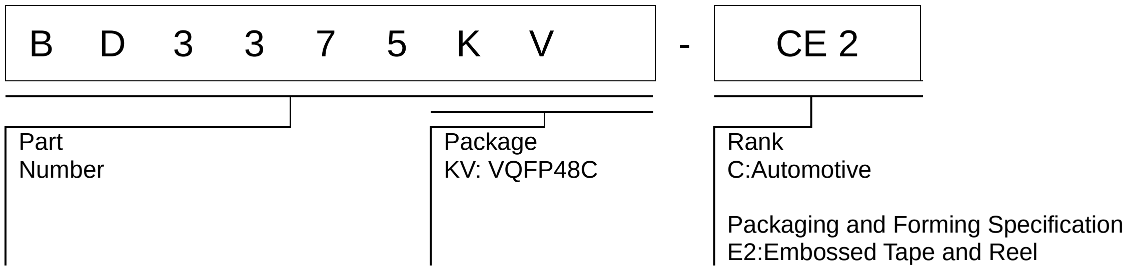


Figure 124. Ordering Information

Marking Diagrams (Top View)

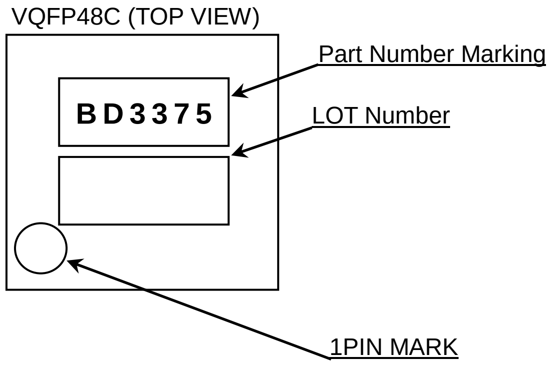
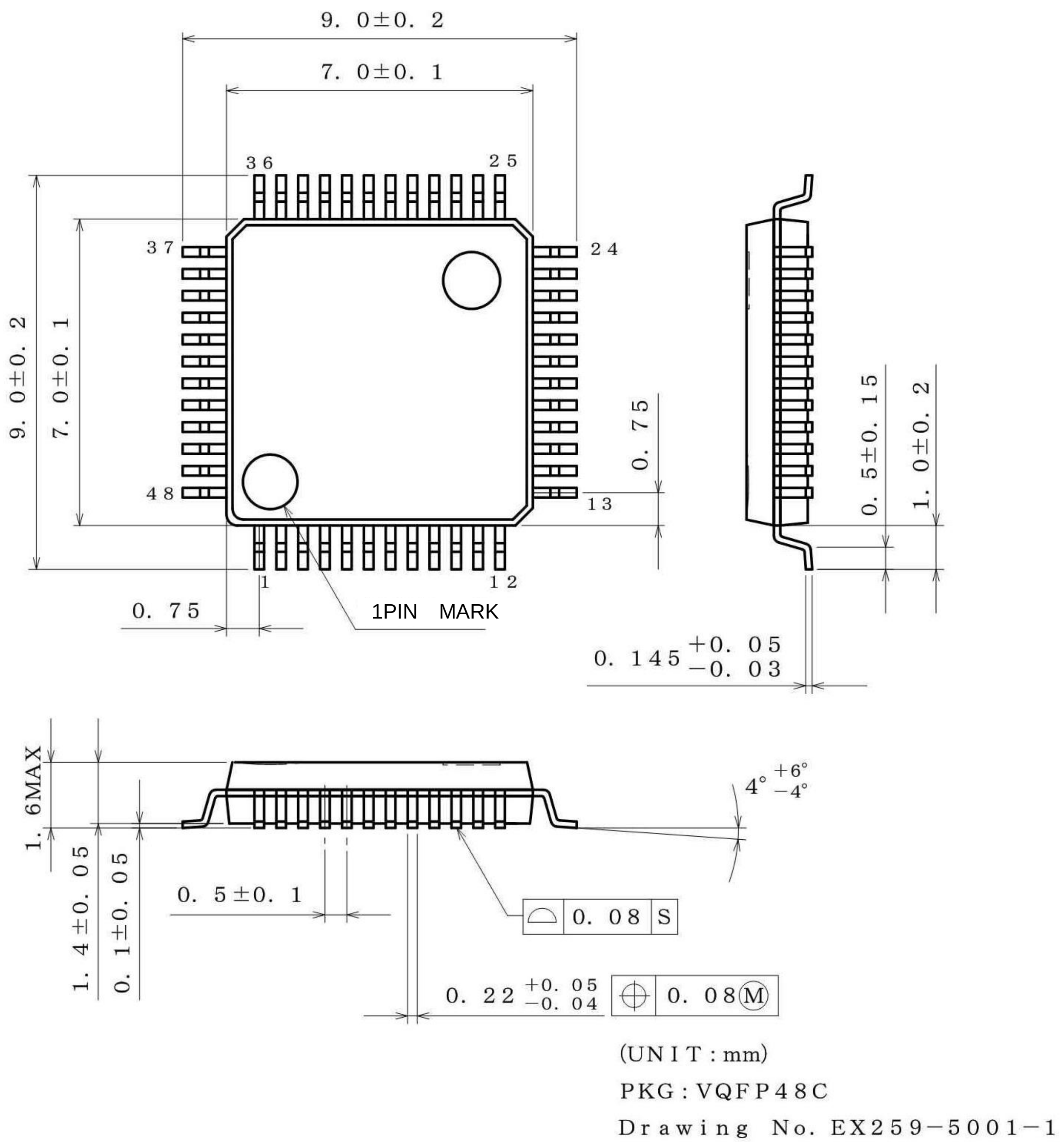


Figure 125. Marking Diagrams

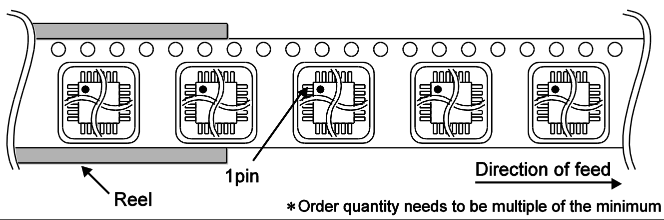
Physical Dimensions, Tape and Reel information

Package Name	VQFP48C



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Figure 126. Physical Dimensions, Tape and Reel information

Revision History

Date	Rev.	History
29.Jan.2016	001	(Japanese Only)
27.Sep.2016	002	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

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- *Подбор аналогов.*
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