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## Serial EEPROM series Standard EEPROM
# MicroWire BUS EEPROM (3-Wire)

# BR93G76-3A

### ●General Description

BR93G76-3A is serial EEPROM of serial 3-line Interface method.
They are 16bit organization and CS PIN is the first PIN in their PIN configuration.

### ●Features

- ■ 3-line communications of chip select, serial clock, serial data input / output (the case where input and output are shared)
- ■ Operations available at high speed 3MHz clock (4.5 V~5.5 V)
- ■ High speed write available (write time 5ms max.)
- ■ Same package and pin configuration from 1Kbit to 16Kbit
- ■ 1.7~5.5V single power source operation
- ■ Address auto increment function at read operation
- ■ Write mistake prevention function
  - » Write prohibition at power on
  - » Write prohibition by command code
  - » Write mistake prevention function at low voltage
- ■ Self-timed programming cycle
- ■ Program condition display by READY / $\overline{\text{BUSY}}$
- ■ Compact package
  SOP8/SOP-J8/SSOP-B8/TSSOP-B8/MSOP8/
  TSSOP-B8J/DIP-T8/VSON008X2030
- ■ More than 40 years data retention
- ■ More than 1 million write cycles
- ■ Initial delivery state all addresses FFFFh

### ●Packages W(Typ.) x D(Typ.)x H(Max.)

**DIP-T8**
9.30mm x 6.50mm x 7.10mm

**TSSOP-B8**
3.00mm x 6.40mm x 1.20mm

**SOP8**
5.00mm x 6.20mm x 1.71mm

**TSSOP-B8J**
3.00mm x 4.90mm x 1.10mm

**SOP- J8**
4.90mm x 6.00mm x 1.65mm

**MSOP8**
2.90mm x 4.00mm x 0.90mm

**SSOP-B8**
3.00mm x 6.40mm x 1.35mm

**VSON008X2030**
2.00mm x 3.00mm x 0.60mm

### ●BR93G76-3A

| Capacity | Bit format | Type | Power source voltage | DIP-T8*1 | SOP8 | SOP-J8 | SSOP-B8 | TSSOP-B8 | TSSOP-B8J | MSOP8 | VSON008 X2030 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 8Kbit | 512×16 | BR93G76-3A | 1.7~5.5V | ● | ● | ● | ● | ● | ● | ● | ● |

*1 DIP-T8 is not halogen free package

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays


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## ●Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit | Remarks |
|---|---|---|---|---|
| Supply voltage | VCC | -0.3 to +6.5 | V | |
| Permissible dissipation | Pd | 800 (DIP-T8) | mW | When using at Ta=25℃ or higher 8.0mW to be reduced per 1℃. |
| | | 450 (SOP8) | | When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃. |
| | | 450 (SOP-J8) | | When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃. |
| | | 300 (SSOP-B8) | | When using at Ta=25℃ or higher 3.0mW to be reduced per 1℃. |
| | | 330 (TSSOP-B8) | | When using at Ta=25℃ or higher 3.3mW to be reduced per 1℃. |
| | | 310 (TSSOP-B8J) | | When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃. |
| | | 310 (MSOP8) | | When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃. |
| | | 300 (VSON008X2030) | | When using at Ta=25℃ or higher 3.0mW to be reduced per 1℃. |
| Storage temperature | Tstg | −65 to +150 | ℃ | |
| Operating temperature | Topr | −40 to +85 | ℃ | |
| Input voltage/ Output voltage | - | -0.3 to Vcc+1.0 | V | The Max value of Input voltage/Output voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Input voltage /Output voltage is not under -0.8V. |
| Junction temperature | Tjmax | 150 | ℃ | Junction temperature at the storage condition |

## ●Memory cell characteristics (VCC=1.7~5.5V)

| Parameter | Limit | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Write cycles *1 | 1,000,000 | - | - | Times | Ta=25℃ |
| Data retention *1 | 40 | - | - | Years | Ta=25℃ |

○Shipment data all address FFFFh
*1 Not 100% TESTED

## ●Recommended Operation Ratings

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply voltage | VCC | 1.7~5.5 | V |
| Input voltage | $V_{IN}$ | 0~VCC | |


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●**DC characteristics** (Unless otherwise specified, VCC=1.7~5.5V, Ta=-40~+85℃)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input low voltage | $V_{IL}$ | -0.3*1 | - | 0.3VCC | V | 1.7V≦VCC≦5.5V |
| Input high voltage | $V_{IH}$ | 0.7VCC | - | VCC+1.0 | V | 1.7V≦VCC≦5.5V |
| Output low voltage 1 | $V_{OL1}$ | 0 | - | 0.4 | V | $I_{OL}$=2.1mA, 2.7V≦VCC≦5.5V |
| Output low voltage 2 | $V_{OL2}$ | 0 | - | 0.2 | V | $I_{OL}$=100μA |
| Output high voltage 1 | $V_{OH1}$ | 2.4 | - | VCC | V | $I_{OH}$=-0.4mA, 2.7V≦VCC≦5.5V |
| Output high voltage 2 | $V_{OH2}$ | VCC-0.2 | - | VCC | V | $I_{OH}$=-100μA |
| Input leakage current1 | $I_{LI1}$ | -1 | - | +1 | μA | $V_{IN}$=0V~VCC(CS,SK,DI) |
| Output leakage current | $I_{LO}$ | -1 | - | +1 | μA | $V_{OUT}$=0V~VCC, CS=0V |
| Supply current | $I_{CC1}$ | - | - | 1.0 | mA | VCC=1.7V, $f_{SK}$=1MHz, $t_{E/W}$=5ms (WRITE) |
| | | - | - | 2.0 | mA | VCC=5.5V ,$f_{SK}$=3MHz, $t_{E/W}$=5ms (WRITE) |
| | $I_{CC2}$ | - | - | 0.5 | mA | $f_{SK}$=1MHz (READ) |
| | | - | - | 1.0 | mA | $f_{SK}$=3MHz (READ) |
| | $I_{CC3}$ | - | - | 2.0 | mA | VCC=2.5V, $f_{SK}$=1MHz<br>$t_{E/W}$=5ms (WRAL, ERAL) |
| | | - | - | 3.0 | mA | VCC=5.5V ,$f_{SK}$=3MHz<br>$t_{E/W}$=5ms (WRAL, ERAL) |
| Standby current | $I_{SB1}$ | - | - | 2.0 | μA | CS=0V |

*1 When the pulse width is 50ns or less, the Min value of $V_{IL}$ is admissible to -0.8V.


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●**AC characteristics** (Unless otherwise specified, VCC=1.7~2.5V, Ta=-40~+85℃)

| Parameter | Symbol | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| SK frequency | $f_{SK}$ | - | - | 1 | MHz |
| SK high time | $t_{SKH}$ | 250 | - | - | ns |
| SK low time | $t_{SKL}$ | 250 | - | - | ns |
| CS low time | $t_{CS}$ | 250 | - | - | ns |
| CS setup time | $t_{CSS}$ | 200 | - | - | ns |
| DI setup time | $t_{DIS}$ | 100 | - | - | ns |
| CS hold time | $t_{CSH}$ | 0 | - | - | ns |
| DI hold time | $t_{DIH}$ | 100 | - | - | ns |
| Data “1” output delay | $t_{PD1}$ | - | - | 400 | ns |
| Data “0” output delay | $t_{PD0}$ | - | - | 400 | ns |
| Time from CS to output establishment | $t_{SV}$ | - | - | 400 | ns |
| Time from CS to High-Z | $t_{DF}$ | - | - | 200 | ns |
| Write cycle time | $t_{E/W}$ | - | - | 5 | ms |

(Unless otherwise specified, VCC=2.5~4.5V, Ta=-40~+85℃)

| Parameter | Symbol | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| SK frequency | $f_{SK}$ | - | - | 2 | MHz |
| SK high time | $t_{SKH}$ | 230 | - | - | ns |
| SK low time | $t_{SKL}$ | 200 | - | - | ns |
| CS low time | $t_{CS}$ | 200 | - | - | ns |
| CS setup time | $t_{CSS}$ | 50 | - | - | ns |
| DI setup time | $t_{DIS}$ | 100 | - | - | ns |
| CS hold time | $t_{CSH}$ | 0 | - | - | ns |
| DI hold time | $t_{DIH}$ | 100 | | - | ns |
| Data “1” output delay | $t_{PD1}$ | - | - | 200 | ns |
| Data “0” output delay | $t_{PD0}$ | - | - | 200 | ns |
| Time from CS to output establishment | $t_{SV}$ | - | - | 150 | ns |
| Time from CS to High-Z | $t_{DF}$ | - | - | 100 | ns |
| Write cycle time | $t_{E/W}$ | - | - | 5 | ms |

(Unless otherwise specified, VCC=4.5~5.5V, Ta=-40~+85℃)

| Parameter | Symbol | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| SK frequency | $f_{SK}$ | - | - | 3 | MHz |
| SK high time | $t_{SKH}$ | 100 | - | - | ns |
| SK low time | $t_{SKL}$ | 100 | - | - | ns |
| CS low time | $t_{CS}$ | 200 | - | - | ns |
| CS setup time | $t_{CSS}$ | 50 | - | - | ns |
| DI setup time | $t_{DIS}$ | 50 | - | - | ns |
| CS hold time | $t_{CSH}$ | 0 | - | - | ns |
| DI hold time | $t_{DIH}$ | 50 | - | - | ns |
| Data “1” output delay | $t_{PD1}$ | - | - | 200 | ns |
| Data “0” output delay | $t_{PD0}$ | - | - | 200 | ns |
| Time from CS to output establishment | $t_{SV}$ | - | - | 150 | ns |
| Time from CS to High-Z | $t_{DF}$ | - | - | 100 | ns |
| Write cycle time | $t_{E/W}$ | - | - | 5 | ms |


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## ●Serial input / output timing

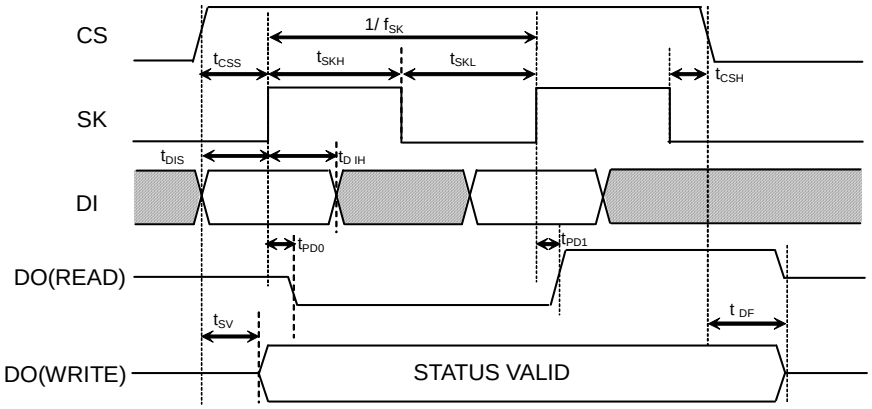


Figure 1. Sync data input / output timing

○Data is taken by DI sync with the rise of SK.
○At read operation, data is output from DO in sync with the rise of SK.
○The STATUS signal at write (READY / BUSY) is output after $t_{CS}$ from the fall of CS after write command input, at the area DO where CS is high, and valid until the next command start bit is input. And, while CS is low, DO becomes High-Z.
○After completion of each mode execution, set CS low once for internal circuit reset, and execute the following operation mode.
○$1/f_{SK}$ is the SK clock cycle, even if $f_{SK}$ is maximum, the SK clock cycle can't be $t_{SKH}$(Min.)+$t_{SKL}$(Min.)
○For "Write cycle time $t_{E/W}$", please see Figure 36,37,39,40.
○For "CS low time $t_{CS}$", please see Figure 36,37,39,40.

## ●Block diagram

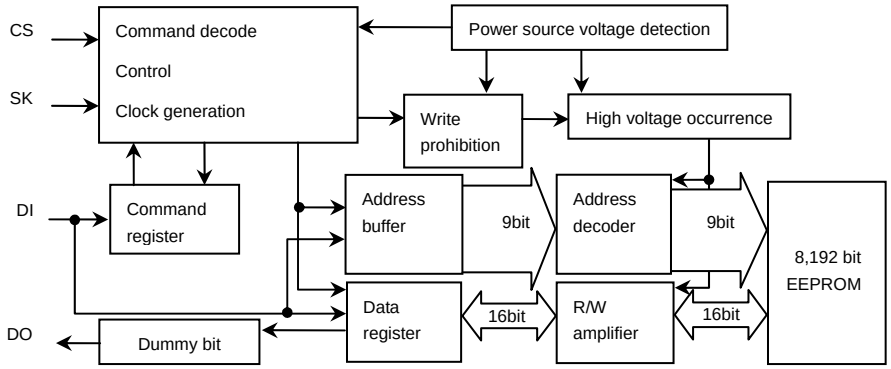


Figure 2. Block diagram


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## ●Pin Configuration

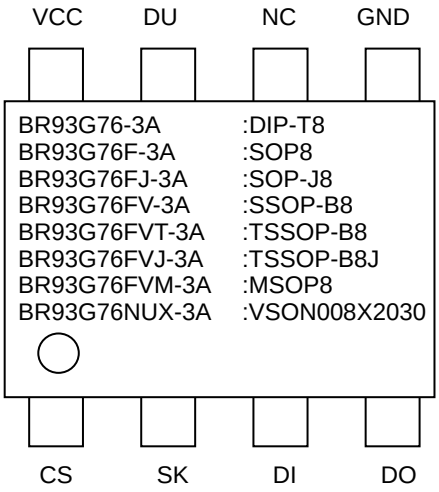


Figure 3. Pin Configuration

## ●Pin Descriptions

| Pin name | I / O | Function |
|---|---|---|
| CS | Input | Chip select input |
| SK | Input | Serial clock input |
| DI | Input | Start bit, ope code, address, and serial data input |
| DO | Output | Serial data output, READY / $\overline{\text{BUSY}}$ STATUS display output |
| GND | - | All input / output reference voltage, 0V |
| NC | - | Non connected terminal*1 |
| DU | - | Don't use terminal*1 |
| VCC | - | Supply voltage |

*1 Terminals not used may be set to any of high,low, and OPEN


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●**Typical Performance Curves**

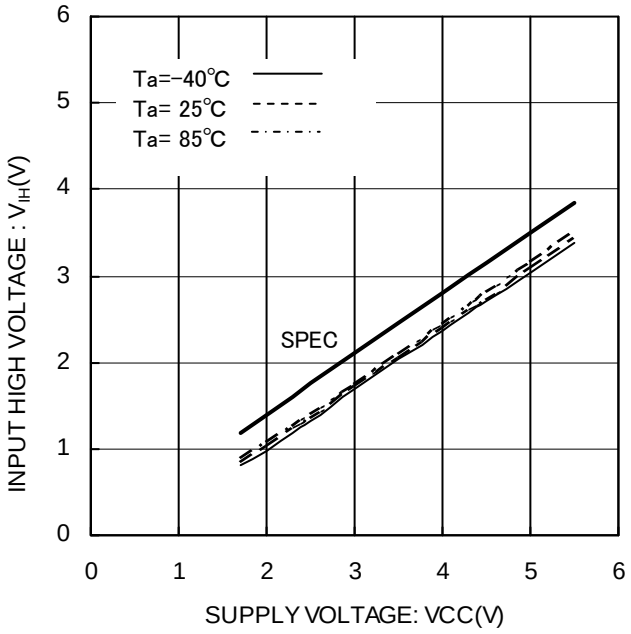


Figure 4. Input high voltage $V_{IH}$(CS,SK,DI)

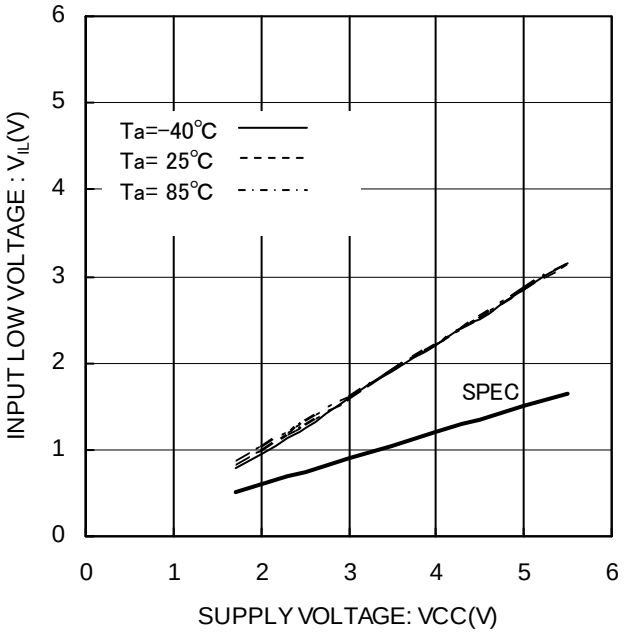


Figure 5. Input low voltage $V_{IL}$(CS,SK,DI)

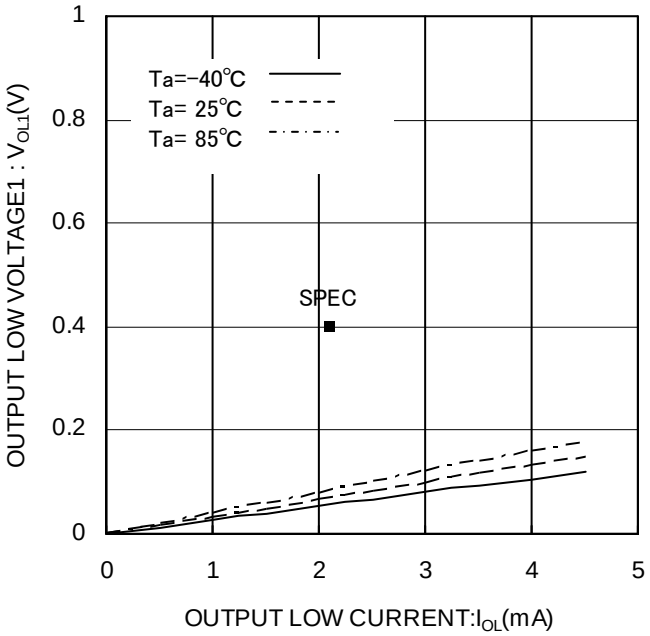


Figure 6. Output low voltage1 $V_{OL1}$(VCC=2.7V)

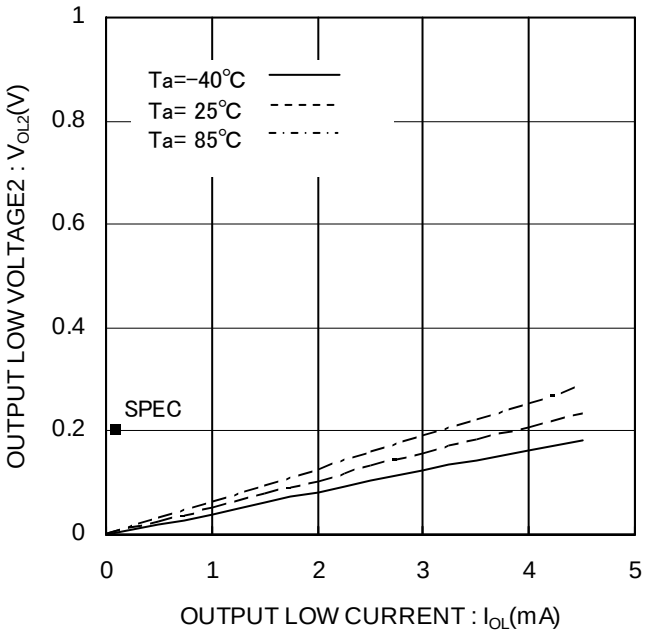


Figure 7. Output low voltage2 $V_{OL2}$(VCC=1.7V)


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●**Typical Performance Curves - Continued**

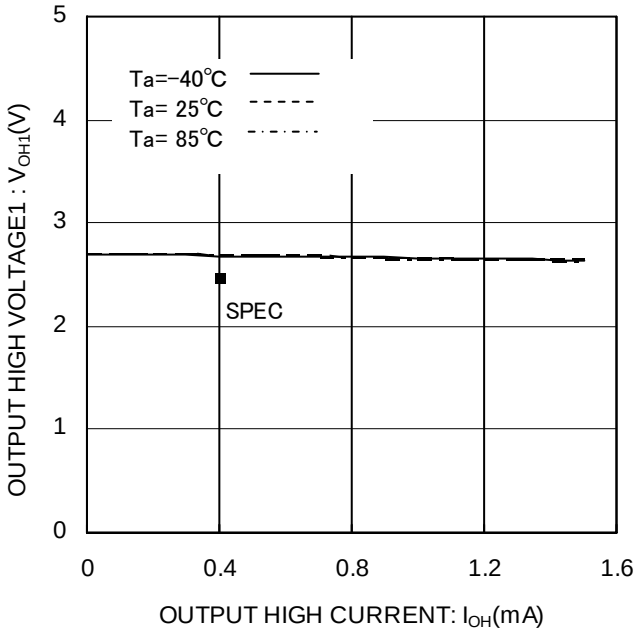


Figure 8. Output high voltage1 $V_{OH1}$(VCC=2.7V)

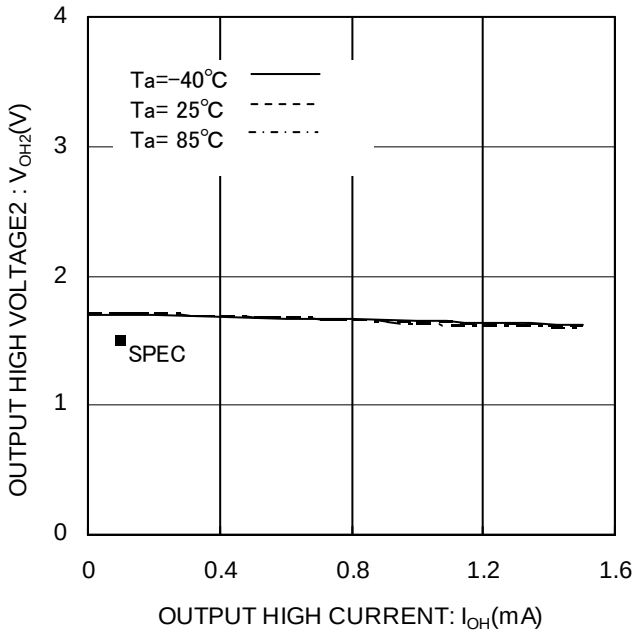


Figure 9. Output high voltage2 $V_{OH2}$(VCC=1.7V)

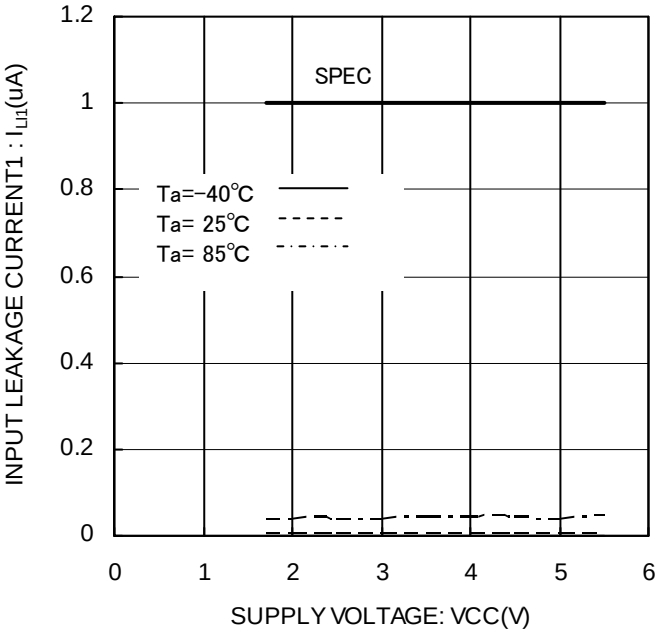


Figure 10. Input leakage current1 $I_{LI1}$ (CS)

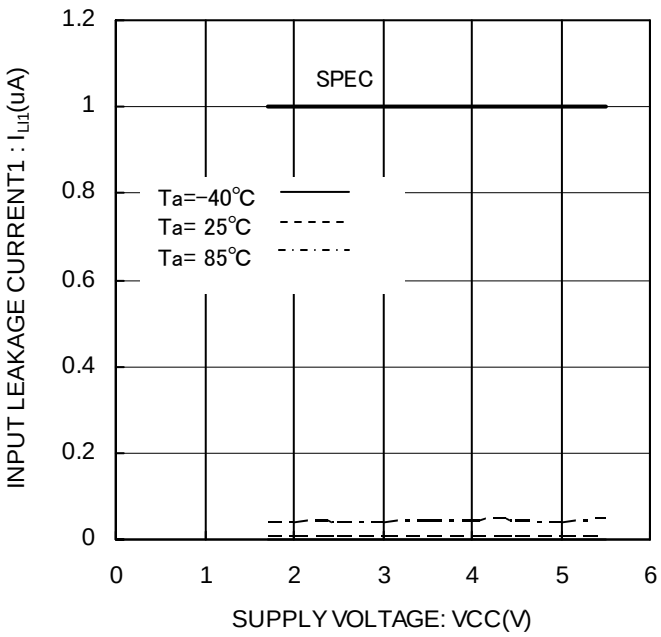


Figure 11. Input leakage current1 $I_{LI1}$(SK)


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●**Typical Performance Curves - Continued**

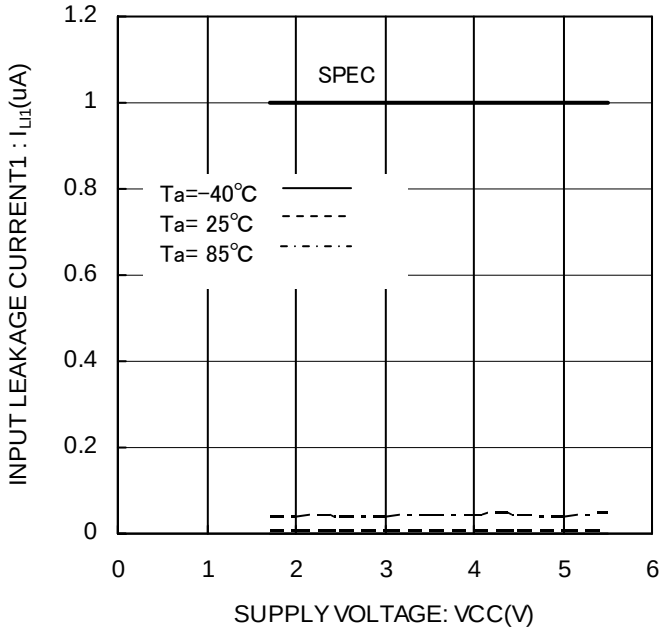


Figure 12. Input leakage current1 $I_{LI1}$(DI)

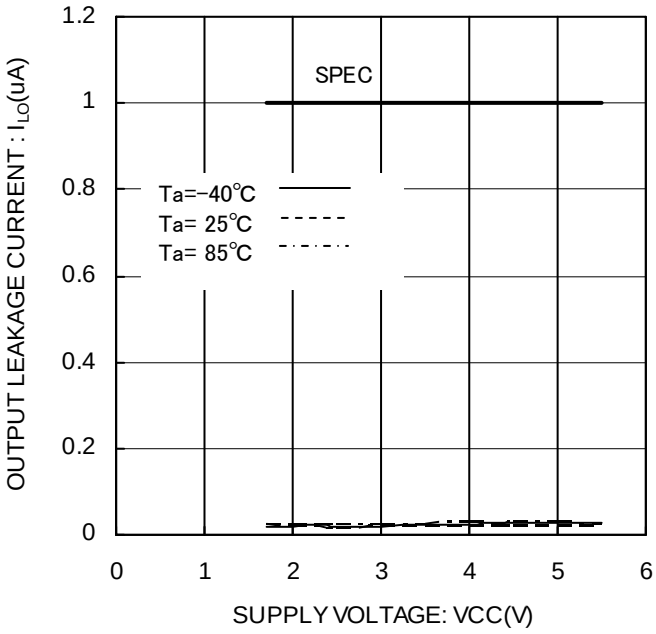


Figure 13. Output leakage current $I_{LO}$(DO)

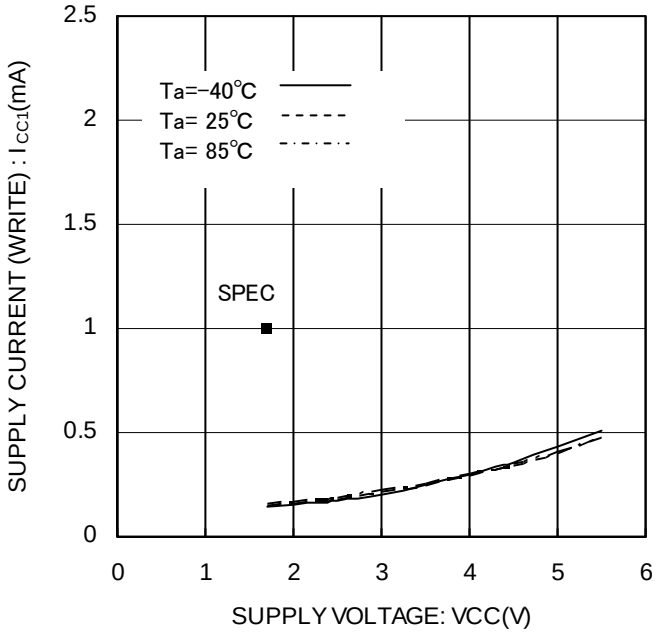


Figure 14. Supply current (WRITE)
$I_{CC1}$(WRITE, $f_{SK}$=1MHz)

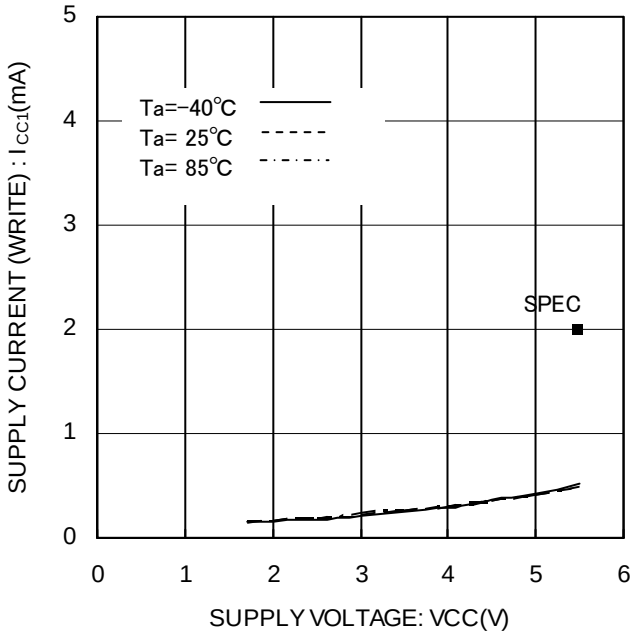


Figure 15. Supply current (WRITE)
$I_{CC1}$(WRITE,$f_{SK}$=3MHz)


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●**Typical Performance Curves - Continued**

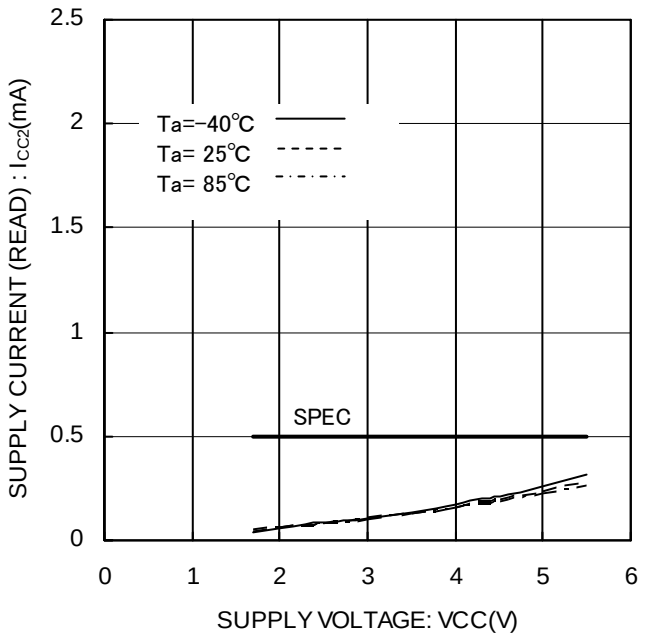


Figure 16. Supply current (READ)
$I_{CC2}$(READ,$f_{SK}$=1MHz).

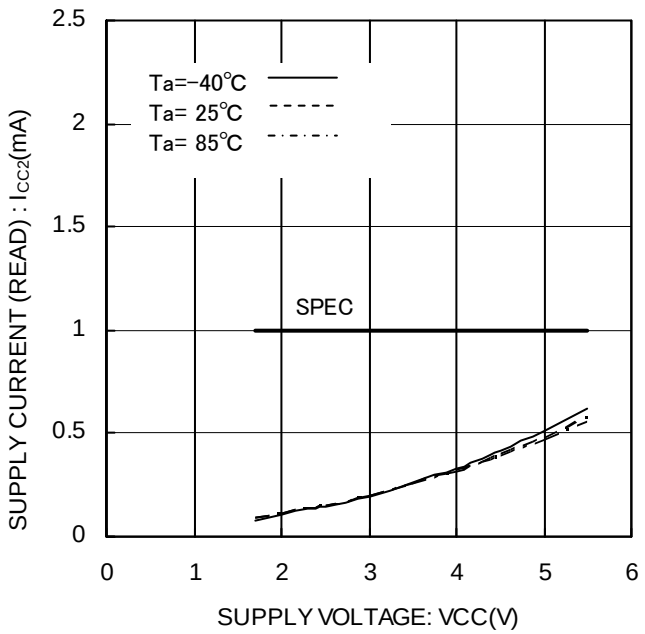


Figure 17. Supply current (READ)
$I_{CC2}$(READ,$f_{SK}$=3MHz)

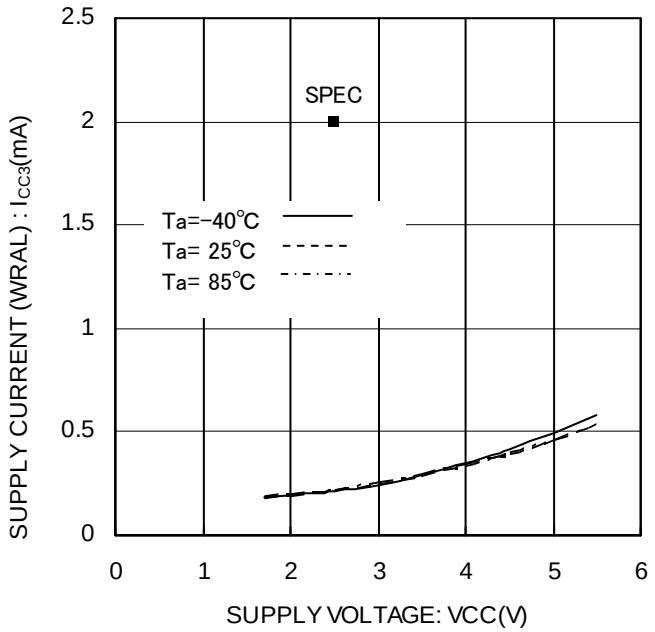


Figure 18. Supply current (WRAL)
$I_{CC3}$(WRAL,$f_{SK}$=1MHz)

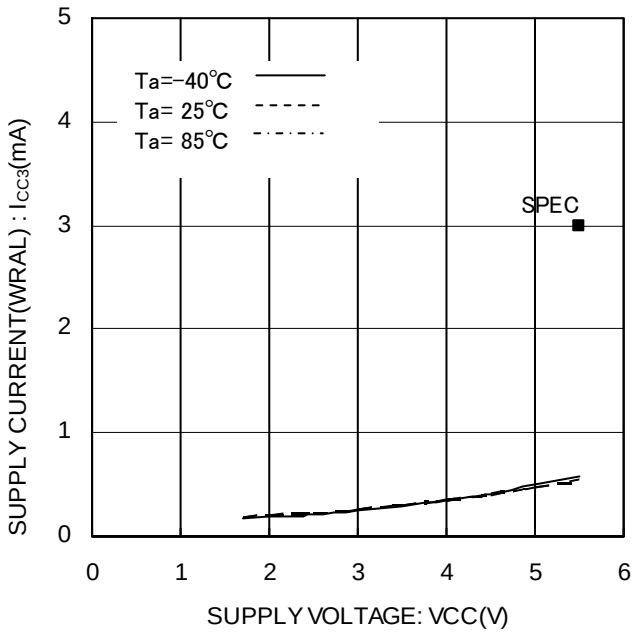


Figure 19. Supply current (WRAL)
$I_{CC3}$(WRAL,$f_{SK}$=3MHz)


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●**Typical Performance Curves - Continued**

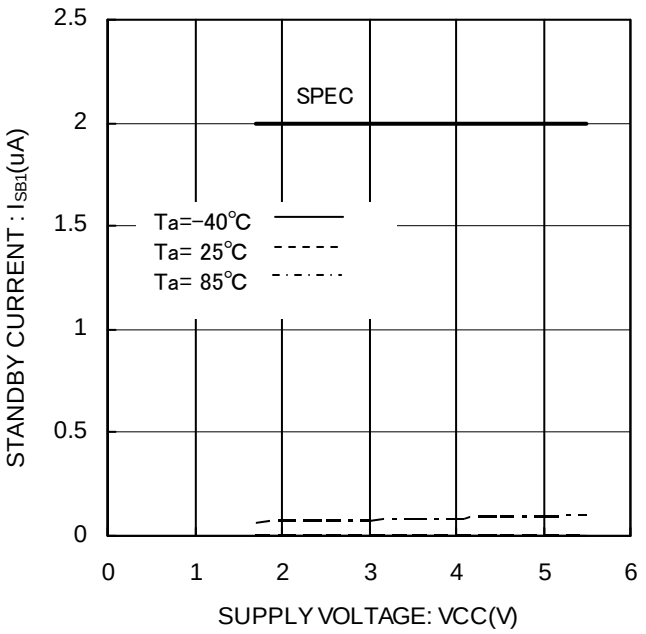


Figure 20. Standby current $I_{SB1}$(CS=0V)

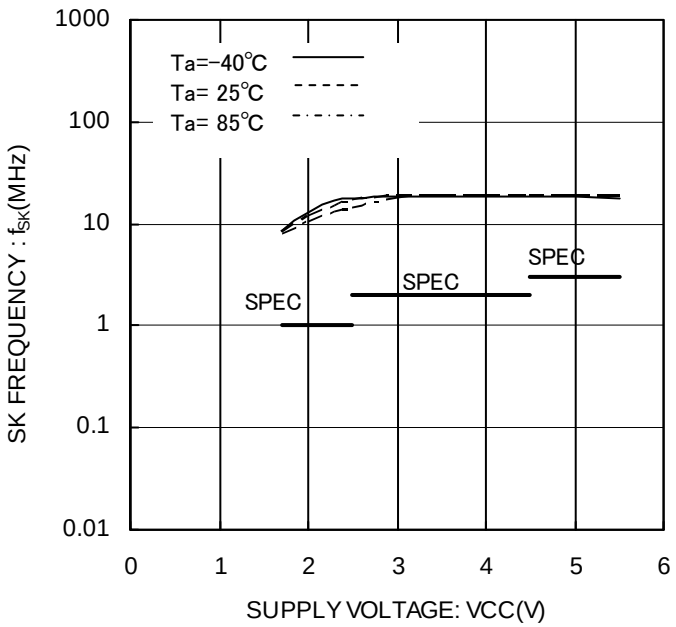


Figure 21. SK frequency $f_{SK}$

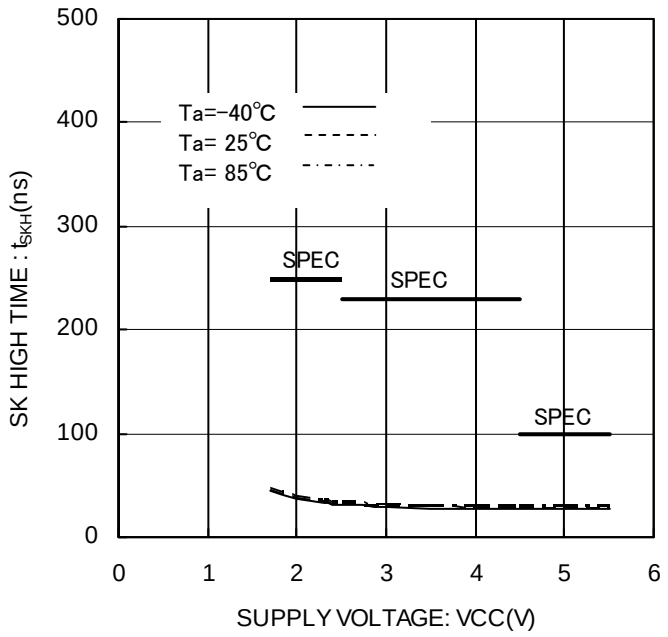


Figure 22. SK high time $t_{SKH}$

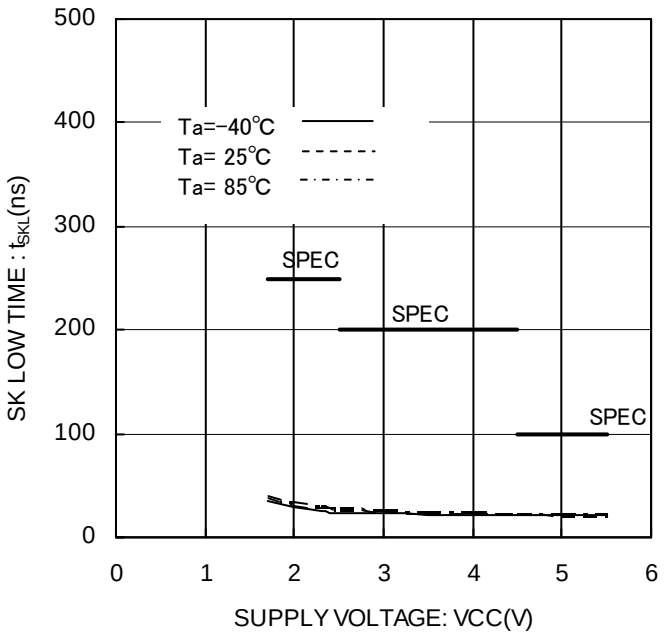


Figure 23. SK low time $t_{SKL}$


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●**Typical Performance Curves - Continued**

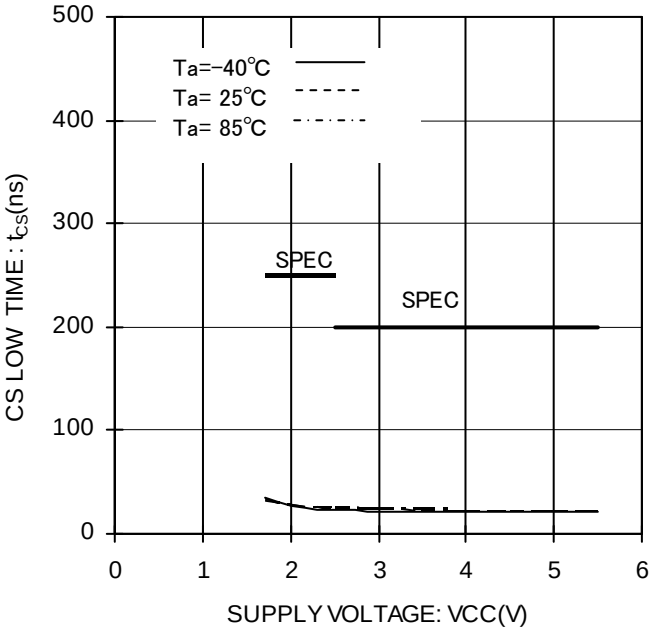


Figure 24. CS low time $t_{CS}$

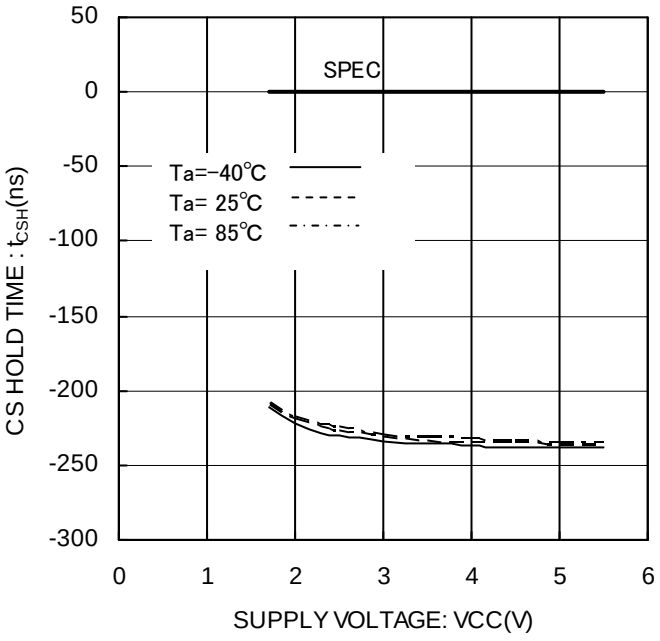


Figure 25. CS hold time $t_{CSH}$

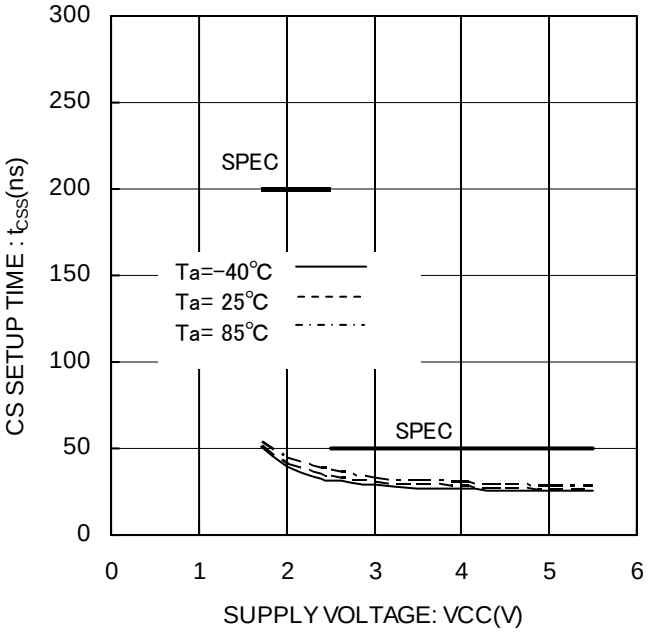


Figure 26. CS setup time $t_{CSS}$

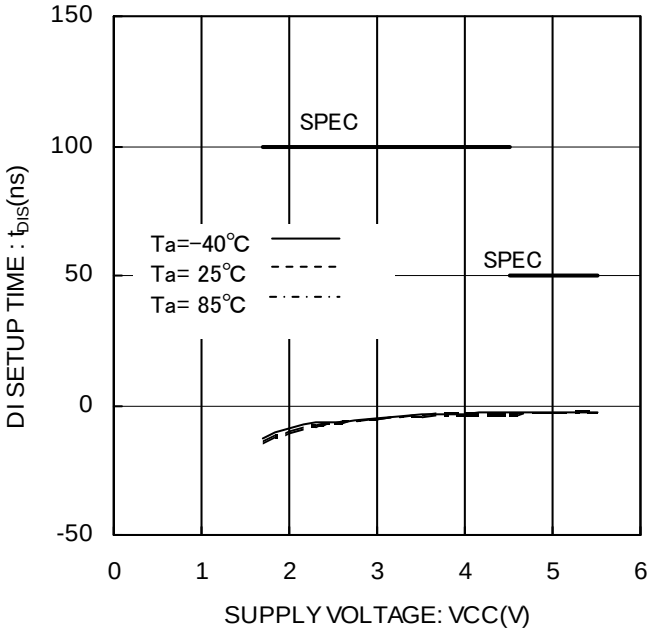


Figure 27. DI setup time $t_{DIS}$


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●**Typical Performance Curves - Continued**

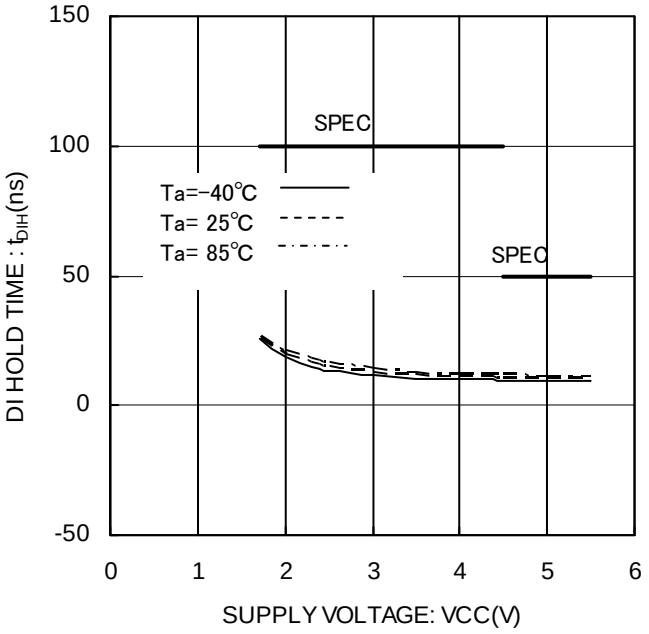


Figure 28. DI hold time $t_{DIH}$

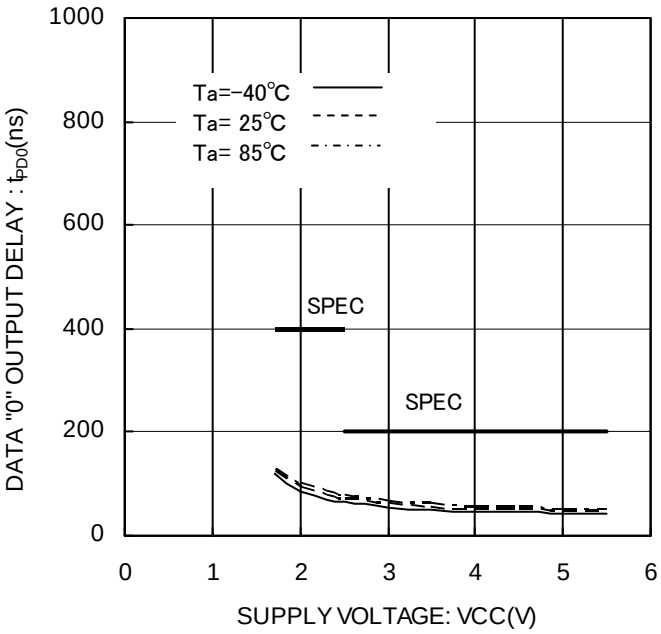


Figure 29. Data "0" output delay $t_{PD0}$

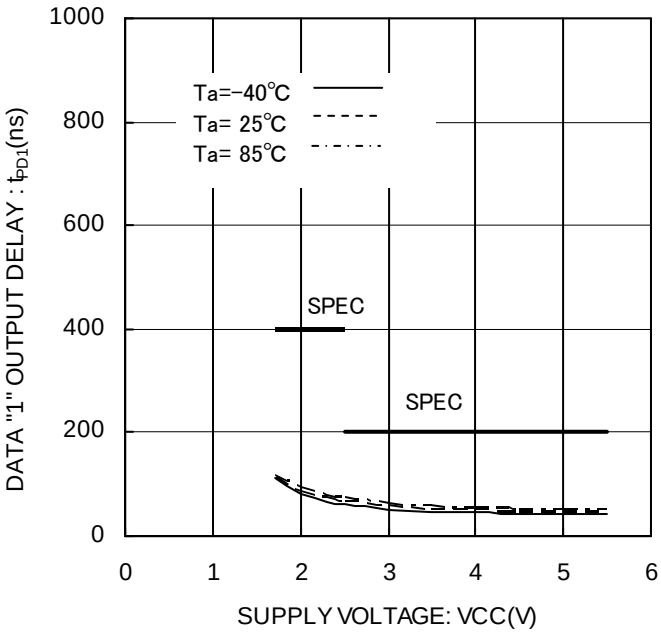


Figure 30. Data "1" output delay $t_{PD1}$

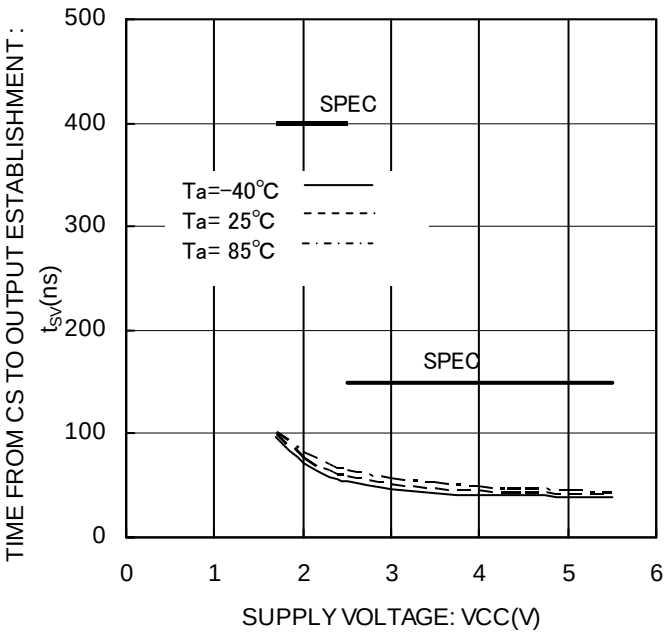


Figure 31. Time from CS to output establishment $t_{SV}$


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●**Typical Performance Curves - Continued**

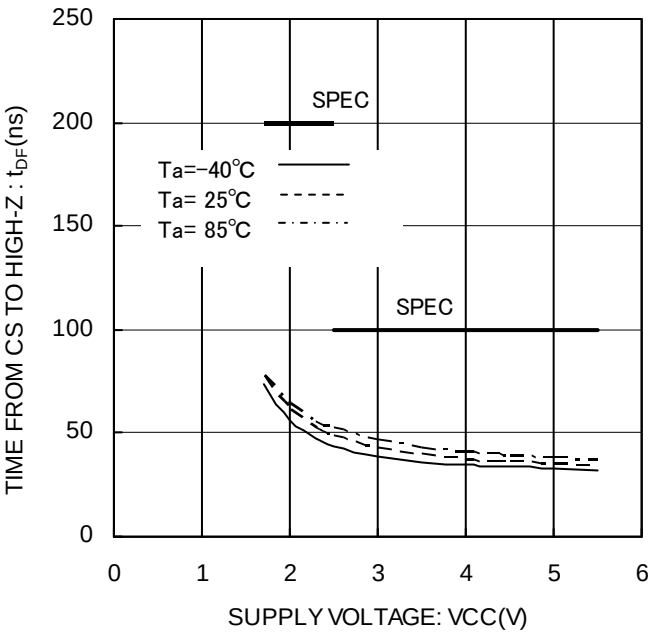


Figure 32. Time from CS to High-Z $t_{DF}$

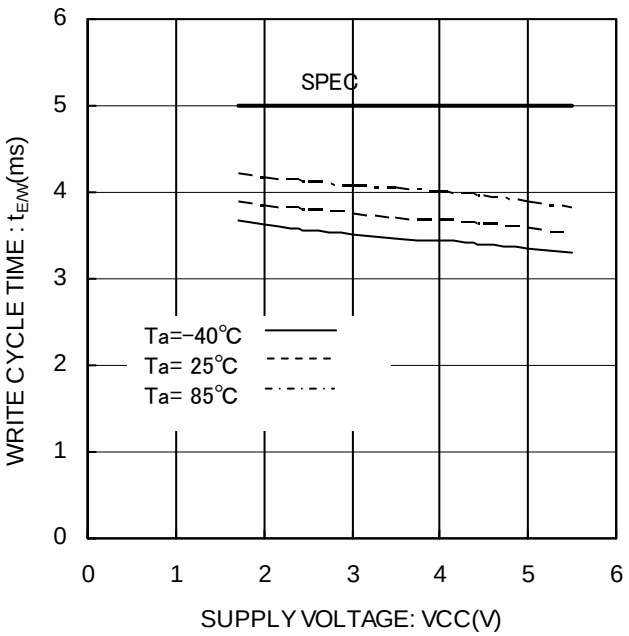


Figure 33. Write cycle time $t_{E/W}$


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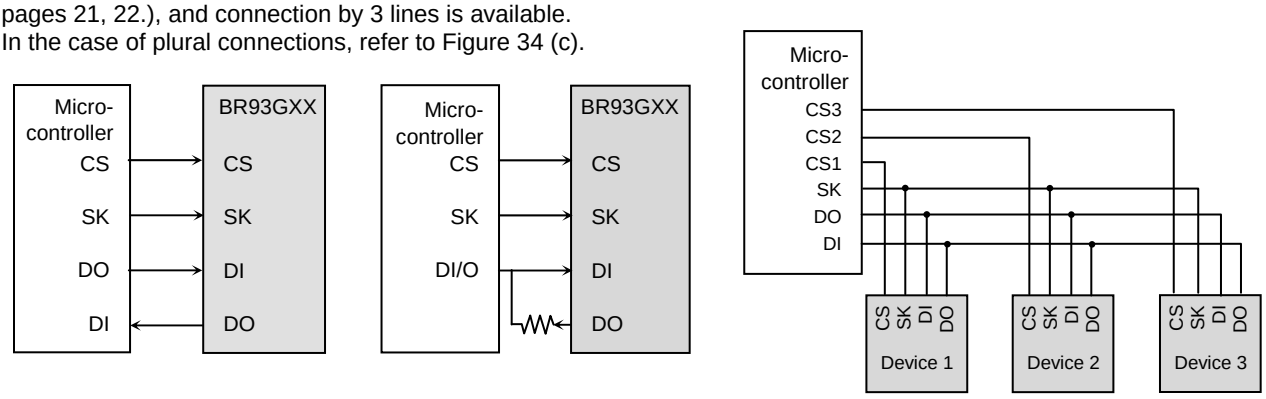
## ●Description of operations

Communications of the MicroWire BUS are carried out by SK (serial clock), DI (serial data input),DO (serial data output) ,and CS (chip select) for device selection.
When to connect one EEPROM to a microcontroller, connect it as shown in Figure 34(a) or Figure 34(b). When to use the input and output common I/O port of the microcontroller, connect DI and DO via a resistor as shown in Figure 34(b) (Refer to pages 21, 22.), and connection by 3 lines is available.
In the case of plural connections, refer to Figure 34 (c).




(a). Connection by 4 lines (b). Connection by 3 lines (c). Connection example of plural devices

Figure 34. Connection method with microcontroller

Communications of the MicroWire BUS are started by the first “1” input after the rise of CS. This input is called a start bit. After input of the start bit, input ope code, address and data. Address and data are input all in MSB first manners.
“0” input after the rise of CS to the start bit input is all ignored. Therefore, when there is limitation in the bit width of PIO of the microcontroller, input “0” before the start bit input, to control the bit width.

## ●Command mode

| Command | Start bit | Ope code | Address<br>BR93G76-3<br>MSB of Address(Am) is A9 | Data<br>MSB of Data(Dx) is D15 | Required clocks(n) |
|---|---|---|---|---|---|
| Read (READ) *1 | 1 | 10 | A9,A8,A7,A6,A5,A4,A3,A2,A1,A0 | D15~D0(READ DATA) | BR93G76-3:n=29 |
| Write enable (WEN) | 1 | 00 | 1 1 * * * * * * * * | | BR93G76-3:n=13 |
| Write disable (WDS) | 1 | 00 | 0 0 * * * * * * * * | | |
| Write (WRITE) *2 | 1 | 01 | A9,A8,A7,A6,A5,A4,A3,A2,A1,A0 | D15~D0(WRITE DATA) | BR93G76-3:n=29 |
| Write all (WRAL) *2 | 1 | 00 | 0 1 * * * * * * * * | D15~D0(WRITE DATA) | |
| Erase (ERASE) | 1 | 11 | A9,A8,A7,A6,A5,A4,A3,A2,A1,A0 | | BR93G76-3:n=13 |
| Erase all (ERAL) | 1 | 00 | 1 0 * * * * * * * * | | |

A9 of BR93G76 becomes Don't Care.

- Input the address and the data in MSB first manners.
- As for *, input either “1” or “0” .

*Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit.
The start bit means the first “1” input after the rise of CS.

*1 As for read, by continuous SK clock input after setting the read command, data output of the set address starts, and address data in significant order are sequentially output continuously. (Auto increment function)
*2 For write or write all commands, an internal erase or erase all is included and no separate erase or erase all is needed before write or write all command.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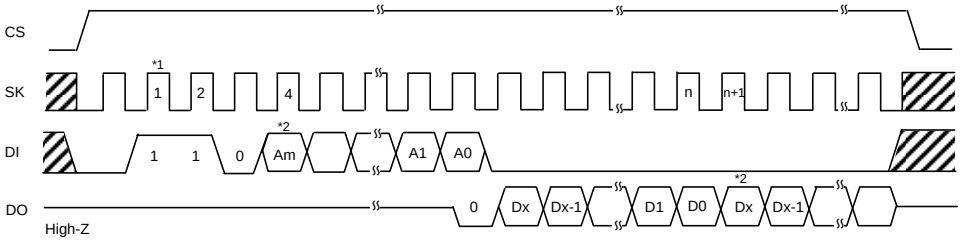
## ●Timing chart

1) Read cycle (READ)



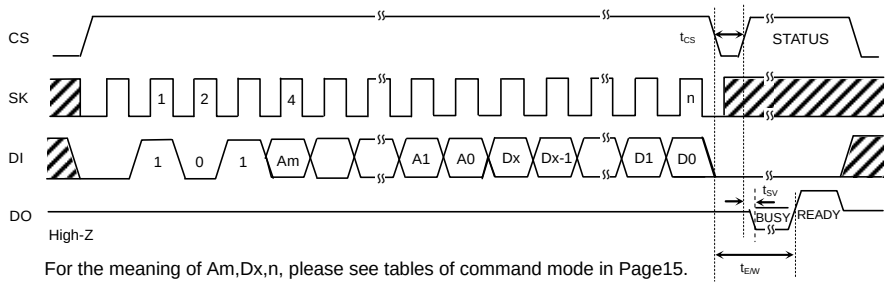

Am: MSB of address
Dx: MSB of data
n: required clocks

*1 Start bit
When data "1" is input for the first time after the rise of CS, this is recognized as a start bit. And when "1" is input after plural "0" are input, it is recognized as a start bit, and the following operation is started. This is common to all the commands to described hereafter.
*2 For the meaning of Am,Dx,n,please see tables of command mode in Page15. For example, Am=A9,Dx=D15,n=29.

Figure 35. Read cycle

○When the read command is recognized, input address data (16bit) is output to serial. And at that moment, at taking A0, in sync with the rise of SK, "0" (dummy bit) is output. And, the following data is output in sync with the rise of SK.
This IC has an address auto increment function which is valid only at read command. This is the function where after the above read execution, by continuously inputting SK clock, the above address data is read sequentially. And, during the auto increment, keep CS at high.

2) Write cycle (WRITE)



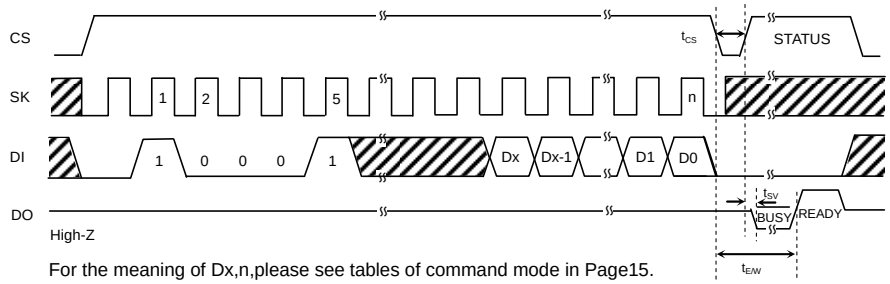

Am: MSB of address
Dx: MSB of data
n: required clocks

For the meaning of Am,Dx,n, please see tables of command mode in Page15.

Figure 36. Write cycle

○In this command, input 16bit data are written to designated addresses (Am~A0). The actual write starts by the fall of CS of D0 taken SK clock.
When STATUS is not detected (CS=low fixed),make sure Max 5ms time is in comforming with $t_{E/W}$.
When STATUS is detected (CS=high), all commands are not accepted for areas where low ($\overline{BUSY}$) is output from DO, therefore, do not input any command.

3) Write all cycyle (WRAL)




Dx: MSB of data
n: required clocks

For the meaning of Dx,n,please see tables of command mode in Page15.

Figure 37. Write all cycle

○In this command, input 16bit data is written simultaneously to all adresses. Data is not written continuously per one word but is written in bulk, the write time is only Max. 5ms in conformity with $t_{E/W}$.
In WRAL, STATUS can be detected in the same manner as in WRITE command.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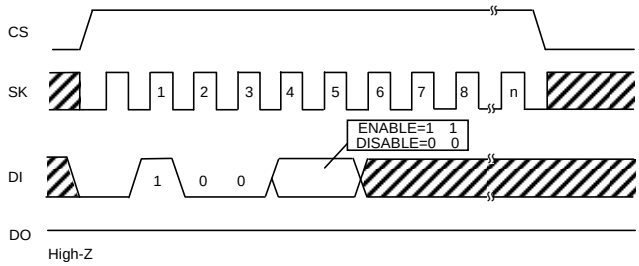
4) Write enable (WEN) / disable (WDS) cycle




n: required clocks

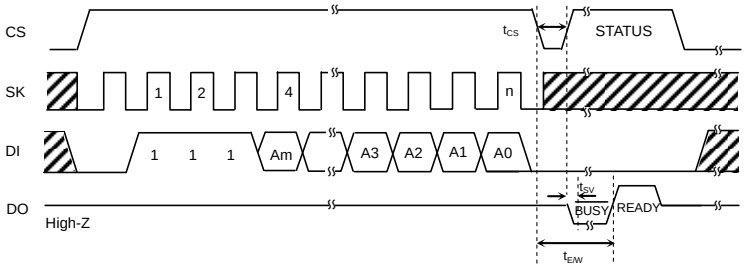
For the meaning of n,please see tables of command mode in Page15.

Figure 38. Write enable (WEN) / disable (WDS) cycle

○At power on, this IC is in write disable status by the internal RESET circuit. Before executing the write command, it is necessary to execute the write enable command. And, once this command is executed, it is valid unitl the write disable command is executed or the power is turned off. However, the read command is valid irrespective of write enable / diable command. Input to SK after 6 clocks of this command is available by either “1” or “0”, but be sure to input it.

○When the write enable command is executed after power on, write enable status gets in. When the write disable command is executed then, the IC gets in write disable status as same as at power on, and then the write command is canceled thereafter in software manner. However, the read command is executable. In write enable status, even when the write command is input by mistake, write is started. To prevent such a mistake, it is recommended to execute the write disable command after completion of write.

5) Erase cycle (ERASE)



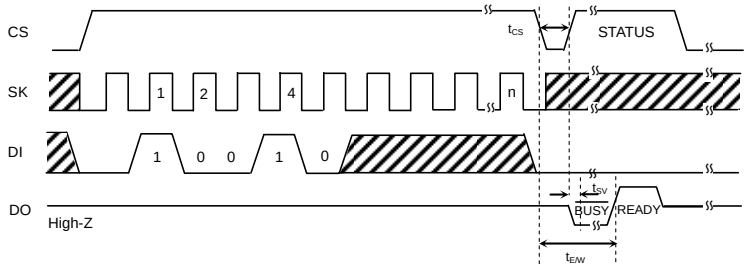

Am: MSB of address
n: required clocks

For the meaning of Am,n,please see tables of command mode in Page15.

Figure 39. Erase cycle

○In this command, data of the designated address is made into “1”. The data of the designated address becomes “FFFFh”.
Actual ERASE starts at the fall of CS after the fall of A0 taken SK clock.
In ERASE, STATUS can be detected in the same manner as in WRITE command.

6) Erase all cycle (ERAL)




n: required clocks

For the meaning of n,please see tables of command mode in Page15.

Figure 40. Erase all cycle

○In this command, data of all addresses is made into “1”. Data of all addresses becomes ”FFFFh”.
Actual ERASE starts at the fall of CS after the falll of the n-th clock from the start bit input.
In ERAL, STATUS can be detected in the same manner as in WRAL command.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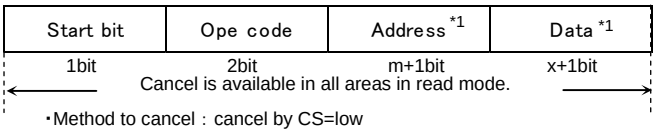
## ●Application

1)Method to cancel each command

○READ

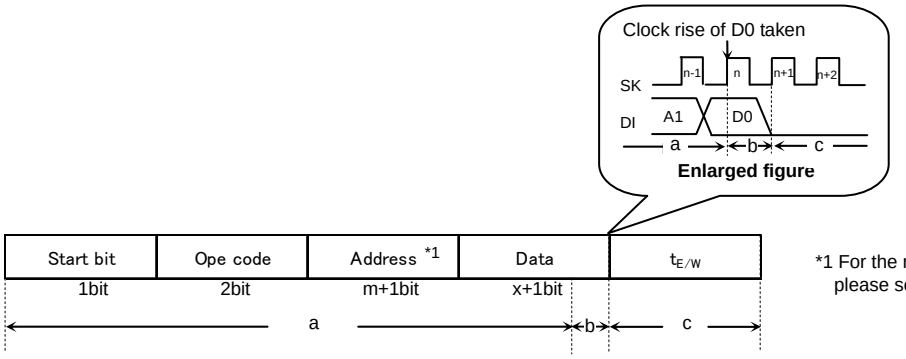



*1 For the meaning of m,x, please see tables of command mode in Page15

・Method to cancel : cancel by CS=low

Figure 41. READ cancel available timing

○WRITE,WRAL




*1 For the meaning of m,n,x, please see tables of command mode in Page15

a : From start bit to the clock rise of D0 taken
Cancel by CS=low

b : The clock rise of D0 taken and after
Cancellation is not available by any means.

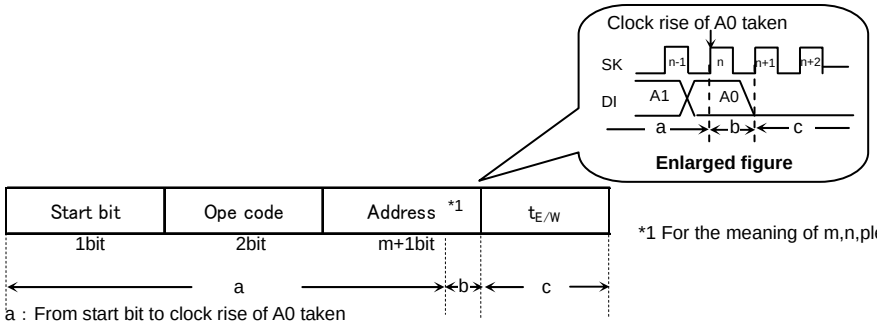
c : n+1 clock rise and after
Cancel by CS=low
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is output continuously cancel function is not available.

Note 1) If VCC is made OFF in this area, designated address data is not guaranteed, therefore write once again is suggested.

Note 2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes unstable, therefore, it is recommended to fall in SK=low area.
As for SK rise, recommend timing of $t_{CSS}/t_{CSH}$ or higher.

Figure 42. WRITE, WRAL cancel available timing

○ERASE, ERAL




*1 For the meaning of m,n,please see tables of command mode in Page15

a : From start bit to clock rise of A0 taken
Cancel by CS=low

b : Clock rise of A0 taken
Cancellation is not available by any means.

c : n+1 clock rise and after
Cancel by CS=low
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is output continuously cancel function is not available.

Note 1) If VCC is made OFF in this area, designated address data is not guaranteed, therefore write once again is suggested.

Note 2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes unstable, therefore, it is recommended to fall in SK=low area.
As for SK rise, recommend timing of $t_{CSS}/t_{CSH}$ or higher.

Figure 43. ERASE, ERAL cancel available timing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2) At standby

When CS is low , even if SK,DI,DO are low,high or with middle electric potential, current does not over $I_{SB1}$ Max.

3) I/O peripheral circuit

3-1) Pull down CS.

By making CS=low at power ON/OFF, mistake in operation and mistake write are prevented.

○Pull down resistance Rcs of CS pin

To prevent mistake in operation and mistake write at power ON/OFF, CS pull down resistance is necessary. Select an appropriate value to this resistance value from microcontroller $V_{OH}$, $I_{OH}$, and $V_{IL}$ characteristics of this IC.

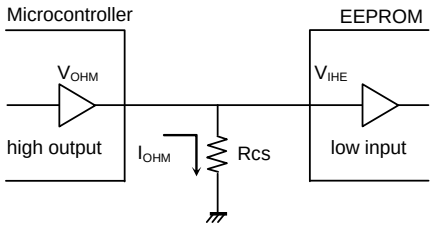


Figure 44. CS pull down resistance

$$Rcs \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ①$$

$$V_{OHM} \geqq V_{IHE} \quad \cdots ②$$

Example) When VCC =5V, $V_{IHE}$=2V, $V_{OHM}$=2.4V, $I_{OHM}$=2mA, from the equation ①,

$$Rcs \geqq \frac{2.4}{2 \times 10^{-3}}$$

$$\therefore \quad Rcs \geqq 1.2\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, $V_{OHM}$ becomes 2.4V or higher, and $V_{IHE}$ (=2.0V), the equation ② is also satisfied.

- $V_{IHE}$ : EEPROM VIH specifications
- $V_{OHM}$ : Microcontroller $V_{OH}$ specifications
- $I_{OHM}$ : Microcontroller $I_{OH}$ specifications

3-2) DO is available in both pull up and pull down.

Do output always is High-Z except in READY / $\overline{\text{BUSY}}$ STATUS and data output in read command.
Malfunction may occur when High-Z is input to the microcontroller port connected to DO, it is necessary to pull down and pull up DO. When there is no influence upon the microcontroller operations, DO may be OPEN.
If DO is OPEN, and at timing to output STATUS READY, at timing of CS=high, SK=high, DI=high, EEPROM recognizes this as a start bit, resets READY output, and DO=High-Z, therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

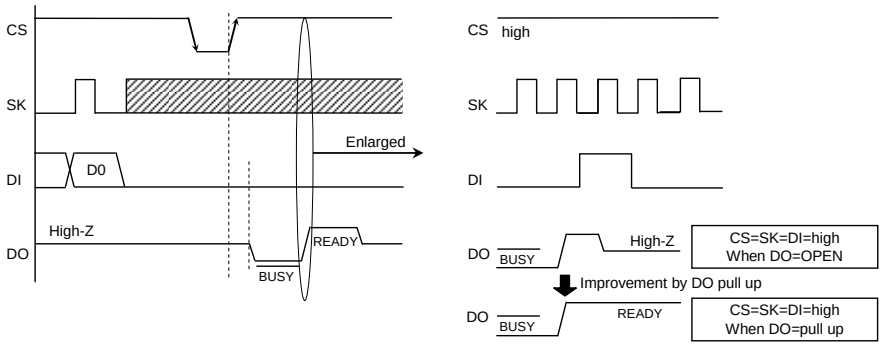


Figure 45. READY output timing at DO=OPEN


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○Pull up resistance Rpu and pull down resistance Rpd of DO pin

As for pull up and pull down resistance value, select an appropriate value to this resistance value from microcontroller $V_{IH}$, $V_{IL}$, and $V_{OH}$, $I_{OH}$, $V_{OL}$, $I_{OL}$ characteristics of this IC.

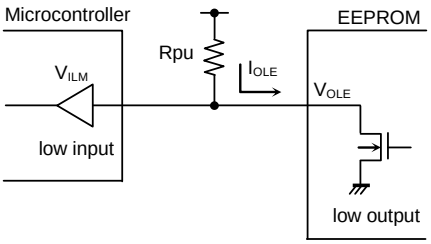


Figure 46. DO pull up resistance

$$Rpu \geqq \frac{VCC - V_{OLE}}{I_{OLE}} \quad \cdot\cdot\cdot ③$$

$$V_{OLE} \leqq V_{ILM} \quad \cdot\cdot\cdot ④$$

Example) When VCC =5V, $V_{OLE}$=0.4V, $I_{OLE}$=2.1mA, $V_{ILM}$=0.8V, from the equation ③,

$$Rpu \geqq \frac{5-0.4}{2.1\times10^{-3}}$$

$$\therefore \quad Rpu \geqq 2.2\ [k\Omega]$$

With the value of Rpu to satisfy the above equation, $V_{OLE}$ becomes 0.4V or below, and with $V_{ILM}$(=0.8V), the equation ④ is also satisfied.

- $V_{OLE}$ : EEPROM $V_{OL}$ specifications
- $I_{OLE}$ : EEPROM $I_{OL}$ specifications
- $V_{ILM}$ : Microcontroller $V_{IL}$ specifications

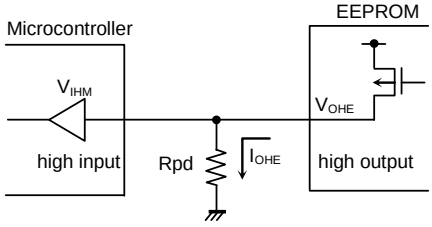


Figure 47. DO pull down resistance

$$Rpd \geqq \frac{V_{OHE}}{I_{OHE}} \quad \cdot\cdot\cdot ⑤$$

$$V_{OHE} \geqq V_{IHM} \quad \cdot\cdot\cdot ⑥$$

Example) When VCC =5V, $V_{OHE}$=VCC－0.2V, $I_{OHE}$=0.1mA, $V_{IHM}$=VCC×0.7V from the equation ⑤,

$$Rpd \geqq \frac{5-0.2}{0.1\times10^{-3}}$$

$$\therefore \quad Rpd \geqq 48\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, $V_{OHE}$ becomes 2.4V or below, and with $V_{IHM}$ (=3.5V), the equation ⑥ is also satisfied.

- $V_{OHE}$ : EEPROM $V_{OH}$ specifications
- $I_{OHE}$ : EEPROM $I_{OH}$ specifications
- $V_{IHM}$ : Microcontroller $V_{IH}$ specifications

○READY / $\overline{BUSY}$ STATUS display (DO terminal)

This display outputs the internal STATUS signal. When CS is started after $t_{CS}$ from CS fall after write command input, high or low is output.

R/$\overline{B}$ display =low ($\overline{BUSY}$) = write under execution
(DO STATUS) After the timer circuit in the IC works and creates the period of $t_{E/W}$, this timer circuit completes automatically. And the memory cell is written in the period of $t_{E/W}$, and during this period, other command is not accepted.

R/$\overline{B}$ display = high (READY) = command wait STATUS
(DO STATUS) After $t_{E/W}$ (max.5ms) the following command is accepted.
Therefore, CS=high in the period of $t_{E/W}$, and If signals are input in SK, DI, malfunction may occur, therefore, DI=low in the area
CS=high. (Especially, in the case of shared input port, attention is required.)

*Do not input any command while STATUS signal is output. Command input in $\overline{BUSY}$ area is cancelled, but command input in READY area is accepted. Therefore, STATUS READY output is cancelled, and malfunction and mistake write may occur.

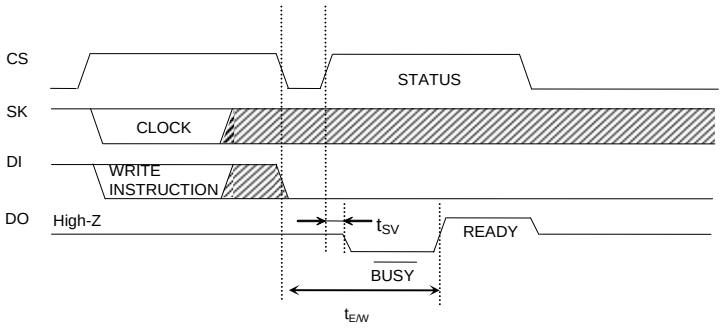


Figure 48. READY/$\overline{BUSY}$ STATUS output timing chart


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4) When to directly connect DI and DO

This IC has independent input terminal DI and output terminal DO, and separate signals are handled on timing chart, meanwhile, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by 1 control line.

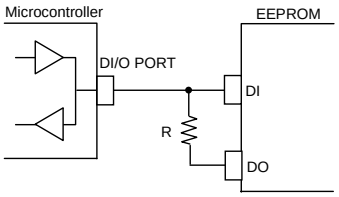



Figure 49. DI, DO control line common connection

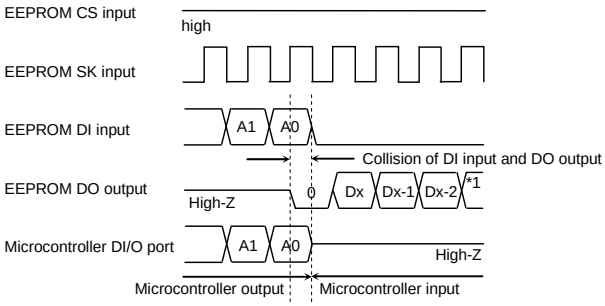
○Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input of EEPROM.

Drive from the microcontroller DI/O output to DI input of EEPROM on I/O timing, and output signal from DO output of EEPROM occur at the same time in the following points.

4-1) 1 clock cycle to take in A0 address data at read command

Dummy bit “0” is output to DO terminal.

→When address data A0 = “1” input, through current route occurs.




*1 X=15,for the meaning of x ,
please see tables of command mode in Page15.

Figure 50. Collision timing at read data output at DI, DO direct connection

4-2) Timing of CS = high after write command. DO terminal in READY / $\overline{\text{BUSY}}$ function output.

When the next start bit input is recognized, High-Z gets in.

→Especially, at command input after write, when CS input is started with microcontroller DI/O output low, READY output high is output from DO terminal, and through current route occurs.

Feedback input at timing of these (4-1) and (4-2) does not cause disorder in basic operations, if resistance R is inserted.

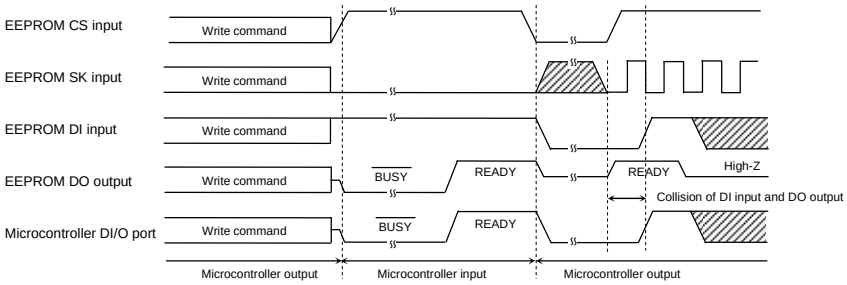



Figure 51. Collision timing at DI, DO direct connection

Note) As for the case (4-2), attention must be paid to the following.

When STATUS READY is output, DO and DI are shared, DI=high and the microcontroller DI/O=High-Z or the microcontroller DI/O=high,if SK clock is input, DO output is input to DI and is recognized as a start bit, and malfunction may occur. As a method to avoid malfunction, at STATUS READY output, set SK=low, or start CS within 4 clocks after high of READY signal is output.

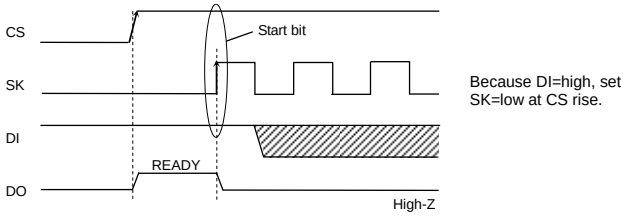



Figure.52 Start bit input timing at DI, DO direct connection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○Selection of resistance value R

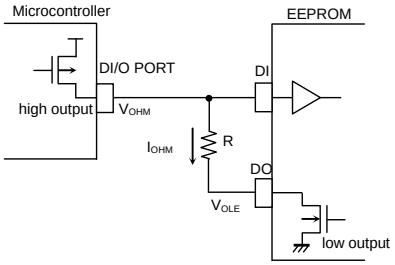
The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current amount in consideration of impedance and so forth of power source line in set. And insert resistance R, and set the value R to satisfy EEPROM input level $V_{IH}/V_{IL}$ even under influence of voltage decline owing to leak current and so forth. Insertion of R will not cause any influence upon basic operations.

4-3) Address data A0 = “1” input, dummy bit “0” output timing

(When microcontroller DI/O output is high, EEPROM DO outputs low, and high is input to DI)

・Make the through current to EEPROM 10mA or below.

・See to it that the level $V_{IH}$ of EEPROM should satisfy the following.




Conditions

$$V_{IHE} \leqq I_{OHM} \times R + V_{OLE}$$

At this moment, if $V_{OLE}$=0V,

$$V_{IHE} \leqq I_{OHM} \times R$$

$$\therefore \quad R \geqq \frac{V_{IHE}}{I_{OHM}} \quad \cdots ⑦$$

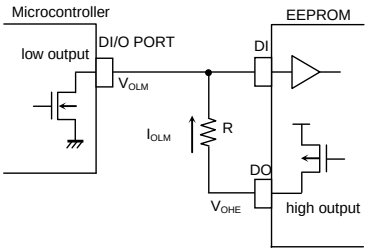
・$V_{IHE}$ : EEPROM $V_{IH}$ specifications
・$V_{OLE}$ : EEPROM $V_{OL}$ specifications
・$I_{OHM}$ : Microcontroller $I_{OH}$ specifications

Figure 53. Circuit at DI, DO direct connection (Microcontroller DI/O high output, EEPROM low output)

4-4) DO STATUS READY output timing

(When the microcontroller DI/O is low, EEPROM DO output high, and low is input to DI)

・Set the EEPROM input level $V_{IL}$ so as to satisfy the following.




Conditions

$$V_{ILE} \geqq V_{OHE} - I_{OLM} \times R$$

As this moment, $V_{OHE}$=VCC

$$V_{ILE} \geqq VCC - I_{OLM} \times R$$

$$\therefore \quad R \geqq \frac{VCC - V_{ILE}}{I_{OLM}} \quad \cdots ⑧$$

・$V_{ILE}$ : EEPROM $V_{IL}$ specifications
・$V_{OHE}$ : EEPROM $V_{OH}$ specifications
・$I_{OLM}$ : Microcontroller $I_{OL}$ specifications

Example) When VCC=5V, $V_{OHM}$=5V, $I_{OHM}$=0.4mA, $V_{OLM}$=5V, $I_{OLM}$=0.4mA,

From the equation ⑦,

$$R \geqq \frac{V_{IHE}}{I_{OHM}}$$

$$R \geqq \frac{3.5}{0.4 \times 10^{-3}}$$

$$\therefore \quad R \geqq 8.75\ [k\Omega] \quad \cdots ⑨$$

From the equation⑧,

$$R \geqq \frac{VCC - V_{ILE}}{I_{OLM}}$$

$$R \geqq \frac{5 - 1.5}{2.1 \times 10^{-3}}$$

$$\therefore \quad R \geqq 1.67\ [k\Omega] \quad \cdots ⑩$$

Therefore, from the equations ⑨ and ⑩,

$$\therefore \quad R \geqq 8.75\ [k\Omega]$$

Figure 54. Circuit at DI, DO direct connection (Microcontroller DI/O low output, EEPROM high output)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5) I/O equivalence circuit

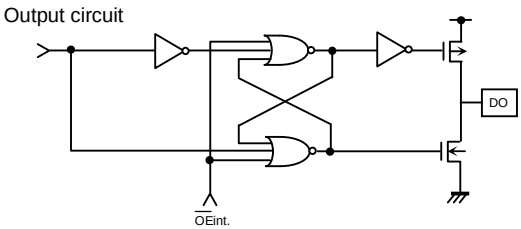



Figure 55. Output circuit (DO)

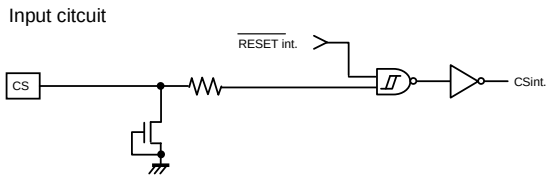



Figure 56. Input circuit (CS)

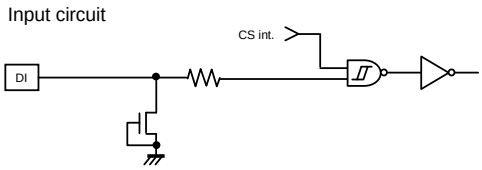



Figure 57. Input circuit (DI)

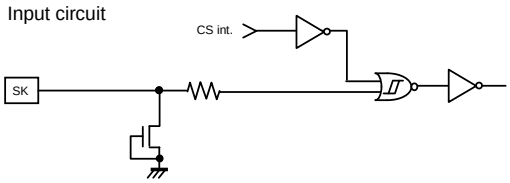



Figure 58. Input circuit (SK)

6)Power-Up/Down conditions

○At power ON/OFF, set CS low.

When CS is high, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CS low. (When CS is in low status all inputs are cancelled.) And at power decline, owing to power line capacity and so forth, low power status may continue long. At this case too, owing to the same reason, malfunction, mistake write may occur, therefore, at power OFF too, set CS low.

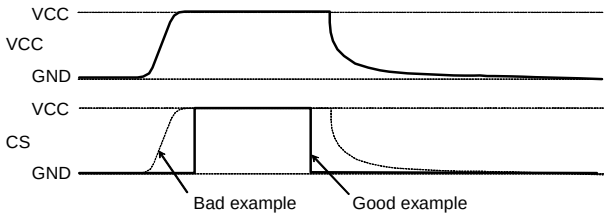



Figure 59. Timing at power ON/OFF

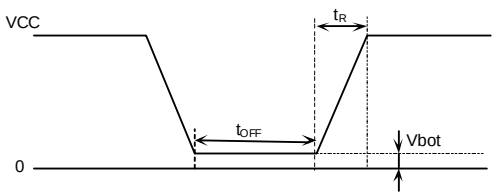
（Bad example）CS pin is pulled up to VCC
In this case, CS becomes high (active status), and EEPROM may have malfunction, mistake write owing to noise and the likes.
Even when CS input is High-Z, the status becomes like this case, which please note.

（Good example）It is low at power ON/OFF.
Set 10ms or higher to recharge at power OFF.
When power is turned on without observing this condition, IC internal circuit may not be reset, which please note.

○POR citcuit

This IC has a POR (Power On Reset) circuit as a mistake write countermeasure. After POR operation, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is high at power ON/OFF, it may become write enable status owing to noises and the likes. For secure operations, observe the follwing conditions.

1. Set CS=low
2. Turn on power so as to satisfy the recommended conditions of $t_R$, $t_{OFF}$, Vbot for POR circuit operation.




Recommended conditions of $t_R$, $t_{OFF}$, Vbot

| $t_R$ | $t_{OFF}$ | Vbot |
|---|---|---|
| 10ms or below | 10ms or higher | 0.3V or below |
| 100ms or below | 10ms or higher | 0.2V or below |

Figure 60. Rise waveform diagram

○LVCC circuit

LVCC (VCC-Lockout) circuit prevents data rewrite operation at low power, and prevents wrong write.
At LVCC voltage (Typ.=1.2V) or below, it prevent data rewrite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7)Noise countermeasures

○VCC noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC VCC and GND, At that moment, attach it as close to IC as possible.And, it is also recommended to attach a bypass capacitor between board VCC and GND.

○SK noise

When the rise time of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time of SK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.


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## ●Operational Notes

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute Maximum Ratings
If the absolute maximum ratings such as supply voltage and operating temperature and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any operating condition. Make sure that each terminal voltage is not lower than that of GND terminal in consideration of transition status.

(5) Heat design
In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal short circuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of pin short between LSI terminals and terminals, terminals and power source, terminals and GND owing to unconnect use, LSI may be destructed.

(7) Using this LSI in a strong electromagnetic field may cause malfunction, therefore, evaluate the design sufficiently.


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●**Part numbering**

| B | R | 9 | 3 | G | 7 | 6 | x | x | x | – | 3 | x | | x | x |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**BUS type**
93 : MicroWire

**Operating temperature / Operating Voltage**
-40℃ to +85℃/ 1.7V to 5.5V

**Capacity**
76=8K

**Package**

| | |
|---|---|
| Blank | :DIP-T8 |
| F | :SOP8 |
| FJ | :SOP-J8 |
| FV | :SSOP-B8 |
| FVT | :TSSOP-B8 |
| FVJ | :TSSOP-B8J |
| FVM | :MSOP8 |
| NUX | :VSON008X2030 |

**Process code**

**Pin assignment**
Blank: Pin1~8: CS, SK, DI, DO, GND, ORG, DU, VCC respectively
A : Pin1~8: CS, SK, DI, DO, GND, NC, DU, VCC respectively
B : Pin1~8: DU, VCC, CS, SK, DI, DO, GND, NC respectively

**Packaging and forming specification**

| | |
|---|---|
| E2 | : Embossed tape and reel (SOP8,SOP-J8, SSOP-B8,TSSOP-B8, TSSOP-B8J) |
| TR | : Embossed tape and reel (MSOP8, VSON008X2030) |
| Blank | : Tube (DIP-T8) |


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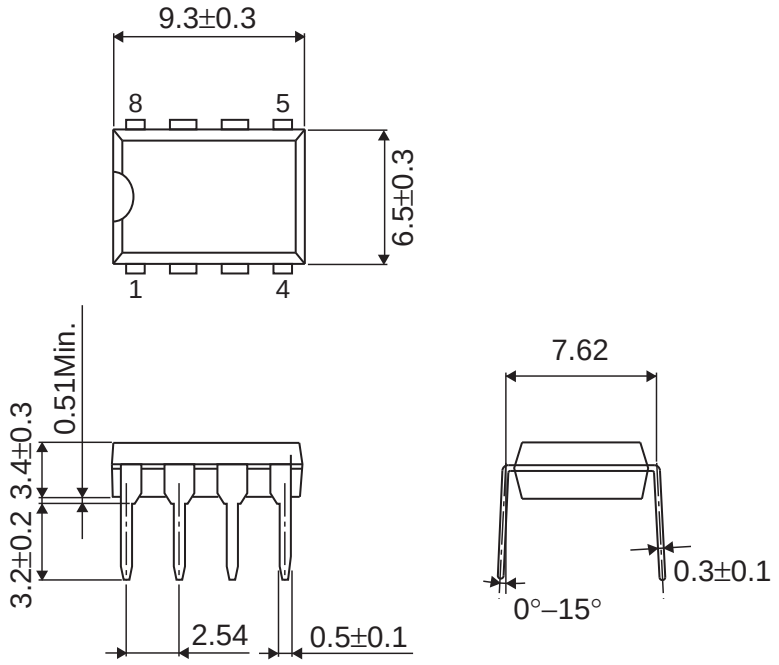
●**Physical Dimensions Tape and Reel information**

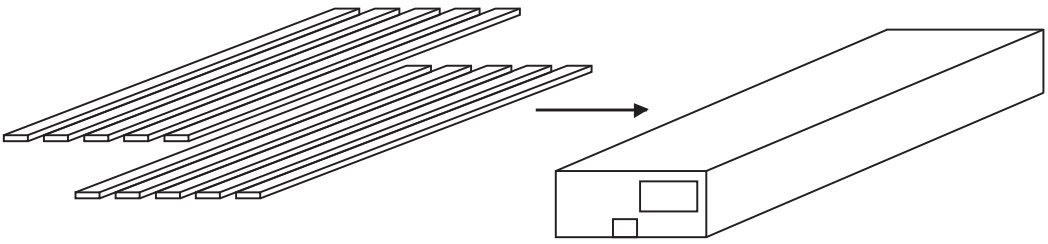
# DIP-T8




(Unit : mm)

<Tape and Reel information>

| | |
|---|---|
| Container | Tube |
| Quantity | 2000pcs |
| Direction of feed | Direction of products is fixed in a container tube |



∗Order quantity needs to be multiple of the minimum quantity.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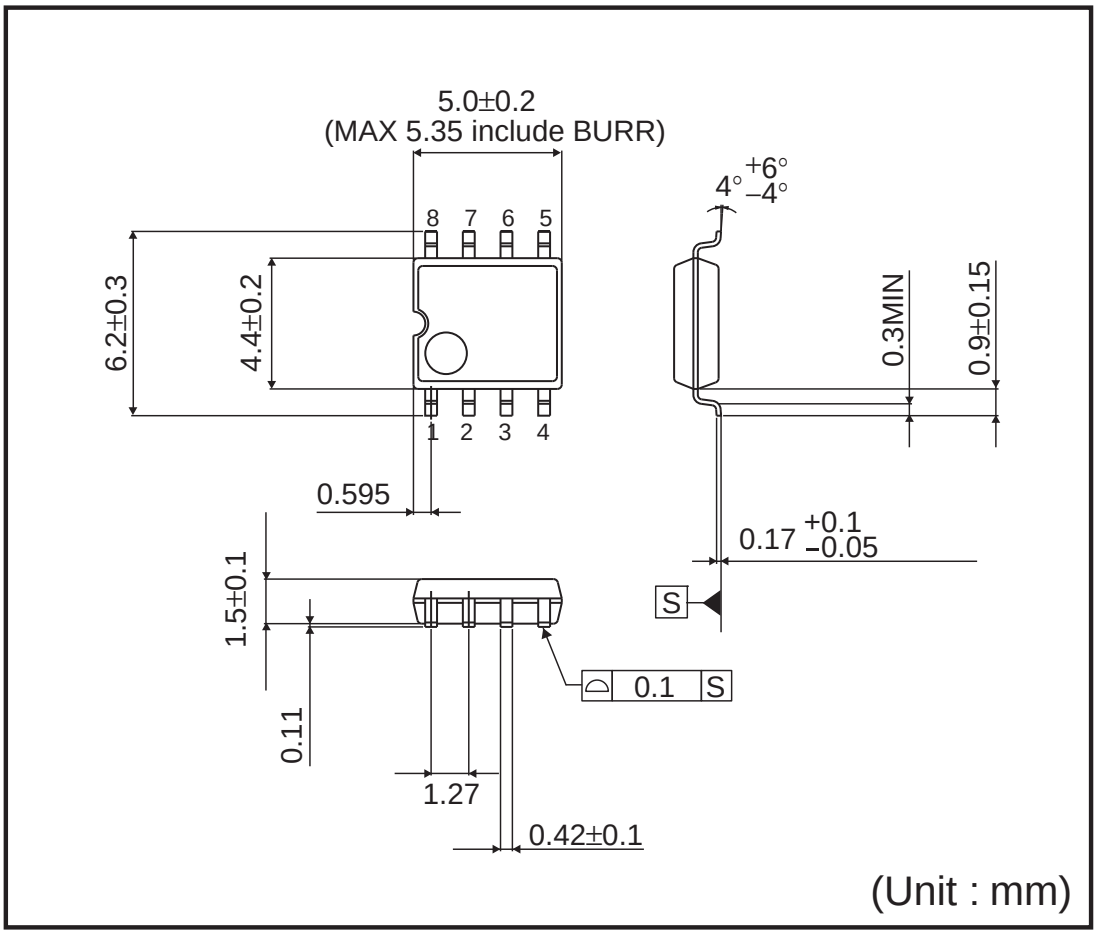
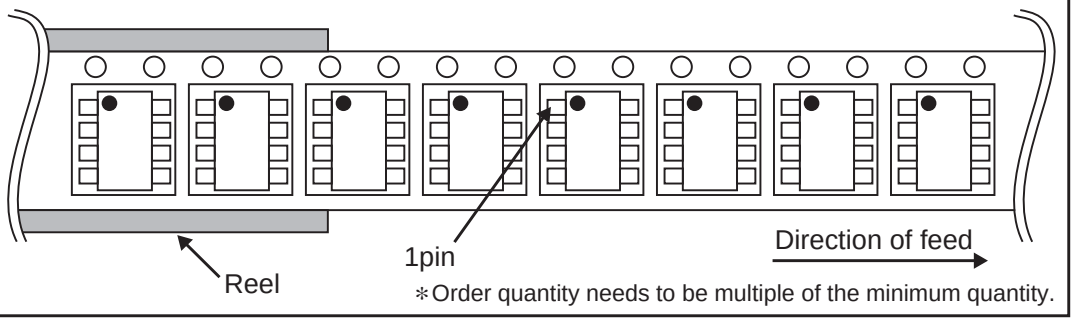
# SOP8




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.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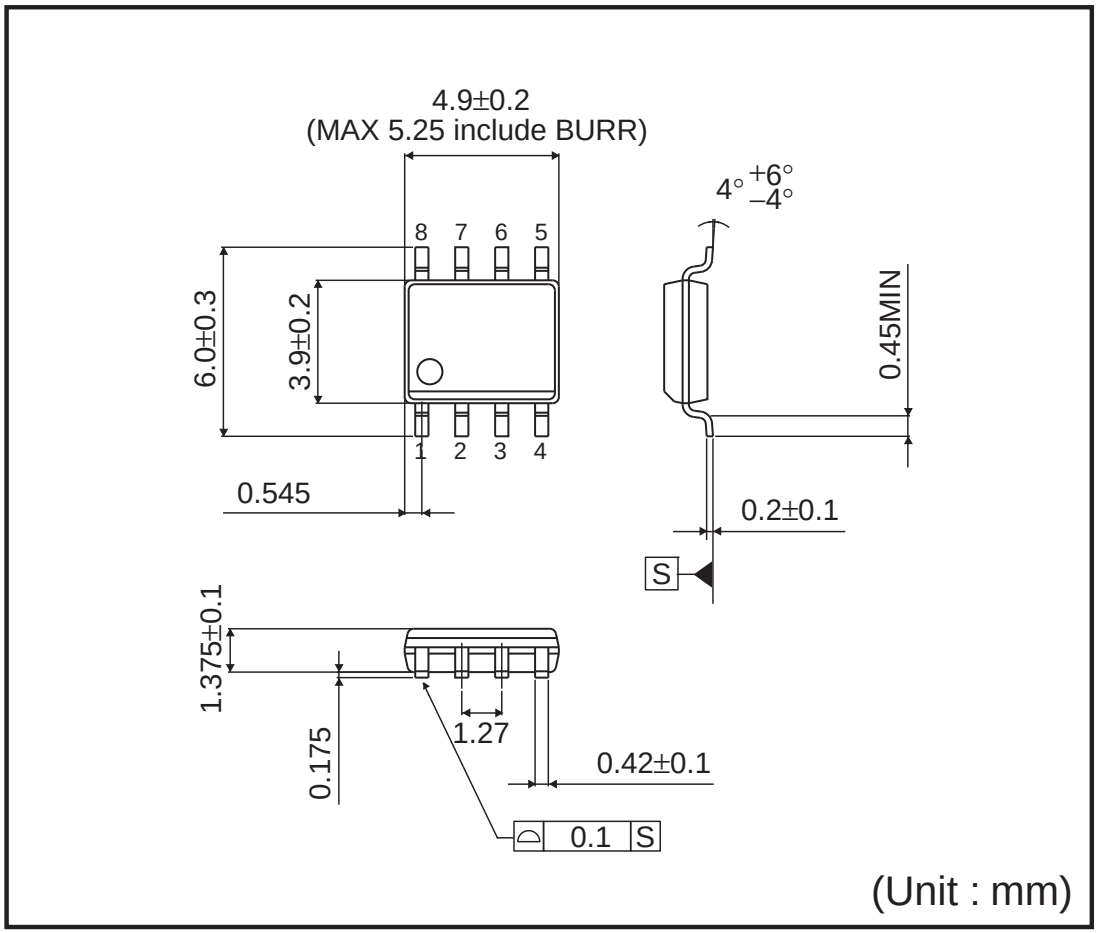
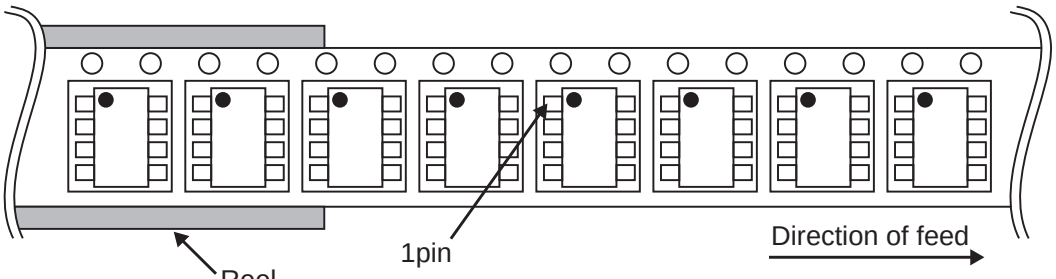
# SOP-J8




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.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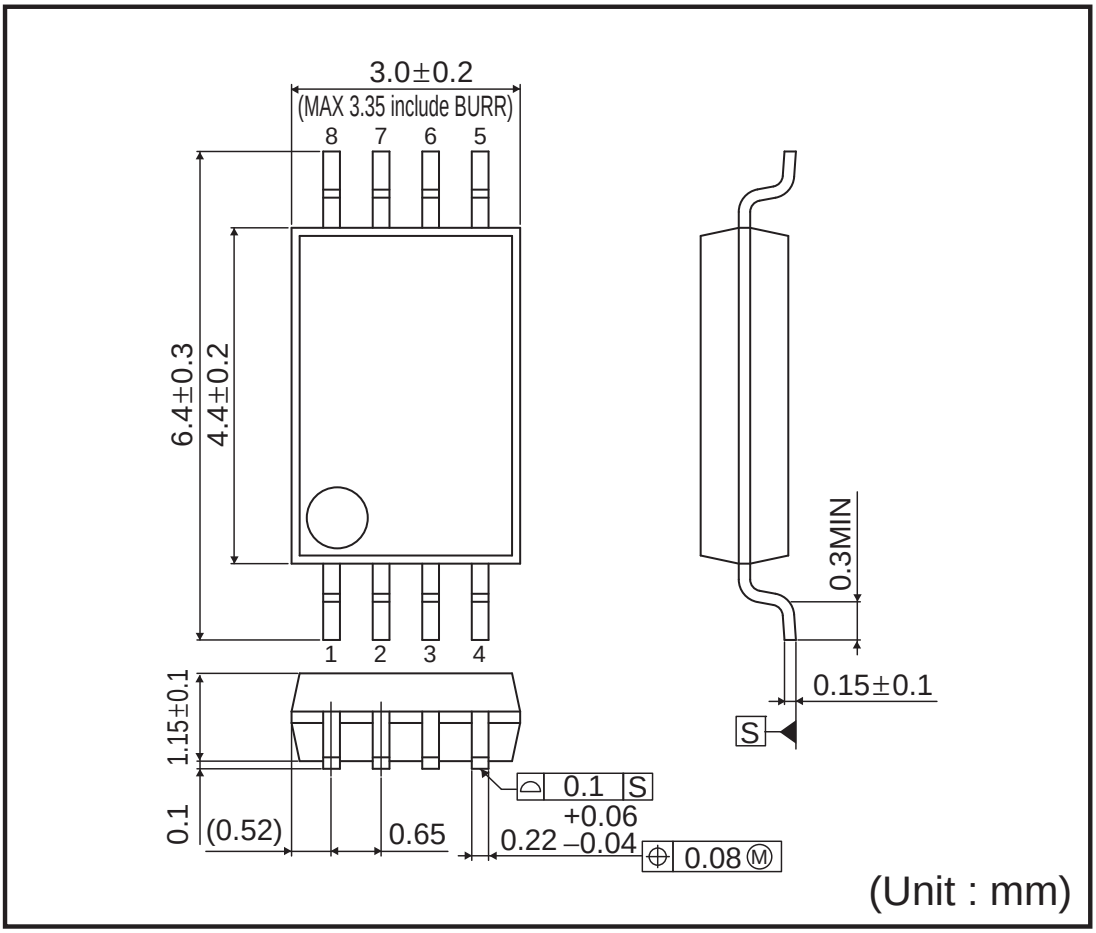
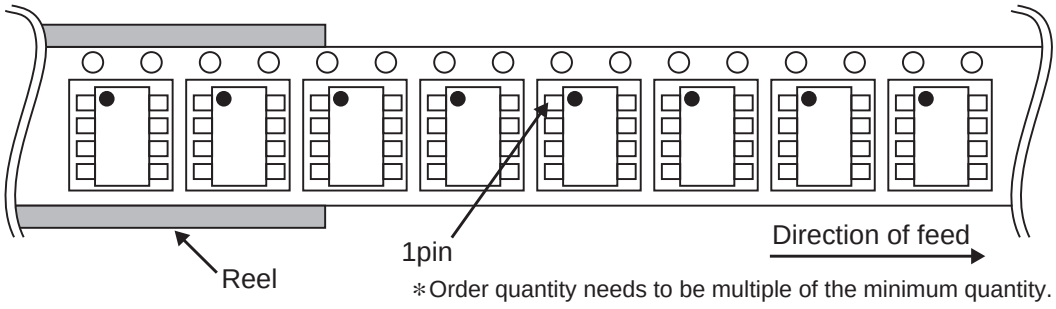
# SSOP-B8




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.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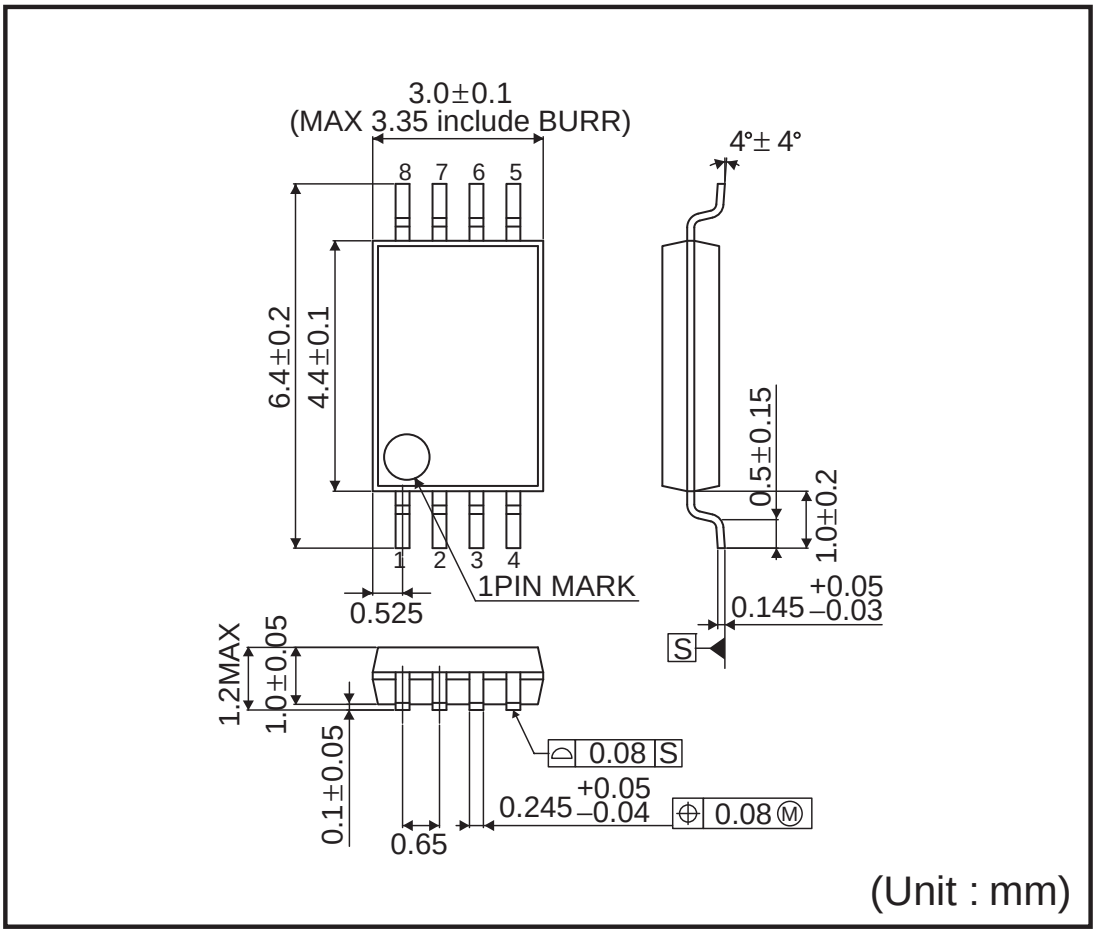
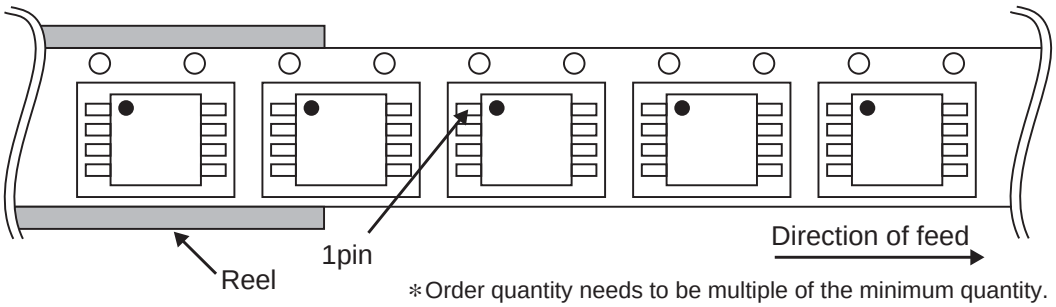
# TSSOP-B8




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.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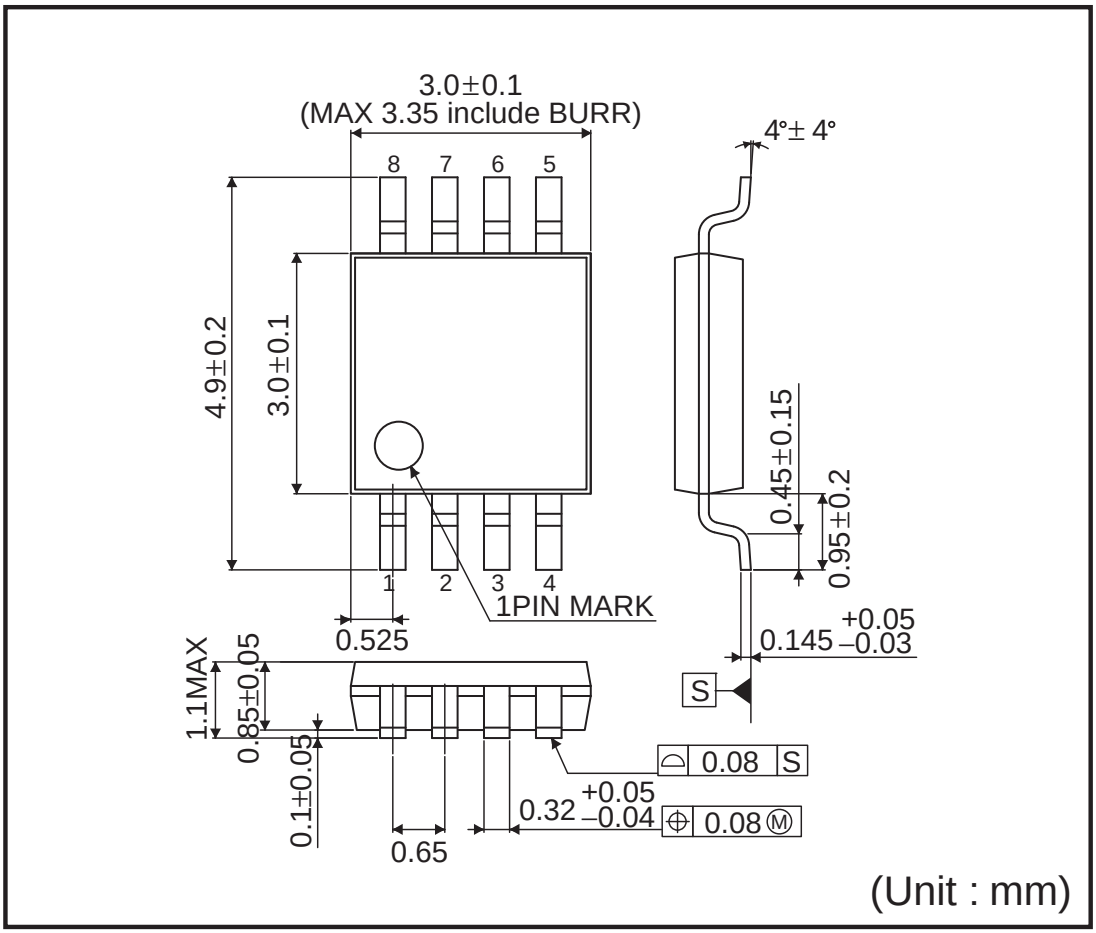
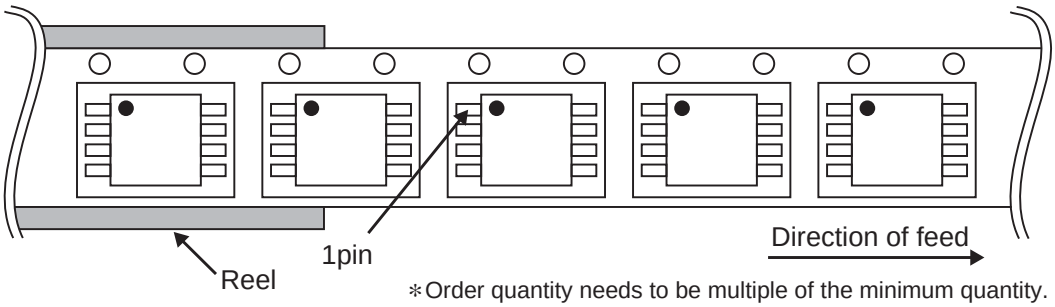
# TSSOP-B8J




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.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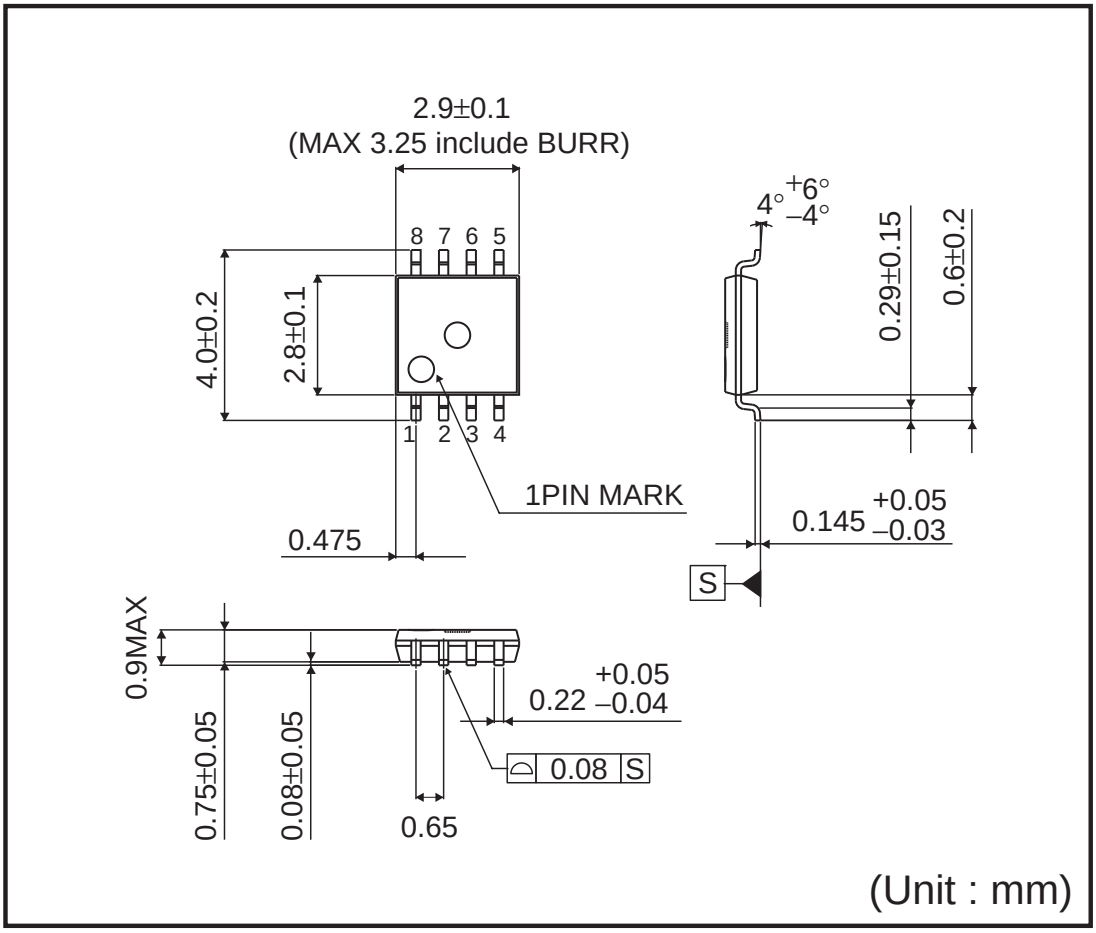
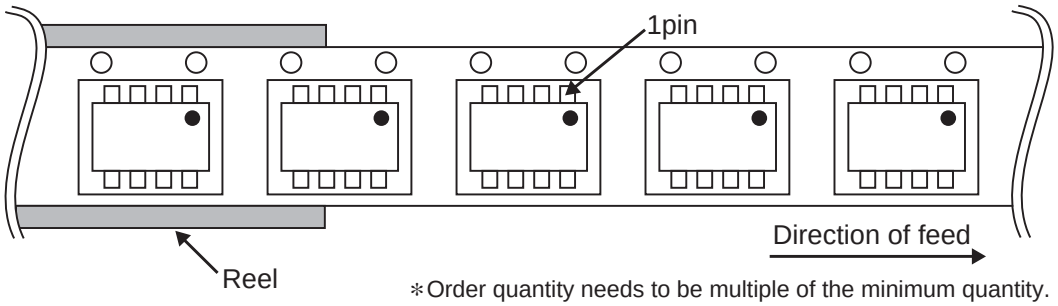
# MSOP8




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | TR<br>( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.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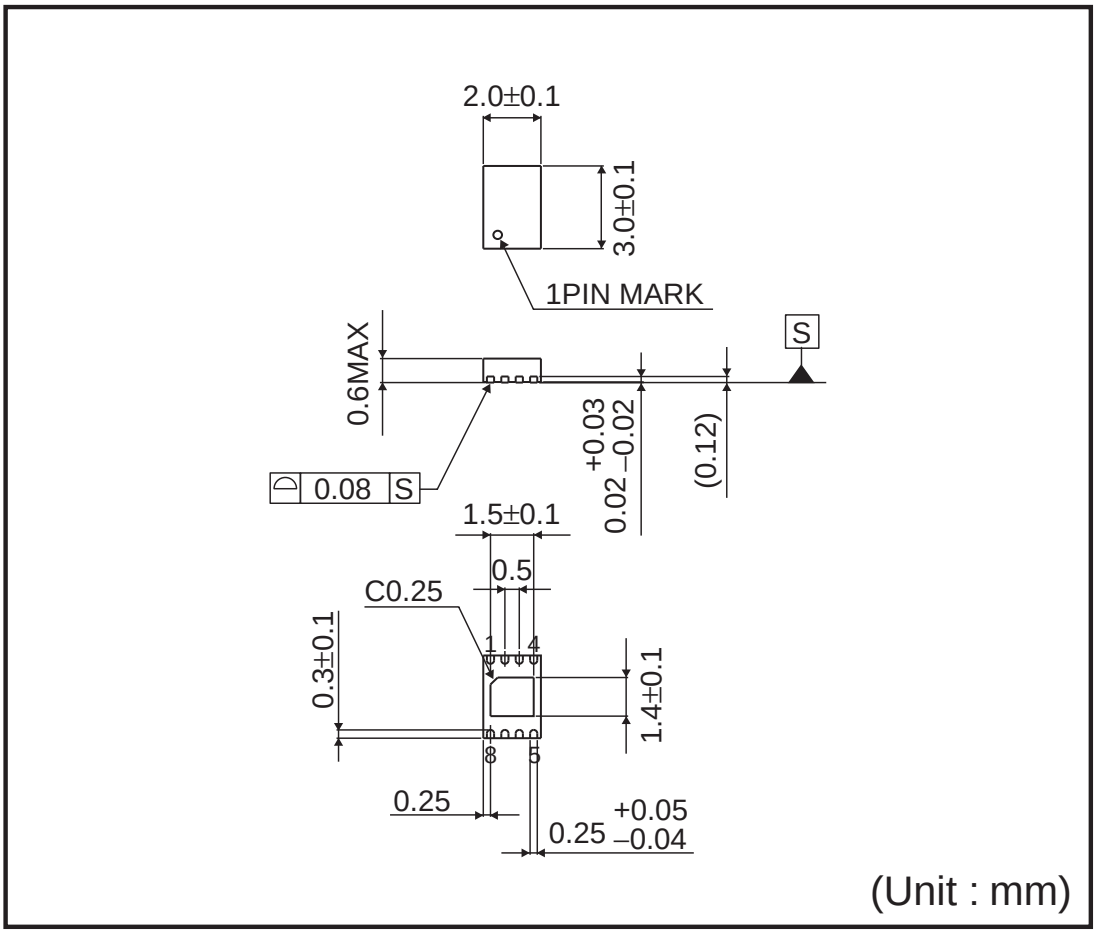
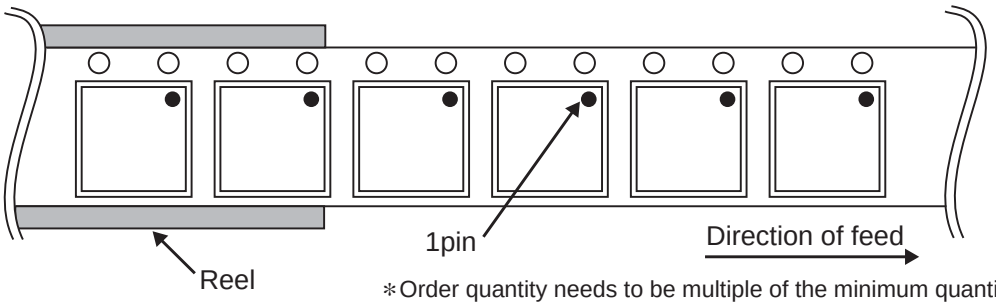
# VSON008X2030




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 4000pcs |
| Direction of feed | TR<br>( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.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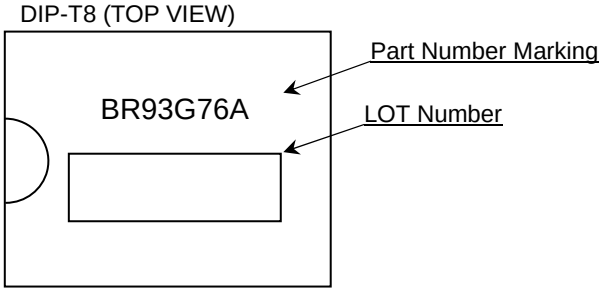
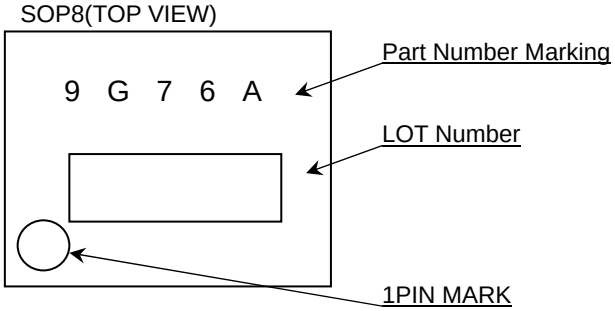
●**Marking Diagrams**

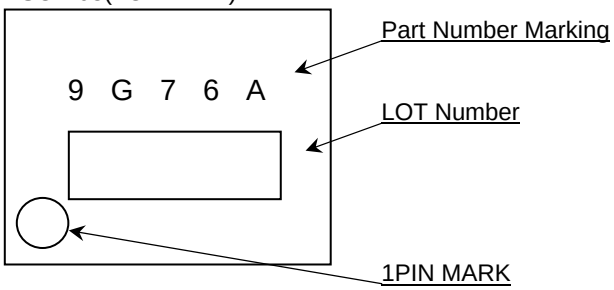
DIP-T8 (TOP VIEW)



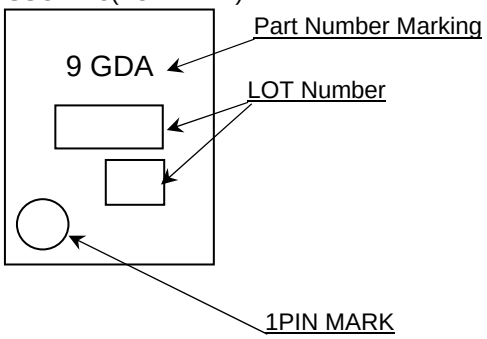

SOP8(TOP VIEW)



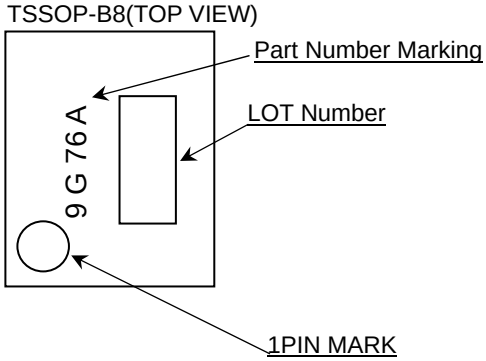

SOP-J8(TOP VIEW)



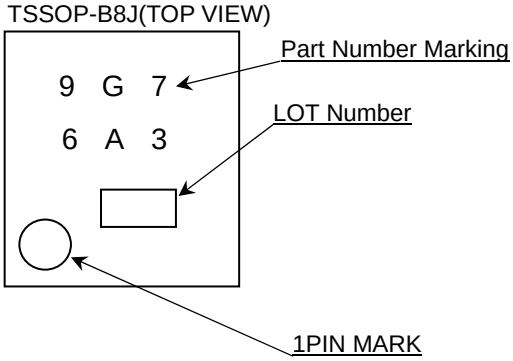

SSOP-B8(TOP VIEW)



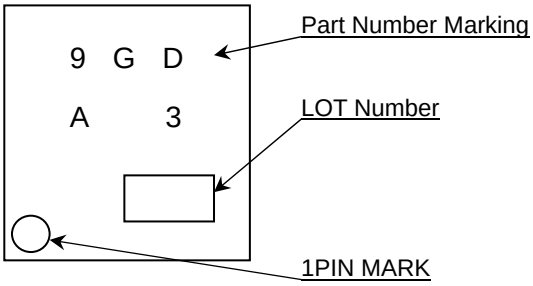

TSSOP-B8(TOP VIEW)



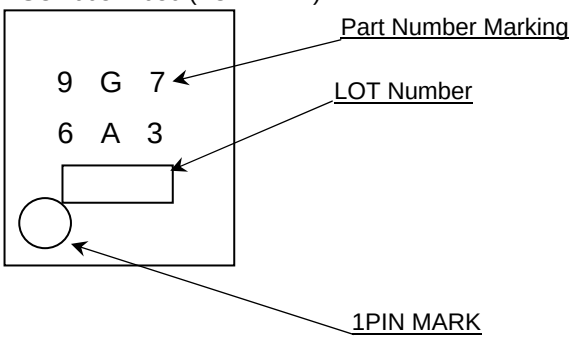

TSSOP-B8J(TOP VIEW)




MSOP8(TOP VIEW)




VSON008X2030 (TOP VIEW)





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●**Revision History**

| Date | Revision | Changes |
|---|---|---|
| 07.Jan.2013 | 001 | New Release |


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# Notice

## Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification


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## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

## Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

## Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

## Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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ООО «ЛайфЭлектроникс» “LifeElectronics” LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
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- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
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- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
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- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
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*Тел: +7 (812) 336 43 04 (многоканальный)*
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