35FS4500, 35FS6500

Grade 0 safety power system basis chip with CAN flexible data transceiver

Rev. 1.0 — 15 December 2017 Short data sheet: advance information

1 General description

The 35FS4500/35FS6500 SMARTMOS devices are a multi-output, power supply, integrated circuit, including CAN Flexible Data (FD) transceiver, dedicated to harsh automotive and transportation markets requiring high reliability (Grade 0) and high functional safety (fit for ASIL D) performance.

Multiple switching and linear voltage regulators, including low-power mode (32 µA) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 1.5 A).

The 35FS4500/35FS6500 includes configurable fail-safe/fail silent safety behavior and features, with two fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level (up to ASIL D).

The built-in CAN FD interface fulfills the ISO 11898-2 and -5 standards.

High temperature capability up to T_A = 150 °C and T_J = 175 °C, compliant with AEC-Q100 Grade 0 automotive qualification.

2 Features

- Battery voltage sensing and MUX output pin
- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- 36 V maximum input operating voltage
- Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A or 1.5 A) or LDO (0.5 A)
- Linear voltage regulator dedicated to auxiliary functions, or to sensor supply (V_{CCA} tracker or independent), 5.0 V or 3.3 V
- Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (V_{CCA}), 5.0 V or 3.3 V
- 3.3 V keep alive memory supply available in low-power mode
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Multiple wake-up sources in low-power mode: CAN, IOs, LDT
- Five configurable I/Os

3 Applications

- T_A up to 150 °C and T_J up to 175 °C
- Drive train electrification (BMS, hybrid EV and HEV, inverter, DCDC, alterno starter)
- Drive train - chassis and safety (active suspension, steering, safety domain gateway)
- Power train (EMS, TCU, gear box)

4 Simplified application diagram

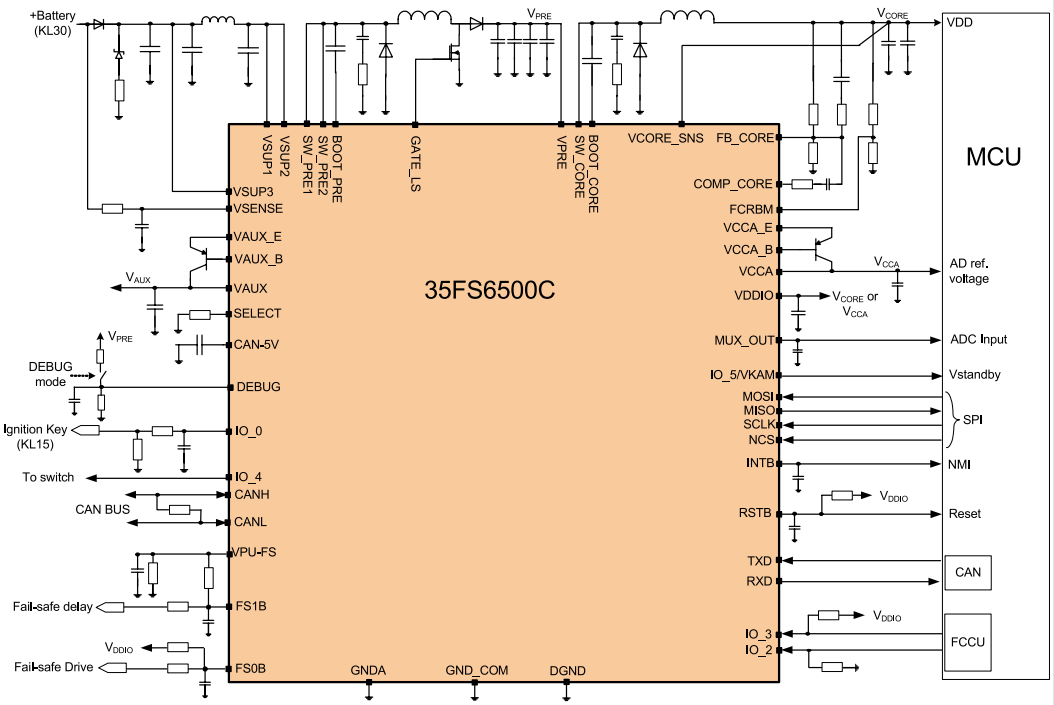

Figure 1. 35FS6500C simplified application diagram - buck boost configuration - FS1B

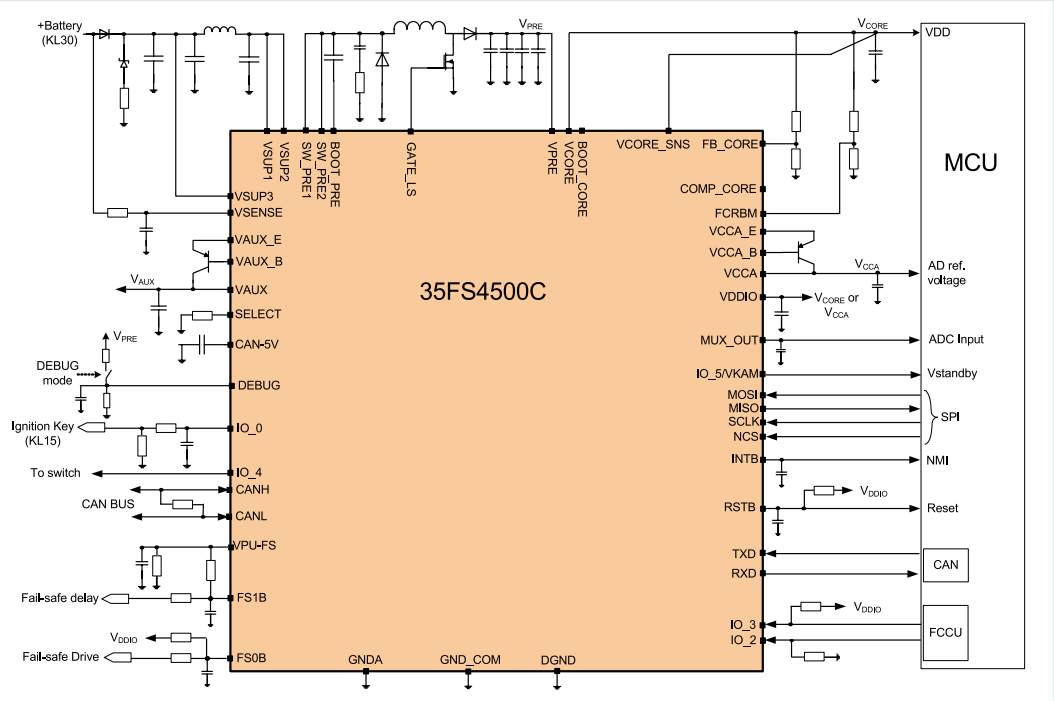

Figure 2. 35FS4500C simplified application diagram - buck boost configuration - FS1B

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5 Ordering information

5.1 Part numbers definition

MC35FS c 5 x y z AE/R2

Table 1. Part number breakdown

Code	Option	Variable	Description
c	4 series	V_{CORE} type	Linear
	6 series		DCDC
x	0	V_{CORE} current	0.5 A or 0.8 A
	1		1.5 A
y	0	Functions	none
	1		FS1B
	2		LDT
	3		FS1B, LDT
z	N	Physical interface	none
	C		CAN FD

5.2 Part numbers list

Table 2. Orderable part variations

Part number	Temperature (T_A)	Package	FS1B	LDT	VCORE	VCORE type	VKAM on	CAN FD	Notes
MC35FS4500CAE	–40 °C to 150 °C	48-pin LQFP exposed pad	0	0	0.5 A	Linear	by SPI	1	[1]
MC35FS4500NAE			0	0	0.5 A	Linear	by SPI	0	
MC35FS4501CAE			1	0	0.5 A	Linear	by SPI	1	
MC35FS4501NAE			1	0	0.5 A	Linear	by SPI	0	
MC35FS4502CAE			0	1	0.5 A	Linear	by SPI	1	
MC35FS4502NAE			0	1	0.5 A	Linear	by SPI	0	
MC35FS4503CAE			1	1	0.5 A	Linear	by SPI	1	
MC35FS4503NAE			1	1	0.5 A	Linear	by SPI	0	

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Part number	Temperature (T_A)	Package	FS1B	LDT	VCORE	VCORE type	VKAM on	CAN FD	Notes
MC35FS6500CAE	–40 °C to 150 °C	48-pin LQFP exposed pad	0	0	0.8 A	DC DC	by SPI	1	[1]
MC35FS6500NAE			0	0	0.8 A	DC DC	by SPI	0	
MC35FS6501CAE			1	0	0.8 A	DC DC	by SPI	1	
MC35FS6501NAE			1	0	0.8 A	DC DC	by SPI	0	
MC35FS6502CAE			0	1	0.8 A	DC DC	by SPI	1	
MC35FS6502NAE			0	1	0.8 A	DC DC	by SPI	0	
MC35FS6503CAE			1	1	0.8 A	DC DC	by SPI	1	
MC35FS6503NAE			1	1	0.8 A	DC DC	by SPI	0	
MC35FS6510CAE			0	0	1.5 A	DC DC	by SPI	1	
MC35FS6510NAE			0	0	1.5 A	DC DC	by SPI	0	
MC35FS6511CAE			1	0	1.5 A	DC DC	by SPI	1	
MC35FS6511NAE			1	0	1.5 A	DC DC	by SPI	0	
MC35FS6512CAE			0	1	1.5 A	DC DC	by SPI	1	
MC35FS6512NAE			0	1	1.5 A	DC DC	by SPI	0	
MC35FS6513CAE			1	1	1.5 A	DC DC	by SPI	1	
MC35FS6513NAE			1	1	1.5 A	DC DC	by SPI	0	

[1] To order parts in tape and reel, add the R2 suffix to the part number.

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6 Block diagram

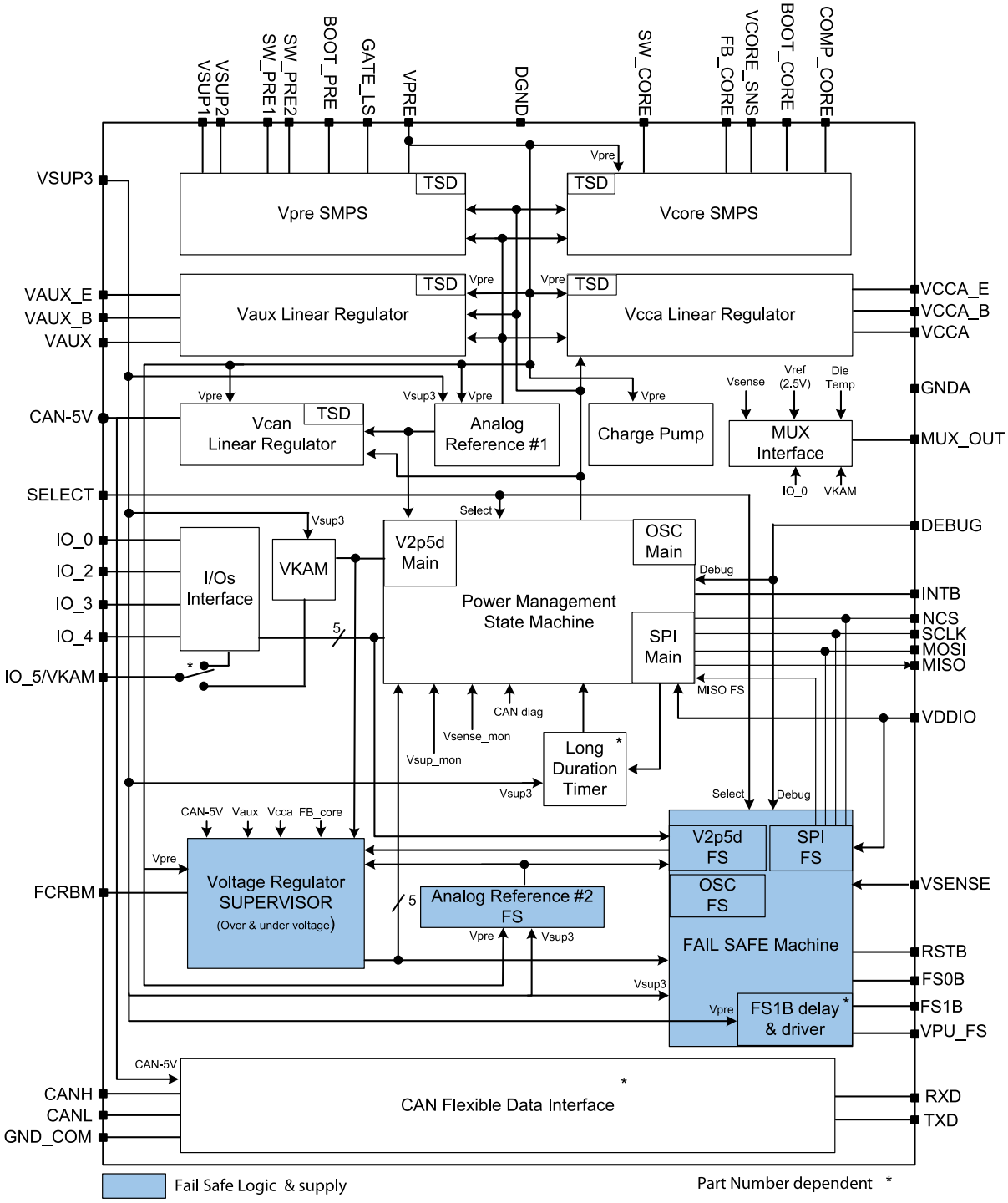

Figure 3. 35FS4500/35FS6500 simplified internal block diagram

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7 Pinning information

7.1 Pinning

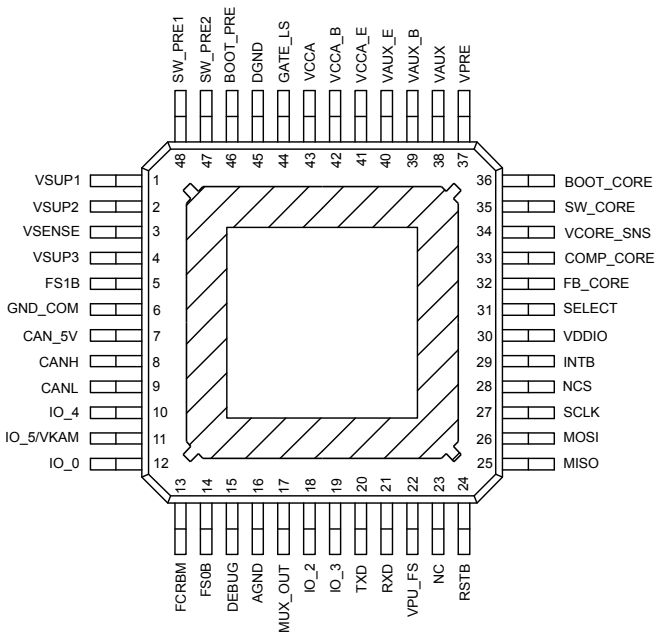

Figure 4. 35FS6500 pinout with CAN and FS1B

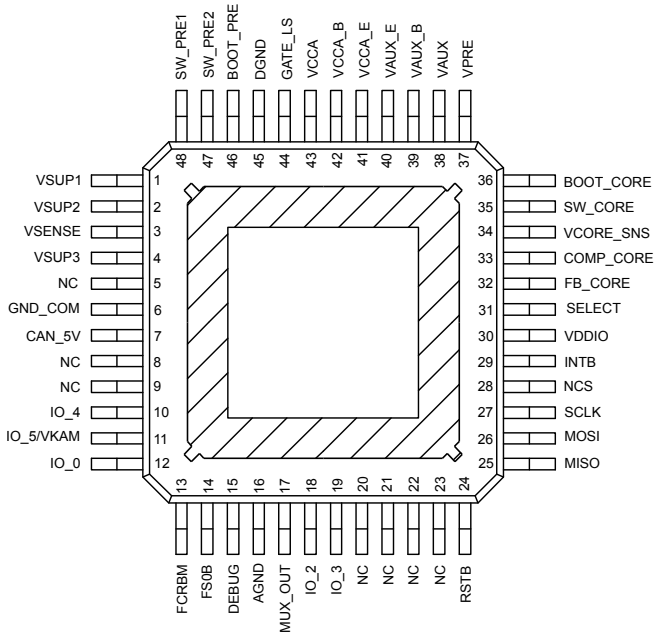

Figure 5. 35FS6500 pinout without CAN

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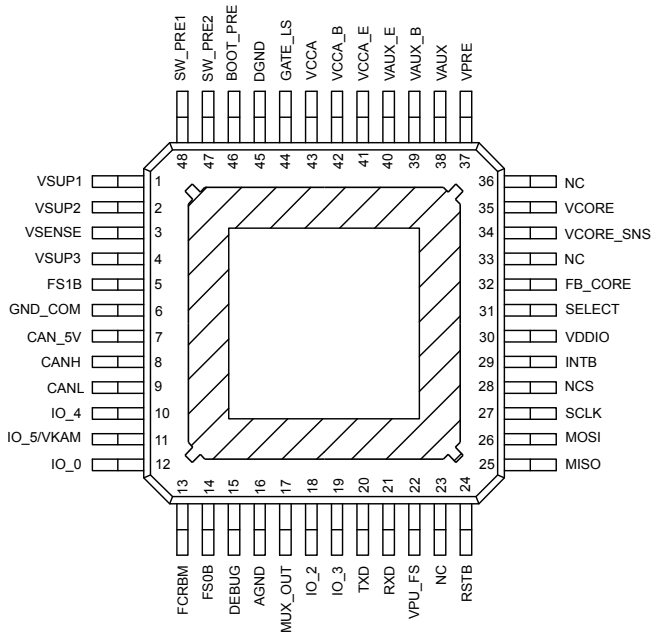

Figure 6. 35FS4500 pinout with CAN and FS1B

7.2 Pin description

Table 3. 35FS4500/35FS6500 pin definition

Pin	Symbol	Type	Definition
1	VSUP1	A_IN	Power supply of the device. An external reverse battery protection diode in series is mandatory.
2	VSUP2	A_IN	Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally.
3	VSENSE	A_IN	Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.
4	VSUP3	A_IN	Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter.
5	FS1B	D_OUT	Second output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected, with a configurable delay or duration versus FS0B output terminal. Open drain structure.
6	GND_COM	GROUND	Dedicated ground for physical layers
7	CAN_5V	A_OUT	Output voltage for the embedded CAN FD interface
8	CANH	A_IN/OUT	CAN output high. If CAN function is not used, this pin must be left open.
9	CANL	A_IN/OUT	CAN output low. If CAN function is not used, this pin must be left open.

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Pin	Symbol	Type	Definition
10	IO_4	D_IN A_OUT	Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver **Digital input:** Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used in conjunction with IO_5). **Wake-up capability:** Can be selectable to wake-up on edges or levels. **Output gate driver:** Can drive a logic level low-side NMOS transistor. Controlled by the SPI.
11	IO_5/VKAM	A_IN D_IN A_OUT	Can be used as digital input with wake-up capability or as an analog output providing keep alive memory supply in low-power mode. **Analog input:** Pin status can be read through the MUX output terminal. **Digital input:** Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used in conjunction with IO_4). **Wake-up capability:** Can be selectable to wake-up on edges or levels. **Supply output:** Provide keep alive memory supply in low-power mode.
12	IO_0	A_IN D_IN	Can be used as analog or digital input (load dump proof) with wake-up capability (selectable). **Analog input:** Pin status can be read through the MUX output terminal. **Digital input:** Pin status can be read through the SPI. **Wake-up capability:** Can be selectable to wake-up on edges or levels.
13	FCRBM	A_IN	Feedback core resistor bridge monitoring: For safety purposes, this pin is used to monitor the middle point of a redundant resistor bridge connected on V_{CORE} (in parallel to the one used to set the V_{CORE} voltage). If not used, this pin must be connected directly to FB_CORE.
14	FS0B	D_OUT	First output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure.
15	DEBUG	D_IN	Debug mode entry input
16	AGND	GROUND	Analog ground connection
17	MUX_OUT	A_OUT	Multiplexed output to be connected to a MCU ADC. Selection of the analog parameter is available at MUX-OUT through the SPI.
18 19	IO_2:3	D_IN	Digital input pin with wake-up capability (logic level compatible) **Digital input:** Pin status can be read through the SPI. Can be used to monitor FCCU error signals from MCU for safety purposes. **Wake-up capability:** Can be selectable to wake-up on edges or levels.
20	TXD	D_IN	Transceiver input from the MCU which controls the state of the CAN bus. Internal pull-up to VDDIO. If CAN function is not used, this pin must be left open.
21	RXD	D_OUT	Receiver output which reports the state of the CAN bus to the MCU If CAN function is not used, this pin must be left open.
22	VPU_FS	A_OUT	Pull-up output for FS1B function
23	NC	N/A	Not connected. Pin must be left open.
24	RSTB	D_OUT	This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.
25	MISO	D_OUT	SPI bus. Master input slave output

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Pin	Symbol	Type	Definition
26	MOSI	D_IN	SPI bus. Master output slave input
27	SCLK	D_IN	SPI Bus. Serial clock
28	NCS	D_IN	Not chip select (active low)
29	INTB	D_OUT	This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO.
30	VDDIO	A_IN	Input voltage for MISO output buffer Allows voltage compatibility with MCU I/Os
31	SELECT	D_IN	Hardware selection pin for VAUX and VCCA output voltages
32	FB_CORE	A_IN	VCORE voltage feedback. Input of the error amplifier.
33	COMP_CORE	A_OUT	Compensation network. Output of the error amplifier. For FS4500 series, this pin must be left open (NC).
34	VCORE_SNS	A_IN	VCORE input voltage sense
35	SW_CORE	A_OUT	VCORE output switching point for FS6500 series
	or VCORE	A_OUT	VCORE output voltage for FS4500 series
36	BOOT_CORE	A_IN/OUT	Bootstrap capacitor for VCORE internal NMOS gate drive. For FS4500 series, this pin must be left open (NC).
37	VPRE	A_IN	VPRE input voltage sense
38	VAUX	A_OUT	VAUX output voltage. External PNP ballast transistor. Collector connection
39	VAUX_B	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Base connection
40	VAUX_E	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Emitter connection
41	VCCA_E	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Emitter connection
42	VCCA_B	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Base connection
43	VCCA	A_OUT	VCCA output voltage. External PNP ballast transistor. Collector connection
44	GATE_LS	A_OUT	Low-side MOSFET gate drive for non-inverting buck-boost configuration
45	DGND	GROUND	Digital ground connection
46	BOOT_PRE	A_IN/OUT	Bootstrap capacitor for the VPRE internal NMOS gate drive
47	SW_PRE2	A_OUT	Second pre-regulator output switching point
48	SW_PRE1	A_OUT	First pre-regulator output switching point

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8 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP1/2/3}$	DC voltage at power supply pins	–1.0 to 40	V	[1]
V_{SENSE}	DC voltage at battery sense pin (with ext R in series mandatory)	–14 to 40	V	
$V_{SW1,2}$	DC voltage at SW_PRE1 and SW_PRE2 Pins	–1.0 to 40	V	
V_{PRE}	DC voltage at VPRE Pin	–0.3 to 8	V	
V_{GATE_LS}	DC voltage at Gate_LS pin	–0.3 to 8	V	
V_{BOOT_PRE}	DC voltage at BOOT_PRE pin	–1.0 to 50	V	
V_{SW_CORE}	DC voltage at SW_CORE pin	–1.0 to 8	V	
V_{CORE_SNS}	DC voltage at VCORE_SNS pin	0.0 to 8	V	
V_{BOOT_CORE}	DC voltage at BOOT_CORE pin	0.0 to 15	V	
V_{FB_CORE}	DC voltage at FB_CORE pin	–0.3 to 2.5	V	
V_{COMP_CORE}	DC voltage at COMP_CORE pin	–0.3 to 2.5	V	
V_{FCRBM}	DC voltage at FCRBM pin	–0.3 to 8	V	
$V_{AUX\_B,E}$	DC voltage at VAUX_B, VAUX_E pins	–0.3 to 40	V	
V_{AUX}	DC voltage at VAUX pin	–2.0 to 40	V	
$V_{CCA\_B,E}$	DC voltage at VCCA_B, VCCA_E pins	–0.3 to 8	V	
V_{CCA}	DC voltage at VCCA pin	–0.3 to 8	V	
V_{DDIO}	DC voltage at VDDIO pin	–0.3 to 8	V	
V_{CAN_5V}	DC voltage on CAN_5V pin	–0.3 to 8	V	
V_{PU_FS}	DC voltage at VPU_FS pin	–0.3 to 8	V	
V_{FSxB}	DC voltage at FS0B, FS1B pins (with ext R in series mandatory)	–0.3 to 40	V	
V_{DEBUG}	DC voltage at DEBUG pin	–0.3 to 40	V	
$V_{IO\_0,4}$	DC voltage at IO_0, IO_4 pins (with ext R in series mandatory)	–0.3 to 40	V	
V_{IO_5}	DC voltage at IO_5 pin	–0.3 to 20	V	
V_{KAM}	DC voltage at VKAM pin	–0.3 to 8	V	
V_{DIG}	DC voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, IO_2, IO_3 pins	–0.3 to 8	V	
V_{SELECT}	DC voltage at SELECT pin	–0.3 to 8	V	
V_{BUS_CAN}	DC voltage on CANL, CANH pins	–27 to 40	V	
I_I_{SENSE}	V_{SENSE} maximum current capability	–5.0 to 5.0	mA	
$I\_IO_{0,\ 4,\ 5}$	IOs maximum current capability (IO_0, IO_4, IO_5)	–5.0 to 5.0	mA	

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Symbol	Ratings	Value	Unit	Notes
ESD voltage				
	Human body model (JESD22/A114) – 100 pF, 1.5 kΩ			[2]
$V_{ESD-HBM1}$	• All pins	±2.0	kV	
$V_{ESD-HBM2}$	• VSUP1,2,3, VSENSE, VAUX, IO_0,4, FS0B, FS1B, DEBUG	±4.0	kV	
$V_{ESD-HBM3}$	• CANH, CANL	±6.0	kV	
	Charge device model (JESD22/C101):			
$V_{ESD-CDM1}$	• All pins	±500	V	
$V_{ESD-CDM2}$	• Corner pins	±750	V	
	System level ESD (gun test) • VSUP1, 2, 3, VSENSE, VAUX, IO_0, 4, 5, FS0B, FS1B			
$V_{ESD-GUN1}$	330 Ω/150 pF unpowered according to IEC61000-4-2	±8.0	kV	
$V_{ESD-GUN2}$	330 Ω/150 pF unpowered according to OEM LIN, CAN, FLexray Conformance	±8.0	kV	
$V_{ESD-GUN3}$	2.0 kΩ/150 pF unpowered according to ISO10605.2008	±8.0	kV	
$V_{ESD-GUN4}$	2.0 kΩ/330 pF powered according to ISO10605.2008 • CANH, CANL	±8.0	kV	
$V_{ESD-GUN5}$	330 Ω/150 pF unpowered according to IEC61000-4-2	±15.0	kV	
$V_{ESD-GUN6}$	330 Ω/150 pF unpowered according to OEM LIN, CAN, FLexray Conformance	±12.0	kV	
$V_{ESD-GUN7}$	2.0 kΩ/150 pF unpowered according to ISO10605.2008	±15.0	kV	
$V_{ESD-GUN8}$	2.0 kΩ/330 pF powered according to ISO10605.2008	±12.0	kV	
Thermal ratings				
T_A	Ambient temperature	–40 to 150	°C	
T_J	Junction temperature	–40 to 175	°C	
T_{STG}	Storage temperature	–55 to 150	°C	
Thermal resistance				
$R_{\theta JA}$	Thermal resistance junction to ambient	30	°C/W	[3]
$R_{\theta JCTOP}$	Thermal resistance junction to case top	23.8	°C/W	[4]
$R_{\theta JCBOTTOM}$	Thermal resistance junction to case bottom	0.9	°C/W	[5]

[1] All VSUPs ($V_{SUP1/2/3}$) must be connected to the same supply
[2] Compared to AGND
[3] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal
[4] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1).
[5] Thermal resistance between the die and the solder par on the bottom of the packaged based on simulation without any interface resistance.

9 Packaging

9.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

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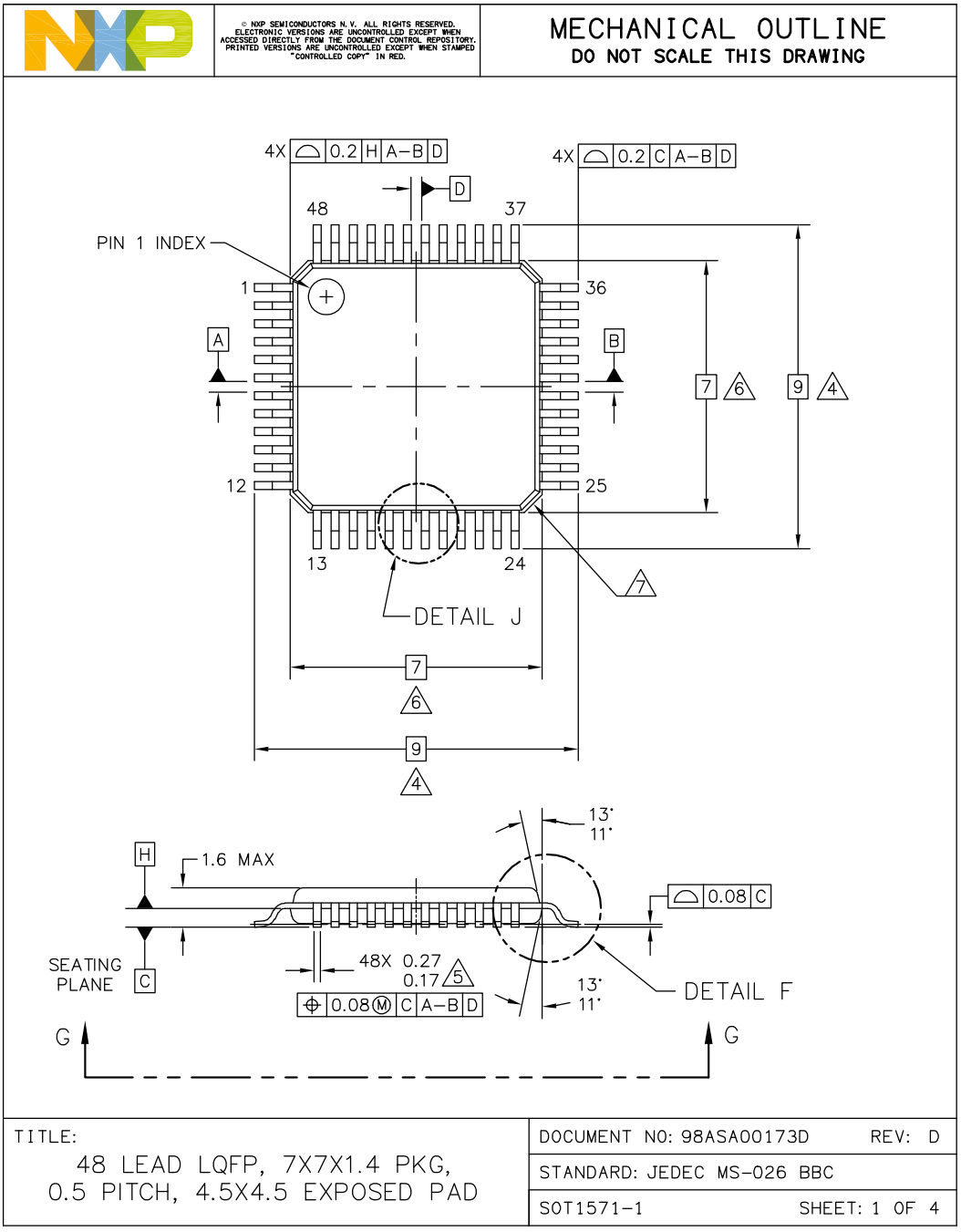
Table 5. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00173D



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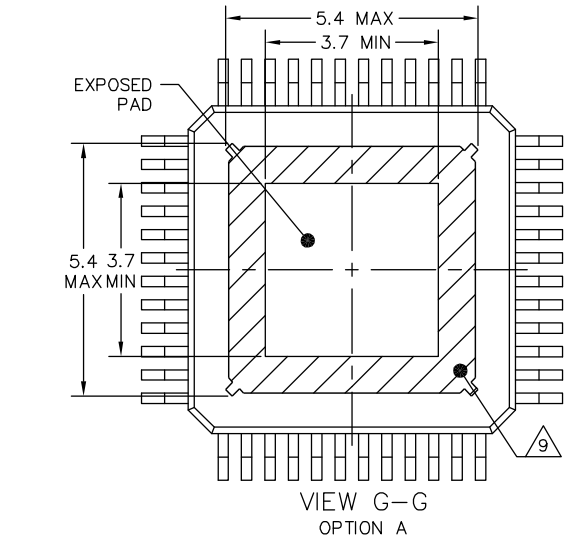

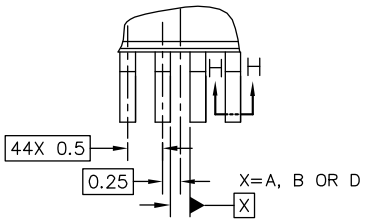

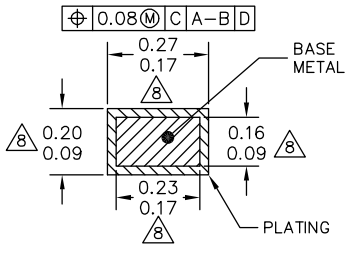

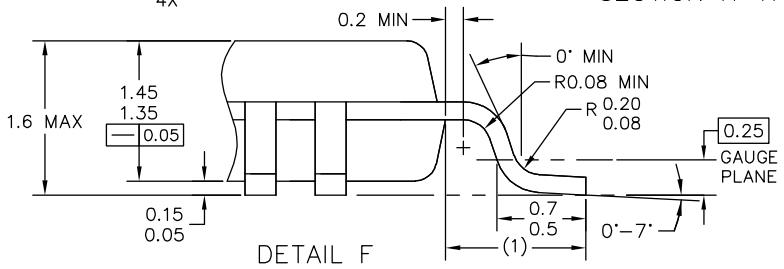

TITLE:	DOCUMENT NO: 98ASA00173D	REV: D
48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	STANDARD: JEDEC MS-026 BBC	
	SOT1571-1	SHEET: 2

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

TITLE:	DOCUMENT NO: 98ASA00173D	REV: D
48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	STANDARD: JEDEC MS-026 BBC	
	SOT1571-1	SHEET: 3

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10 References

The following are URLs where you can obtain information on related NXP products and application solutions.

NXP.com support pages	Description	URL
AN5238	Hardware design and product guidelines	http://www.nxp.com/AN5238-DOWNLOAD
AN4388	Quad flat package (QFP)	http://www.nxp.com/files/analog/doc/app_note/AN4388.pdf
Power dissipation tool (Excel file)		http://www.nxp.com/files/analog/software_tools/FS6500-FS4500-power-dissipation-calculator.xlsx
V_{CORE} compensation network simulation tool (CNC)		Upon demand
FMEDA	35FS6500/35FS4500 FMEDA	Upon demand
35FS4500-35FS6500SMUG	35FS4500/35FS6500 Safety Manual – user guide	https://www.nxp.com/webapp/Download?colCode=35FS4500-35FS6500SMUG
FS6500-FS4500	Power System Basis Chip with CAN Flexible Data and LIN Transceivers data sheet	https://www.nxp.com/webapp/Download?colCode=FS6500-FS4500
KITFS4503CAEEVM	FS4500 evaluation board with FS1B	http://www.nxp.com/KITFS4503CAEEVM
KITFS6523CAEEVM	FS6500 evaluation board with FS1B	http://www.nxp.com/KITFS6523CAEEVM
35FS4500 product summary page		http://www.nxp.com/FS4500
35FS6500 product summary page		http://www.nxp.com/FS6500
Analog power management home page		http://www.nxp.com/products/power-management

11 Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
35FS4500-35FS6500SDS v.1.0	20171215	Data sheet: advance information	—	—

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12 Legal information

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