

# MC74HC368A

## Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections

### High-Performance Silicon-Gate CMOS

The MC74HC368A is identical in pinout to the LS368. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC368A has inverting outputs.

#### Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- These are Pb-Free Devices

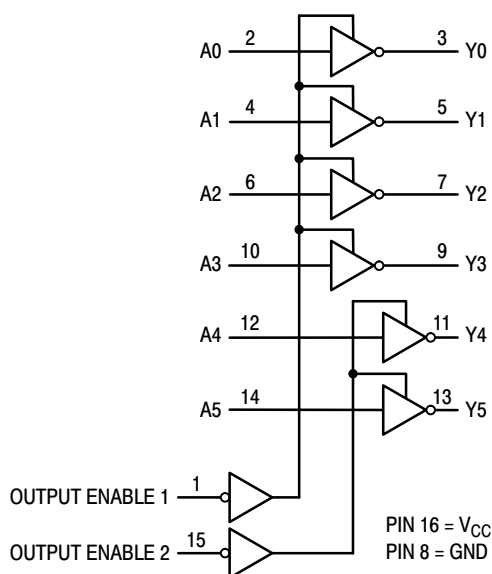
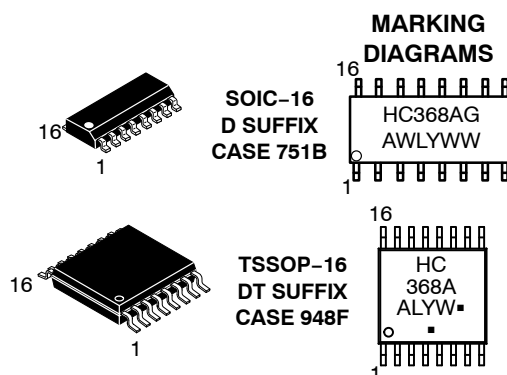


Figure 1. Logic Diagram



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A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN ASSIGNMENT

|                    |   |    |                    |
|--------------------|---|----|--------------------|
| OUTPUT<br>ENABLE 1 | 1 | 16 | V <sub>CC</sub>    |
| A0                 | 2 | 15 | OUTPUT<br>ENABLE 2 |
| Y0                 | 3 | 14 | A5                 |
| A1                 | 4 | 13 | Y5                 |
| Y1                 | 5 | 12 | A4                 |
| A2                 | 6 | 11 | Y4                 |
| Y2                 | 7 | 10 | A3                 |
| GND                | 8 | 9  | Y3                 |

#### FUNCTION TABLE

| Inputs                |   | Output |
|-----------------------|---|--------|
| Enable 1,<br>Enable 2 | A | Y      |
| L                     | L | H      |
| L                     | H | L      |
| H                     | X | Z      |

X = don't care

Z = high-impedance

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC74HC368A

## MAXIMUM RATINGS

| Symbol    | Parameter                                                                          | Value                  | Unit |
|-----------|------------------------------------------------------------------------------------|------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                              | -0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                               | -0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                              | -0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin                                                          | $\pm 20$               | mA   |
| $I_{out}$ | DC Output Current, per Pin                                                         | $\pm 25$               | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                           | $\pm 50$               | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>Plastic DIP†<br>SOIC Package†<br>TSSOP Package† | 750<br>500<br>450      | mW   |
| $T_{stg}$ | Storage Temperature                                                                | - 65 to + 150          | °C   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol                             | Parameter                                            | Min                                                                           | Max             | Unit               |    |
|------------------------------------|------------------------------------------------------|-------------------------------------------------------------------------------|-----------------|--------------------|----|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)                | 2.0                                                                           | 6.0             | V                  |    |
| V <sub>in</sub> , V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND) | 0                                                                             | V <sub>CC</sub> | V                  |    |
| T <sub>A</sub>                     | Operating Temperature, All Package Types             | −55                                                                           | +125            | °C                 |    |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise and Fall Time<br>(Figure 2)               | V <sub>CC</sub> = 2.0 V<br>V <sub>CC</sub> = 4.5 V<br>V <sub>CC</sub> = 6.0 V | 0<br>0<br>0     | 1000<br>500<br>400 | ns |

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions                                                                                                                     | V <sub>CC</sub><br>V | Guaranteed Limit   |                    |                    | Unit |
|-----------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------------|--------------------|--------------------|------|
|                 |                                                |                                                                                                                                     |                      | - 55 to 25°C       | ≤ 85°C             | ≤ 125°C            |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                                                             | 2.0<br>4.5<br>6.0    | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                                           | 2.0<br>4.5<br>6.0    | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                                    | 2.0<br>4.5<br>6.0    | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V    |
|                 |                                                | V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA<br> I <sub>out</sub>   ≤ 7.8 mA                                      | 4.5<br>6.0           | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub><br> I <sub>out</sub>   ≤ 20 μA                                                                    | 2.0<br>4.5<br>6.0    | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
|                 |                                                | V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 6.0 mA<br> I <sub>out</sub>   ≤ 7.8 mA                                      | 4.5<br>6.0           | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND                                                                                            | 6.0                  | ± 0.1              | ± 1.0              | ± 1.0              | μA   |
| I <sub>OZ</sub> | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND | 6.0                  | ± 0.5              | ± 5.0              | ± 10               | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                                                                 | 6.0                  | 8                  | 80                 | 160                | μA   |

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter                                                                 | V <sub>CC</sub><br>V | Guaranteed Limit |                 |                 | Unit |
|----------------------------------------|---------------------------------------------------------------------------|----------------------|------------------|-----------------|-----------------|------|
|                                        |                                                                           |                      | - 55 to 25°C     | ≤ 85°C          | ≤ 125°C         |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input A to Output Y<br>(Figures 2 and 4)       | 2.0<br>4.5<br>6.0    | 95<br>19<br>16   | 120<br>24<br>20 | 145<br>29<br>25 | ns   |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 3 and 5) | 2.0<br>4.5<br>6.0    | 175<br>35<br>30  | 220<br>44<br>37 | 265<br>53<br>45 | ns   |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 3 and 5) | 2.0<br>4.5<br>6.0    | 190<br>38<br>32  | 240<br>48<br>41 | 285<br>57<br>48 | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 2 and 4)           | 2.0<br>4.5<br>6.0    | 60<br>12<br>10   | 75<br>15<br>13  | 90<br>18<br>15  | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance                                                 | –                    | 10               | 10              | 10              | pF   |
| C <sub>out</sub>                       | Maximum Three-State Output Capacitance (Output in High-Impedance State)   | –                    | 15               | 15              | 15              | pF   |

|                 |                                             |                                         |    |
|-----------------|---------------------------------------------|-----------------------------------------|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Per Buffer)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|                 |                                             | 40                                      |    |



## MC74HC368A

### ORDERING INFORMATION

| Device          | Package              | Shipping†        |
|-----------------|----------------------|------------------|
| MC74HC368ADG    | SOIC–16<br>(Pb–Free) | 48 Units / Rail  |
| MC74HC368ADR2G  | SOIC–16<br>(Pb–Free) | 2500 Tape & Reel |
| MC74HC368ADTR2G | TSSOP–16*            | 2500 Tape & Reel |

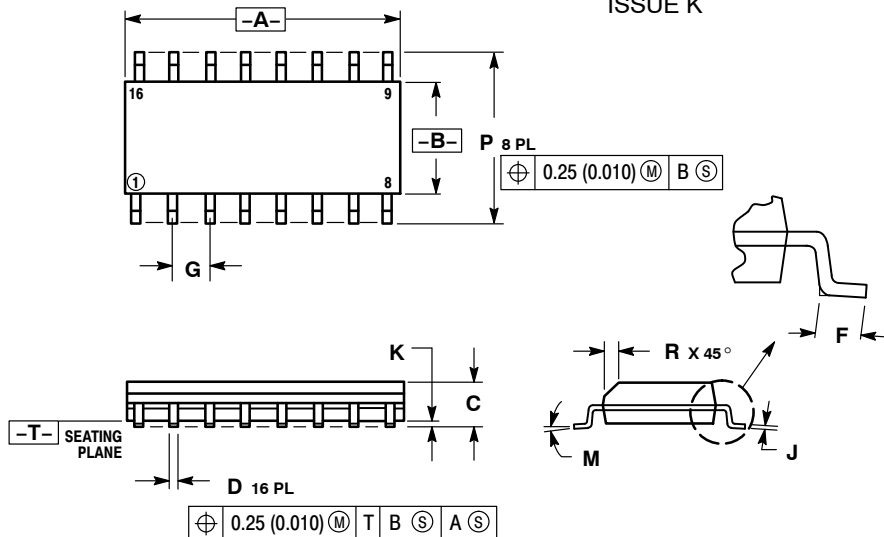
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb–Free.

# MC74HC368A

## PACKAGE DIMENSIONS

SOIC-16  
CASE 751B-05  
ISSUE K

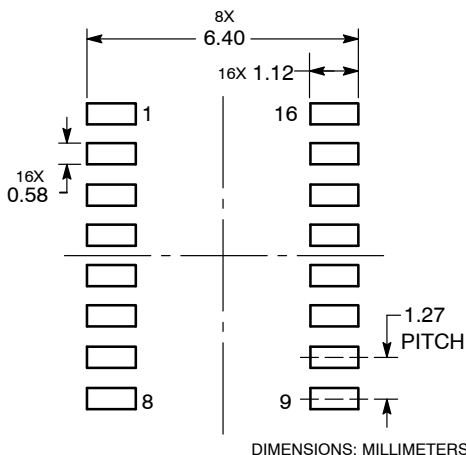


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

### SOLDERING FOOTPRINT\*

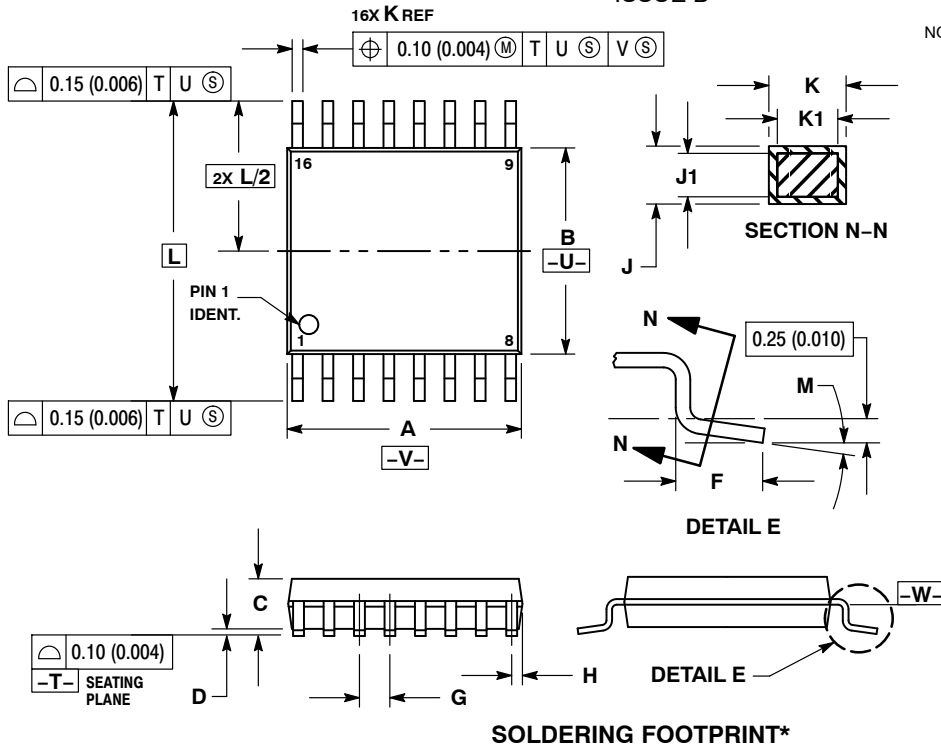


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC368A

## PACKAGE DIMENSIONS

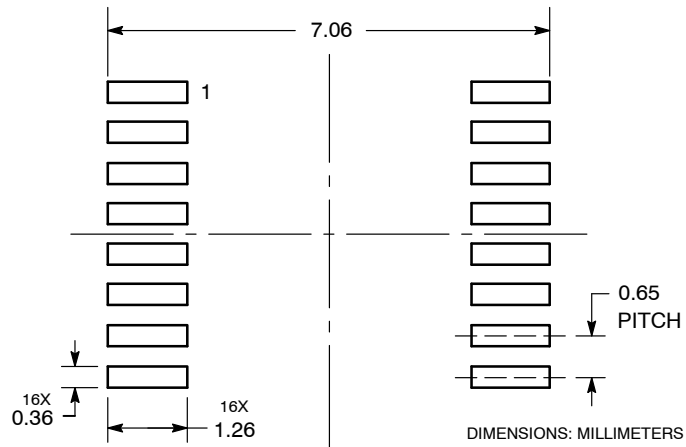
TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE B



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
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