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January 2015

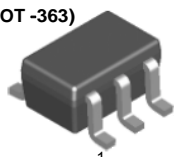
# 2N7002DW

## N-Channel Enhancement Mode Field Effect Transistor

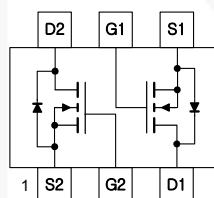
### Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Lead Free/RoHS Compliant

SC70-6 (SOT -363)



Marking : 2N



### Ordering Information

Part Number	Top Mark	Package	Packing Method
2N7002DW	2N	SC70 6L	Tape and Reel

### Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter		Value	Unit
$V_{DSS}$	Drain-Source Voltage		60	V
$V_{DGR}$	Drain-Gate Voltage ( $R_{GS} \leq 1.0 \text{ M}\Omega$ )		60	V
$V_{GSS}$	Gate-Source Voltage	Continuous	$\pm 20$	V
		Pulsed	$\pm 40$	
$I_D$	Drain Current	Continuous	115	mA
		Continuous at $100^\circ\text{C}$	73	
		Pulsed	800	
$T_J, T_{STG}$	Junction and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

## Thermal Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$P_D$	Total Device Dissipation	200	mW
	Derate Above $T_A = 25^\circ\text{C}$	1.6	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient <sup>(1)</sup>	625	$^\circ\text{C/W}$

### Note:

1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.

## Electrical Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics <sup>(2)</sup>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 μA	60	78		V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V		0.001	1.0	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C		7	500	
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V		0.2	±10	nA
On Characteristics <sup>(2)</sup>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.00	1.76	2.00	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 5 V, I <sub>D</sub> = 0.05 A		1.6	7.5	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.5 A			2.0	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 125°C		2.53	13.5	
I <sub>D(ON)</sub>	On-State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 7.5 V	0.50	1.43		A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.2 A	80.0	356.5		mS
Dynamic Characteristics						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		37.8	50	pF
C <sub>oss</sub>	Output Capacitance			12.4	25	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			6.5	7	pF
Switching Characteristics						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 0.2 A,		5.85	20	ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time	V <sub>GEN</sub> = 10 V, R <sub>L</sub> = 150 Ω, R <sub>GEN</sub> = 25 Ω		12.5	20	ns

### Note:

2. Short duration test pulse used to minimize self-heating effect.

## Typical Performance Characteristics

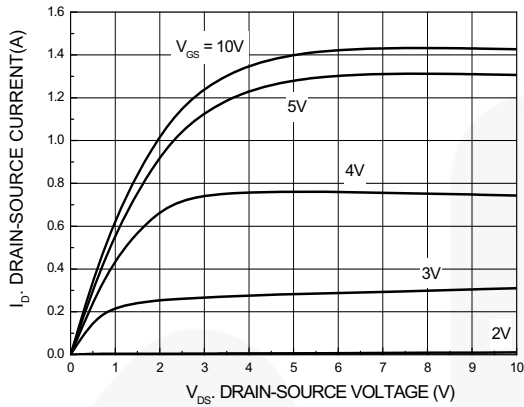


Figure 1. On-Region Characteristics

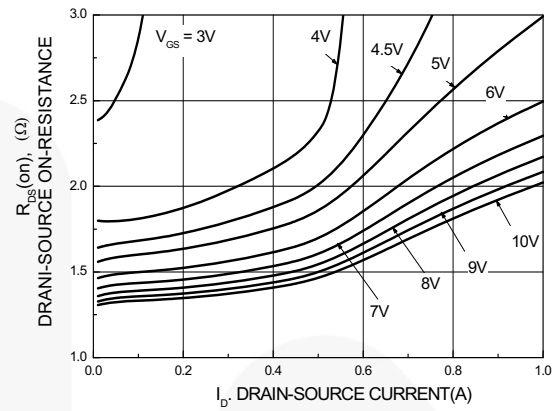


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

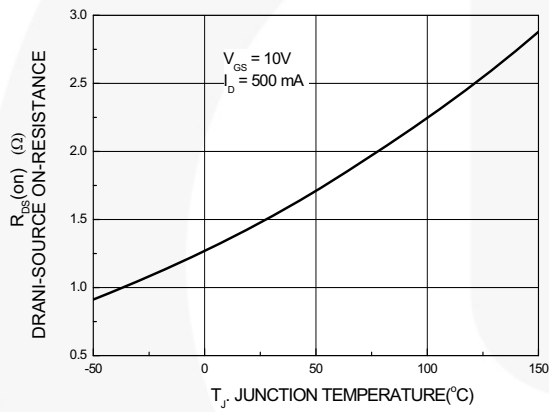


Figure 3. On-Resistance Variation with Temperature

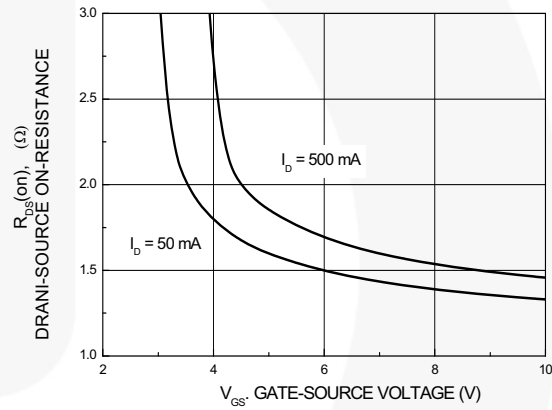


Figure 4. On-Resistance Variation with Gate-Source Voltage

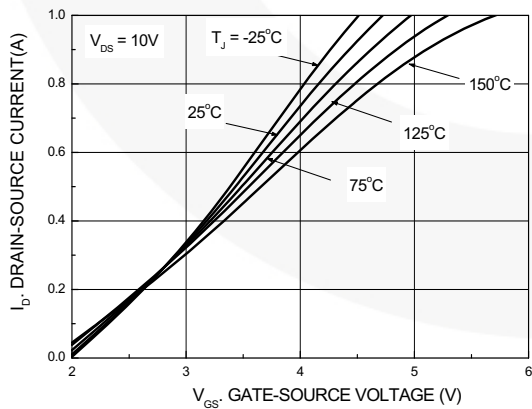


Figure 5. Transfer Characteristics

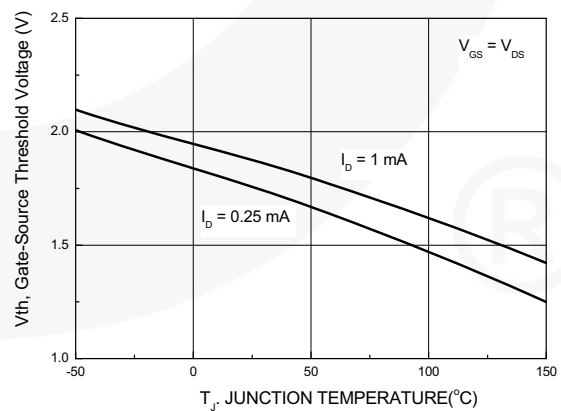


Figure 6. Gate Threshold Variation with Temperature

## Typical Performance Characteristics (Continued)

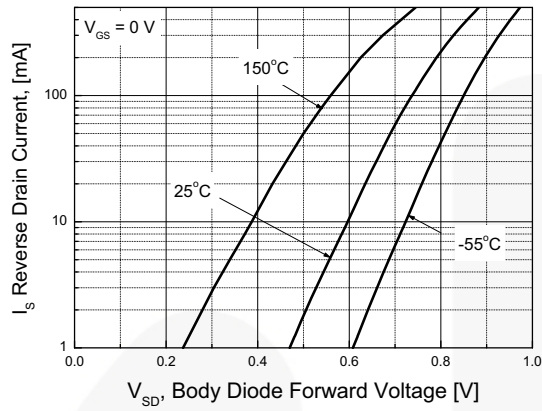


Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature

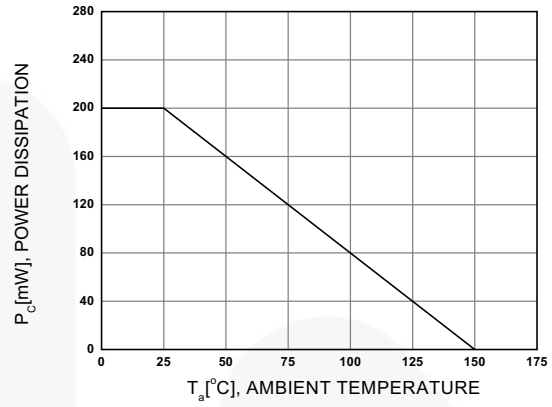


Figure 8. Power Derating







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