#### **Features**

- Fast Read Access Time 70 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
- · Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum (Standard)
    - 2 ms Maximum (Option Ref. AT28HC64BF Datasheet)
  - 1 to 64-byte Page Write Operation
- · Low Power Dissipation
  - 40 mA Active Current
  - 100 µA CMOS Standby Current
- · Hardware and Software Data Protection
- DATA Polling and Toggle Bit for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- Single 5 V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Industrial Temperature Ranges
- · Green (Pb/Halide-free) Packaging Option Only

### 1. Description

The AT28HC64B is a high-performance electrically-erasable and programmable read-only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100  $\mu$ A.

The AT28HC64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by  $\overline{\text{DATA}}$  polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28HC64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.



64K (8K x 8)
High-speed
Parallel
EEPROM with
Page Write and
Software Data
Protection

AT28HC64B

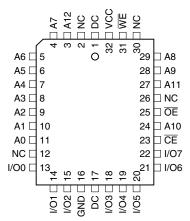




## 2. Pin Configurations

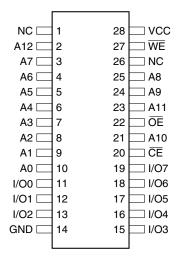
Pin Name	Function
A0 - A12	Addresses
CE	Chip Enable
ŌE	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

### 2.2 32-lead PLCC Top View

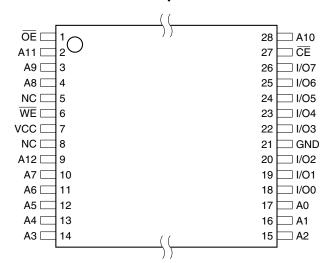


Note: PLCC package pins 1 and 17 are Don't Connect.

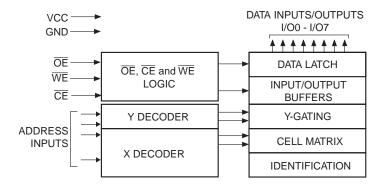
### 2.1 28-lead SOIC Top View



### 2.3 28-lead TSOP Top View



### 3. Block Diagram



### 4. Device Operation

#### 4.1 Read

The AT28HC64B is accessed like a Static RAM. When  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  are low and  $\overline{\text{WE}}$  is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

### 4.2 Byte Write

A low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{CE}$  or  $\overline{WE}$  low (respectively) and  $\overline{OE}$  high initiates a write cycle. The address is latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. The data is latched by the first rising edge of  $\overline{CE}$  or  $\overline{WE}$ . Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of  $t_{WC}$ , a read operation will effectively be a polling operation.

### 4.3 Page Write

The page write operation of the AT28HC64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150  $\mu$ s ( $t_{BLC}$ ) of the previous byte. If the  $t_{BLC}$  limit is exceeded, the AT28HC64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each  $\overline{\rm WE}$  high-to-low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

## 4.4 DATA Polling

The AT28HC64B features  $\overline{\text{DATA}}$  Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin.  $\overline{\text{DATA}}$  Polling may begin at any time during the write cycle.





### 4.5 Toggle Bit

In addition to DATA Polling, the AT28HC64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

#### 4.6 Data Protection

If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel® has incorporated both hardware and software features that will protect the memory against inadvertent writes.

#### 4.6.1 Hardware Protection

Hardware features protect against inadvertent writes to the AT28HC64B in the following ways: (a)  $V_{CC}$  sense – if  $V_{CC}$  is below 3.8 V (typical), the write function is inhibited; (b)  $V_{CC}$  power-on delay – once  $V_{CC}$  has reached 3.8 V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit – holding any one of  $\overline{OE}$  low,  $\overline{CE}$  high or  $\overline{WE}$  high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the  $\overline{WE}$  or  $\overline{CE}$  inputs will not initiate a write cycle.

#### 4.6.2 Software Data Protection

A software-controlled data protection feature has been implemented on the AT28HC64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (refer to the "Software Data Protection Algorithm" diagram on page 10). After writing the 3-byte command sequence and waiting  $t_{WC}$ , the entire AT28HC64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28HC64B. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28HC64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device, however. For the duration of  $t_{WC}$ , read operations will effectively be polling operations.

#### 4.7 Device Identification

An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12 V  $\pm 0.5$  V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

## 5. DC and AC Operating Range

	AT28HC64B-70	AT28HC64B-90	AT28HC64B-120
Operating Temperature (Case)	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V <sub>CC</sub> Power Supply	5 V ±10%	5 V ±10%	5 V ±10%

### 6. Operating Modes

Mode	CE	OE	WE	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	$V_{IH}$	D <sub>OUT</sub>
Write <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	$V_{IL}$	D <sub>IN</sub>
Standby/Write Inhibit	V <sub>IH</sub>	X <sup>(1)</sup>	X	High Z
Write Inhibit	X	X	V <sub>IH</sub>	
Write Inhibit	X	V <sub>IL</sub>	Х	
Output Disable	Х	V <sub>IH</sub>	Х	High Z
Chip Erase	V <sub>IL</sub>	V <sub>H</sub> (3)	$V_{IL}$	High Z

Notes: 1. X can be VIL or VIH.

2. See "AC Write Waveforms" on page 8.

3.  $VH = 12.0 V \pm 0.5 V$ .

## 7. Absolute Maximum Ratings\*

Temperature Under Bias55°C to +125°C
Storage Temperature65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground0.6 V to +6.25 V
All Output Voltages with Respect to Ground0.6 V to V <sub>CC</sub> + 0.6 V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground0.6 V to +13.5V

\*NOTICE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

### 8. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0 V to V <sub>CC</sub> + 1 V		10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>I/O</sub> = 0 V to V <sub>CC</sub>		10	μΑ
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current CMOS	$\overline{\text{CE}}$ = V <sub>CC</sub> - 0.3 V to V <sub>CC</sub> + 1 V		100 <sup>(1)</sup>	μA
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current TTL	CE = 2.0 V to V <sub>CC</sub> + 1 V		2 <sup>(1)</sup>	mA
I <sub>cc</sub>	V <sub>CC</sub> Active Current	f = 5 MHz; I <sub>OUT</sub> = 0 mA		40	mA
V <sub>IL</sub>	Input Low Voltage			0.8	V
V <sub>IH</sub>	Input High Voltage		2.0		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.40	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V

Note: 1.  $I_{SB1}$  and  $I_{SB2}$  for the 55 ns part is 40 mA maximum.

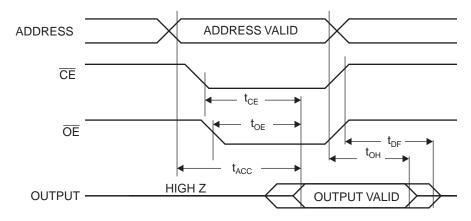




### 9. AC Read Characteristics

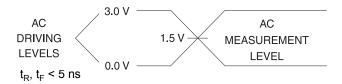
		AT28H0	C64B-70	AT28H0	C64B-90	AT28HC	64B-120	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
t <sub>ACC</sub>	Address to Output Delay		70		90		120	ns
t <sub>CE</sub> <sup>(1)</sup>	CE to Output Delay		70		90		120	ns
t <sub>OE</sub> <sup>(2)</sup>	OE to Output Delay	0	35	0	40	0	50	ns
t <sub>DF</sub> <sup>(3)(4)</sup>	OE to Output Float	0	35	0	40	0	50	ns
t <sub>OH</sub>	Output Hold	0		0		0		ns

# 10. AC Read Waveforms<sup>(1)(2)(3)(4)</sup>

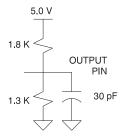


- Notes: 1.  $\overline{\text{CE}}$  may be delayed up to  $t_{\text{ACC}}$   $t_{\text{CE}}$  after the address transition without impact on  $t_{\text{ACC}}$ .
  - 2.  $\overline{\text{OE}}$  may be delayed up to  $t_{\text{CE}}$   $t_{\text{OE}}$  after the falling edge of  $\overline{\text{CE}}$  without impact on  $t_{\text{CE}}$  or by  $t_{\text{ACC}}$   $t_{\text{OE}}$  after an address change without impact on  $t_{\mbox{\scriptsize ACC}}.$
  - 3.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$  whichever occurs first ( $C_L$  = 5 pF).
  - 4. This parameter is characterized and is not 100% tested.

# 11. Input Test Waveforms and Measurement Level



# 12. Output Test Load



## 13. Pin Capacitance

 $f = 1 \text{ MHz}, T = 25^{\circ}C^{(1)}$ 

Symbol	Тур	Max	Units	Conditions
C <sub>IN</sub>	4	6	pF	V <sub>IN</sub> = 0 V
C <sub>OUT</sub>	8	12	pF	V <sub>OUT</sub> = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

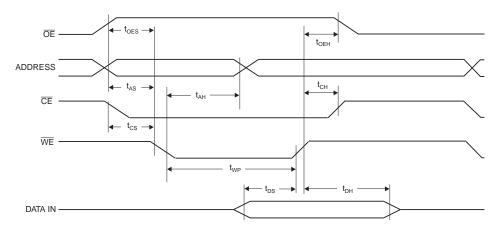


### 14. AC Write Characteristics

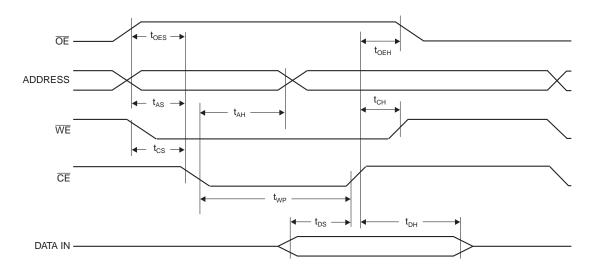
Symbol	Parameter	Min	Max	Units
$t_{AS}$ , $t_{OES}$	Address, OE Setup Time	0		ns
t <sub>AH</sub>	Address Hold Time	50		ns
t <sub>CS</sub>	Chip Select Setup Time	0		ns
t <sub>CH</sub>	Chip Select Hold Time	0		ns
t <sub>WP</sub>	Write Pulse Width (WE or CE)	100		ns
t <sub>DS</sub>	Data Setup Time	50		ns
t <sub>DH</sub> , t <sub>OEH</sub>	Data, OE Hold Time	0		ns

### 15. AC Write Waveforms

## 15.1 WE Controlled



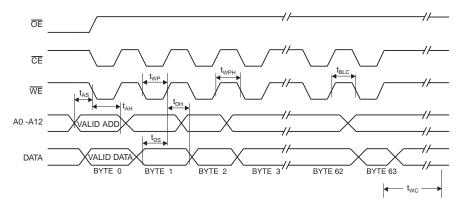
### 15.2 CE Controlled



# 16. Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t <sub>WC</sub>	Write Cycle Time		10	ms
t <sub>WC</sub>	Write Cycle Time (Use AT28HC64BF))		2	ms
t <sub>AS</sub>	Address Setup Time	0		ns
t <sub>AH</sub>	Address Hold Time	50		ns
t <sub>DS</sub>	Data Setup Time	50		ns
t <sub>DH</sub>	Data Hold Time	0		ns
t <sub>WP</sub>	Write Pulse Width	100		ns
t <sub>BLC</sub>	Byte Load Cycle Time		150	μs
t <sub>WPH</sub>	Write Pulse Width High	50		ns

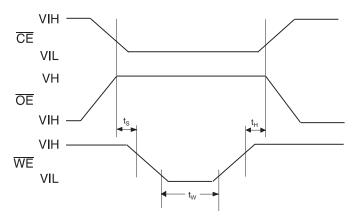
# 17. Page Mode Write Waveforms<sup>(1)(2)</sup>



Notes: 1. A6 through A12 must specify the same page address during each high to low transition of WE (or CE).

2.  $\overline{OE}$  must be high only when  $\overline{WE}$  and  $\overline{CE}$  are both low.

## 18. Chip Erase Waveforms

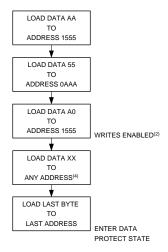


 $t_S = t_H = 5 \mu s \text{ (min.)}$   $t_W = 10 \text{ ms (min.)}$  $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$ 



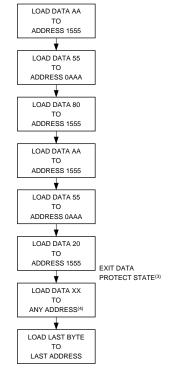


## 19. Software Data Protection Enable Algorithm<sup>(1)</sup>



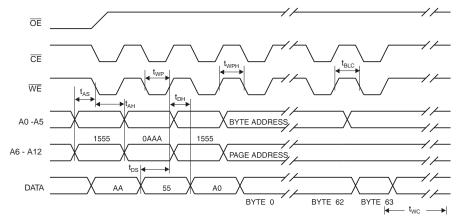
- Notes: 1. Data Format: I/O7 I/O0 (Hex); Address Format: A12 - A0 (Hex).
  - 2. Write Protect state will be activated at end of write even if no other data is loaded.
  - 3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
  - 4. 1 to 64 bytes of data are loaded.

## 20. Software Data Protection Disable Algorithm<sup>(1)</sup>



- Data Format: I/O7 I/O0 (Hex); Address Format: A12 - A0 (Hex).
- 2. Write Protect state will be activated at end of write even if no other data is loaded.
- Write Protect state will be deactivated at end of write period even if no other data is loaded.
- 4. 1 to 64 bytes of data are loaded.

## 21. Software Protected Write Cycle Waveforms<sup>(1)(2)</sup>



- 1. A6 through A12 must specify the same page address during each high to low transition of WE (or CE) after the software Notes: code has been entered.
  - 2. OE must be high only when WE and CE are both low.

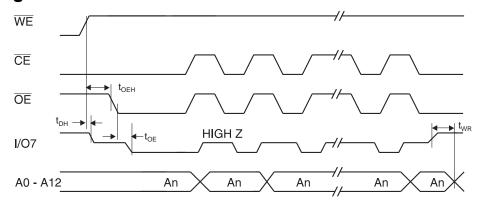
10

## 22. Data Polling Characteristics<sup>(1)</sup>

Symbol	Parameter	Min	Тур	Max	Units
t <sub>DH</sub>	Data Hold Time	0			ns
t <sub>OEH</sub>	OE Hold Time	0			ns
t <sub>OE</sub>	OE to Output Delay <sup>(1)</sup>				ns
t <sub>WR</sub>	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested. See "AC Read Characteristics" on page 6.

# 23. Data Polling Waveforms



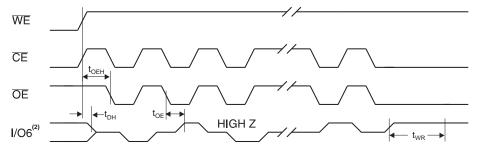
# 24. Toggle Bit Characteristics<sup>(1)</sup>

Symbol	Parameter	Min	Тур	Max	Units
t <sub>DH</sub>	Data Hold Time	10			ns
t <sub>OEH</sub>	OE Hold Time	10			ns
t <sub>OE</sub>	OE to Output Delay <sup>(2)</sup>				ns
t <sub>OEHP</sub>	OE High Pulse	150			ns
t <sub>WR</sub>	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

2. See "AC Read Characteristics" on page 6.

# 25. Toggle Bit Waveforms<sup>(1)(2)(3)</sup>



Notes: 1. Toggling either  $\overline{OE}$  or  $\overline{CE}$  or both  $\overline{OE}$  and  $\overline{CE}$  will operate toggle bit.

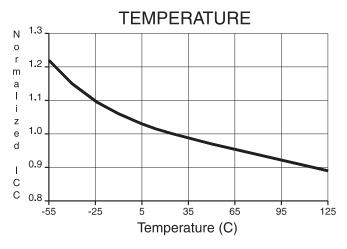
- 2. Beginning and ending state of I/O6 will vary.
- 3. Any address location may be used, but the address should not vary.



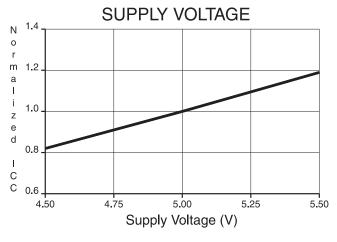


# 26. Normalized I<sub>CC</sub> Graphs

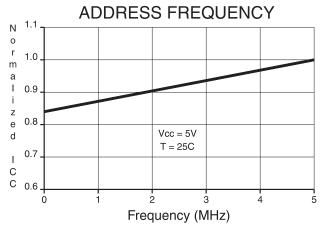
### NORMALIZED SUPPLY CURRENT vs.



## NORMALIZED SUPPLY CURRENT vs.



## NORMALIZED SUPPLY CURRENT vs.



# 27. Ordering Information

## 27.1 Green Package Option (Pb/Halide-free)

t <sub>ACC</sub> I <sub>CC</sub>		(mA)			
	Active	Standby	Ordering Code	Package	Operation Range
			AT28HC64B-70TU	28T	
70	40	0.1	AT28HC64B-70JU	32J	
			AT28HC64B-70SU	28S	
			AT28HC64B-90JU	32J	Industrial
90	40	0.1	AT28HC64B-90SU	28S	(-40°C to 85°C)
			AT28HC64B-90TU	28T	,
120	40	0.1	AT28HC64B-12JU	32J	
120	40	0.1	AT28HC64B-12SU	28S	

Package Type		
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)	
28S 28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)		
28T 28-lead, Plastic Thin Small Outline Package (TSOP)		

### 27.2 Die Products

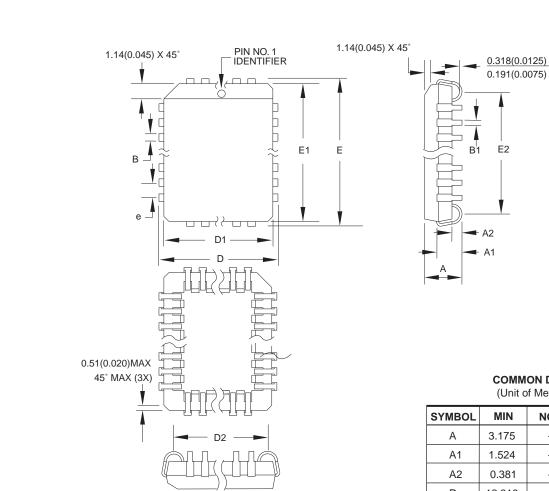
Contact Atmel Sales for die sales options.





## 28. Packaging Information

### 28.1 32J - PLCC



Notes:

- 1. This package conforms to JEDEC reference MS-016, Variation AE.
- Dimensions D1 and E1 do not include mold protrusion.
   Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
- 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

### COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
А	3.175	_	3.556	
A1	1.524	_	2.413	
A2	0.381	_	_	
D	12.319	_	12.573	
D1	11.354	_	11.506	Note 2
D2	9.906	_	10.922	
E	14.859	_	15.113	
E1	13.894	_	14.046	Note 2
E2	12.471	_	13.487	
В	0.660	_	0.813	
B1	0.330	_	0.533	
е		1.270 TYF	)	

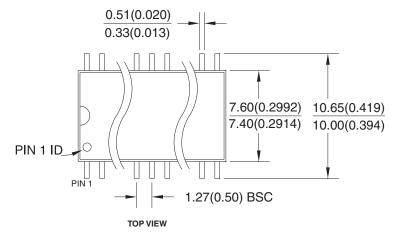
10/04/01

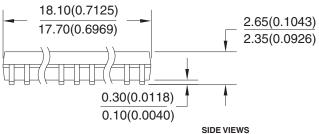
IIILE			
<b>32J</b> ,	32-lead,	, Plastic J-leaded Chip Carrier (PLCC	;)

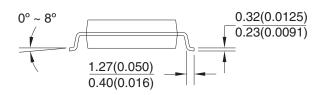
DRAWING NO.	REV
32J	В

#### 28.2 28S - SOIC

Dimensions in Millimeters and (Inches). Controlling dimension: Millimeters.







8/4/03

2325 Orchard Parkway San Jose, CA 95131 TITLE

**28S**, 28-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC) JEDEC Standard MS-013

DRAWING NO. REV.

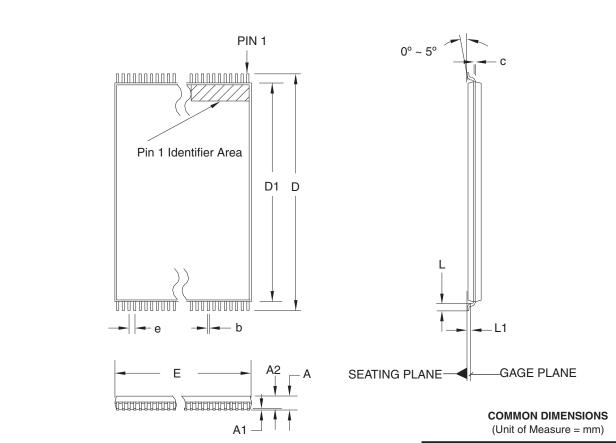
28S

В





#### 28.3 28T - TSOP



Notes:

- 1. This package conforms to JEDEC reference MO-183.
- 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
- 3. Lead coplanarity is 0.10 mm maximum.

(0 00000.0)					
SYMBOL	MIN	NOM	MAX	NOTE	
Α	_	_	1.20		
A1	0.05	_	0.15		
A2	0.90	1.00	1.05		
D	13.20	13.40	13.60		
D1	11.70	11.80	11.90	Note 2	
Е	7.90	8.00	8.10	Note 2	
L	0.50	0.60	0.70		
L1	0.25 BASIC				
b	0.17	0.22	0.27		
С	0.10	_	0.21		
е	0.55 BASIC				

12/06/02

Ī			DRAWING NO.	REV.
	2325 Orchard Parkway San Jose, CA 95131	<b>28T</b> , 28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)	28T	С



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OOO «ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

#### Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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