

FEATURES

Enhanced system-level ESD performance per IEC 61000-4-x

Low power operation

5 V operation

1.4 mA per channel maximum at 0 Mbps to 2 Mbps

4.3 mA per channel maximum at 10 Mbps

34 mA per channel maximum at 90 Mbps

3.3 V operation

0.9 mA per channel maximum at 0 Mbps to 2 Mbps

2.4 mA per channel maximum at 10 Mbps

20 mA per channel maximum at 90 Mbps

Bidirectional communication

3.3 V/5 V level translation

High temperature operation: 105°C

High data rate: dc to 90 Mbps (NRZ)

Precise timing characteristics

2 ns maximum pulse width distortion

2 ns maximum channel-to-channel matching

High common-mode transient immunity: >25 kV/ μ s

Output enable function

16-lead SOIC wide body, RoHS-compliant package

Safety and regulatory approvals

UL recognition: 2500 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

VDE Certificate of Conformity

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12

$V_{IORM} = 560$ V peak

APPLICATIONS

General-purpose multichannel isolation

SPI/data converter isolation

RS-232/RS-422/RS-485 transceivers

Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM3400/ADuM3401/ADuM3402¹ are 4-channel digital isolators based on the Analog Devices, Inc., *iCoupler*® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

iCoupler devices remove the design difficulties commonly associated with optocouplers. Typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *iCoupler* digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *iCoupler* products. Furthermore, *iCoupler* devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. The isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

In comparison to the ADuM1400/ADuM1401/ADuM1402 isolators, the ADuM3400/ADuM3401/ADuM3402 isolators contain various circuit and layout changes to provide increased capability relative to system-level IEC 61000-4-x testing (ESD/burst/surge). The precise capability in these tests for either set of isolators is strongly determined by the design and layout of the user board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

FUNCTIONAL BLOCK DIAGRAMS

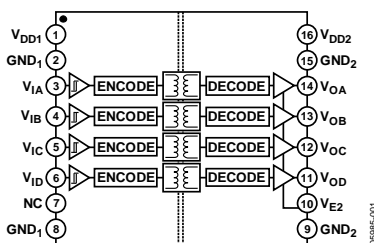


Figure 1. ADuM3400 Functional Block Diagram

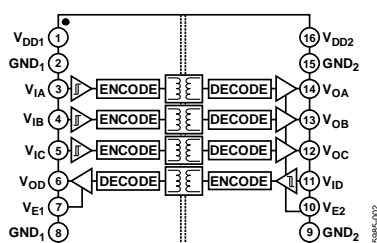


Figure 2. ADuM3401 Functional Block Diagram

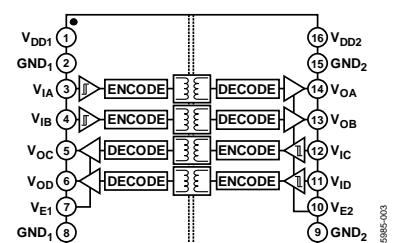


Figure 3. ADuM3402 Functional Block Diagram

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329.

Rev. F

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REVISION HISTORY

7/2017—Rev. E to Rev. F

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2/2012—Rev. A to Rev. B

| | |
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6/2007—Rev. 0 to Rev. A

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| Inserted Figure 21, Figure 22, and Figure 23 | 22 |
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3/2006—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--|--------------------------------|-------|------|---------------|--|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current per Channel, Quiescent | $I_{DD1(Q)}$ | | 0.57 | 0.83 | mA | |
| Output Supply Current per Channel, Quiescent | $I_{DD0(Q)}$ | | 0.29 | 0.35 | mA | |
| ADuM3400, Total Supply Current, Four Channels ¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | 2.9 | 3.5 | mA | DC to 1 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | 1.2 | 1.9 | mA | DC to 1 MHz logic signal freq. |
| 10 Mbps (BRW and CRW Grades Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | 9.0 | 11.6 | mA | 5 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | 3.0 | 5.5 | mA | 5 MHz logic signal freq. |
| 90 Mbps (CRW Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(90)}$ | | 72 | 100 | mA | 45 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(90)}$ | | 19 | 36 | mA | 45 MHz logic signal freq. |
| ADuM3401, Total Supply Current, Four Channels ¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | 2.5 | 3.2 | mA | DC to 1 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | 1.6 | 2.4 | mA | DC to 1 MHz logic signal freq. |
| 10 Mbps (BRW and CRW Grades Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | 7.4 | 10.6 | mA | 5 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | 4.4 | 6.5 | mA | 5 MHz logic signal freq. |
| 90 Mbps (CRW Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(90)}$ | | 59 | 82 | mA | 45 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(90)}$ | | 32 | 46 | mA | 45 MHz logic signal freq. |
| ADuM3402, Total Supply Current, Four Channels ¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} or V_{DD2} Supply Current | $I_{DD1(Q)}, I_{DD2(Q)}$ | | 2.0 | 2.8 | mA | DC to 1 MHz logic signal freq. |
| 10 Mbps (BRW and CRW Grades Only) | | | | | | |
| V_{DD1} or V_{DD2} Supply Current | $I_{DD1(10)}, I_{DD2(10)}$ | | 6.0 | 7.5 | mA | 5 MHz logic signal freq. |
| 90 Mbps (CRW Grade Only) | | | | | | |
| V_{DD1} or V_{DD2} Supply Current | $I_{DD1(90)}, I_{DD2(90)}$ | | 51 | 62 | mA | 45 MHz logic signal freq. |
| For All Models | | | | | | |
| Input Currents | $I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}$ | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1}$ or V_{DD2} , $0\text{ V} \leq V_{E1}, V_{E2} \leq V_{DD1}$ or V_{DD2} |
| Logic High Input Threshold | V_{IH}, V_{EH} | 2.0 | | | V | |
| Logic Low Input Threshold | V_{IL}, V_{EL} | | | 0.8 | V | |
| Logic High Output Voltages | $V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}$ | $(V_{DD1}$ or $V_{DD2}) - 0.1$ | 5.0 | | V | $I_{OX} = -20\ \mu\text{A}, V_{IX} = V_{IXH}$ |
| | | $(V_{DD1}$ or $V_{DD2}) - 0.4$ | 4.8 | | V | $I_{OX} = -3.2\ \text{mA}, V_{IX} = V_{IXH}$ |
| Logic Low Output Voltages | $V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}$ | | 0.0 | 0.1 | V | $I_{OX} = 20\ \mu\text{A}, V_{IX} = V_{IXL}$ |
| | | | 0.04 | 0.1 | V | $I_{OX} = 400\ \mu\text{A}, V_{IX} = V_{IXL}$ |
| | | | 0.2 | 0.4 | V | $I_{OX} = 3.2\ \text{mA}, V_{IX} = V_{IXL}$ |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-------------------------------------|-----|-----|------|-------|--|
| SWITCHING SPECIFICATIONS | | | | | | |
| ARW Package | | | | | | |
| Minimum Pulse Width ² | PW | | | 1000 | ns | C _L = 15 pF, CMOS signal levels |
| Maximum Data Rate ³ | | 1 | | | Mbps | C _L = 15 pF, CMOS signal levels |
| Propagation Delay ⁴ | t _{PHL} , t _{PLH} | 50 | 65 | 100 | ns | C _L = 15 pF, CMOS signal levels |
| Pulse Width Distortion, t _{PLH} – t _{PHL} ⁴ | PWD | | | 40 | ns | C _L = 15 pF, CMOS signal levels |
| Propagation Delay Skew ⁵ | t _{PSK} | | | 50 | ns | C _L = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching ⁶ | t _{PSKCD/OD} | | | 50 | ns | C _L = 15 pF, CMOS signal levels |
| BRW Package | | | | | | |
| Minimum Pulse Width ² | PW | | | 100 | ns | C _L = 15 pF, CMOS signal levels |
| Maximum Data Rate ³ | | 10 | | | Mbps | C _L = 15 pF, CMOS signal levels |
| Propagation Delay ⁴ | t _{PHL} , t _{PLH} | 20 | 32 | 50 | ns | C _L = 15 pF, CMOS signal levels |
| Pulse Width Distortion, t _{PLH} – t _{PHL} ⁴ | PWD | | | 3 | ns | C _L = 15 pF, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | C _L = 15 pF, CMOS signal levels |
| Propagation Delay Skew ⁵ | t _{PSK} | | | 15 | ns | C _L = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels ⁶ | t _{PSKCD} | | | 3 | ns | C _L = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels ⁶ | t _{PSKOD} | | | 6 | ns | C _L = 15 pF, CMOS signal levels |
| CRW Package | | | | | | |
| Minimum Pulse Width ² | PW | | 8.3 | 11.1 | ns | C _L = 15 pF, CMOS signal levels |
| Maximum Data Rate ³ | | 90 | 120 | | Mbps | C _L = 15 pF, CMOS signal levels |
| Propagation Delay ⁴ | t _{PHL} , t _{PLH} | 18 | 27 | 32 | ns | C _L = 15 pF, CMOS signal levels |
| Pulse Width Distortion, t _{PLH} – t _{PHL} ⁴ | PWD | | 0.5 | 2 | ns | C _L = 15 pF, CMOS signal levels |
| Change vs. Temperature | | | 3 | | ps/°C | C _L = 15 pF, CMOS signal levels |
| Propagation Delay Skew ⁵ | t _{PSK} | | | 10 | ns | C _L = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels ⁶ | t _{PSKCD} | | | 2 | ns | C _L = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels ⁶ | t _{PSKOD} | | | 5 | ns | C _L = 15 pF, CMOS signal levels |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--------------------|-----|------|-----|-------------|---|
| For All Models | | | | | | |
| Output Disable Propagation Delay (High/Low-to-High Impedance) | t_{PHZ}, t_{PLH} | | 6 | 8 | ns | $C_L = 15$ pF, CMOS signal levels |
| Output Enable Propagation Delay (High Impedance-to-High/Low) | t_{PZH}, t_{PZL} | | 6 | 8 | ns | $C_L = 15$ pF, CMOS signal levels |
| Output Rise/Fall Time (10% to 90%) | t_R/t_F | | 2.5 | | ns | $C_L = 15$ pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output ⁷ | $ CM_H $ | 25 | 35 | | kV/ μ s | $V_{ix} = V_{DD1}/V_{DD2}$, $V_{CM} = 1000$ V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output ⁷ | $ CM_L $ | 25 | 35 | | kV/ μ s | $V_{ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V |
| Refresh Rate | f_r | | 1.2 | | Mbps | |
| Input Dynamic Supply Current per Channel ⁸ | $I_{DDI(D)}$ | | 0.20 | | mA/Mbps | |
| Output Dynamic Supply Current per Channel ⁸ | $I_{DDO(D)}$ | | 0.05 | | mA/Mbps | |

¹ The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM3400/ADuM3401/ADuM3402 channel configurations.

² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective ground. $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.3\text{ V}$.

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--|--------------------------------|-------|------|---------------|--|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current per Channel, Quiescent | $I_{DD1(Q)}$ | | 0.31 | 0.49 | mA | |
| Output Supply Current per Channel, Quiescent | $I_{DDO(Q)}$ | | 0.19 | 0.27 | mA | |
| ADuM3400 , Total Supply Current, Four Channels ¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | 1.6 | 2.1 | mA | DC to 1 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | 0.7 | 1.2 | mA | DC to 1 MHz logic signal freq. |
| 10 Mbps (BRW and CRW Grades Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | 4.8 | 7.1 | mA | 5 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | 1.8 | 2.3 | mA | 5 MHz logic signal freq. |
| 90 Mbps (CRW Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(90)}$ | | 37 | 54 | mA | 45 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(90)}$ | | 11 | 15 | mA | 45 MHz logic signal freq. |
| ADuM3401 , Total Supply Current, Four Channels ¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | 1.4 | 1.9 | mA | DC to 1 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | 0.9 | 1.5 | mA | DC to 1 MHz logic signal freq. |
| 10 Mbps (BRW and CRW Grades Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | 4.1 | 5.6 | mA | 5 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | 2.5 | 3.3 | mA | 5 MHz logic signal freq. |
| 90 Mbps (CRW Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(90)}$ | | 31 | 44 | mA | 45 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(90)}$ | | 17 | 24 | mA | 45 MHz logic signal freq. |
| ADuM3402 , Total Supply Current, Four Channels ¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} or V_{DD2} Supply Current | $I_{DD1(Q)}, I_{DD2(Q)}$ | | 1.2 | 1.7 | mA | DC to 1 MHz logic signal freq. |
| 10 Mbps (BRW and CRW Grades Only) | | | | | | |
| V_{DD1} or V_{DD2} Supply Current | $I_{DD1(10)}, I_{DD2(10)}$ | | 3.3 | 4.4 | mA | 5 MHz logic signal freq. |
| 90 Mbps (CRW Grade Only) | | | | | | |
| V_{DD1} or V_{DD2} Supply Current | $I_{DD1(90)}, I_{DD2(90)}$ | | 24 | 39 | mA | 45 MHz logic signal freq. |
| For All Models | | | | | | |
| Input Currents | $I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}$ | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1}$ or V_{DD2} , $0\text{ V} \leq V_{E1}, V_{E2} \leq V_{DD1}$ or V_{DD2} |
| Logic High Input Threshold | V_{IH}, V_{EH} | 1.6 | | | V | |
| Logic Low Input Threshold | V_{IL}, V_{EL} | | | 0.4 | V | |
| Logic High Output Voltages | $V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}$ | $(V_{DD1}$ or $V_{DD2}) - 0.1$ | 3.0 | | V | $I_{OX} = -20\text{ }\mu\text{A}, V_{IX} = V_{IXH}$ |
| | | $(V_{DD1}$ or $V_{DD2}) - 0.4$ | 2.8 | | V | $I_{OX} = -3.2\text{ mA}, V_{IX} = V_{IXH}$ |
| Logic Low Output Voltages | $V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}$ | | 0.0 | 0.1 | V | $I_{OX} = 20\text{ }\mu\text{A}, V_{IX} = V_{IXL}$ |
| | | | 0.04 | 0.1 | V | $I_{OX} = 400\text{ }\mu\text{A}, V_{IX} = V_{IXL}$ |
| | | | 0.2 | 0.4 | V | $I_{OX} = 3.2\text{ mA}, V_{IX} = V_{IXL}$ |
| SWITCHING SPECIFICATIONS | | | | | | |
| ARW Package | | | | | | |
| Minimum Pulse Width ² | PW | | | 1000 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | 1 | | | Mbps | $C_L = 15\text{ pF}$, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 50 | 75 | 100 | ns | $C_L = 15\text{ pF}$, CMOS signal levels |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------------|-----|------|------|---------|--|
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^4$ | PWD | | | 40 | ns | $C_L = 15$ pF, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 50 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching ⁶ | $t_{PSKCD/OD}$ | | | 50 | ns | $C_L = 15$ pF, CMOS signal levels |
| BRW Package | | | | | | |
| Minimum Pulse Width ² | PW | | | 100 | ns | $C_L = 15$ pF, CMOS signal levels |
| Maximum Data Rate ³ | | 10 | | | Mbps | $C_L = 15$ pF, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 20 | 38 | 50 | ns | $C_L = 15$ pF, CMOS signal levels |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^4$ | PWD | | | 3 | ns | $C_L = 15$ pF, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | $C_L = 15$ pF, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 22 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels ⁶ | t_{PSKCD} | | | 3 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels ⁶ | t_{PSKOD} | | | 6 | ns | $C_L = 15$ pF, CMOS signal levels |
| CRW Package | | | | | | |
| Minimum Pulse Width ² | PW | | 8.3 | 11.1 | ns | $C_L = 15$ pF, CMOS signal levels |
| Maximum Data Rate ³ | | 90 | 120 | | Mbps | $C_L = 15$ pF, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 20 | 34 | 45 | ns | $C_L = 15$ pF, CMOS signal levels |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^4$ | PWD | | 0.5 | 2 | ns | $C_L = 15$ pF, CMOS signal levels |
| Change vs. Temperature | | | 3 | | ps/°C | $C_L = 15$ pF, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 16 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels ⁶ | t_{PSKCD} | | | 2 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels ⁶ | t_{PSKOD} | | | 5 | ns | $C_L = 15$ pF, CMOS signal levels |
| For All Models | | | | | | |
| Output Disable Propagation Delay (High/Low-to-High Impedance) | t_{PHZ}, t_{PLH} | | 6 | 8 | ns | $C_L = 15$ pF, CMOS signal levels |
| Output Enable Propagation Delay (High Impedance-to-High/Low) | t_{PZH}, t_{PZL} | | 6 | 8 | ns | $C_L = 15$ pF, CMOS signal levels |
| Output Rise/Fall Time (10% to 90%) | t_R/t_F | | 3 | | ns | $C_L = 15$ pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output ⁷ | $ CM_H $ | 25 | 35 | | kV/μs | $V_{ix} = V_{DD1}/V_{DD2}, V_{CM} = 1000$ V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output ⁷ | $ CM_L $ | 25 | 35 | | kV/μs | $V_{ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V |
| Refresh Rate | f_r | | 1.1 | | Mbps | |
| Input Dynamic Supply Current per Channel ⁸ | $I_{DDI(D)}$ | | 0.10 | | mA/Mbps | |
| Output Dynamic Supply Current per Channel ⁸ | $I_{DDO(D)}$ | | 0.03 | | mA/Mbps | |

¹ The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM3400/ADuM3401/ADuM3402 channel configurations.

² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OR 3.3 V/5 V OPERATION

All voltages are relative to their respective ground. 5 V/3.3 V operation: $4.5 \text{ V} \leq V_{DD1} \leq 5.5 \text{ V}$, $3.0 \text{ V} \leq V_{DD2} \leq 3.6 \text{ V}$; 3.3 V/5 V operation: $3.0 \text{ V} \leq V_{DD1} \leq 3.6 \text{ V}$, $4.5 \text{ V} \leq V_{DD2} \leq 5.5 \text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$; $V_{DD1} = 3.3 \text{ V}$, $V_{DD2} = 5 \text{ V}$ or $V_{DD1} = 5 \text{ V}$, $V_{DD2} = 3.3 \text{ V}$.

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|---------------|-----|------|------|------|--------------------------------|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current per Channel, Quiescent | $I_{DD1(Q)}$ | | | | | |
| 5 V/3.3 V Operation | | | 0.57 | 0.83 | mA | |
| 3.3 V/5 V Operation | | | 0.31 | 0.49 | mA | |
| Output Supply Current per Channel, Quiescent | $I_{DDO(Q)}$ | | | | | |
| 5 V/3.3 V Operation | | | 0.29 | 0.27 | mA | |
| 3.3 V/5 V Operation | | | 0.19 | 0.35 | mA | |
| ADuM3400, Total Supply Current, Four Channels¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | | | | |
| 5 V/3.3 V Operation | | | 2.9 | 3.5 | mA | DC to 1 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 1.6 | 2.1 | mA | DC to 1 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | | | | |
| 5 V/3.3 V Operation | | | 0.7 | 1.2 | mA | DC to 1 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 1.2 | 1.9 | mA | DC to 1 MHz logic signal freq. |
| 10 Mbps (BRW and CRW Grades Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | | | | |
| 5 V/3.3 V Operation | | | 9.0 | 11.6 | mA | 5 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 4.8 | 7.1 | mA | 5 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | | | | |
| 5 V/3.3 V Operation | | | 1.8 | 2.3 | mA | 5 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 3.0 | 5.5 | mA | 5 MHz logic signal freq. |
| 90 Mbps (CRW Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(90)}$ | | | | | |
| 5 V/3.3 V Operation | | | 72 | 100 | mA | 45 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 37 | 54 | mA | 45 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(90)}$ | | | | | |
| 5 V/3.3 V Operation | | | 11 | 15 | mA | 45 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 19 | 36 | mA | 45 MHz logic signal freq. |
| ADuM3401, Total Supply Current, Four Channels¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | | | | |
| 5 V/3.3 V Operation | | | 2.5 | 3.2 | mA | DC to 1 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 1.4 | 1.9 | mA | DC to 1 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | | | | |
| 5 V/3.3 V Operation | | | 0.9 | 1.5 | mA | DC to 1 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 1.6 | 2.4 | mA | DC to 1 MHz logic signal freq. |
| 10 Mbps (BRW and CRW Grades Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | | | | |
| 5 V/3.3 V Operation | | | 7.4 | 10.6 | mA | 5 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 4.1 | 5.6 | mA | 5 MHz logic signal freq. |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | | | | |
| 5 V/3.3 V Operation | | | 2.5 | 3.3 | mA | 5 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 4.4 | 6.5 | mA | 5 MHz logic signal freq. |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--|---|---|-------------------|-------------|--|
| 90 Mbps (CRW Grade Only) | | | | | | |
| V _{DD1} Supply Current | I _{DD1 (90)} | | | | | |
| 5 V/3.3 V Operation | | | 59 | 82 | mA | 45 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 31 | 44 | mA | 45 MHz logic signal freq. |
| V _{DD2} Supply Current | I _{DD2 (90)} | | | | | |
| 5 V/3.3 V Operation | | | 17 | 24 | mA | 45 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 32 | 46 | mA | 45 MHz logic signal freq. |
| ADuM3402, Total Supply Current, Four Channels ¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V _{DD1} Supply Current | I _{DD1 (Q)} | | | | | |
| 5 V/3.3 V Operation | | | 2.0 | 2.8 | mA | DC to 1 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 1.2 | 1.7 | mA | DC to 1 MHz logic signal freq. |
| V _{DD2} Supply Current | I _{DD2 (Q)} | | | | | |
| 5 V/3.3 V Operation | | | 1.2 | 1.7 | mA | DC to 1 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 2.0 | 2.8 | mA | DC to 1 MHz logic signal freq. |
| 10 Mbps (BRW and CRW Grades Only) | | | | | | |
| V _{DD1} Supply Current | I _{DD1 (10)} | | | | | |
| 5 V/3.3 V Operation | | | 6.0 | 7.5 | mA | 5 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 3.3 | 4.4 | mA | 5 MHz logic signal freq. |
| V _{DD2} Supply Current | I _{DD2 (10)} | | | | | |
| 5 V/3.3 V Operation | | | 3.3 | 4.4 | mA | 5 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 6.0 | 7.5 | mA | 5 MHz logic signal freq. |
| 90 Mbps (CRW Grade Only) | | | | | | |
| V _{DD1} Supply Current | I _{DD1 (90)} | | | | | |
| 5 V/3.3 V Operation | | | 46 | 62 | mA | 45 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 24 | 39 | mA | 45 MHz logic signal freq. |
| V _{DD2} Supply Current | I _{DD2 (90)} | | | | | |
| 5 V/3.3 V Operation | | | 24 | 39 | mA | 45 MHz logic signal freq. |
| 3.3 V/5 V Operation | | | 46 | 62 | mA | 45 MHz logic signal freq. |
| For All Models | | | | | | |
| Input Currents | I _{IA} , I _{IB} , I _{IC} , I _{ID} , I _{E1} , I _{E2} | -10 | +0.01 | +10 | μA | 0 V ≤ V _{IA} , V _{IB} , V _{IC} , V _{ID} ≤ V _{DD1} or V _{DD2} , 0 V ≤ V _{E1} , V _{E2} ≤ V _{DD1} or V _{DD2} |
| Logic High Input Threshold | V _{IH} , V _{EH} | | | | | |
| 5 V/3.3 V Operation | | 2.0 | | | V | |
| 3.3 V/5 V Operation | | 1.6 | | | V | |
| Logic Low Input Threshold | V _{IL} , V _{EL} | | | | | |
| 5 V/3.3 V Operation | | | | 0.8 | V | |
| 3.3 V/5 V Operation | | | | 0.4 | V | |
| Logic High Output Voltages | V _{OAH} , V _{OBH} | (V _{DD1} or V _{DD2}) - 0.1 | (V _{DD1} or V _{DD2}) - 0.1 | | V | I _{OX} = -20 μA, V _{IX} = V _{IXH} |
| | V _{OCH} , V _{ODH} | (V _{DD1} or V _{DD2}) - 0.4 | (V _{DD1} or V _{DD2}) - 0.2 | | V | I _{OX} = -3.2 mA, V _{IX} = V _{IXH} |
| Logic Low Output Voltages | V _{OAL} , V _{OBL} , V _{OCL} , V _{ODL} | | 0.0 0.04 0.2 | 0.1 0.1 0.4 | V V V | I _{OX} = 20 μA, V _{IX} = V _{IXL} I _{OX} = 400 μA, V _{IX} = V _{IXL} I _{OX} = 3.2 mA, V _{IX} = V _{IXL} |
| SWITCHING SPECIFICATIONS | | | | | | |
| ARW Package | | | | | | |
| Minimum Pulse Width ² | PW | | | 1000 | ns | C _L = 15 pF, CMOS signal levels |
| Maximum Data Rate ³ | | 1 | | | Mbps | C _L = 15 pF, CMOS signal levels |
| Propagation Delay ⁴ | t _{PHL} , t _{PLH} | 50 | 70 | 100 | ns | C _L = 15 pF, CMOS signal levels |
| Pulse Width Distortion, t _{PLH} - t _{PHL} ⁴ | PWD | | | 40 | ns | C _L = 15 pF, CMOS signal levels |
| Propagation Delay Skew ⁵ | t _{PSK} | | | 50 | ns | C _L = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching ⁶ | t _{PSKCD/OD} | | | 50 | ns | C _L = 15 pF, CMOS signal levels |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------------|-----|-----|------|-------------|--|
| BRW Package | | | | | | |
| Minimum Pulse Width ² | PW | | | 100 | ns | $C_L = 15$ pF, CMOS signal levels |
| Maximum Data Rate ³ | | 10 | | | Mbps | $C_L = 15$ pF, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 15 | 35 | 50 | ns | $C_L = 15$ pF, CMOS signal levels |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴ | PWD | | | 3 | ns | $C_L = 15$ pF, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | $C_L = 15$ pF, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 22 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels ⁶ | t_{PSKCD} | | | 3 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels ⁶ | t_{PSKOD} | | | 6 | ns | $C_L = 15$ pF, CMOS signal levels |
| CRW Package | | | | | | |
| Minimum Pulse Width ² | PW | | 8.3 | 11.1 | ns | $C_L = 15$ pF, CMOS signal levels |
| Maximum Data Rate ³ | | 90 | 120 | | Mbps | $C_L = 15$ pF, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 20 | 30 | 40 | ns | $C_L = 15$ pF, CMOS signal levels |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴ | PWD | | 0.5 | 2 | ns | $C_L = 15$ pF, CMOS signal levels |
| Change vs. Temperature | | | 3 | | ps/°C | $C_L = 15$ pF, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 14 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels ⁶ | t_{PSKCD} | | | 2 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels ⁶ | t_{PSKOD} | | | 5 | ns | $C_L = 15$ pF, CMOS signal levels |
| For All Models | | | | | | |
| Output Disable Propagation Delay (High/Low-to-High Impedance) | t_{PHZ}, t_{PLH} | | 6 | 8 | ns | $C_L = 15$ pF, CMOS signal levels |
| Output Enable Propagation Delay (High Impedance-to-High/Low) | t_{PZH}, t_{PZL} | | 6 | 8 | ns | $C_L = 15$ pF, CMOS signal levels |
| Output Rise/Fall Time (10% to 90%) | t_R/t_F | | | | | $C_L = 15$ pF, CMOS signal levels |
| 5 V/3.3 V Operation | | | 3.0 | | ns | |
| 3.3 V/5 V Operation | | | 2.5 | | ns | |
| Common-Mode Transient Immunity at Logic High Output ⁷ | $ CM_H $ | 25 | 35 | | kV/ μ s | $V_{IX} = V_{DD1}/V_{DD2}, V_{CM} = 1000$ V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output ⁷ | $ CM_L $ | 25 | 35 | | kV/ μ s | $V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--------------|-----|------|-----|---------|--------------------------|
| Refresh Rate | f_r | | | | | |
| 5 V/3.3 V Operation | | | 1.2 | | Mbps | |
| 3.3 V/5 V Operation | | | 1.1 | | Mbps | |
| Input Dynamic Supply Current per Channel ⁸ | $I_{DDI(D)}$ | | | | | |
| 5 V/3.3 V Operation | | | 0.20 | | mA/Mbps | |
| 3.3 V/5 V Operation | | | 0.10 | | mA/Mbps | |
| Output Dynamic Supply Current per Channel ⁸ | $I_{DDO(D)}$ | | | | | |
| 5 V/3.3 V Operation | | | 0.03 | | mA/Mbps | |
| 3.3 V/5 V Operation | | | 0.05 | | mA/Mbps | |

¹ The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM3400/ADuM3401/ADuM3402 channel configurations.

² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8 V$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 4.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------------------|-----|------------------|-----|------|---|
| Resistance (Input-to-Output) ¹ | R _{I-O} | | 10 ¹² | | Ω | |
| Capacitance (Input-to-Output) ¹ | C _{I-O} | | 2.2 | | pF | f = 1 MHz |
| Input Capacitance ² | C _I | | 4.0 | | pF | |
| IC Junction-to-Case Thermal Resistance, Side 1 | θ _{JCI} | | 33 | | °C/W | Thermocouple located at center of package underside |
| IC Junction-to-Case Thermal Resistance, Side 2 | θ _{JCO} | | 28 | | °C/W | |

¹ Device considered a 2-terminal device; Pin 1 to Pin 8 are shorted together and Pin 9 to Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM3400/ADuM3401/ADuM3402 are approved by the organizations listed in Table 5. Refer to Table 10 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 5.

| UL | CSA | CQC | VDE |
|--|--|---|--|
| Recognized Under 1577 Component Recognition Program ¹ | Approved under CSA Component Acceptance Notice 5A | Approved under CQC11-471543-2012 | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ² |
| Single Protection, 2500 V rms Isolation Voltage | Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage | Basic insulation per GB4943.1-2011 400 V rms (588 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 meters | Reinforced insulation, 560 V peak |
| File E214100 | File 205078 | File CQC14001117249 | File 2471900-4880-0001 |

¹ In accordance with UL 1577, each ADuM3400/ADuM3401/ADuM3402 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).

² In accordance with DIN V VDE V 0884-10, each ADuM3400/ADuM3401/ADuM3402 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

| Parameter | Symbol | Value | Unit | Conditions |
|--|--------|-----------|-------|--|
| Rated Dielectric Insulation Voltage | | 2500 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 7.7 min | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 8.1 min | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 min | mm | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 7.

| Description | Conditions | Symbol | Characteristic | Unit |
|---|--|------------|--------------------------------|--------|
| Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms | | | I to IV I to III I to II | |
| Climatic Classification | | | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum Working Insulation Voltage | | V_{IORM} | 560 | V peak |
| Input-to-Output Test Voltage, Method B1 | $V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC | V_{PR} | 1050 | V peak |
| Input-to-Output Test Voltage, Method A | $V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC | V_{PR} | | |
| After Environmental Tests Subgroup 1 | | | 896 | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC | | 672 | V peak |
| Highest Allowable Overvoltage | Transient overvoltage, $t_{TR} = 10$ seconds | V_{TR} | 4000 | V peak |
| Safety-Limiting Values | Maximum value allowed in the event of a failure (see Figure 4) | | | |
| Case Temperature | | T_S | 150 | °C |
| Side 1 Current | | I_{S1} | 265 | mA |
| Side 2 Current | | I_{S2} | 335 | mA |
| Insulation Resistance at T_S | $V_{IO} = 500$ V | R_S | >10 ⁹ | Ω |



Figure 4. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 8.

| Parameter | Rating |
|--|-----------------|
| Operating Temperature Range (T_A) | -40°C to +105°C |
| Supply Voltages (V_{DD1} , V_{DD2}) ¹ | 3.0 V to 5.5 V |
| Input Signal Rise and Fall Times | 1.0 ms |

¹ All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

| Parameter | Rating |
|---|-----------------------------|
| Storage Temperature Range (T_{ST}) | -65°C to +150°C |
| Ambient Operating Temperature Range (T_A) | -40°C to +105°C |
| Supply Voltages (V_{DD1} , V_{DD2}) ¹ | -0.5 V to +7.0 V |
| Input Voltage (V_{IA} , V_{IB} , V_{IC} , V_{ID} , V_{E1} , V_{E2}) ^{1, 2} | -0.5 V to $V_{DD1} + 0.5$ V |
| Output Voltage (V_{OA} , V_{OB} , V_{OC} , V_{OD}) ^{1, 2} | -0.5 V to $V_{DD0} + 0.5$ V |
| Average Output Current per Pin ³ | |
| Side 1 (I_{O1}) | -18 mA to +18 mA |
| Side 2 (I_{O2}) | -22 mA to +22 mA |
| Common-Mode Transients (CM_H , CM_L) ⁴ | -100 kV/μs to +100 kV/μs |

¹ All voltages are relative to their respective ground.

² V_{DD1} and V_{DD0} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.

³ See Figure 4 for maximum rated current values for various temperatures.

⁴ Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage¹

| Parameter | Max | Unit | Constraint |
|-------------------------------|------|--------|--|
| AC Voltage, Bipolar Waveform | 565 | V peak | 50-year minimum lifetime |
| AC Voltage, Unipolar Waveform | | | |
| Basic Insulation | 1131 | V peak | Maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 560 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |
| DC Voltage | | | |
| Basic Insulation | 1131 | V peak | Maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 560 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |

¹ Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 11. Truth Table (Positive Logic)

| V_{IX} Input ¹ | V_{EX} Input ² | V_{DD1} State ¹ | V_{DD0} State ¹ | V_{OX} Output ¹ | Notes |
|-----------------------------|-----------------------------|------------------------------|------------------------------|------------------------------|--|
| H | H or NC | Powered | Powered | H | |
| L | H or NC | Powered | Powered | L | |
| x | L | Powered | Powered | Z | |
| x | H or NC | Unpowered | Powered | H | Outputs return to the input state within 1 μs of V_{DD1} power restoration. |
| x | L | Unpowered | Powered | Z | |
| x | x | Powered | Unpowered | Indeterminate | Outputs return to the input state within 1 μs of V_{DD0} power restoration if V_{EX} state is H or NC. Outputs return to high impedance state within 8 ns of V_{DD0} power restoration if V_{EX} state is L. |

¹ V_{IX} and V_{OX} refer to the input and output signals of a given channel (A, B, C, or D). V_{EX} refers to the output enable signal on the same side as the V_{OX} outputs. V_{DD1} and V_{DD0} refer to the supply voltages on the input and output sides of the given channel, respectively.

² In noisy environments, connecting V_{EX} to an external logic high or low is recommended.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND₁ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND₂ IS RECOMMENDED. IN NOISY ENVIRONMENTS, CONNECTING OUTPUT ENABLES (PIN 7 FOR ADuM3401/ADuM3402 AND PIN 10 FOR ALL MODELS) TO AN EXTERNAL LOGIC HIGH OR LOW IS RECOMMENDED.

Figure 5. ADuM3400 Pin Configuration

Table 12. ADuM3400 Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|------------------|--|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 2, 8 | GND ₁ | Ground 1. Ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{IC} | Logic Input C. |
| 6 | V _{ID} | Logic Input D. |
| 7 | NC | No Connect. |
| 9, 15 | GND ₂ | Ground 2. Ground reference for Isolator Side 2. |
| 10 | V _{E2} | Output Enable 2. Active high logic input. V _{OA} , V _{OB} , V _{OC} , and V _{OD} outputs are enabled when V _{E2} is high or disconnected. V _{OA} , V _{OB} , V _{OC} , and V _{OD} outputs are disabled when V _{E2} is low. In noisy environments, connecting V _{E2} to an external logic high or low is recommended. |
| 11 | V _{OD} | Logic Output D. |
| 12 | V _{OC} | Logic Output C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND₁ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND₂ IS RECOMMENDED. IN NOISY ENVIRONMENTS, CONNECTING OUTPUT ENABLES (PIN 7 FOR ADuM3401/ADuM3402 AND PIN 10 FOR ALL MODELS) TO AN EXTERNAL LOGIC HIGH OR LOW IS RECOMMENDED.

Figure 6. ADuM3401 Pin Configuration

Table 13. ADuM3401 Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|------------------|--|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 2, 8 | GND ₁ | Ground 1. Ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{IC} | Logic Input C. |
| 6 | V _{OD} | Logic Output D. |
| 7 | V _{E1} | Output Enable 1. Active high logic input. V _{OD} output is enabled when V _{E1} is high or disconnected. V _{OD} is disabled when V _{E1} is low. In noisy environments, connecting V _{E1} to an external logic high or low is recommended. |
| 9, 15 | GND ₂ | Ground 2. Ground reference for Isolator Side 2. |
| 10 | V _{E2} | Output Enable 2. Active high logic input. V _{OA} , V _{OB} , and V _{OC} outputs are enabled when V _{E2} is high or disconnected. V _{OA} , V _{OB} , and V _{OC} outputs are disabled when V _{E2} is low. In noisy environments, connecting V _{E2} to an external logic high or low is recommended. |
| 11 | V _{ID} | Logic Input D. |
| 12 | V _{OC} | Logic Output C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND₁ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND₂ IS RECOMMENDED. IN NOISY ENVIRONMENTS, CONNECTING OUTPUT ENABLES (PIN 7 FOR ADuM3401/ADuM3402 AND PIN 10 FOR ALL MODELS) TO AN EXTERNAL LOGIC HIGH OR LOW IS RECOMMENDED.

Figure 7. ADuM3402 Pin Configuration

Table 14. ADuM3402 Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|------------------|--|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 2, 8 | GND ₁ | Ground 1. Ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{OC} | Logic Output C. |
| 6 | V _{OD} | Logic Output D. |
| 7 | V _{E1} | Output Enable 1. Active high logic input. V _{OC} and V _{OD} outputs are enabled when V _{E1} is high or disconnected. V _{OC} and V _{OD} outputs are disabled when V _{E1} is low. In noisy environments, connecting V _{E1} to an external logic high or low is recommended. |
| 9, 15 | GND ₂ | Ground 2. Ground reference for Isolator Side 2. |
| 10 | V _{E2} | Output Enable 2. Active high logic input. V _{OA} and V _{OB} outputs are enabled when V _{E2} is high or disconnected. V _{OA} and V _{OB} outputs are disabled when V _{E2} is low. In noisy environments, connecting V _{E2} to an external logic high or low is recommended. |
| 11 | V _{ID} | Logic Input D. |
| 12 | V _{IC} | Logic Input C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 8. Typical Input Supply Current per Channel vs. Data Rate (No Load)



Figure 11. Typical ADuM3400 V_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation



Figure 9. Typical Output Supply Current per Channel vs. Data Rate (No Load)



Figure 12. Typical ADuM3400 V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation



Figure 10. Typical Output Supply Current per Channel vs. Data Rate (15 pF Output Load)



Figure 13. Typical ADuM3401 V_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation



Figure 14. Typical ADuM3401 V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation



Figure 16. Propagation Delay vs. Temperature, C Grade



Figure 15. Typical ADuM3402 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

APPLICATION INFORMATION

PC BOARD LAYOUT

The ADuM3400/ADuM3401/ADuM3402 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 17). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2} . The capacitor value must be between 0.01 μF and 0.1 μF . The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered unless the ground pair on each package side is connected close to the package.



Figure 17. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care must be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout must be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design, which varies widely by application. The ADuM3400/ADuM3401/ADuM3402 incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include:

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices minimized by use of guarding and isolation technique between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and respective ground.

While the ADuM3400/ADuM3401/ADuM3402 improve system-level ESD reliability, they are no substitute for a robust system-level design. See the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products* for detailed recommendations on board layout and system-level design.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high.



Figure 18. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM3400/ADuM3401/ADuM3402 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM3400/ADuM3401/ADuM3402 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~ 1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~ 1 μs , a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 μs , the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 11) by the watchdog timer circuit.

The limitation on the magnetic field immunity of the ADuM3400/ADuM3401/ADuM3402 is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition of the ADuM3400/ADuM3401/ADuM3402 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2; N = 1, 2, \dots, N$$

where:

β is magnetic flux density (gauss).

N is the number of turns in the receiving coil.

r_n is the radius of the n^{th} turn in the receiving coil (cm).

Given the geometry of the receiving coil in the [ADuM3400/ADuM3401/ADuM3402](#) and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.



Figure 19. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil, which is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the [ADuM3400/ADuM3401/ADuM3402](#) transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the [ADuM3400/ADuM3401/ADuM3402](#) are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, place a 0.5 kA current 5 mm away from the [ADuM3400/ADuM3401/ADuM3402](#) to affect the operation of the component.



Figure 20. Maximum Allowable Current for Various Current-to-ADuM3400/ADuM3401/ADuM3402 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care must be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the [ADuM3400/ADuM3401/ADuM3402](#) isolator is a function of the supply voltage, the channel data rate, and the channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5 f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5 f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.

f_r is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 8 provides the per-channel input supply current as a function of the data rate. Figure 9 and Figure 10 provide the per-channel supply output current as a function of the data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 11 through Figure 15 provide the total V_{DD1} and V_{DD2} supply current as a function of the data rate for the [ADuM3400/ADuM3401/ADuM3402](#) channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the [ADuM3400/ADuM3401/ADuM3402](#).

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Figure 21 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition, and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the [ADuM3400/ADuM3401/ADuM3402](#) depends on the voltage waveform type imposed across the isolation barrier. The *iCoupler* insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 21, Figure 22, and Figure 23 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the recommended maximum working voltage of Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 10 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross insulation voltage waveform that does not conform to Figure 22 or Figure 23 must be treated as a bipolar ac waveform and the peak voltage must be limited to the 50-year lifetime voltage value listed in Table 10.

Note that the voltage presented in Figure 22 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.



Figure 21. Bipolar AC Waveform



Figure 22. Unipolar AC Waveform



Figure 23. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 24. 16-Lead Standard Small Outline Package [SOIC_W]
 Wide Body (RW-16)
 Dimensions shown in millimeters and (inches)

ORDERING GUIDE

| Model ^{1,2} | Number of Inputs, V _{DD1} Side | Number of Inputs, V _{DD2} Side | Maximum Data Rate (Mbps) | Maximum Propagation Delay, 5 V (ns) | Maximum Pulse Width Distortion (ns) | Temperature Range | Package Description | Package Option |
|----------------------|---|---|--------------------------|-------------------------------------|-------------------------------------|-------------------|---------------------|----------------|
| ADuM3400ARWZ | 4 | 0 | 1 | 100 | 40 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM3400BRWZ | 4 | 0 | 10 | 50 | 3 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM3400CRWZ | 4 | 0 | 90 | 32 | 2 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM3401ARWZ | 3 | 1 | 1 | 100 | 40 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM3401BRWZ | 3 | 1 | 10 | 50 | 3 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM3401CRWZ | 3 | 1 | 90 | 32 | 2 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM3402ARWZ | 2 | 2 | 1 | 100 | 40 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM3402BRWZ | 2 | 2 | 10 | 50 | 3 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM3402CRWZ | 2 | 2 | 90 | 32 | 2 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |

¹ Z = RoHS Compliant Part.

² Tape and reel are available. The addition of an -RL suffix designates a 13" (1,000 units) tape-and-reel option.

NOTES

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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
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