



# Photocoupler

## Product Data Sheet

### 6N135 / 6N136 series

Spec No.: DS70-2008-0032

Effective Date: 12/15/2009

Revision: -

**LITE-ON DCC**

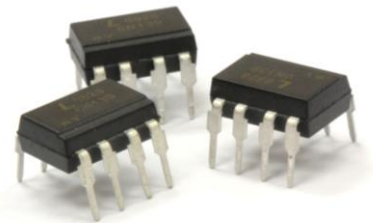
**RELEASE**

BNS-OD-FC001/A4

## 6N135, 6N136 Single Channel, High Speed Optocouplers



Jan.2009



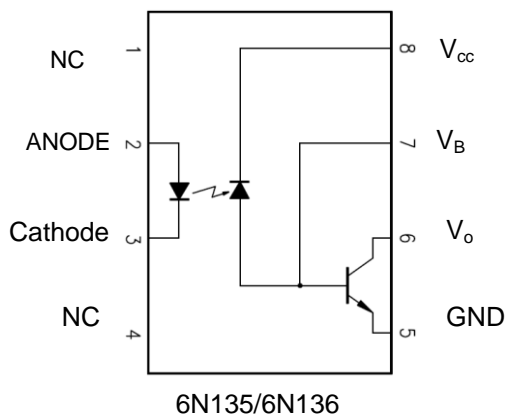
### Description

The 6N135/6 consists of a high efficient AlGaAs Light Emitting Diode and a high speed optical detector. This design provides excellent AC and DC isolation between the input and output sides of the Optocoupler. Connection for the bias of the photodiode improves the speed that of a conventional phototransistor coupler by reducing the base-collector capacitances. The internal shield ensures high common mode transient immunity. A guaranteed common mode transient immunity is up to 1KV/ $\mu$  sec.

### Features

- High speed – 1MBd typical
- Available in Dual-in-line, Wide lead spacing, Surface mounting package.
- Storable output.
- UL, CSA approval

### Functional Diagram



Truth Table (Positive Logic)

LED	OUT
ON	L
OFF	H

A 0.1 $\mu$ F bypass Capacitor must be connected between Pin8 and Pin5

### Application

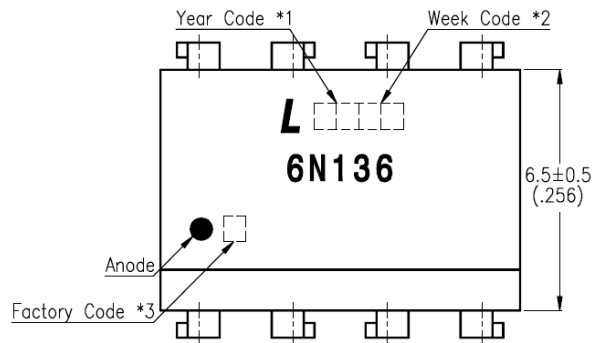
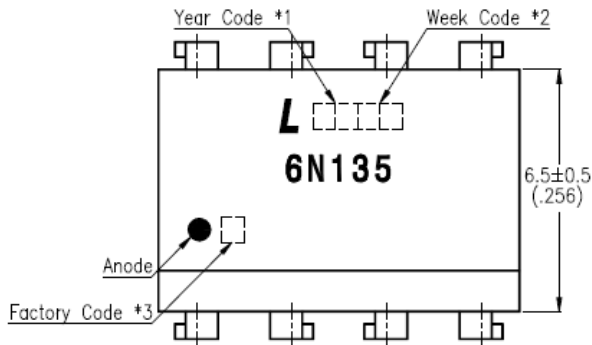
- High Voltage Isolation
- Isolation in line receivers
- Feedback element in switching mode power supplier
- Power transistor isolation in motor drives
- Interface between Microprocessor system, computer and their peripheral
- Replace pulse transformers.
- Replace slower optocoupler isolators.

## Ordering Information

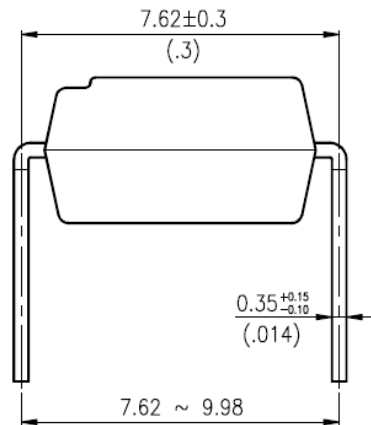
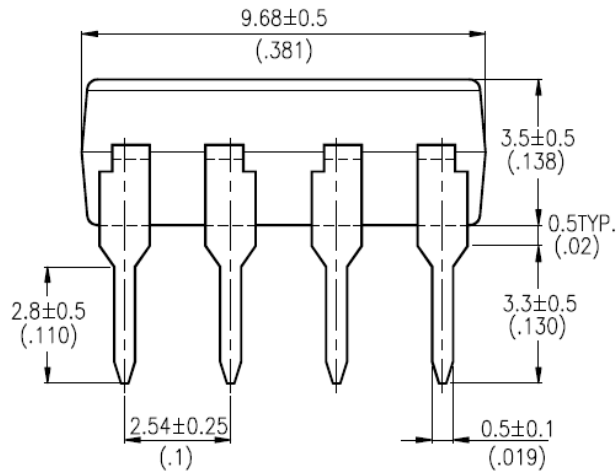
Part	Option	Minimum CMR		CTR	Remarks
		dV/dt (V/ $\mu$ s)	V <sub>CM</sub> (V)		
6N135	M	1000	10	7	Single Channel, DIP-8
	S				Single Channel, Wide Lead Spacing
6N136	M	1000	10	19	Single Channel, SMD-8
	S				Single Channel, DIP-8
					Single Channel, Wide Lead Spacing
					Single Channel, SMD-8

## Package Dimensions

### 8-pin DIP Package (6N135 / 6N136)

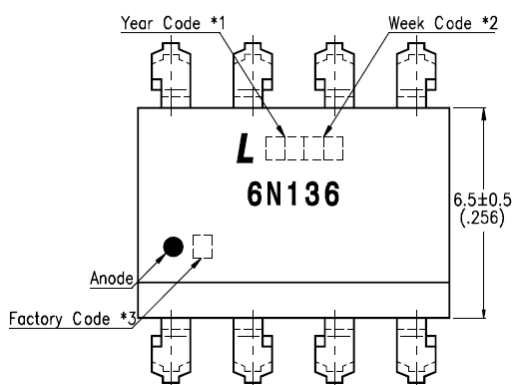
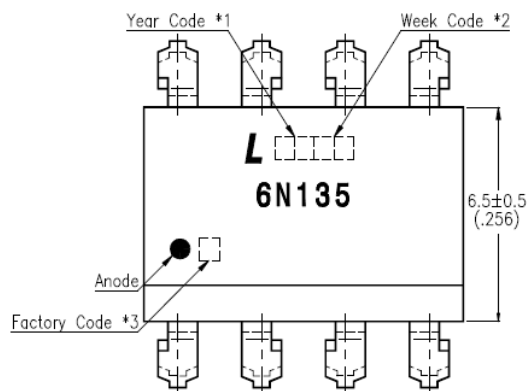


- \*1. Year date code.
  - \*2. 2-digit work week.
  - \*3. Factory identification mark  
(Z : Taiwan, Y : Thailand).
- Dimensions are in Millimeters and (Inches).



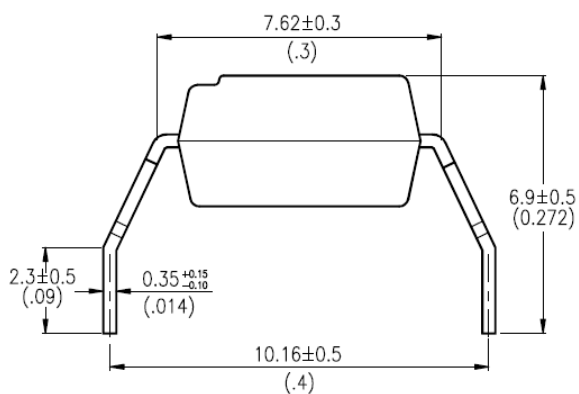
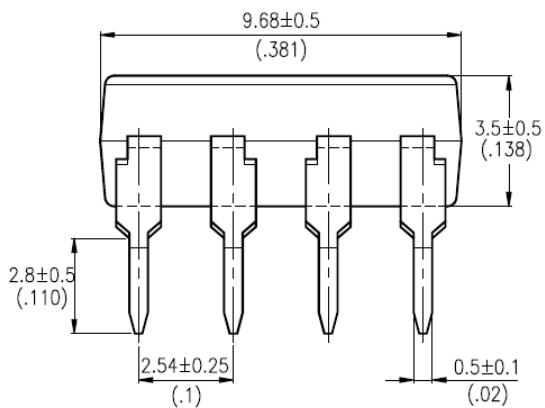
## Package Dimensions

### 8-pin DIP Wide Lead Spacing Package (6N135M / 6N136M)



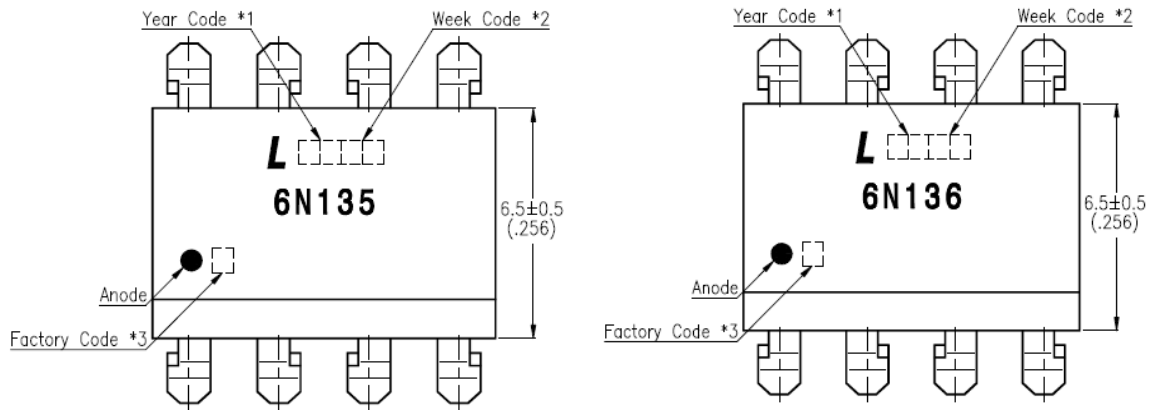
- \*1. Year date code.
- \*2. 2-digit work week.
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(Z : Taiwan, Y : Thailand).

Dimensions are in Millimeters and (Inches).

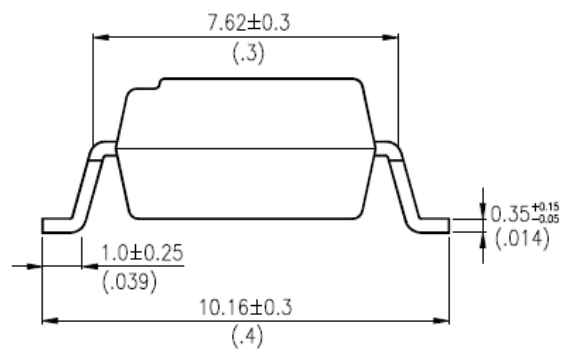
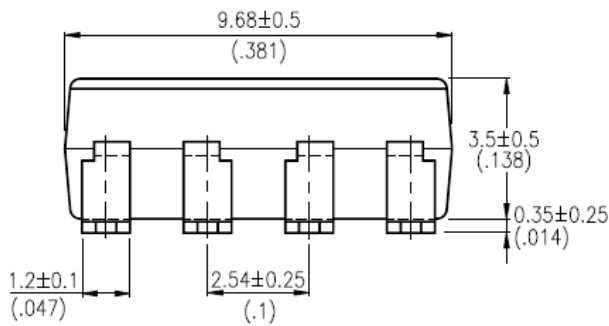


## Package Dimensions

### 8-pin DIP Surface Mount Package (6N135S / 6N136S)

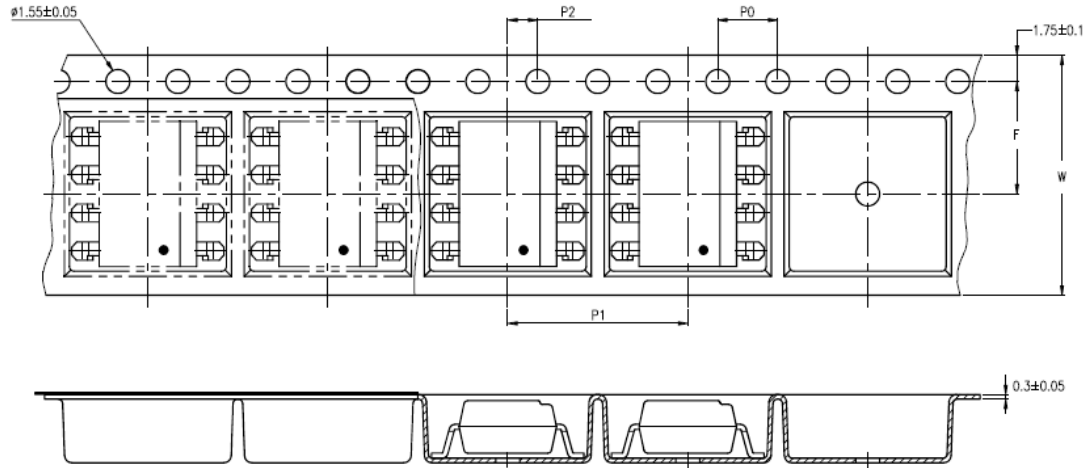


- \*1. Year date code.
  - \*2. 2-digit work week.
  - \*3. Factory identification mark  
(Z : Taiwan, Y : Thailand).
- Dimensions are in Millimeters and (Inches).

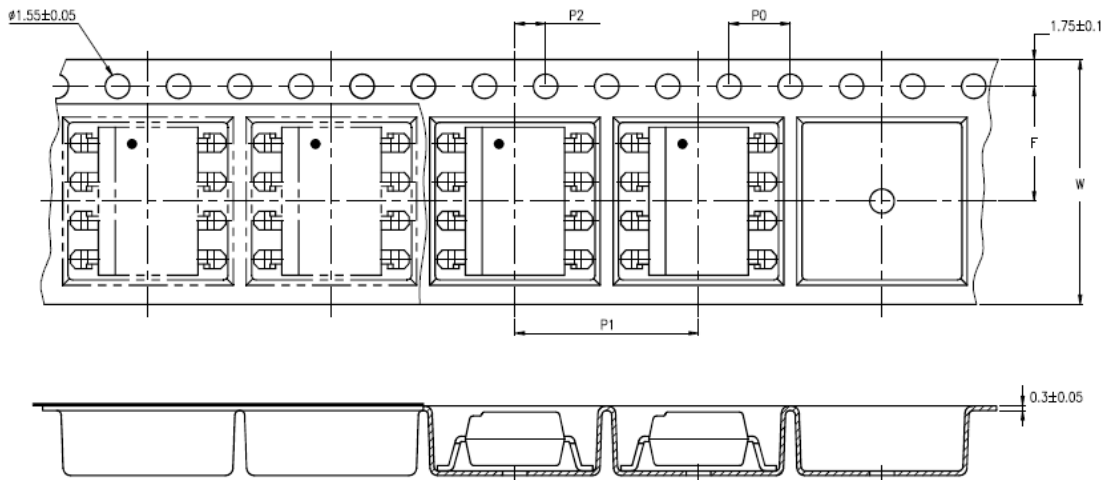


## Taping Dimensions

### 6N135S/136S-TA

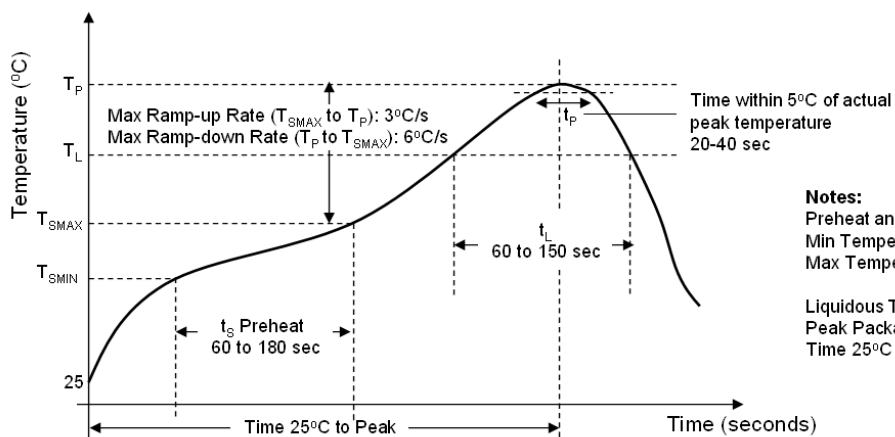


### 6N135S/136S-TA1



Description	Symbol	Dimensions in millimeters ( inches )
Tape wide	W	$16 \pm 0.3$ ( .63 )
Pitch of sprocket holes	P0	$4 \pm 0.1$ ( .15 )
Distance of compartment	F	$7.5 \pm 0.1$ ( .295 )
Distance of compartment to compartment	P1	$2 \pm 0.1$ ( .079 )

### Recommended Lead Free Reflow Profile





## Absolute Maximum Ratings\*1

Parameter	Symbol	Min	Max	Units	Note
Storage Temperature	$T_{ST}$	-55	125	°C	
Operating Temperature	$T_A$	-40	85	°C	
Isolation Voltage	$V_{ISO}$	5000		$V_{RMS}$	
Supply Voltage	$V_{CC}$		15	V	
Lead Solder Temperature * 2			260	°C	2
<b>Input</b>					
Average Forward Input Current	$I_F$		25	mA	
Reverse Input Voltage	$V_R$		5	V	
Input Power Dissipation	$P_I$		45	mW	
<b>Output</b>					
Output Collector Current	$I_O$		8	mA	
Output Collector Voltage	$V_O$	-0.5	20	V	
Output Collector Power Dissipation	$P_O$		100	mW	

1. Ambient temperature = 25°C, unless otherwise specified. Stresses exceeding the absolute maximum ratings can cause permanent damage to the device. Exposure to absolute maximum ratings for long periods of time can adversely affect reliability.

2. 260°C for 10 seconds. Refer to Lead Free Reflow Profile.

### Electrical Specifications

Parameters	Test Condition	Symbol	Device	Min	Typ	Max	Units
<b>Input</b>							
Input Forward Voltage	$I_F=16\text{mA}$ , $T_A=25^\circ\text{C}$	$V_F$	6N135		1.4	1.7	V
Input Reverse Voltage	$I_R=10\mu\text{A}$	$BV_R$	6N136	5			V
<b>Detector</b>							
Current transfer ratio	$I_F=16\text{mA}$ ; $V_{CC}=4.5\text{V}$ ; $T_A=25^\circ\text{C}$ ; $V_o=0.4\text{V}$	CTR	6N135	7	18	50	%
			6N136	19	24	50	
Logic low output voltage output voltage	$I_F=16\text{mA}$ ; $V_{CC}=4.5\text{V}$ ; $I_o=1.1\text{mA}$ ; $T_A=25^\circ\text{C}$	$V_{OL}$	6N135		0.18	0.4	V
	$I_F=16\text{mA}$ ; $V_{CC}=4.5\text{V}$ ; $I_o=3\text{mA}$ ; $T_A=25^\circ\text{C}$		6N136		0.25	0.4	
Logic high output current	$I_F=0\text{mA}$ , $V_o=V_{CC}=5.5\text{V}$ $T_A=25^\circ\text{C}$	$I_{OH}$	6N135			0.5	$\mu\text{A}$
	$I_F=0\text{mA}$ , $V_o=V_{CC}=15\text{V}$ $T_A=25^\circ\text{C}$		6N136			1	
Logic low supply current	$I_F=16\text{mA}$ , $V_o=\text{open}$ ( $V_{CC}=15\text{V}$ )	$I_{ccl}$	6N135 6N136		400		$\mu\text{A}$
Logic high supply current	$I_F=0\text{mA}$ , $V_o=\text{open}$ ; $T_A=25^\circ\text{C}$ ( $V_{CC}=15\text{V}$ )	$I_{cch}$	6N135 6N136			1	$\mu\text{A}$

\*All Typical at  $T_A=25^\circ\text{C}$

## Property of Lite-on Only

### Switching Specifications

$T_A=0\sim 70^{\circ}\text{C}$ ,  $V_{CC}=5\text{V}$ , unless otherwise specified.

Parameter	Test Condition	Symbol	Device	Min	Typ	Max	Units
Propagation Delay Time to Low Output Level	$T_A=25^{\circ}\text{C}$ ( $R_L=4.1\text{K}\Omega$ , $I_F=16\text{mA}$ )	$t_{\text{PHL}}$	6N135		0.09	1.5	$\mu\text{s}$
	$T_A=25^{\circ}\text{C}$ ( $R_L=1.9\text{K}\Omega$ , $I_F=16\text{mA}$ )		6N136		0.1	0.8	$\mu\text{s}$
Propagation Delay Time to High Output Level	$T_A=25^{\circ}\text{C}$ ( $R_L=4.1\text{K}\Omega$ , $I_F=16\text{mA}$ )	$t_{\text{PLH}}$	6N135		0.8	1.5	$\mu\text{s}$
	$T_A=25^{\circ}\text{C}$ ( $R_L=1.9\text{K}\Omega$ , $I_F=16\text{mA}$ )		6N136		0.4	0.8	$\mu\text{s}$
Logic High Common Mode Transient Immunity	$I_F=0\text{mA}$ ; $V_{\text{CM}}=10\text{Vp-p}$ ; $R_L=4.1\text{K}\Omega$ ; $T_A=25^{\circ}\text{C}$	$ CM_H $	6N135	1			$\text{KV}/\mu\text{s}$
	$I_F=0\text{mA}$ ; $V_{\text{CM}}=10\text{Vp-p}$ ; $R_L=1.9\text{K}\Omega$ ; $T_A=25^{\circ}\text{C}$		6N136	1			$\text{KV}/\mu\text{s}$
Logic Low Common Mode Transient Immunity	$I_F=0\text{mA}$ ; $V_{\text{CM}}=10\text{Vp-p}$ ; $R_L=4.1\text{K}\Omega$ ; $T_A=25^{\circ}\text{C}$	$ CM_L $	6N135	1			$\text{KV}/\mu\text{s}$
	$I_F=0\text{mA}$ ; $V_{\text{CM}}=10\text{Vp-p}$ ; $R_L=1.9\text{K}\Omega$ ; $T_A=25^{\circ}\text{C}$		6N136	1			$\text{KV}/\mu\text{s}$

\*All Typical at  $T_A=25^{\circ}\text{C}$

### Isolation Characteristics

Parameter	Test Condition	Symbol	Min	Typ	Max	Units
Input-Output Insulation Leakage Current	45% RH, t = 5s, $V_{I-O} = 3kV$ DC, $T_A = 25^{\circ}C$	$I_{I-O}$			1.0	$\mu A$
Withstand Insulation Test Voltage	$RH \leq 50\%$ , t = 1min, $T_A = 25^{\circ}C$	$V_{ISO}$	5000			$V_{RMS}$
Input-Output Resistance	$V_{I-O} = 500V$ DC	$R_{I-O}$		$10^{12}$		$\Omega$

\*All Typical at  $T_A = 25^{\circ}C$

### Notes

1. A  $0.1\mu F$  or bigger bypass capacitor for  $V_{CC}$  is needed as shown in Fig.1
2. Current Transfer Ratio is defined as the ratio of output collector current  $I_o$ , to the forward LED input current  $I_F$ , times 100.
3. The  $1.9K\Omega$  load represents 1TTL unit load of 1.6mA and the  $5.6K\Omega$  pull-up resistor.
4. The  $4.1K\Omega$  load represents 1LSTTL unit load of 0.36mA and the  $6.1K\Omega$  pull-up resistor.

## Switching Time Test Circuit

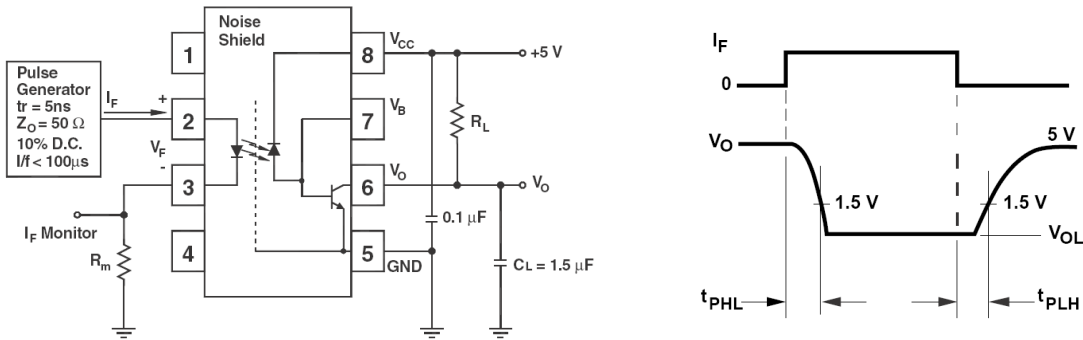


Figure 1: Single Channel Test Circuit for  $t_{PHL}$  and  $t_{PLH}$

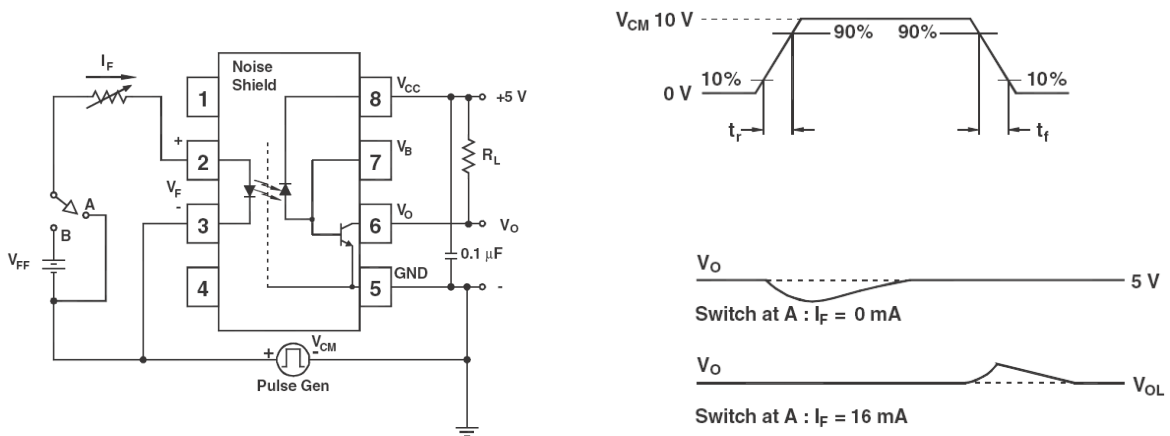


Figure 2: Single Channel Test Circuit for Common Mode Transient Immunity

## Characteristics Curves

Figure 3: DC and pulsed transfer characteristics

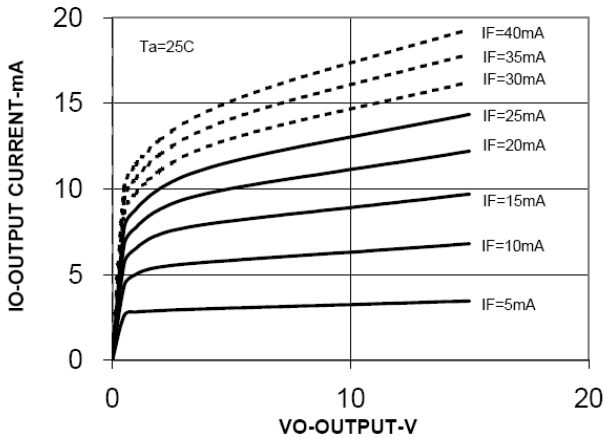


Figure 6: Current transfer ratio vs. input

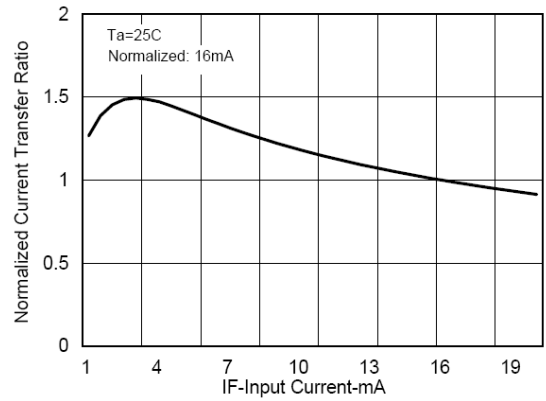


Figure 4: Input current vs. forward voltage

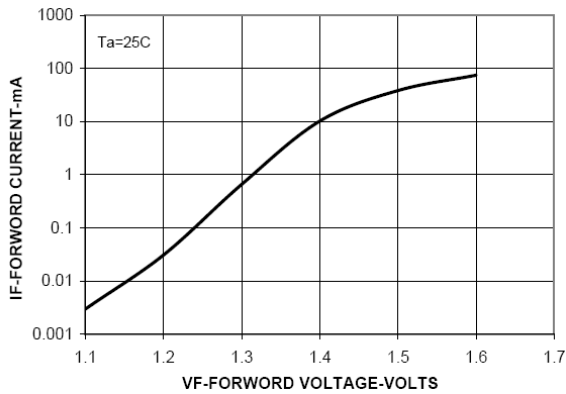


Figure 7: Current transfer ratio vs. temperature

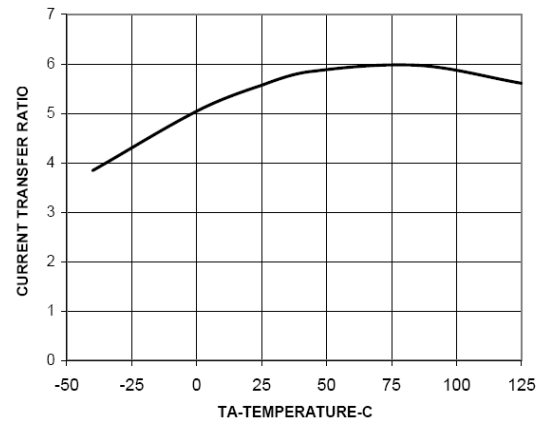


Figure 5: Logic high output current vs. temperature

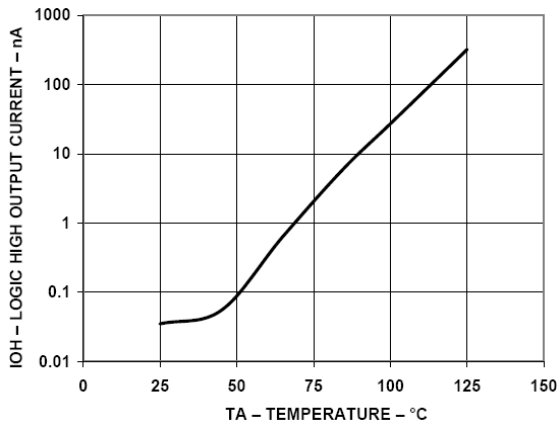
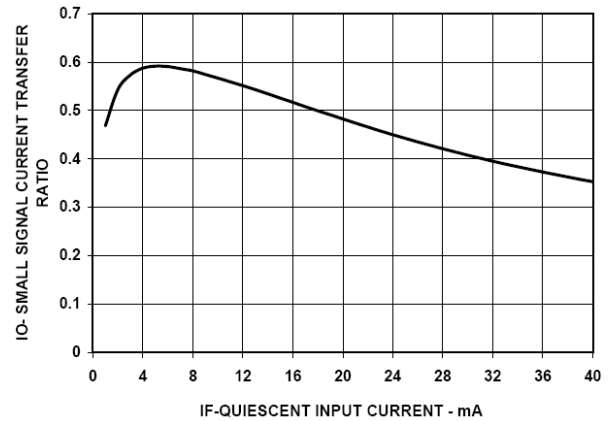


Figure 8: Small-signal current transfer ratio vs. quiescent current



## Property of Lite-on Only

### Characteristics Curves

Figure 9: Propagation delay time vs. temperature

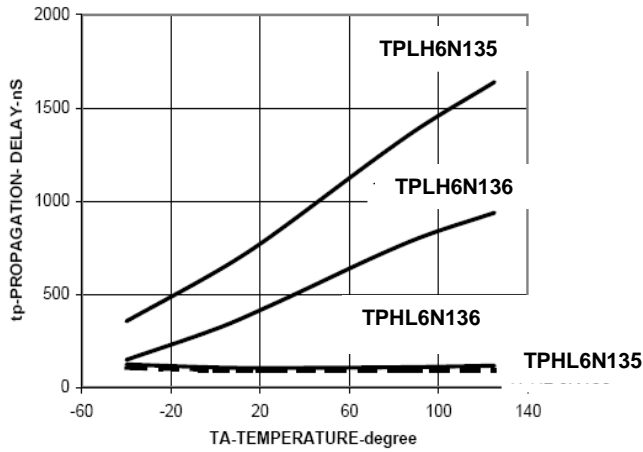
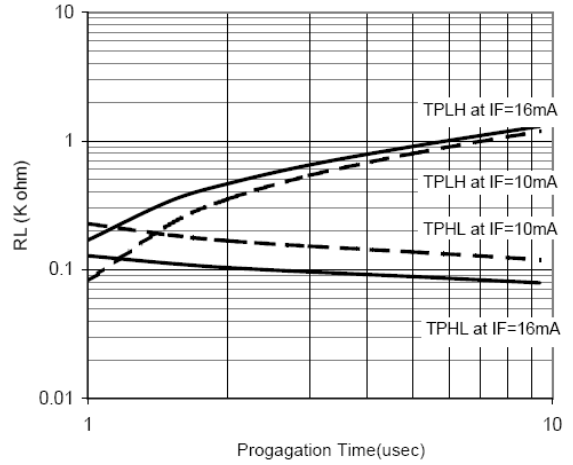


Figure 10: Propagation delay time vs. load resistance



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