Surge Stopper with Ideal Diode

FEATURES

- **Wide Operating Voltage Range: 4V to 80V**
- **Withstands Surges Over 80V with V_{CC} Clamp**
- **Adjustable Output Clamp Voltage**
- **Ideal Diode Controller Holds Up Output Voltage During Input Brownouts**
- **Reverse Input Protection to –40V**
- Reverse Output Protection to –20V
- Overcurrent Protection
- Low 10µA Shutdown Current at 12V
- Adjustable Fault Timer
- 0.1% Retry Duty Cycle During Faults (LTC4364-2)
- Available in 4mm × 3mm 14-Lead DFN, 16-Lead MSOP, and 16-Lead SO Packages

APPLICATIONS

- Automotive/Avionic Surge Protection
- Hot Swap/Live Insertion
- Redundant Supply ORing
- Output Port Protection

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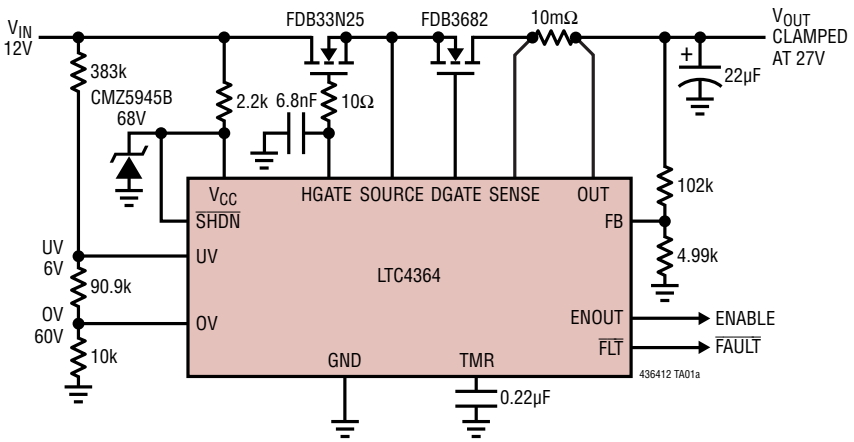
DESCRIPTION

The LTC®4364 surge stopper with ideal diode controller protects loads from high voltage transients. It limits and regulates the output during an overvoltage event, such as load dump in automobiles, by controlling the voltage drop across an external N-channel MOSFET pass device. The LTC4364 also includes a timed, current limited circuit breaker. In a fault condition, an adjustable fault timer must expire before the pass device is turned off. The LTC4364-1 latches off the pass device while the LTC4364-2 automatically restarts after a delay. The LTC4364 precisely monitors the input supply for overvoltage (OV) and undervoltage (UV) conditions. The external MOSFET is held off in undervoltage and auto-retry is disabled in overvoltage.

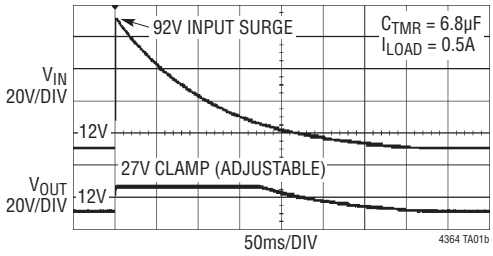
An integrated ideal diode controller drives a second MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. The LTC4364 controls the forward voltage drop across the MOSFET and minimizes reverse current transients upon power source failure, brownout or input short.

TYPICAL APPLICATION

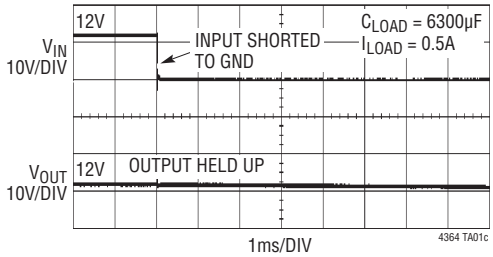
4A, 12V Overvoltage Output Regulator with Ideal Diode Withstands 200V 1ms Transient at V_{IN}



Overvoltage Protector Regulates Output at 27V During Input Transient



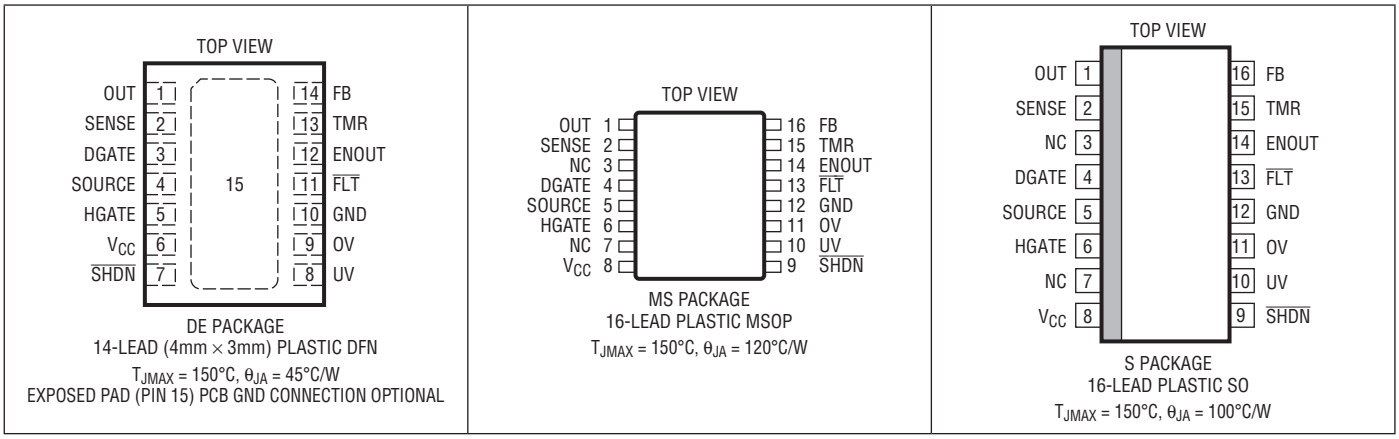
Ideal Diode Holds Up Output During Input Short



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage: V_{CC} ..... –40V to 100V
SOURCE, OV, UV, $\overline{SHDN}$ Voltages ..... –40V to 100V
DGATE, HGATE Voltages
(Note 3)..... SOURCE – 0.3V to SOURCE + 10V
ENOUT, $\overline{FLT}$ Voltages..... –0.3V to 100V
OUT, SENSE Voltages.....–20V to 100V
Voltage Difference (SENSE to OUT) ..... –30V to 30V
Voltage Difference (OUT to V_{CC}) .....–100V to 100V
Voltage Difference (SENSE to SOURCE) ..–100V to 100V
FB, TMR Voltages ..... –0.3V to 5.5V
Operating Ambient Temperature Range
LTC4364C..... 0°C to 70°C
LTC4364I .....–40°C to 85°C
LTC4364H..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS, SO Packages ..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4364CDE-1#PBF	LTC4364CDE-1#TRPBF	43641	14-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC4364IDE-1#PBF	LTC4364IDE-1#TRPBF	43641	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4364HDE-1#PBF	LTC4364HDE-1#TRPBF	43641	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4364CDE-2#PBF	LTC4364CDE-2#TRPBF	43642	14-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC4364IDE-2#PBF	LTC4364IDE-2#TRPBF	43642	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4364HDE-2#PBF	LTC4364HDE-2#TRPBF	43642	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4364CMS-1#PBF	LTC4364CMS-1#TRPBF	43641	16-Lead Plastic MSOP	0°C to 70°C
LTC4364IMS-1#PBF	LTC4364IMS-1#TRPBF	43641	16-Lead Plastic MSOP	–40°C to 85°C
LTC4364HMS-1#PBF	LTC4364HMS-1#TRPBF	43641	16-Lead Plastic MSOP	–40°C to 125°C
LTC4364CMS-2#PBF	LTC4364CMS-2#TRPBF	43642	16-Lead Plastic MSOP	0°C to 70°C
LTC4364IMS-2#PBF	LTC4364IMS-2#TRPBF	43642	16-Lead Plastic MSOP	–40°C to 85°C
LTC4364HMS-2#PBF	LTC4364HMS-2#TRPBF	43642	16-Lead Plastic MSOP	–40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4364CS-1#PBF	LTC4364CS-1#TRPBF	LTC4364S-1	16-Lead Plastic SO	0°C to 70°C
LTC4364IS-1#PBF	LTC4364IS-1#TRPBF	LTC4364S-1	16-Lead Plastic SO	–40°C to 85°C
LTC4364HS-1#PBF	LTC4364HS-1#TRPBF	LTC4364S-1	16-Lead Plastic SO	–40°C to 125°C
LTC4364CS-2#PBF	LTC4364CS-2#TRPBF	LTC4364S-2	16-Lead Plastic SO	0°C to 70°C
LTC4364IS-2#PBF	LTC4364IS-2#TRPBF	LTC4364S-2	16-Lead Plastic SO	–40°C to 85°C
LTC4364HS-2#PBF	LTC4364HS-2#TRPBF	LTC4364S-2	16-Lead Plastic SO	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Operating Supply Range		●	4		80	V
I_{CC}	Supply Current	V_{CC} = SOURCE = SENSE = OUT = 12V, No Fault	●		370	750	µA
$I_{CC(SHDN)}$	Supply Current in Shutdown	Shutdown	●		10	50	µA
$I_{CC(REV)}$	Reverse Input Current	V_{CC} = –30V	●		0	–10	µA
Surge Stopper							
ΔV_{HGATE}	HGATE Gate Drive, (V_{HGATE} – V_{SOURCE})	V_{CC} = 4V, DGATE Low, I_{HGATE} = 0µA, –1µA V_{CC} = 8V to 80V, DGATE Low, I_{HGATE} = 0µA, –1µA	● ●	5 10	7 12	9 16	V V
$I_{HGATE(UP)}$	HGATE Pull-Up Current	V_{CC} = HGATE = DGATE = SOURCE = 12V	●	–10	–20	–30	µA
$I_{HGATE(DN)}$	HGATE Pull-Down Current	Overvoltage: FB = 1.5V, ΔV_{HGATE} = 5V	●	60	130		mA
		Overcurrent: ΔV_{SNS} = 100mV, ΔV_{HGATE} = 5V	●	60	130		mA
		Shutdown/Fault Turn-Off: ΔV_{HGATE} = 5V	●	0.4	1		mA
I_{SRC}	SOURCE Input Current	V_{CC} = SOURCE = SENSE = OUT = 12V V_{CC} = SOURCE = 12V, Shutdown V_{SOURCE} = –30V	● ● ●		18 32 –2.0	40 90 –3.5	µA µA mA
V_{FB}	FB Servo Voltage	V_{CC} = 12V to 80V	●	1.22	1.25	1.28	V
I_{FB}	FB Input Current	FB = 1.25V	●		0	1	µA
ΔV_{SNS}	Overcurrent Fault Threshold, (V_{SENSE} – V_{OUT})	V_{CC} = 4V to 80V, OUT = 2.5V to V_{CC}, 0°C to 125°C V_{CC} = 4V to 80V, OUT = 2.5V to V_{CC}, –40°C to 125°C V_{CC} = 4V to 80V, OUT = 0V to 1.5V	● ● ●	45 43 18	50 50 25	55 57 32	mV mV mV
I_{SNS}	SENSE Input Current	SENSE = V_{CC} = SOURCE = OUT = 12V SENSE = –15V	● ●		55 –2	110 –4	µA mA
$I_{TMR(UP)}$	TMR Pull-Up Current, Overvoltage	TMR = 1V, FB = 1.5V, V_{CC} – OUT = 0.5V TMR = 1V, FB = 1.5V, V_{CC} – OUT = 75V	● ●	–1.3 –40	–2.2 –50	–3 –60	µA µA
	TMR Pull-Up Current, Overcurrent	TMR = 1V, ΔV_{SNS} = 60mV, V_{CC} – OUT = 0.5V TMR = 1V, ΔV_{SNS} = 60mV, V_{CC} – OUT = 75V	● ●	–6 –210	–10 –260	–14 –310	µA µA
	TMR Pull-Up Current, Warning	TMR = 1.3V, FB = 1.5V, V_{CC} – OUT = 0.5V	●	–3	–5	–7	µA
	TMR Pull-Up Current, Retry	TMR = 1V, FB = 1.5V	●	–1.3	–2	–3	µA
$I_{TMR(DN)}$	TMR Pull-Down Current	TMR = 1V, FB = 1.5V, Retry Shutdown	● ●	1.1 0.3	2 0.75	2.7 1.5	µA mA
$V_{TMR(F)}$	TMR Fault Threshold	$\overline{FLT}$ Falling, V_{CC} = 4V to 80V	●	1.22	1.25	1.28	V
$V_{TMR(G)}$	TMR Gate Off Threshold	HGATE Falling, V_{CC} = 4V to 80V	●	1.32	1.35	1.38	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{TMR(R)}$	TMR Retry Threshold	HGATE Rising (After 32 Cycles), V_{CC} = 4V to 80V	●	0.125	0.15	0.175	V
ΔV_{TMR}	Early Warning Timer Window	$V_{TMR(G)} - V_{TMR(F)}$, V_{CC} = 4V to 80V	●	75	100	125	mV
V_{UV}	UV Input Threshold	UV Falling, V_{CC} = 4V to 80V	●	1.22	1.25	1.28	V
$V_{UV(HYST)}$	UV Input Hysteresis		●	25	50	80	mV
$V_{UV(RST)}$	UV Reset Threshold	UV Falling, V_{CC} = 4V to 80V, LTC4364-1 Only	●	0.5	0.6	0.7	V
V_{OV}	OV Input Threshold	OV Rising, V_{CC} = 4V to 80V	●	1.22	1.25	1.28	V
$V_{OV(HYST)}$	OV Input Hysteresis				12		mV
I_{IN}	UV, OV Input Current	UV, OV = 1.25V UV, OV = –30V	● ●		0 –0.3	1 –0.6	µA mA
V_{OL}	ENOUT, $\overline{FLT}$ Output Low	I_{SINK} = 0.25mA I_{SINK} = 2mA	● ●		0.1 0.5	0.3 1.3	V V
I_{LEAK}	ENOUT, $\overline{FLT}$ Leakage Current	ENOUT, $\overline{FLT}$ = 80V	●		0	2.5	µA
$\Delta V_{OUT(TH)}$	Out High Threshold ($V_{CC} - V_{OUT}$)	ENOUT from Low to High	●	0.4	0.7	1	V
$V_{OUT(RST)}$	Out Reset Threshold	ENOUT from High to Low	●	1.4	2.2	3	V
I_{OUT}	OUT Input Current	V_{CC} = OUT = 12V, $\overline{SHDN}$ Open OUT = –15V	● ●		40 –4	80 –8	µA mA
	Output Current in Shutdown, $I_{SNS} + I_{OUT}$	V_{CC} = SOURCE = SENSE = OUT = 12V, Shutdown	●		12	40	µA
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Threshold	V_{CC} = 4V to 80V	●	0.5	1.6	2.2	V
$V_{\overline{SHDN}(FLT)}$	$\overline{SHDN}$ Pin Float Voltage	V_{CC} = 12V to 80V	●	2.3	4	6.5	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 0.5V Maximum Allowable Leakage, V_{CC} = 4V $\overline{SHDN}$ = –30V	● ●	–1	–3.3 –1.5 –120	 –300	µA µA µA
D	Retry Duty Cycle, Overvoltage Retry Duty Cycle, Output Short	FB = 1.5V, V_{CC} = 80V, OUT = 16V ΔV_{SNS} = 60mV, V_{CC} – OUT = 12V	● ●		0.125 0.075	0.2 0.12	% %
$t_{OFF,HGATE(UV)}$	Undervoltage to HGATE Low Propagation Delay	UV Steps from 1.5V to 1V	●		1.3	4	µs
$t_{OFF,HGATE(OV)}$	Overvoltage to HGATE Low Propagation Delay	FB Steps from 1V to 1.5V	●		0.25	1	µs
$t_{OFF,HGATE(OC)}$	Overcurrent to HGATE Low Propagation Delay	ΔV_{SNS} Steps from 0mV to 150mV, OUT = 0V	●		0.5	2	µs
Ideal Diode							
ΔV_{DGATE}	DGATE Gate Drive, ($V_{DGATE} - V_{SOURCE}$)	V_{CC} = 4V, No Fault, I_{DGATE} = 0µA, –1µA V_{CC} = 8V to 80V, No Fault, I_{DGATE} = 0µA, –1µA	● ●	5 10	8.5 12	12 16	V V
$I_{DGATE(UP)}$	DGATE Pin Pull-Up Current	DGATE = SOURCE = V_{CC} = 12V, ΔV_{SD} = 0.1V	●	–5	–10	–15	µA
$I_{DGATE(DN)}$	DGATE Pin Pull-Down Current	ΔV_{DGATE} = 5V, ΔV_{SD} = –0.2V ΔV_{DGATE} = 5V, Shutdown/Fault Turn-Off	● ●	60 0.4	130 1		mA mA
ΔV_{SD}	Ideal Diode Regulation Voltage, ($V_{SOURCE} - V_{SENSE}$)	ΔV_{DGATE} = 2.5V, V_{CC} = SOURCE = 12V ΔV_{DGATE} = 2.5V, V_{CC} = SOURCE = 4V	● ●	10 24	30 48	45 72	mV mV
$t_{OFF(DGATE)}$	DGATE Turn-Off Propagation Delay	ΔV_{SD} Steps from 0.1V to –1V	●		0.35	1.5	µs

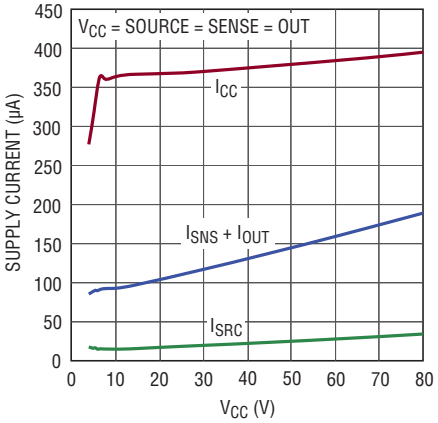
Note 1: Stress beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All Currents into device pins are positive and all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

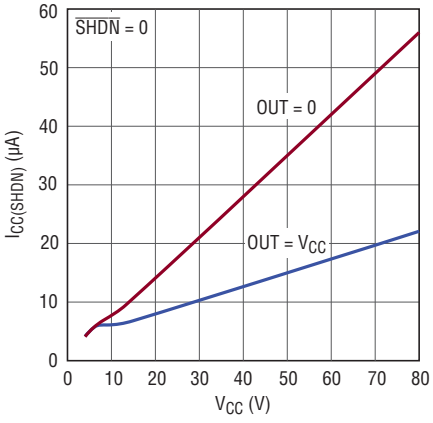
Note 3: Internal clamps limit the HGATE and DGATE pins to minimum of 10V above the SOURCE pin. Driving these pins to voltages beyond the clamp may damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

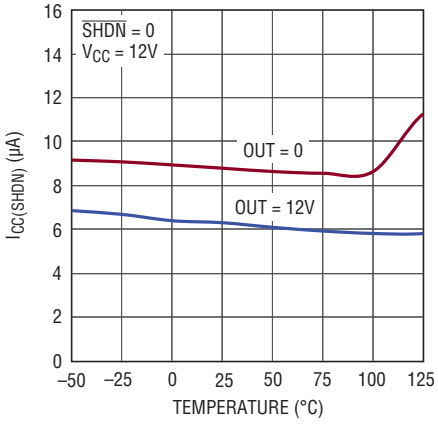
Supply Current vs V_{CC}



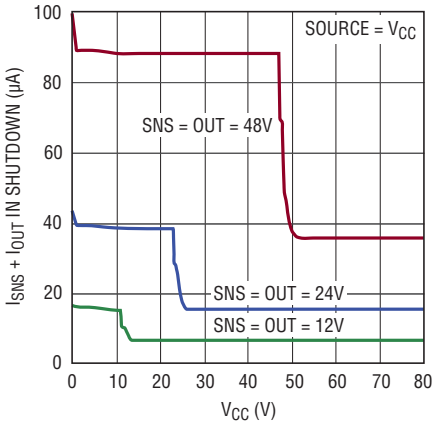
$I_{CC(SHDN)}$ vs V_{CC}



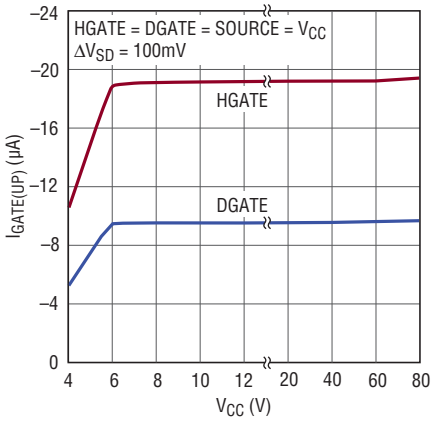
$I_{CC(SHDN)}$ vs Temperature



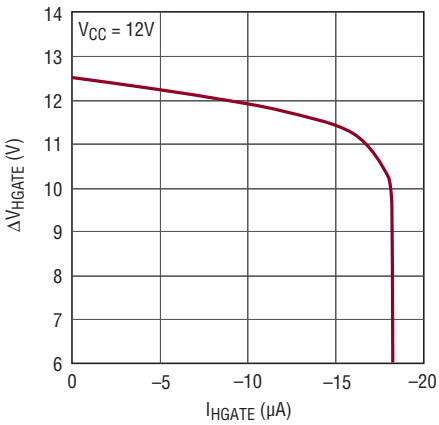
$I_{SNS} + I_{OUT}$ in Shutdown vs V_{CC}



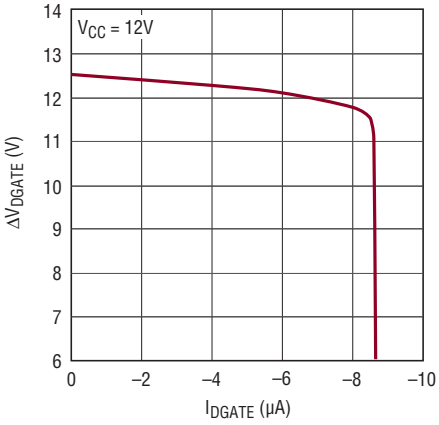
GATE Pull-Up Current vs V_{CC}



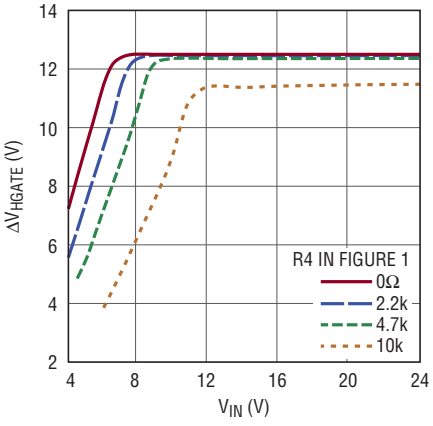
ΔV_{HGATE} vs I_{HGATE}



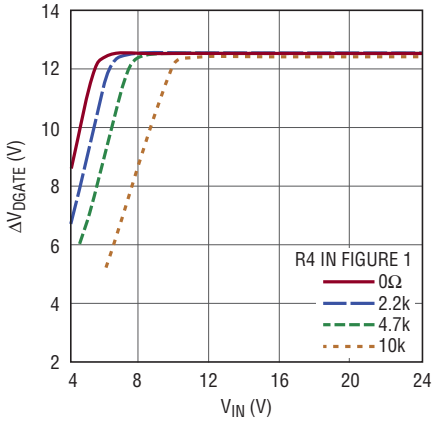
ΔV_{DGATE} vs I_{DGATE}



ΔV_{HGATE} vs V_{IN} in Figure 1

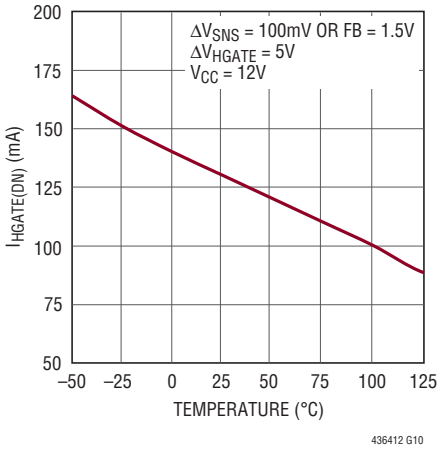


ΔV_{DGATE} vs V_{IN} in Figure 1

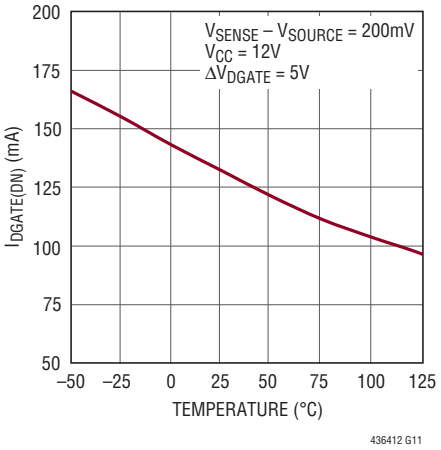


TYPICAL PERFORMANCE CHARACTERISTICS

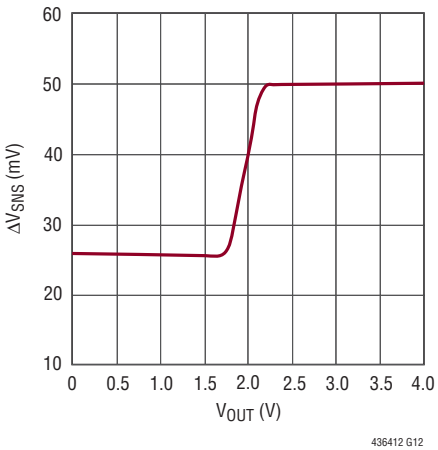
HGATE Pull-Down Current vs Temperature



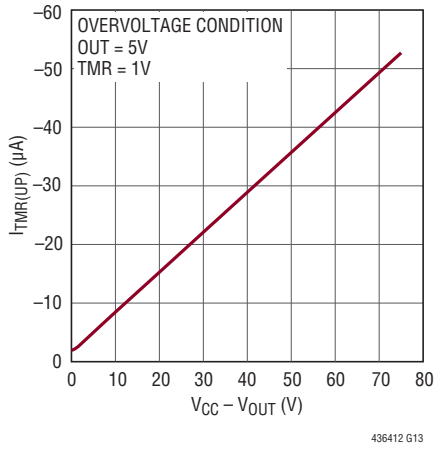
DGATE Pull-Down Current vs Temperature



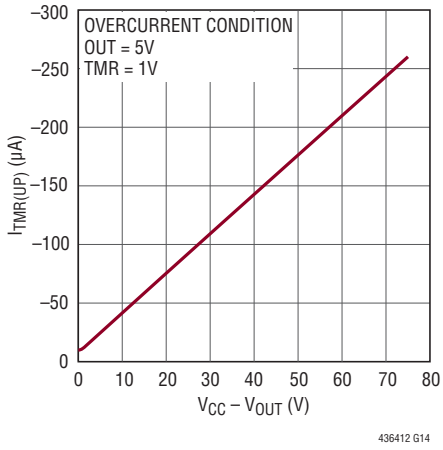
Overcurrent Threshold vs OUT Voltage



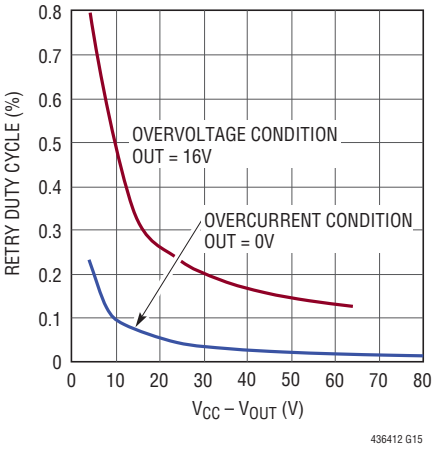
Overvoltage TMR Current vs $V_{CC} - V_{OUT}$



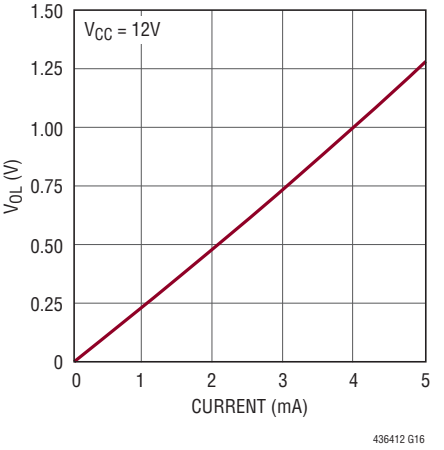
Overcurrent TMR Current vs $V_{CC} - V_{OUT}$



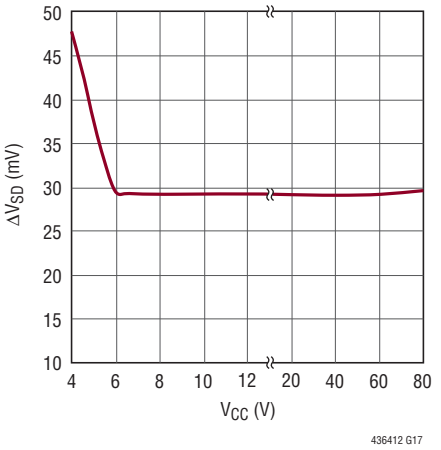
Retry Duty Cycle vs $V_{CC} - V_{OUT}$ (LTC4364-2 Only)



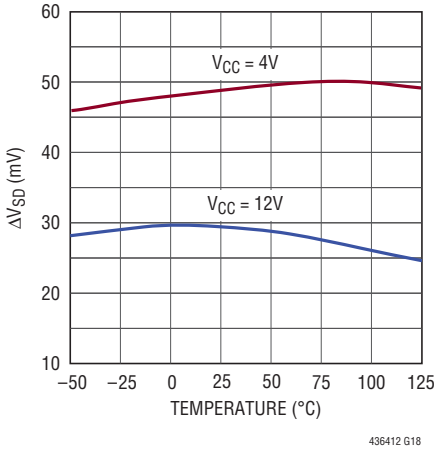
EN, $\overline{FLT}$ Output Low vs Current



Ideal Diode Regulation Voltage vs V_{CC}



Ideal Diode Regulation Voltage vs Temperature



PIN FUNCTIONS

DGATE: Diode Controller Gate Drive Output. When the load current creates more than 30mV of drop across the MOSFET, the DGATE pin is pulled high by an internal charge pump current source and clamped to 12V above the SOURCE pin. When the load current is small, the DGATE pin is actively driven to maintain 30mV across the MOSFET. If reverse current develops, a 130mA fast pull-down circuit quickly connects the DGATE pin to the SOURCE pin, turning off the MOSFET. Connect to SOURCE or leave open if unused.

ENOUT: Enable Output. An open-drain output that goes high impedance when the voltage at the OUT pin is above (V_{CC} – 0.7V), indicating the external MOSFETs are fully on. The state of the pin is latched and resets when the OUT pin drops below 2.2V. The internal FET is capable of sinking up to 2mA and can withstand up to 80V. Connect to GND if unused.

Exposed Pad (DE Package Only): Exposed pad may be left open or connected to device ground (GND).

FB: Voltage Regulator Feedback Input. Connect this pin to the resistive divider connected between the OUT pin and ground. During an overvoltage condition, the HGATE pin is controlled to maintain 1.25V at the FB pin. Connect to GND to disable the overvoltage clamp.

$\overline{\text{FLT}}$: Fault Output. An open-drain output that pulls low after the TMR pin reaches the warning threshold of 1.25V. It indicates the pass device controlled by the HGATE pin is about to turn off because either the supply voltage has stayed at an elevated level for an extended period of time (overvoltage fault) or the device is in an overcurrent condition (overcurrent fault). The internal FET is capable of sinking up to 2mA and can withstand up to 80V. Connect to GND if unused.

GND: Device Ground.

HGATE: Surge Stopper Gate Drive Output. The HGATE pin is pulled up by an internal charge pump current source and clamped to 12V above the SOURCE pin. Both voltage and current amplifiers control the HGATE pin to regulate the output voltage and limit the current through the MOSFET.

OUT: Output Voltage Sense Input. This pin senses the voltage at the drain of the external N-channel MOSFET connected to the DGATE pin. The voltage difference between V_{CC} and OUT sets the fault timer current. When this difference drops below 0.7V, the ENOUT pin goes high impedance.

OV: Overvoltage Comparator Input. When OV is above its threshold of 1.25V, the fault retry function is inhibited. When OV falls below its threshold, the HGATE pin is allowed to turn back on when fault conditions are cleared. At power-up, an OV voltage higher than its threshold blocks turn-on of the external N-channel MOSFET controlled by the HGATE pin (see Applications Information). Connect to GND if unused.

SENSE: Current Sense Input. Connect this pin to the input side of the current sense resistor. The current limit circuit controls the HGATE pin to limit the sense voltage between the SENSE and OUT pins to 50mV if OUT is above 2.5V. When OUT drops below 1.5V, the sense voltage is reduced to 25mV for additional protection during an output short. The sense amplifier also starts a current source to charge up the TMR pin. The voltage difference between SENSE and OUT must be limited to less than 30V. Connect to OUT if unused.

$\overline{\text{SHDN}}$: Shutdown Control Input. Pulling the $\overline{\text{SHDN}}$ pin below 0.5V shuts off the LTC4364 and reduces the V_{CC} pin current to 10µA. Pull this pin above 2.2V or disconnect it to allow the internal current source to turn the part back on. When left open, the $\overline{\text{SHDN}}$ voltage is internally clamped to 4V. The leakage current to ground at the pin should be limited to no more than 1µA if no pull-up device is used to turn the part on. The $\overline{\text{SHDN}}$ pin can be pulled up to 100V or below GND by 40V without damage.

SOURCE: Common Source Input and Gate Drive Return. Connect this pin directly to the sources of the external back-to-back N-channel MOSFETs. SOURCE is the anode of the ideal diode and the voltage sensed between this pin and the SENSE pin is used to control the source-drain voltage across the N-channel MOSFET (forward voltage of the ideal diode).

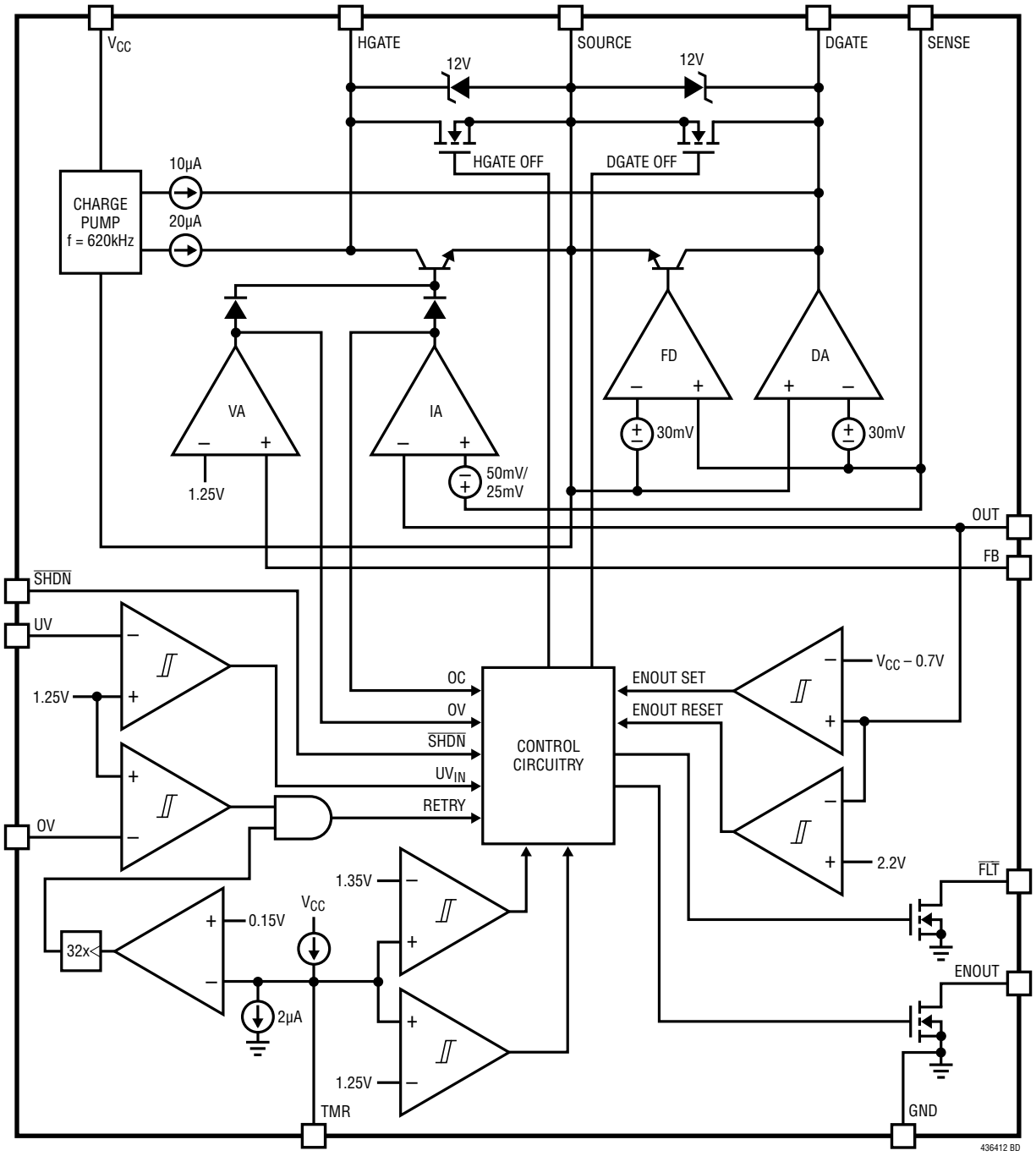
PIN FUNCTIONS

TMR: Fault Timer Input. Connect a capacitor between this pin and ground to set the times for fault warning, fault turn-off, and cool down periods. Either voltage regulation or current regulation starts pulling up the TMR pin. The current charging up this pin during the fault conditions increases with the voltage difference between V_{CC} and OUT pins (see Applications Information). When TMR reaches 1.25V, the $\overline{FLT}$ pin pulls low to indicate the detection of a fault condition. If the condition persists, the pass device controlled by HGATE turns off when TMR reaches the threshold of 1.35V. As soon as the fault condition disappears, a cool down interval commences while the TMR pin cycles 32 times between 0.15V and 1.35V with 2µA charge and discharge currents. When TMR crosses 0.15V the 32nd time, the HGATE pin is allowed to pull high turning the pass device back on if the OV pin voltage is below its threshold for the LTC4364-2 version. The HGATE pin latches low after fault time-out for the LTC4364-1.

UV: Undervoltage Comparator Input. When the UV pin falls below its 1.25V threshold, the HGATE pin is pulled down with a 1mA current. When the UV pin rises above 1.25V plus the hysteresis, the HGATE pin is pulled up by the internal charge pump. For LTC4364-1, after HGATE is latched off, pulling the UV pin below 0.6V resets the latch and allows HGATE to retry. If unused, connect to the $\overline{SHDN}$ pin.

V_{CC}: Positive Supply Voltage Input. The positive supply input ranges from 4V to 80V for normal operation. It can also be pulled below ground potential by up to 40V during a reverse battery condition, without damaging the part. Shutting down the LTC4364 by pulling the $\overline{SHDN}$ pin to ground reduces the V_{CC} current to 10µA.

BLOCK DIAGRAM



OPERATION

The LTC4364 is designed to suppress high voltage surges and limit the output voltage to protect load circuitry and ensure normal operation in high availability power systems. It features an overvoltage protection regulator that drives an external N-channel MOSFET (M1) as the pass device and an ideal diode controller that drives a second external N-channel MOSFET (M2) for reverse input protection and output voltage holdup.

The LTC4364 operates from a wide range of supply voltage, from 4V to 80V. With a clamp limiting the V_{CC} supply, the input voltage may be higher than 80V. The input supply can also be pulled below ground potential by up to 40V without damaging the LTC4364. The low power supply requirement of 4V allows it to operate even during cold cranking conditions in automotive applications.

Normally, the pass device M1 is fully on, supplying current to the load with very little power loss. If the input voltage surges too high, the voltage amplifier (VA) controls the gate of M1 and regulates the voltage at the OUT pin to a level that is set by an external resistive divider from the OUT pin to ground and the internal 1.25V reference. The LTC4364 also detects an overcurrent condition by monitoring the voltage across an external sense resistor placed between the SENSE and OUT pins. An active current limit circuit (IA) controls the gate of M1 to limit the sense voltage to 50mV if OUT is above 2.5V. In the case of a severe output short that brings OUT below 1.5V, the sense voltage is reduced to 25mV to reduce the stress on M1.

During an overvoltage or overcurrent event, a current source starts charging up the capacitor connected at the TMR pin to ground. The pull-up current source in overcurrent condition is 5 times of that in overvoltage to accelerate turn-off. When TMR reaches 1.25V, the $\overline{FLT}$ pin pulls low to warn of impending turn-off. The pass device M1 stays on and the TMR pin is further charged up until it reaches 1.35V, at which point the HGATE pin pulls low and turns off M1. The fault timer allows the load to continue functioning during brief transient events while protecting the MOSFET from being damaged by a long period of input overvoltage, such as load dump in vehicles. The fault timer period decreases with the voltage across the MOSFET, to help keep the MOSFET within its safe operating area (SOA). The LTC4364-1 latches off M1 and keeps $\overline{FLT}$ low after a fault timeout. The LTC4364-2 allows M1 to turn back on and $\overline{FLT}$ to go high impedance after a cool down timer cycle, provided the OV pin is below its threshold.

After the HGATE pin is latched low following fault, momentarily pulling the $\overline{SHDN}$ pin below 0.5V resets the fault and allows HGATE to pull high for both LTC4364-1 and LTC4364-2. In addition, momentarily pulling the UV pin below 0.6V allows HGATE to pull high after the cool down timer delay for LTC4364-1, but has no effect on LTC4364-2.

The source and drain of MOSFET M2 serve as the anode and cathode of the ideal diode. The LTC4364 controls the DGATE pin to maintain a 30mV forward voltage across the drain and source terminals of M2. It reduces the power dissipation and increases the available supply voltage to the load, as compared to using a discrete blocking diode. If M2 is driven fully on and the load current results in more than 30mV of forward voltage, the forward voltage is equal to $R_{DS(ON)} \bullet I_{LOAD}$.

In the event of an input short or a power supply failure, reverse current temporarily flows through the MOSFET M2 that is on. If the reverse voltage exceeds –30mV, the LTC4364 pulls the DGATE pin low strongly and turns off M2, minimizing the disturbance at the output.

If the input supply drops below the GND pin voltage, the DGATE pin is pulled to the SOURCE pin voltage, keeping M2 off. When the HGATE pin pulls low in any fault condition, the DGATE pin also pulls low, so both pass devices are turned off.

If the output (and so the SOURCE pin, through the body diode of M2) drops below GND, the HGATE pin is pulled to the SOURCE pin voltage, turning M1 off and shutting down the forward current path.

An input undervoltage condition is accurately detected using the UV pin. The HGATE and DGATE pins remain low if UV is below its 1.25V threshold. The $\overline{SHDN}$ pin not only turns off the pass devices but also shuts down the internal circuitry, reducing the supply current to 10µA.

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Some power systems must cope with high voltage surges of short duration such as those in automobiles. Load circuitry must be protected from these transients, yet critical systems may need to continue operating during these events.

The LTC4364 drives an N-channel MOSFET (M1) at the HGATE pin to limit the voltage and current to the load circuitry during supply transients or overcurrent events. The selection of M1 is critical for this application. It must stay on and provide a low impedance path from the input supply to the load during normal operation and then dissipate power during overvoltage or overcurrent conditions. The LTC4364 also drives a second N-channel MOSFET (M2) at the DGATE pin as an ideal diode to protect the load from damage during reverse polarity input conditions, and to block reverse current flow in the event the input collapses. A typical application circuit using the LTC4364 to regulate the output at 27V during input surges with reverse input protection is shown in Figure 1.

Overvoltage Fault

The LTC4364 limits the voltage at the OUT pin during an overvoltage situation. An internal voltage amplifier regulates the HGATE pin voltage to maintain 1.25V at the FB pin. During this period of time, the N-channel MOSFET M1 remains on and supplies current to the load. This allows uninterrupted operation during brief overvoltage transient events.

If the voltage regulation loop is engaged for longer than the timeout period, set by the timer capacitor, an overvoltage fault is detected. The HGATE pin is pulled down to the SOURCE pin by a 130mA current, turning M1 off. This prevents M1 from being damaged during a long period of overvoltage, such as during load dump in automobiles. After the fault condition has disappeared and a cool down period has transpired, the HGATE pin starts to pull high again (LTC4364-2). The LTC4364-1 latches the HGATE pin low after an overvoltage fault timeout and can be reset using the $\overline{SHDN}$ or UV pin (see Resetting Faults).

Overcurrent Fault

The LTC4364 features an adjustable current limit that protects against short circuits and excessive load current. During an overcurrent event, the HGATE pin is regulated to limit the current sense voltage across the SENSE and OUT pins (ΔV_{SNS}) to 50mV when OUT is above 2.5V. The current limit sense voltage is reduced to 25mV when OUT is below 1.5V for additional protection during an output short.

A current sense resistor is placed between SENSE and OUT and its value (R_{SNS}) is determined by:

$$R_{SNS} = \frac{\Delta V_{SNS}}{I_{LIM}}$$

where I_{LIM} is the desired current limit.

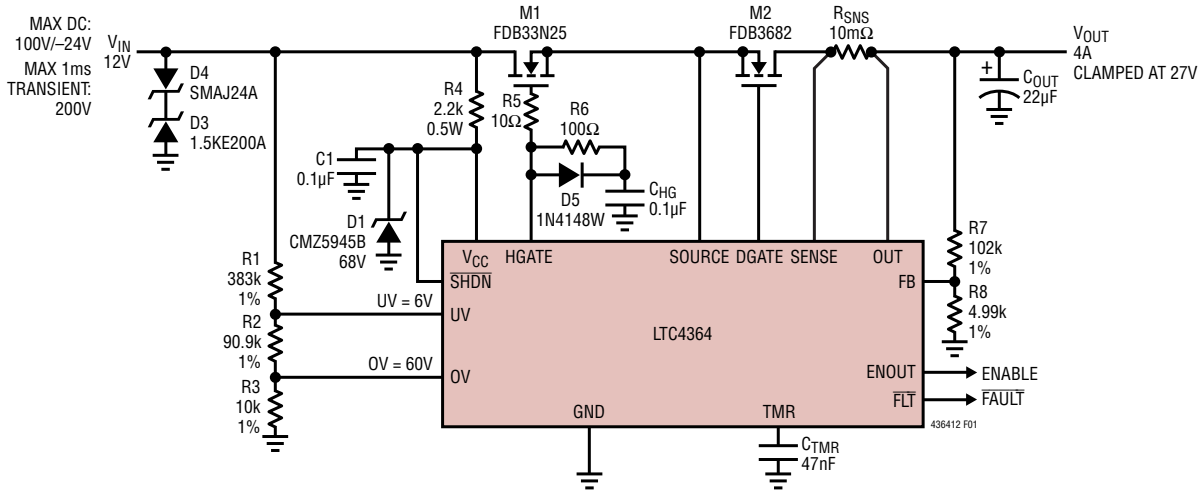

Figure 1. 4A, 12V Overvoltage Output Regulator with Reverse Current Protection

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An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the timeout delay set by the timer capacitor. The HGATE pin is then immediately pulled low by 130mA to the SOURCE pin, turning off the MOSFET M1. After the fault condition has disappeared and a cool down period has transpired, the HGATE pin is allowed to pull back up and turn on the pass device (LTC4364-2). The LTC4364-1 latches the HGATE pin low after the overcurrent fault timeout and can be reset using the $\overline{SHDN}$ or UV pin (see Resetting Faults).

Input Overvoltage Comparator

Input overvoltage is detected with the OV pin and an external resistive divider connected to the input (Figure 1). At power-up, if the OV pin voltage is higher than its 1.25V threshold before the 100µs internal power-on-reset expires, or before the input undervoltage condition is cleared at the UV pin, the HGATE pin will be held low until the OV pin voltage drops below its threshold. To prevent start-up in the event the board is hot swapped into an overvoltage supply, separate resistive dividers with filtering capacitors can be used for the OV and UV pins (Figure 2). The RC constants should be skewed so that $\tau_{UV}/\tau_{OV} > 50$. In Figure 2, If the board is plugged into a supply that is higher than 60V, the LTC4364 will not turn on the pass devices until the supply voltage drops below 60V.

Once the HGATE pin begins pulling high, an input overvoltage condition detected by OV will not turn off the pass device. Instead, OV prevents the LTC4364 from restarting following a fault (see Cool Down Period and Restart). This prevents the pass device from cycling between ON and OFF states when the input voltage stays at an elevated level for a long period of time, reducing the stress on the MOSFET.

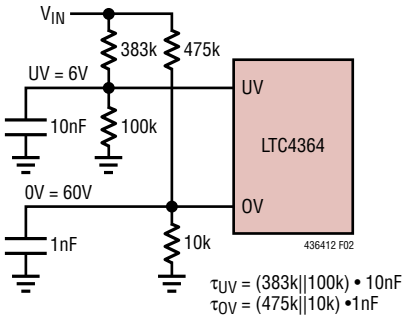

Figure 2. External UV and OV Configuration Blocks Start-Up Into an Overvoltage Condition

Input Undervoltage Comparator

The LTC4364 detects input undervoltage conditions such as low battery using the UV pin. When the voltage at the UV pin is below its 1.25V threshold, the HGATE pin pulls low to keep the pass device off. Once the UV pin voltage rises above the UV threshold plus the UV hysteresis (50mV typical), the HGATE pin is allowed to pull up without going through a timer cycle. In Figure 1 and Figure 2, the input UV threshold is set by the resistive dividers to 6V. An undervoltage condition does not produce an output at the $\overline{FLT}$ pin.

Fault Timer

The LTC4364 includes an adjustable fault timer. Connecting a capacitor from the TMR pin to ground sets the delay period before the MOSFET M1 is turned off during an overvoltage or overcurrent fault condition. The same capacitor also sets the cool down period before M1 is allowed to turn back on after the fault condition has disappeared. Once a fault condition is detected, a current source charges up the TMR pin. The current level varies depending on the voltage drop across the V_{CC} pin and the OUT pin, corresponding to the MOSFET V_{DS}. The on time is inversely proportional to the voltage drop across the MOSFET. This scheme therefore takes better advantage of the available safe operating area (SOA) of the MOSFET than would a fixed timer current.

The timer current starts at around 2µA with 0.5V or less of $V_{CC} – V_{OUT}$, increasing linearly to 50µA with 75V of $V_{CC} – V_{OUT}$ during an overvoltage fault (Figure 3a):

$$I_{TMR(UP)OV} = 2\mu A + 0.644[\mu A/V] \bullet (V_{CC} – V_{OUT} – 0.5V)$$

During an overcurrent fault, the timer current starts at 10µA with 0.5V or less of $V_{CC} – V_{OUT}$ and increases to 260µA with 75V of $V_{CC} – V_{OUT}$ (Figure 3b):

$$I_{TMR(UP)OC} = 10\mu A + 3.36[\mu A/V] \bullet (V_{CC} – V_{OUT} – 0.5V)$$

This arrangement allows the pass device to turn off faster during an overcurrent event, since more power is dissipated under this condition. Refer to the Typical Performance Characteristics section for the timer current at different $V_{CC} – V_{OUT}$ in both overvoltage and overcurrent events.

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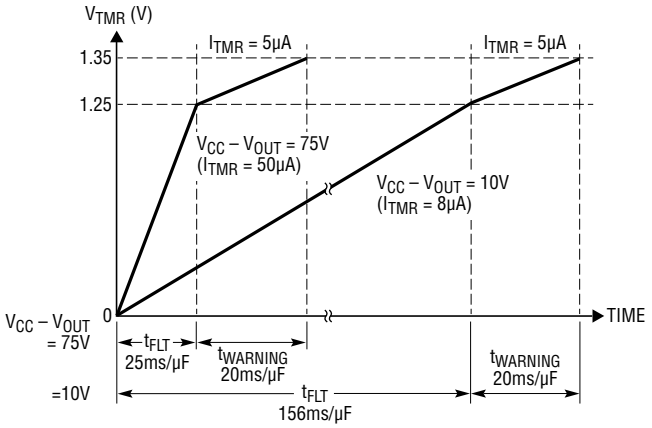
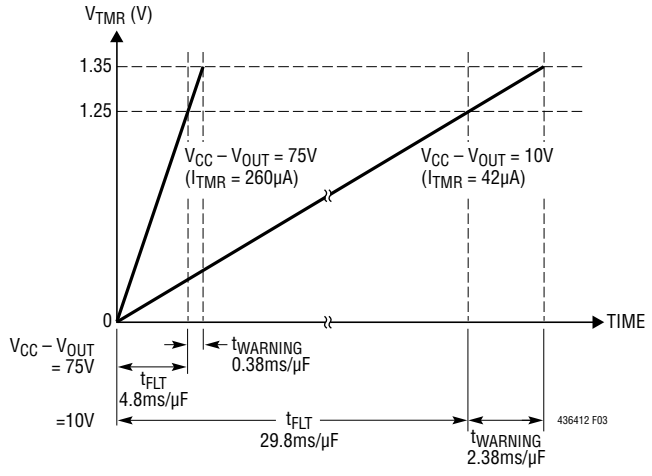


(3a) Overvoltage Fault Timer Current



(3b) Overcurrent Fault Timer Current

Figure 3. Fault Timer Current of the LTC4364

When the voltage at the TMR pin, V_{TMR}, reaches 1.25V, the $\overline{FLT}$ pin pulls low to indicate the detection of a fault condition and provide warning of the impending power loss. In the case of an overvoltage fault, the timer current then switches to a fixed 5µA. The interval between $\overline{FLT}$ asserting low and the MOSFET M1 turning off is given by:

$$t_{WARNING} = \frac{C_{TMR} \bullet 100mV}{5\mu A}$$

This constant early warning period allows the load to perform necessary backup or housekeeping functions before the supply is cut off. After V_{TMR} crosses the 1.35V threshold, the pass device M1 turns off immediately. Note that during an overcurrent event, the timer current is not reduced to 5µA after V_{TMR} has reached 1.25V threshold, since it would lengthen the overall fault timer period and cause more stress on the power transistor during an overcurrent event.

Assuming $V_{CC} – V_{OUT}$ remains constant, the on-time of HGATE during an overvoltage fault is:

$$t_{OV} = \frac{C_{TMR} \bullet 1.25V}{I_{TMR(UP)OV}} + \frac{C_{TMR} \bullet 100mV}{5\mu V}$$

and that during an overcurrent fault is:

$$t_{OC} = \frac{C_{TMR} \bullet 1.35V}{I_{TRM(UP)OC}}$$

If the fault condition disappears after TMR reaches 1.25V but is lower than 1.35V, the TMR pin is discharged by 2µA. When TMR drops to 0.15V, the $\overline{FLT}$ pin resets to a high impedance state.

Cool Down Period and Restart

As soon as TMR reaches 1.35V and HGATE pulls low in a fault condition, the TMR pin starts discharging with a 2µA current. When the TMR pin voltage drops to 0.15V, TMR charges with 2µA. When TMR reaches 1.35V, it starts discharging again with 2µA. This pattern repeats 32 times to form a long cool down timer period before retry (Figure 4). At the end of the cool down period (when the TMR pin voltage drops to 0.15V the 32nd time), the voltage at the OV pin is checked. If the OV voltage is above its 1.25V threshold, retry is inhibited and the HGATE pin remains low. If the OV pin voltage is below 1.25V minus the OV hysteresis, the LTC4364-2 retries, pulling the HGATE pin up and turning on the pass device M1. The $\overline{FLT}$ pin will then go to a high impedance state. The total cool down timer period is given by:

$$t_{COOL} = \frac{63 \bullet C_{TMR} \bullet 1.2V}{2\mu A}$$

The latch-off version, LTC4364-1, latches the HGATE and $\overline{FLT}$ pins low after a fault timeout. It also generates the cool down TMR pulses as shown in Figure 4, but does not retry after the cool down period. There are two ways to restart the part. The first method is to pull the UV pin below 0.6V momentarily (>10µs) after the cool down timer

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period. If the UV reset pulse is asserted during the cool down period, the TMR pulses are unaffected and the part restarts after the cool down period ends. If OV is higher than 1.25V while UV reset pulse is applied, the part will not restart until OV drops below 1.25V even if the cool down period ends.

The second method of restarting the LTC4364-1 is to pulse the $\overline{SHDN}$ pin low for more than 200µs. If this is applied during the cool down period, the cool down timer is reset with 1mA quickly discharging the TMR pin, and the part will restart when TMR drops below 0.15V. If the $\overline{SHDN}$ reset pulse is applied after the cool down period, the part restarts immediately. Sufficient cool down time should be allowed before toggling the $\overline{SHDN}$ pin to prevent overstressing the pass device.

A UV reset pulse has no effect on the operation of the LTC4364-2. However, if a $\overline{SHDN}$ reset pulse as described above is asserted in the middle of the cool down period, the TMR pin quickly discharges with 1mA and the LTC4364-2 is allowed to restart once TMR drops below 0.15V. The OV pin gates the restart of either LTC4364-1 or LTC4364-2 with a $\overline{SHDN}$ reset pulse. The part will not restart until OV drops below 1.25V.

Reverse Input Protection

The LTC4364 can withstand reverse voltage without damage. The V_{CC}, $\overline{SHDN}$, UV, OV, HGATE, SOURCE and DGATE pins can all withstand up to –40V with respect to GND.

The LTC4364 controls a second N-channel MOSFET (M2) as an ideal diode to replace an in-line blocking diode for reverse input protection with minimum voltage drop in normal operation. In the event of an input short or a power supply brownout, reverse current may temporarily flow through M2. The LTC4364 detects this reverse current and immediately pulls the DGATE pin to the SOURCE pin, turning off M2. This minimizes discharge of the output reservoir capacitor and holds up the output voltage. In the case where the input supply drops below ground, the SOURCE pin is pulled below ground through the body diode of M1. The LTC4364 responds to this condition by shorting the DGATE pin to the SOURCE pin, keeping M2 off.

MOSFET Selection

The LTC4364 drives two N-channel MOSFETs, M1 and M2, as the pass devices to conduct the load current (Figure 1). The important features are on-resistance, $R_{DS(ON)}$, the maximum drain-source voltage, $V_{(BR)DSS}$, the threshold voltage, and the safe operating area, SOA.

The maximum drain-source voltage rating must be higher than the maximum input voltage. If the output is shorted to ground or in an overvoltage event, the full supply voltage will appear across M1. If the input is shorted to ground, M2 will be stressed by the voltage held up at the output.

The gate drive for both MOSFETs is guaranteed to be more than 10V and less than 16V for those applications with V_{CC} higher than 8V. This allows the use of standard threshold voltage N-channel MOSFETs. For systems with V_{CC} less than 8V, a logic-level MOSFET is required since the gate drive can be as low as 5V. For supplies of 24V or higher, a 15V Zener diode is recommended to be placed between

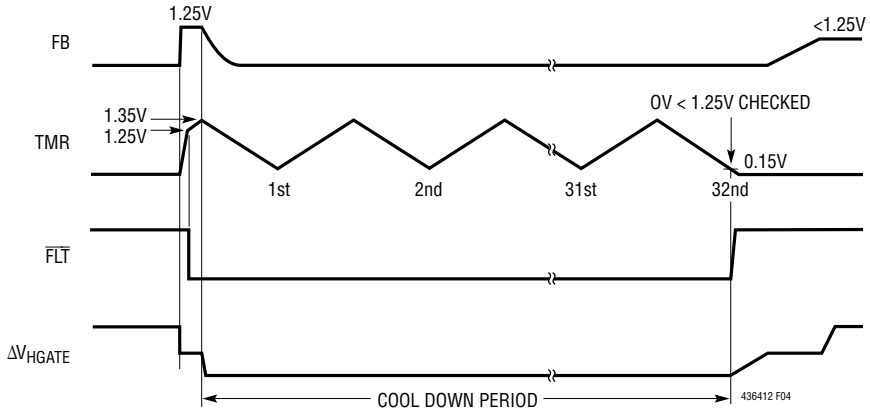

Figure 4. Auto-Retry Cool Down Timer Cycle Following an Overvoltage Fault (LTC4364-2 Only)

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gate and source of each MOSFET for extra protection (Figures 8 to 10).

Transient Stress in the MOSFET

The SOA of the MOSFET must encompass all fault conditions. In normal operation the pass devices are fully on, dissipating very little power. But during either overvoltage or overcurrent faults, the HGATE pin is controlled to regulate either the output voltage or the current through MOSFET M1. Large current and high voltage drop across M1 can coexist in these cases. The SOA curves of the MOSFET must be considered carefully along with the selection of the fault timer capacitor.

During an overvoltage event, the LTC4364 drives the pass MOSFET M1 to regulate the output voltage at an acceptable level. The load circuitry may continue operating throughout this interval, but only at the expense of dissipation in the MOSFET pass device. MOSFET dissipation or stress is a function of the input voltage waveform, regulation voltage and load current. The MOSFET must be sized to survive this stress.

Most transient event specifications use the model shown in Figure 5. The idealized waveform comprises a linear ramp of rise time t_r, reaching a peak voltage of V_{PK} and exponentially decaying back to V_{IN} with a time constant of τ. A typical automotive transient specification has constants of t_r = 10µs, V_{PK} = 80V and τ = 1ms. A surge condition known as "load dump" has constants of t_r = 5ms, V_{PK} = 60V and τ = 200ms.

MOSFET stress is the result of power dissipated within the device. For long duration surges of 100ms or more, stress is increasingly dominated by heat transfer; this is a matter of device packaging and mounting, and heat sink thermal mass. This is analyzed by simulation, using the MOSFET's thermal model.

For short duration transients of less than 100ms, MOSFET survival is increasingly a matter of SOA, an intrinsic property of the MOSFET. SOA quantifies the time required at any given condition of V_{DS} and I_D to raise the junction temperature of the MOSFET to its rated maximum. MOSFET SOA is expressed in units of watt-squared-seconds (P^2t), which is an integral of $P(t)^2dt$ over the duration of the transient. This figure is essentially constant for intervals of less than 100ms for any given device type, and rises to infinity under DC operating conditions. Destruction mechanisms other than bulk die temperature distort the lines of an accurately drawn SOA graph so that P^2t is not the same for all combinations of I_D and V_{DS}. In particular P^2t tends to degrade as V_{DS} approaches the maximum rating, rendering some devices useless for absorbing energy above a certain voltage.

Calculating Transient Stress

To select a MOSFET suitable for any given application, the SOA stress of M1 must be calculated for each input transient which shall not interrupt operation. It is then a simple matter to choose a device which has adequate SOA to survive the maximum calculated stress. P^2t for a prototypical transient waveform is calculated as follows (Figure 6).

Let:

$a = V_{REG} - V_{IN}$

$b = V_{PK} - V_{IN}$

where V_{IN} = Nominal Input Voltage.

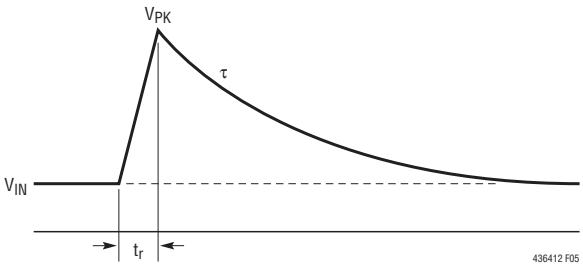

Figure 5. Prototypical Transient Waveform

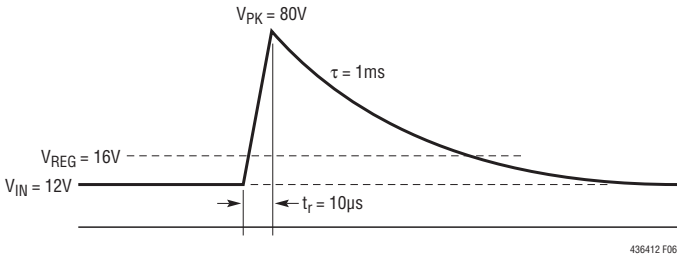

Figure 6. Safe Operating Area Required to Survive Prototypical Transient Waveform

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Then:

$$P^2t = I_{LOAD}{}^2\left[\frac{1}{3}t_r\frac{(b-a)^3}{b}+\frac{1}{2}\tau\left(2a^2\ln\frac{b}{a}+3a^2+b^2-4ab\right)\right]$$

Typically $V_{REG} \approx V_{IN}$ and $\tau >> t_r$ simplifying the above to:

$$P^2t = \frac{1}{2}I_{LOAD}{}^2\left(V_{PK}-V_{REG}\right)^2\tau$$

For the transient conditions of V_{PK} = 80V, V_{IN} = 12V, V_{REG} = 16V, t_r = 10µs and τ = 1ms, and a load current of 3A, P^2t is 18.4W^2s—easily handled by a MOSFET in a D-pak package. The P^2t of other transient waveshapes is evaluated by integrating the square of MOSFET power versus time. LTSpice™ can be used to simulate timer behavior for more complex transients and cases where overvoltage and overcurrent faults coexist.

Short-Circuit Stress

SOA stress of M1 must also be calculated for output short-circuit conditions. Short-circuit P^2t is given by:

$$P^2t = \left(V_{IN}\bullet\frac{\Delta V_{SNS}}{R_{SNS}}\right)^2\bullet t_{OC}$$

where ΔV_{SNS} is the overcurrent fault threshold and t_{OC} is the overcurrent timer interval.

For V_{IN} = 15V, OUT = 0V, ΔV_{SNS} = 25mV, R_{SNS} = 12mΩ and C_{TMR} = 100nF, P^2t is 2.2W^2s—less than the transient SOA calculated in the previous example. Nevertheless, to account for circuit tolerances this figure should be doubled to 4.4W^2s.

Limiting Inrush Current and HGATE Pin Compensation

The LTC4364 limits the inrush current to any load capacitance by controlling the HGATE pin voltage slew rate. An external capacitor, C_{HG}, can be connected from HGATE to ground to slow down the inrush current further at the expense of slower turn-off time. The gate capacitor is set at:

$$C_{HG} = \frac{I_{HGATE(UP)}}{I_{INRUSH}}\bullet C_L$$

where $I_{HGATE(UP)}$ is the HGATE pin pull-up current, I_{INRUSH} is the desired inrush current, C_L is total load capacitance at the output. In typical applications, a C_{HG} of 6.8nF is recommended for loop compensation during overvoltage and overcurrent events. With input voltage steps faster than 5V/µs, a larger gate capacitor helps prevent self enhancement of the N-channel MOSFET.

The added gate capacitor slows down the turn-off time during fault conditions and allows higher peak currents to build up during an output short event. If this is a concern, an extra resistor, R6, in series with C_{HG} can restore the turn-off time. A diode, D5, should be placed across R6 with the cathode connected to C_{HG} as shown in Figure 1. In a fast transient input step, D5 provides a bypass path to C_{HG} for the benefit of holding HGATE low and preventing self enhancement.

Shutdown

The LTC4364 can be shut down to a low current mode by pulling $\overline{SHDN}$ below 0.5V. The quiescent V_{CC} current drops to 10µA for both the LTC4364-1 and the LTC4364-2.

The $\overline{SHDN}$ pin can be pulled up to 100V or below GND by up to 40V without damage. Leaving the pin open allows an internal current source to pull it up to about 4V and turn the part on. The leakage current at the pin should be limited to no more than 1µA if no pull-up device is used to help turn it on.

Supply Transient Protection

The LTC4364 is tested to operate to 80V and guaranteed to be safe from damage between 100V and –40V. Voltage transients above 100V or below –40V may cause permanent damage. During a short-circuit condition, the large change in current flowing through power supply traces coupled with parasitic inductances from associated wiring can cause destructive voltage transients in both positive and negative directions at the V_{CC}, SOURCE, and OUT pins. To reduce the voltage transients, minimize the power trace parasitic inductance by using short, wide traces. A small RC filter (R4 and C1 in Figure 1) at the V_{CC} pin filters high voltage spikes of short pulse width.

APPLICATIONS INFORMATION

Another way to limit supply transients above 100V at the V_{CC} pin is to use a Zener diode and a resistor, D1 and R4, as shown in Figure 1. D1 clamps voltage spikes at the V_{CC} pin while R4 limits the current through D1 to a safe level during the surge. In the negative direction, D1 along with R4 clamps the V_{CC} pin near GND. The inclusion of R4 in series with the V_{CC} pin increases the minimum required supply voltage due to the extra voltage drop across the resistor, which is determined by the supply current of the LTC4364 and the leakage current of D1. 2.2k adds about 1V to the minimum operating voltage.

For sustained, elevated suppy voltages, the power dissipation of R4 becomes unacceptable. This can be resolved by using an external NPN transistor (Q1 in Figure 7) as a buffer. To protect Q1 against supply reversal, block the collector of Q1 with a series diode or tie it to the cathode of D3 and D4 in Figure 1.

Transient suppressor D3 in Figure 1 clamps the input voltage to 200V for voltage transients higher than 200V, to prevent breakdown of M1. It also blocks forward conduction in D4. D4 limits the SOURCE pin voltage to 24V below GND when the input goes negative. C_{OUT} helps absorb the inductive energy at the output upon a sudden input short, protecting the OUT and SENSE pins.

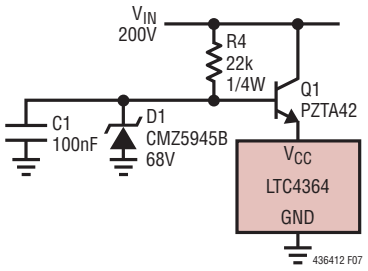


Figure 7. Buffering V_{CC} to Extend Input Supply Range

Output Bypassing

The OUT and SENSE pins can withstand up to 100V above and 20V below GND. In all applications the output must be bypassed with at least 22µF low ESR electrolytic (C_{OUT} in Figure 1) to stabilize the voltage and current limiting loops, and to minimize capacitive feedthrough of input transients. Total ceramic bypassing of up to one-tenth the total electrolytic capacitance is permissible without compromising performance.

Output Port Protection

In applications where the output is on a connector, as shown in Figure 14, if the output is plugged into a supply that is higher than the input, the ideal diode MOSFET, M2, turns off to open the backfeeding path. In the case where the output port is plugged into a supply that is below GND, the SOURCE pin is pulled below GND through the body diode of M2. The LTC4364 responds to this condition by shorting the HGATE pin to the SOURCE pin, turning M1 off and shutting down the current path from V_{IN} to V_{OUT}.

Design Example

As a design example, consider an application with the following specifications: V_{IN} = 8V to 14V DC with a peak transient of 200V and decay time constant τ of 1ms, V_{OUT} ≤ 27V, minimum current limit $I_{LIM(MIN)}$ at 4A, low-battery detection at 6V, input overvoltage level at 60V, and 1ms of overvoltage early warning (Figure 1).

Selection of CMZ5945B for D1 will limit the voltage at the V_{CC} pin to less than 71V during the 200V surge. The minimum required voltage at the V_{CC} pin is 4V when V_{IN} is at 6V; the maximum supply current for LTC4364 is 750µA. The maximum value for R4 to ensure proper operation is:

$$R4 = \frac{6V - 4V}{0.75mA} = 2.7k$$

Select 2.2k for R4 to accommodate all conditions.

With the minimum Zener voltage at 64V, the peak current through R4 into D1 is then calculated as:

$$I_{D1(PK)} = \frac{200V - 64V}{2.2k} = 62mA$$

which can be handled by the CMZ5945B with a peak power rating of 200W at 10/1000µs.

With a bypass capacitance of 0.1µF (C1), along with R4 of 2.2k, high voltage transients up to 250V with a pulse width less than 20µs are filtered out at the V_{CC} pin.

Next, calculate the resistive divider value to limit V_{OUT} to 27V during an overvoltage event:

$$V_{REG} = \frac{1.25V \bullet (R7 + R8)}{R8} = 27V$$

APPLICATIONS INFORMATION

Choosing 250µA for the resistive divider:

$$R8 = \frac{1.25V}{250\mu A} = 5k$$

Select 4.99k for R8.

$$R7 = \frac{(27V - 1.25V) \bullet R8}{1.25V} = 102.8k$$

The closest standard value for R7 is 102k.

Now, calculate the sense resistor, R_{SNS}, value:

$$R_{SNS} = \frac{\Delta V_{SNS(MIN)}}{I_{LIM}} = \frac{45mV}{4A} = 11m\Omega$$

Choose 10mΩ for R_{SNS}.

C_{TMR} is then chosen for 1ms of early warning time:

$$C_{TMR} = \frac{1ms \bullet 5\mu A}{100mV} = 50nF$$

The closest standard value for C_{TMR} is 47nF.

Finally, calculate R1, R2 and R3 for 6V low battery detection and 60V input overvoltage level:

$$\frac{6V}{R1+R2+R3} = \frac{1.25V}{R2+R3}$$

$$\frac{60V}{R1+R2+R3} = \frac{1.25V}{R3}$$

Simplify the equations and choose 10k for R3 to get:

$$R2 = \left(\frac{60V}{6V} - 1\right) \bullet R3 = 9 \bullet R3 = 90k$$

$$R1 = \left(\frac{6V}{1.25V} - 1\right) \bullet (R2+R3) = 3.8 \bullet (R1+R2) = 380k$$

Select 90.9kΩ for R2 and 383kΩ for R1.

The pass device, M1, should be chosen to withstand an output short condition with V_{CC} = 14V. In the case of a severe output short where V_{OUT} = 0V, $I_{TMR(UP)}$ = 55µA and the total overcurrent fault time is:

$$t_{OC} = \frac{C_{TMR} \bullet V_{TMR(G)}}{I_{TRM(UP)}} = \frac{47nF \bullet 1.35V}{55\mu A} = 1.15ms$$

The maximum power dissipation in M1 is:

$$P = \frac{\Delta V_{DS(M1)} \bullet \Delta V_{SNS(MAX)}}{R_{SNS}} = \frac{14V \bullet 32mV}{10m\Omega} = 45W$$

The corresponding P^2t is $2.3W^2s$.

During an output overload or soft short, the voltage at the OUT pin could stay at 2V or higher. The total overcurrent fault time when V_{OUT} = 2V is:

$$t_{OC} = \frac{47nF \bullet 1.35V}{49\mu A} = 1.3ms$$

The maximum power dissipation in M1 is:

$$P = \frac{(14V - 2V) \bullet 55mV}{10m\Omega} = 66W$$

The corresponding P^2t is $5.7W^2s$. Both of the above conditions are well within the safe operating area of FDB33N25.

To select the pass device, M2, first calculate $R_{DS(ON)}$ to achieve the desired forward drop V_{FW} at maximum load current (5.5A). If V_{FW} = 0.25V:

$$R_{DS(ON)} \leq \frac{V_{FW}}{I_{LOAD(MAX)}} = \frac{0.25V}{5.5A} = 45.5m\Omega$$

The FDB3682 offers a maximum $R_{DS(ON)}$ of 36mΩ at V_{GS} = 10V so is a good fit. Its minimum BV_{DSS} of 100V is also sufficient to handle V_{OUT} transients up to 100V during an input short-circuit event.

Layout Considerations

To achieve accurate current sensing, use Kelvin connections to the current sense resistor, R_{SNS}. Limit the resistance from the SOURCE pin to the sources of the MOSFETs to below 10Ω. The minimum trace width for 1oz copper foil is 0.02" per amp to ensure the trace stays at a reasonable temperature. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/square. Small resistances can cause large errors in high current applications. Noise immunity will be improved significantly by locating resistive dividers close to the pins with short V_{CC} and GND traces.

TYPICAL APPLICATIONS

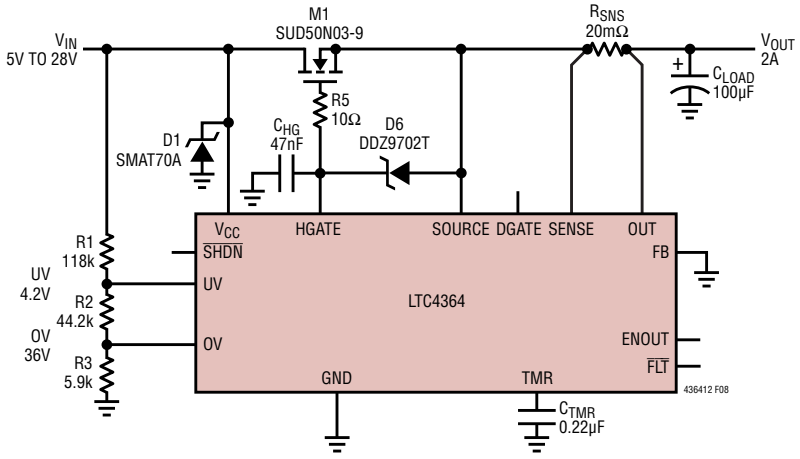


Figure 8. 2A Wide Range Hot Swap Controller with Circuit Breaker

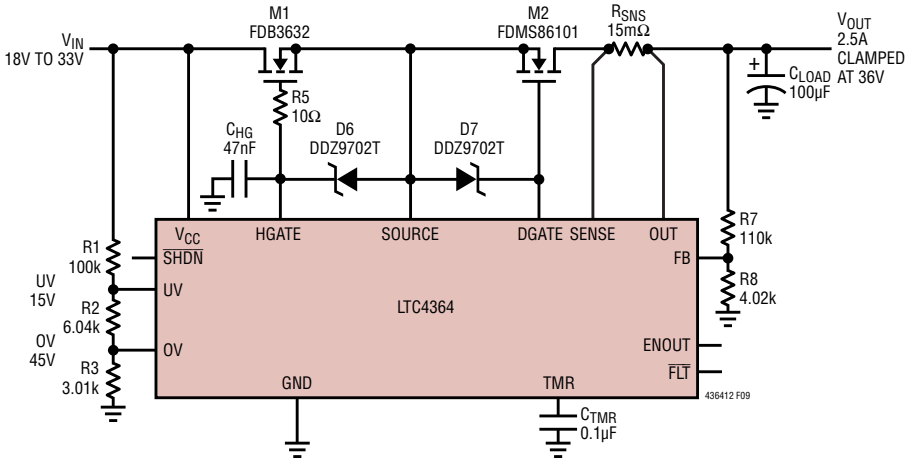


Figure 9. 28V Hot Swap with Overvoltage Output Regulation at 27V, Circuit Breaker, and Reverse Current Protection

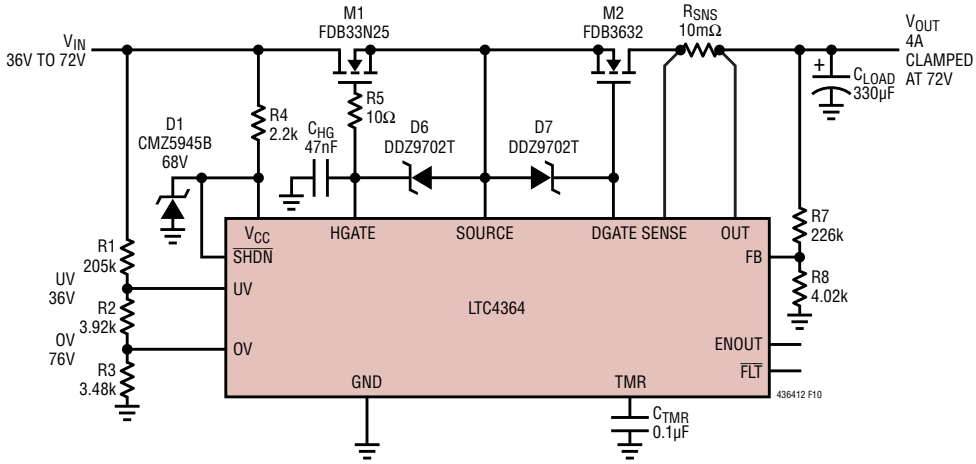


Figure 10. 48V Hot Swap with Overvoltage Output Regulation at 72V, Circuit Breaker, and Reverse Current Protection

TYPICAL APPLICATIONS

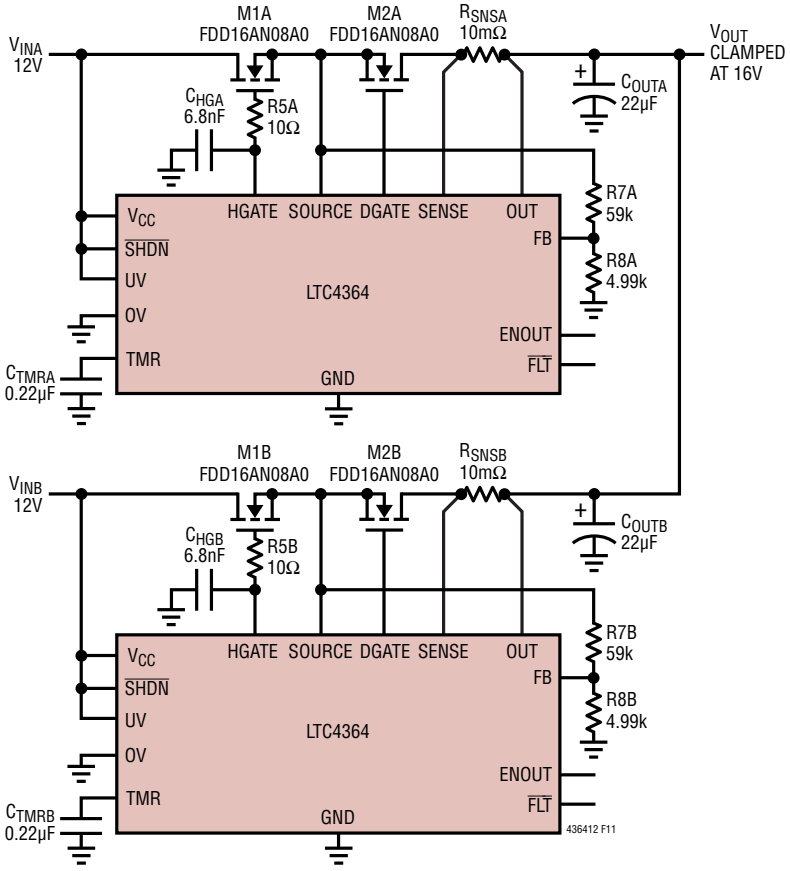


Figure 11. Redundant Supply Diode-OR with Overvoltage Surge Protection

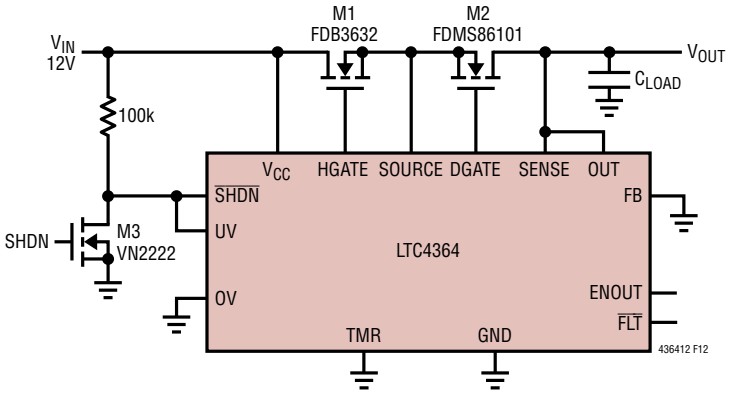


Figure 12. High Side Switch with Ideal Diode for Load Protection

TYPICAL APPLICATIONS

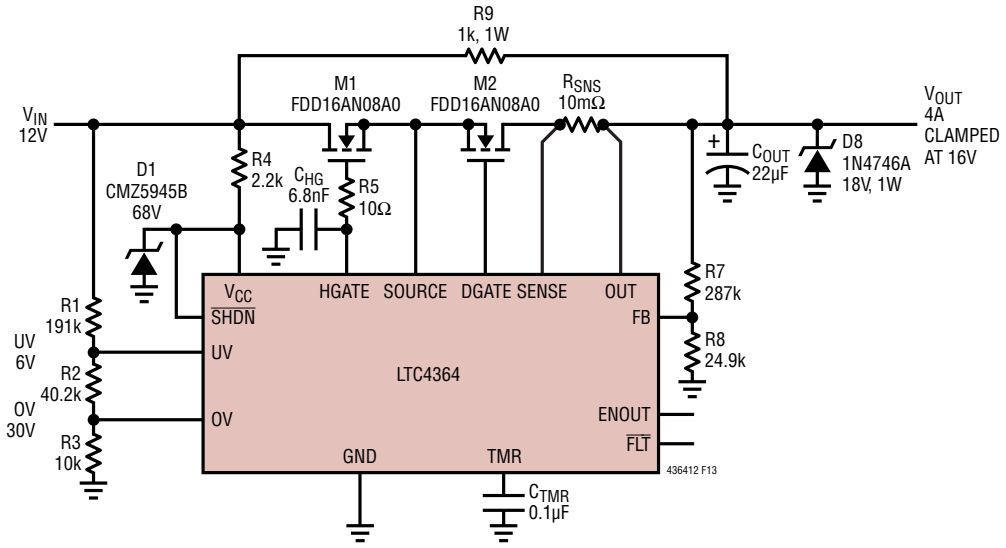
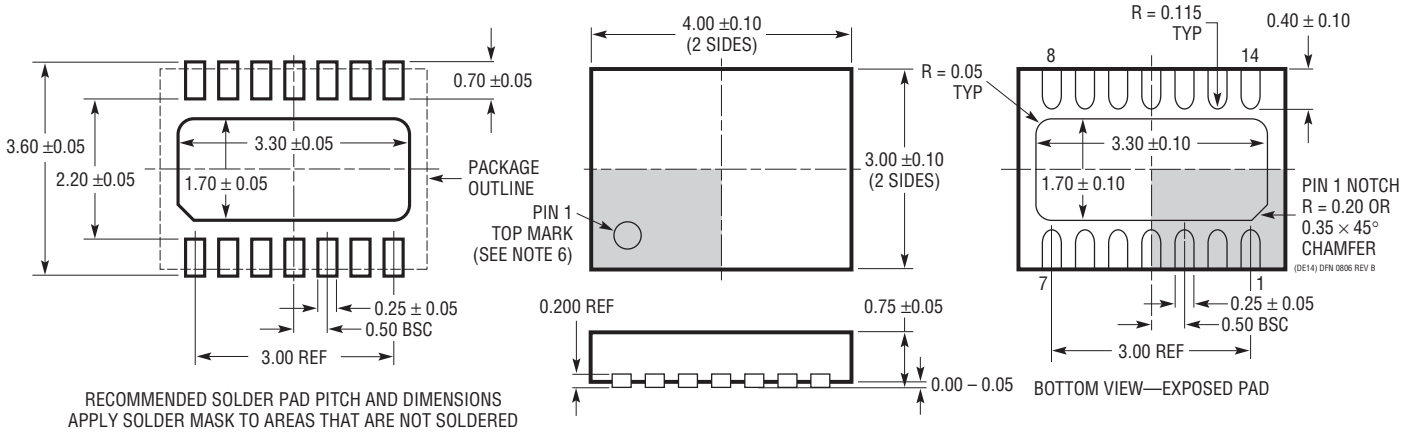


Figure 13. Overvoltage Regulator with Output Keep Alive During Shutdown

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)

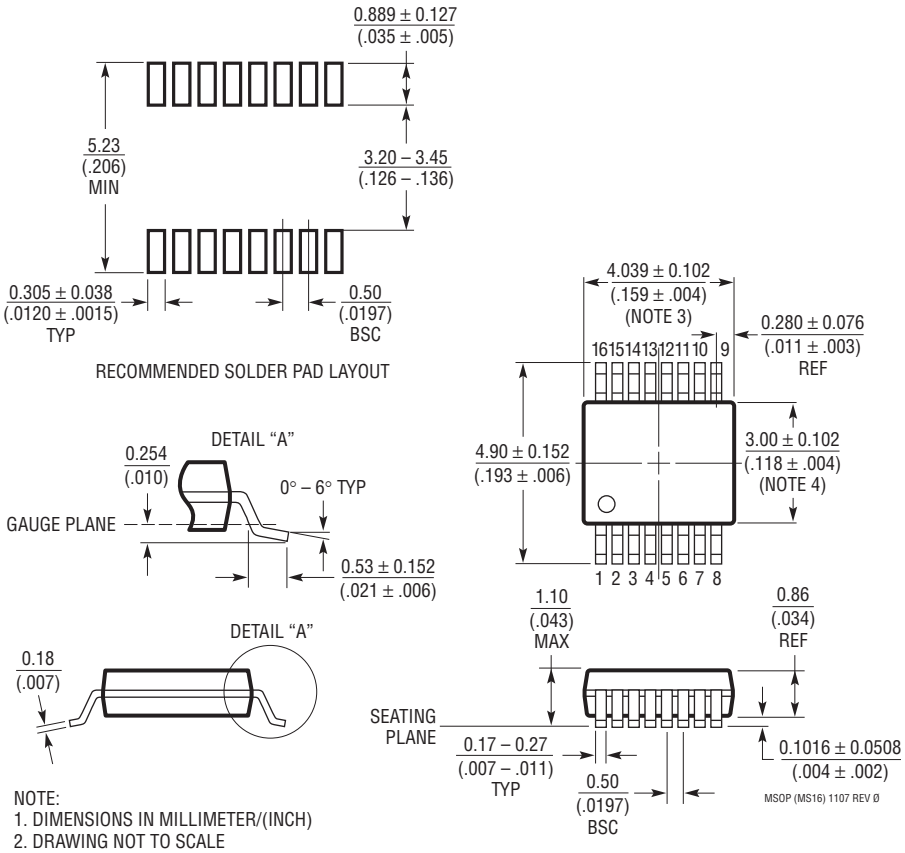


NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)

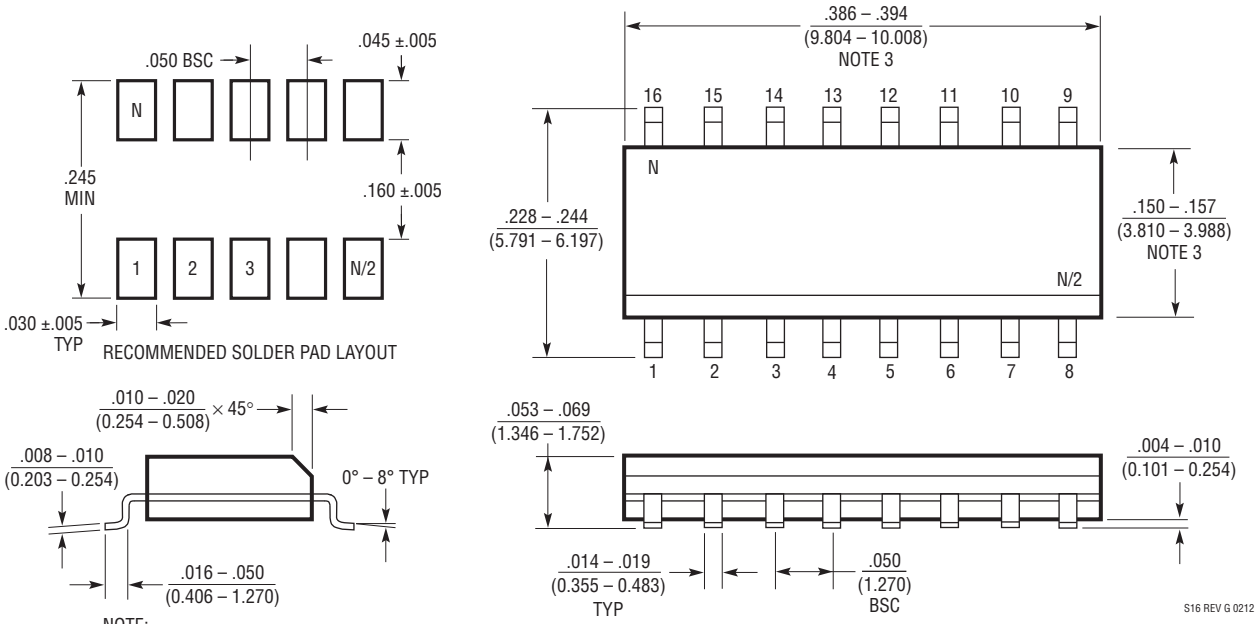


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

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TYPICAL APPLICATION

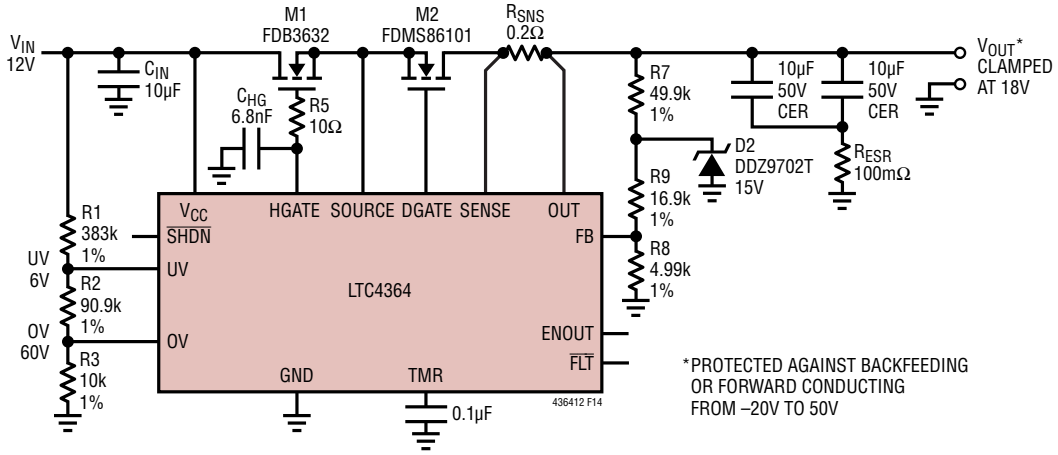

Figure 14. 0.25A, 12V Surge Stopper with Output Port Protection

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®4356-1/LT4356-2 LT4356-3	Surge Stopper	LT4356-1: 7A Shutdown Mode LT4356-2: Auxiliary Amplifier Alive in Shutdown Mode LT4356-3: Fault Latchoff
LTC4363	High Voltage Surge Stopper	4V to 80V, V_{CC} Clamp, Adjustable Output Voltage Clamp, 60V Reverse Input Protection, Overcurrent Protection
LTC4366	Floating Surge Stopper	9V to >500V Operation, Adjustable Output Voltage Clamp
LTC4357	Positive High Voltage Ideal Diode Controller	0.5µs Turn-Off Time, 9V to 80V
LTC4359	Ideal Diode Controller with Reverse Input Protection	4V to 80V Operation, –40V Reverse-Input Protection, Low 13µA Shutdown Current
LTC4352	Ideal MOSFET ORing Diode	External N-Channel MOSFETs Replace ORing Diodes, 0V to 18V
LTC4354	Negative Voltage Diode-OR Controller	Controls Two N-Channel MOSFETs, 1µs Turn-Off, 80V Operation
LTC4355	Positive Voltage Diode-OR Controller	Controls Two N-Channel MOSFETs, 0.5µs Turn-Off, 80V Operation
LTC4365	Window Passer - OV, UV and Reverse Supply Protection Controller	2.5V to 34V Operation, Protects 60V to –40V

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