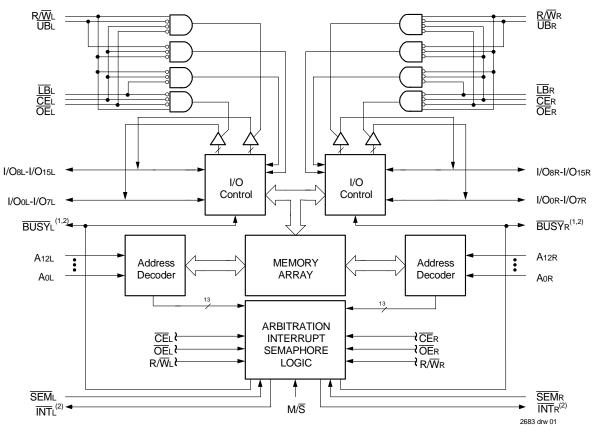
8K x STAT	H-SPEED IDT7025S/L 16 DUAL-PORT FIC RAM
<ul> <li>LEAD FINISH (SNPb) ARE IN EOL PROC Features</li> <li>True Dual-Ported memory cells which allow simultaneous reads of the same memory location</li> <li>High-speed access <ul> <li>Military: 20/25/35/55/70ns (max.)</li> <li>Industrial: 55ns (max.)</li> <li>Commercial: 15/17/20/25/35/55ns (max.)</li> </ul> </li> <li>Low-power operation <ul> <li>IDT7025S</li> <li>Active: 750mW (typ.)</li> <li>Standby: 5mW (typ.)</li> </ul> </li> </ul>	<ul> <li>CESS - LAST TIME BUY EXPIRES JUNE 15, 2018</li> <li>IDT7025 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device</li> <li>M/S = H for BUSY output flag on Master M/S = L for BUSY input on Slave</li> <li>Interrupt Flag</li> <li>On-chip port arbitration logic</li> <li>Full on-chip hardware support of semaphore signaling between ports</li> <li>Fully asynchronous operation from either port</li> <li>Battery backup operation—2V data retention</li> </ul>

- IDT7025L
   Active: 750mW (typ.)
   Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- TTL-compatible, single 5V (±10%) power supply
- Available in 84-pin PGA, Flatpack, PLCC, and 100-pin Thin Quad Flatpack
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information



### NOTES:

2. BUSY outputs and INT outputs are non-tri-stated push-pull.

MARCH 2018

# Functional Block Diagram

<sup>1. (</sup>MASTER): BUSY is output; (SLAVE): BUSY is input.

### Military, Industrial and Commercial Temperature Ranges

## Description

The IDT7025 is a high-speed 8K x 16 Dual-Port Static RAM. The IDT7025 is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit or more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, errorfree operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down

DI/O7L DI/06L DI/06L DI/04L DI/02L DI/02L DI/02L DI/07L DI/07L DI/06L DI/06L DI/06L DI/06L INDEX Ę 11/06/01 10 9 8 7 6 5 4 3 2 1 84 83 82 81 80 79 78 77 75 74 I/O8L 12 A7L I/O9L A6L 73 13 A5L I/O10L 72 14 A4L 71 I/011L 15 A3L I/O12L 70 16 A2L I/O13L 69 17 A1L GND [ 18 68 - Aol I/O14L IDT7025J or F 67 19 J84-1(4) I/O15L 20 66 F84-2(4) BUSYL Vcc 🗆 21 65 84-Pin PLCC/Flatpack GND GND 🗌 22 64 Top View(5) ⊐м/₅ I/OOR 23 63 I/O1R 62 24 61 I/O2R 25 Vcc 🗆 60 AOR 26 □<sub>A1R</sub> I/O3R 27 59 I/O4R 28 58 A2R I/O5R 57 ∃ A3R 29 🗆 A4R I/O6R 30 56 I/O7R A5R 31 55 54 5<u>3</u> A6R I/O8R 32 33 34 35 
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 54</t 2683 drw 02 Index A9L A7L **∆**6L 11/06/01 ΠΠ Π Π ⊐ N/C N/C 76 75 74 N/C N/C ⊏ N/C ⊏ 73 F ⊐ N/C ⊐ N/C N/C ⊏ 72 I/O10L □ 71 F ⊐ A5L I/O11I □ 70 I/O12L 🖵 69 I/O13L □ ⊐ A2L 68 GND 💳 ⊐ A1L 67 I/O14L -10 ⊐ A<sub>0L</sub> IDT7025PF 66 I/O15L 🖵 PN100-1(4) 65 BUSY 64 100-Pin TOFP GND □ 63 ⊐ GND 13 Top View<sup>(5</sup> ⊐ m/s 14 62 F I/O1R □ 15 61 F I/O2R -16 60 F Vcc -17 ⊐ A0R 59 NOTES I/O3R □ ⊐ A1R 18 58 I/O4R -19 ⊐ A2R 1. All Vcc pins must be connected to power supply. 57 I/O5R □ 56 ⊐ A3R 20 2. All GND pins must be connected to ground supply. ⊐ A4R I/O6R 21 55 F 3 J84-1 package body is approximately 1.15 in x 1.15 in x .17 in. 54 N/C N/C ⊏ 22 F84-2 package body is approximately 1.17 in x 1.17 in x .11 in. 53 ⊐ N/C PN100-1 package body is approximately 14mm x 14mm x 1.4mm. N/C ⊏ 52 ⊐ N/C 24 ⊐ N/C N/C = 4. This package code is used to reference the package diagram. 
 No
 No<

# Pin Configurations<sup>(1,2,3)</sup>

feature controlled by Chip Enable (CE) permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

The IDT7025 is packaged in a ceramic 84-pin PGA, an 84-pin Flatpack, PLCC, and a 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

A9R A8R A7R A6R A6R A5R

2683 drw 03

5 This text does not indicate orientation of the actual part-marking.

# Pin Configurations<sup>(1,2,3)</sup> (con't.)

	63	61	60	58	55	54	51	48	46	45	42
11	I/O7L	I/O5L	I/O4L	I/O2L	I/Ool	ŌĒL	SEML	LBL	A11L	A10L	A7L
	66	64	62	59	56	49	50	47	44	43	40
10	I/O10L	I/O8L	I/O6L	I/O3L	I/O1L	UBL	CEL	A12L	A9L	A8L	A5L
	67	65			57	53	52			41	39
09	I/O11L	I/O9L			GND	Vcc	R/WL			A6L	A4L
	69	68						1		38	37
08	I/O13L	I/O12L								АзL	A2L
	72	71	73					33	35	34	
07	I/O15L	I/O14L	Vcc			IDT7025	BUSYL	Aol	INTL		
	75	70	74			G84-3 <sup>(4</sup>		32	31	36	
06	I/O0R	GND	GND			84-Pin PC			GND	M/S	A1L
	76	77	78			Top View	(5)		28	29	30
05	I/O1r	I/O2R	Vcc						Aor	ĪNTR	BUSY
	79	80								26	27
04	I/O3r	I/O4R								A2R	A1R
	81	83			7	11	12	]		23	25
03	I/O5r	I/O7R			GND	GND	SEMR			A5R	Азr
	82	1	2	5	8	10	14	17	20	22	24
02	I/O6R	I/O9R	I/O10R	I/O13R	I/O15R	R/WR	ŪBR	A11R	A8R	A6R	A4R
	84	3	4	6	9	15	13	16	18	19	21
01	I/O8r	I/O11R	I/O12R	I/O14R	ŌĒr	LBR	CER	A12R	A10R	A9R	A7R
1	A	В	С	D	E	F	G	Н	J	К	L
/ dex											2683 dr

#### 11/06/01

### NOTES:

- 1. All Vcc pins must be connected to power supply.
- 2. All GND pins must be connected to ground supply.
- 3. Package body is approximately 1.12 in x 1.12 in x .16 in.
- 4. This package code is used to reference the package diagram.
- 5. This text does not indicate orientation of the actual part-marking.

## Military, Industrial and Commercial Temperature Ranges

# **Pin Names**

Left Port	Right Port	Names					
Ē	ĒĒR	Chip Enable					
R/WL	R/Wr	Read/Write Enable					
OEL	<del>0E</del> r	Output Enable					
Aol - A12l	Aor - A12r	Address					
VO0L - VO15L	1/Oor - 1/015r	Data Input/Output					
SEML	<b>SEM</b> R	Semaphore Enable					
ŪBL	ŪBR	Upper Byte Select					
ĒΒ	<b>LB</b> R	Lower Byte Select					
ĪNTL	ĪNTr	Interrupt Flag					
BUSYL	<b>BUSY</b> R	Busy Flag					
Μ	/ <del>S</del>	Master or Slave Select					
V	сс	Power					
G	ND	Ground					

# Truth Table I: Non-Contention Read/Write Control

		Inpu	uts <sup>(1)</sup>			Outputs		
CE	R/₩	ŌĒ	UB	LB	SEM	I/O8-15	I/O0-7	Mode
Н	Х	Х	Х	Х	Н	High-Z	High-Z	Deselected
Х	Х	Х	Н	Н	Н	High-Z	High-Z	Both Bytes Deselected
L	L	Х	L	Н	Н	DATAIN	High-Z	Write to Upper Byte Only
L	L	Х	Н	L	Н	High-Z	DATAIN	Write to Lower Byte Only
L	L	Х	L	L	Н	DATAIN	DATAIN	Write to Both Bytes
L	Н	L	L	Н	Н	DATAOUT	High-Z	Read Upper Byte Only
L	Н	L	Н	L	Н	High-Z	DATAOUT	Read Lower Byte Only
L	Н	L	L	L	Н	DATAOUT	DATAOUT	Read Both Bytes
Х	Х	Н	Х	Х	Х	High-Z High-Z		Outputs Disabled

NOTE:

1. AOL — A12L  $\neq$  AOR — A12R.

# Truth Table II: Semaphore Read/Write Control<sup>(1)</sup>

		Inp	outs			Outputs		
ĈĒ	R/₩	ŌĒ	ŪB	ĹΒ	SEM	I/O8-15	I/O0-7	Mode
Н	Н	L	Х	Х	L	DATAOUT	DATAOUT	Read Semaphore Flag Data Out
Х	Н	L	Н	Н	L	DATAOUT	DATAOUT	Read Semaphore Flag Data Out
Н	Ŷ	Х	Х	Х	L	DATAIN	DATAIN	Write I/Oo into Semaphore Flag
Х	Ŷ	Х	Н	Н	L	DATAIN	DATAIN	Write I/Oo into Semaphore Flag
L	Х	Х	L	Х	L			Not Allowed
L	Х	Х	Х	L	L			Not Allowed
								2683 tbl 03

### NOTES:

1. There are eight semaphore flags written to via I/Oo and read from I/Oo - I/O15. These eight semaphores are addressed by Ao - A2.

### Military, Industrial and Commercial Temperature Ranges

# Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Military	Unit
Vterm <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
Tbias	Temperature Under Bias	-55 to +125	-65 to +135	٥C
Tstg	Storage Temperature	-65 to +150	-65 to +150	٥C
Іоит	DC Output Current	50	50	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to  $\leq$  20 mA for the period over VTERM  $\geq$  Vcc + 10%.

# Capacitance<sup>(1)</sup> (TA = +25°C, f = 1.0mhz)

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
Cin	Input Capacitance	VIN = 3dV	9	рF
Соит	Output Capacitance	Vout = 3dV	10	pF

NOTES:

 This parameter is determined by device characterization but is not production tested. For TQFP package only.

 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

# $\label{eq:maximum} \begin{array}{l} \text{Maximum Operating Temperature} \\ \text{and Supply Voltage}^{(1)} \end{array}$

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V <u>+</u> 10%
Commercial	0°C to +70°C	0V	5.0V <u>+</u> 10%
Industrial	-40°C to +85°C	0V	5.0V <u>+</u> 10%

NOTES:

2683 tbl 04

2683 tbl 07

1. This is parameter TA. This is the "instant on" case temperature.

# Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit					
Vcc	Supply Voltage	4.5	5.0	5.5	V					
GND	Ground	0	0	0	V					
VIH	Input High Voltage	2.2		6.0 <sup>(2)</sup>	V					
VIL	Vı∟ Input Low Voltage			0.8	V					
	2683 tbl 06									

NOTES:

1. VIL  $\geq$  -1.5V for pulse width less than 10ns.

2. VTERM must not exceed Vcc + 10%.

# DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

			7025S		70:		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Мах.	Unit
lu	Input Leakage Current <sup>(1)</sup>	Vcc = 5.5V, VIN = 0V to Vcc	—	10	I	5	μA
Ilo	Output Leakage Current	Vout = 0V to Vcc	—	10	I	5	μA
Vol	Output Low Voltage	IOL = +4mA	—	0.4	I	0.4	V
Vон	Output High Voltage	IOH = -4mA	2.4	—	2.4	-	V

NOTE:

1. At Vcc  $\leq$  2.0V input leakages are undefined.

2683 tbl 08

2683 tbl 09a

2683 tbl 09b

# DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(1)</sup> ( $Vcc = 5.0V \pm 10\%$ )

				Version		iX15 Only	7025 Com'l		7025 Com' & Mi		7025 Com Milit	1 &	
Symbol	Parameter	Test Condition	Version			Max.	Тур. <sup>(2)</sup>	Max.	Тур. <sup>(2)</sup>	Max.	Тур. <sup>(2)</sup>	Max.	Unit
lcc	Icc Dynamic Operating Current (Both Ports Active)	rrent SEM = V⊮	COM'L	S L	170 170	310 260	170 170	310 260	160 160	290 240	155 155	265 220	mA
		$f = fMAX^{(3)}$	MIL & IND	S L					160 160	370 320	155 155	340 280	
ISB1	(Both Ports - TTL	$\overline{\underline{CE}}_{L} = \overline{\underline{CE}}_{R} = VH$ $\overline{SEMR}_{R} = \overline{SEML}_{L} = VH$	COM'L	S L	20 20	60 50	20 20	60 50	20 20	60 50	16 16	60 50	mA
	Level Inputs)	$f = f_{MAX}^{(3)}$	MIL & IND	S L					20 20	90 70	16 16	80 65	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^{A^*} = V_{IL}$ and $\overline{CE}^{B^*} = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$	COM'L	S L	105 105	190 160	105 105	190 160	95 95	180 150	90 90	170 140	mA
	Level inputs)	$\frac{T = TMAX^{(4)}}{SEMR} = \overline{SEML} = VIH$	MIL & IND	S L					95 95	240 210	90 90	215 180	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	$\label{eq:cell} \overline{CE} \mbox{and } \overline{CE} \mbox{$\ge$ Vcc - 0.2V$,} \\ V_{IN} \mbox{$\ge$ Vcc - 0.2V$ or} \\ V_{IN} \mbox{$<$ 0.2V$, $f = 0^{(4)}$} \\ \end{array}$	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	15 5	mA
	civios Level inpuis)	$\frac{VIN}{SEMR} = \frac{V}{SEML} \ge VCC - 0.2V$	MIL & IND	S L					1.0 0.2	30 10	1.0 0.2	30 10	
ISB4	(One Port - $\overline{CE}_{B''} > Vcc - 0.2V^{(5)}$	$CE'B'' > VCC - 0.2V^{(5)}$	COM'L	S L	100 100	170 140	100 100	170 140	90 90	155 130	85 85	145 120	mA
	CMOS Level Inputs)	$ \begin{array}{l} \overline{SEM_{R}} = \overline{SEM_{L}} \geq Vcc \cdot 0.2V \\ \overline{V_{N}} \geq Vcc \cdot 0.2V \\ or Vin \leq 0.2V \\ Active Port Outputs Disabled, \\ f = f_{MAX}^{(3)} \end{array} $	MIL & IND	S L	_				90 90	225 200	85 85	200 170	

					7025 Com Mili	18	7025X55 Com'l, Ind & Military		7025X70 Military Only		
Symbol	Parameter	Test Condition	Version		Тур. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Мах.	Unit
lcc	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = VIL, Outputs Disabled $\overline{SEM}$ = VIH f = fmAx <sup>(3)</sup>	COM'L	S L	150 150	250 210	150 150	250 210	_		mA
(BUILFOILS ACTIVE)	1 = IMAX''	MIL & IND	S L	150 150	300 250	150 150	300 250	140 140	300 250		
ISB1	SB1 Standby Current $\overline{CE}_{L} = \overline{CE}_{R} = V_{H}$ (Both Ports - TTL SEMR = SEML = V <sub>H</sub> Level Inputs) $f = f_{MAX}^{(3)}$	COM'L	S L	13 13	60 50	13 13	60 50			mA	
	Level inputs)	1 = IMAX''	MIL & IND	S L	13 13	80 65	13 13	80 65	10 10	80 65	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$ 'A <sup>*</sup> = VIL and $\overline{CE}$ 'B <sup>*</sup> = VIH <sup>(5)</sup> Active Port Outputs Disabled, f=fmax <sup>(8)</sup>	COM'L	S L	85 85	155 130	85 85	155 130			mA
	Level inputs)	$\overline{\frac{I=IMAX^{e_{j}}}{SEM}} = \overline{SEM}L = VH$	MIL & IND	S L	85 85	190 160	85 85	190 160	80 80	190 160	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}_{L}$ and $\overline{CE}_{R} \ge Vcc - 0.2V$ , $V_{N} \ge Vcc - 0.2V$ or $V_{N} = 0.2V$ f = 0.40	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5			mA
	Civilos Level Inpuls)	$\frac{V_{\text{IN}} \leq 0.2V_{\text{L}}f = 0^{(4)}}{\text{SEMR} = \text{SEML} \geq \text{Vcc} - 0.2\text{V}}$	MIL & IND	S L	1.0 0.2	30 10	1.0 0.2	30 10	1.0 0.2	30 10	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	<del>CE</del> a∗ <u>≤</u> 0.2V and <del>CE</del> <sup>B</sup> * <u>&gt;</u> Vcc - 0.2V <sup>(5)</sup> SEMR = SEML > Vcc - 0.2V	COM'L	S L	80 80	135 110	80 80	135 110			mA
	Givios Level Inpuis)	$\begin{array}{l} SEMR = SEMR \geq VCC \cdot 0.2V \\ V_{N} \geq VCC \cdot 0.2V \text{ or } V_{N} \leq 0.2V \\ Active \ port \ Outputs \ Disabled, \\ f = f_{MAX^{(3)}} \end{array}$	MIL & IND	S L	80 80	175 150	80 80	175 150	75 75	175 150	

### NOTES:

1. 'X' in part number indicates power rating (S or L)

2. Vcc = 5V, TA = +25°C, and are not production tested. Icc dc = 120mA (TYP)

3. At f = fMAX, address and I/O's are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.

4. f = 0 means no address or control lines change.

5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

# Data Retention Characteristics Over All Temperature Ranges (L Version Only)

Symbol	Parameter	Test Con	dition	Min.	Тур. <sup>(1)</sup>	Max.	Unit
Vdr	Vcc for Data Retention	Vcc = 2V		2.0	_		V
ICCDR	Data Retention Current	CE ≥ VHC	MIL. & IND.	_	100	4000	μA
		Vin $\geq$ Vhc or $\leq$ Vlc	COM'L.	_	100	1500	
tcdr <sup>(3)</sup>	Chip Deselect to Data Retention Time	$\overline{\text{SEM}} \ge \text{VHC}$		0	_	_	ns
tR <sup>(3)</sup>	Operation Recovery Time			tRC <sup>(2)</sup>	_		ns
				-	-	2	683 tbl 10

NOTES:

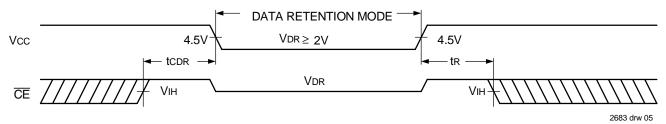
1. TA =  $+25^{\circ}$ C, Vcc = 2V, and are not production tested.

2. tRc = Read Cycle Time

3. This parameter is guaranteed by device characterization, but is not production tested.

4. At Vcc  $\leq$  2.0V input leakages are undefined.

# Data Retention Waveform



# AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2
	2/02 #1 11

2683 tbl 11

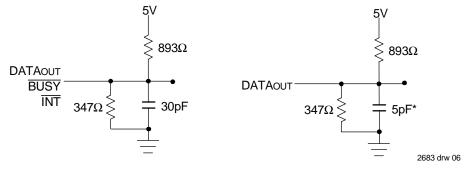


Figure 1. AC Output Test Load

Figure 2. Output Test Load (for tLz, tHz, twz, tow) \* including scope and jig.

# AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(4)</sup>

			5X15 I Only		5X17 I Only	Com	5X20 'I, Ind ilitary	Cor	5X25 n'I & itary	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE			1	1	1	1	1	1	1	1
trc	Read Cycle Time	15	—	17	—	20	—	25	—	ns
taa	Address Access Time		15	-	17	—	20	—	25	ns
tace	Chip Enable Access Time <sup>(3)</sup>	—	15	—	17	—	20	—	25	ns
tabe	Byte Enable Access Time <sup>(3)</sup>	—	15	—	17	—	20	—	25	ns
taoe	Output Enable Access Time <sup>(3)</sup>	_	10	-	10	_	12	_	13	ns
toн	Output Hold from Address Change	3	—	3	—	3	—	3		ns
tLZ	Output Low-Z Time <sup>(1,2)</sup>	3	_	3	_	3	—	3	_	ns
tHZ	Output High-Z Time <sup>(1,2)</sup>		10	—	10		12		15	ns
teu	Chip Enable to Power Up Time <sup>(1,2)</sup>	0	_	0		0	—	0		ns
tPD	Chip Disable to Power Down Time <sup>(1,2)</sup>		15	—	17	_	20	_	25	ns
tsop	Semaphore Flag Update Pulse (OE or SEM)	10	_	10	—	10	—	10		ns
tsaa	Semaphore Address Access <sup>(3)</sup>		15	_	17	_	20	_	25	ns
			I						I	2683 tbl 12
				Cor	5X35 n'l & itary	Com	5X55 'I, Ind ilitary		5X70 'y Only	
Symbol	Parameter			Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE										
trc	Read Cycle Time			35	—	55	—	70		ns
taa	Address Access Time			_	35	_	55	-	70	ns
tace	Chip Enable Access Time <sup>(3)</sup>			—	35	_	55	-	70	ns
tabe	Byte Enable Access Time <sup>(3)</sup>			—	35	_	55		70	ns
taoe	Output Enable Access Time <sup>(3)</sup>			—	20	_	30		35	ns
toн	Output Hold from Address Change			3	-	3	-	3	—	ns
tLZ	Output Low-Z Time <sup>(1,2)</sup>			3	—	3	—	3	—	ns
tнz	Output High-Z Time <sup>(1,2)</sup>			—	15	_	25	_	30	ns
tPU	Chip Enable to Power Up Time <sup>(1,2)</sup>			0	—	0	—	0	—	ns
	Chip Disable to Power Down Time <sup>(1,2)</sup>			—	35	—	50	—	50	ns
tPD										
ted tsop	Semaphore Flag Update Pulse (OE or SEM)			15	—	15	—	15	—	ns

2683 tbl 12b

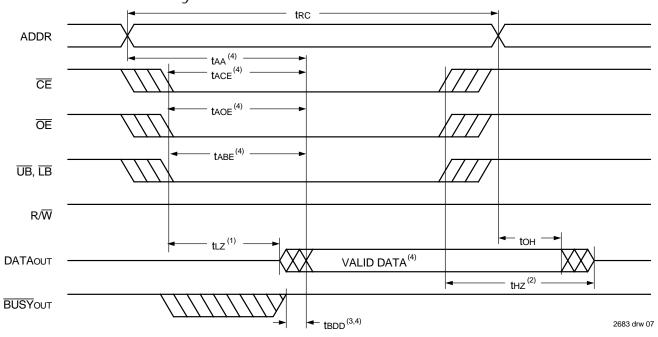
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).

2. This parameter is guaranteed by device characterazation, but is not production tested. 3. To access RAM,  $\overline{CE} = V_{IL}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ , and  $\overline{SEM} = V_{IH}$ . To access semephore,  $\overline{CE} = V_{IH}$  or  $\overline{UB} \& \overline{LB} = V_{IH}$ , and  $\overline{SEM} = V_{IL}$ .

4. 'X' in part number indicates power rating (S or L).

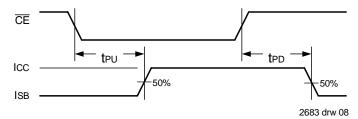
# Waveform of Read Cycles<sup>(5)</sup>



### NOTES:

- 1. Timing depends on which signal is asserted last,  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$ ,  $\overline{\text{LB}}$ , or  $\overline{\text{UB}}$ .
- 2. Timing depends on which signal is de-asserted first,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{LB}}$ , or  $\overline{\text{UB}}$ .
- 3. tbdb delay is required only in case where opposite port is completing a write operation to the same address location for simultaneous read operations BUSY has no relation to valid output data.
- 4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
- 5.  $\overline{SEM} = VIH.$

# Timing of Power-Up Power-Down



# AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(5)</sup>

			5X15 I Only		5X17 'I Only	Com	5X20 I'l, Ind Iilitary	Cor	5X25 n'l & itary	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE		-		•			-	-	•	-
twc	Write Cycle Time	15		17		20	—	25		ns
tew	Chip Enable to End-of-Write <sup>(3)</sup>	12		12		15		20		ns
taw	Address Valid to End-of-Write	12		12	—	15	—	20	—	ns
tas	Address Set-up Time <sup>(3)</sup>	0		0	—	0	—	0	—	ns
twp	Write Pulse Width	12		12	—	15	_	20	_	ns
twr	Write Recovery Time	0		0	_	0	_	0	-	ns
tow	Data Valid to End-of-Write	10		10		15	_	15		ns
tHZ	Output High-Z Time <sup>(1,2)</sup>		10	—	10	—	12		15	ns
tон	Data Hold Time <sup>(4)</sup>	0	-	0	-	0	_	0	_	ns
twz	Write Enable to Output in High-Z <sup>(1,2)</sup>	—	10	_	10	_	12		15	ns
tow	Output Active from End-of-Write <sup>(1,2,4)</sup>	0	_	0		0	_	0		ns
tswrd	SEM Flag Write to Read Time	5	-	5	-	5	-	5	_	ns
tsps	SEM Flag Contention Window	5		5		5	_	5		ns
										2/02 #1 12-
										2083 101 133
				Cor	5X35 n'I & itary	Com	5X55 'l, Ind ilitary		5X70 'y Only	2683 tbl 13a
Symbol	Parameter			Cor	n'l &	Com	'l, Ind		5X70	Unit
Symbol WRITE CYCLE				Cor Mili	n'l & itary	Com & Mi	'l, Ind ilitary	Militar	5X70 'y Only	-
-				Cor Mili	n'l & itary	Com & Mi	'l, Ind ilitary	Militar	5X70 'y Only	-
WRITE CYCLE				Cor Mili Min.	n'I & itary Max.	Com & Mi Min.	'l, Ind litary Max.	Militar Min.	5X70 y Only Max.	Unit
WRITE CYCLE	Write Cycle Time			Cor Mili Min. 35	n'I & itary Max. 	Com & Mi Min. 55	'I, Ind ilitary Max.	Militar Min. 70	5X70 •y Only Max.	<b>Unit</b> ns
WRITE CYCLE twc tew	Write Cycle Time Chip Enable to End-of-Write <sup>(3)</sup>			Cor Mili Min. 35 30	n'I & itary Max. 	Com & Mi Min. 55 45	'I, Ind ilitary Max.	Militar Min. 70 50	5X70 y Only Max.	Unit ns ns
WRITE CYCLE twc tew taw	Write Cycle Time Chip Enable to End-of-Write <sup>(3)</sup> Address Valid to End-of-Write			Cor Mil Min. 35 30 30 30	n'l & itary Max. 	Com & Mi Min. 55 45 45	'I, Ind ilitary Max. 	Militar Min. 70 50 50	5X70 y Only Max.	Unit ns ns
WRITE CYCLE twc tew taw tas	Write Cycle Time Chip Enable to End-of-Write <sup>(3)</sup> Address Valid to End-of-Write Address Set-up Time <sup>(3)</sup>			Cor Mili Min. 35 30 30 0	n'l & itary Max. — — —	Com & Mi Min. 55 45 45 45 0	'l, Ind Ilitary Max.	Militar Min. 70 50 50 0	5X70 y Only Max. 	Unit ns ns ns ns
WRITE CYCLE twc tew taw tas twp	Write Cycle Time Chip Enable to End-of-Write <sup>(3)</sup> Address Valid to End-of-Write Address Set-up Time <sup>(3)</sup> Write Pulse Width			Cor Mil Min. 35 30 30 0 25	n'l & itary Max.	Com & M Min. 55 45 45 0 40	'l, Ind lilitary Max.	Militar Min. 70 50 50 0 50	5X70 y Only Max.	Unit ns ns ns ns ns
WRITE CYCLE Nuc tew taw taw tas twp twr	Write Cycle Time         Chip Enable to End-of-Write <sup>(3)</sup> Address Valid to End-of-Write         Address Set-up Time <sup>(3)</sup> Write Pulse Width         Write Recovery Time         Data Valid to End-of-Write			Cor Mil Min. 35 30 30 0 25 0	n'l & itary Max.	Com & M Min. 55 45 45 0 40 0	'l, Ind litary Max. —————— —————————————————————————————	Militar Min. 70 50 50 0 50 0 0	5X70 y Only Max.	Unit Ins Ins Ins Ins Ins Ins Ins
WRITE CYCLE twc tew taw tas twp twp twr tww tww tww tww tww tww tww	Write Cycle Time         Chip Enable to End-of-Write <sup>(3)</sup> Address Valid to End-of-Write         Address Set-up Time <sup>(3)</sup> Write Pulse Width         Write Recovery Time			Cor Mil 35 30 30 0 25 0 15	n'i & itary Max. — — — — — — — — —	Com & M Min. 55 45 45 0 40 0 30	'l, Ind litary Max. —— —— —— —— —— ——	Militar Min. 70 50 50 0 50 0 0	5X70 y Only Max.	Unit ns ns ns ns ns ns ns ns ns
WRITE CYCLE Nuc tew taw taw tas twp twr twr twr thz	Write Cycle Time         Chip Enable to End-of-Write <sup>(3)</sup> Address Valid to End-of-Write         Address Set-up Time <sup>(3)</sup> Write Pulse Width         Write Recovery Time         Data Valid to End-of-Write         Output High-Z Time <sup>(1,2)</sup>			Cor Mil Min. 35 30 30 0 25 0 25 0 15 	n'i & itary Max. — — — — — — — 15	Com & M Min. 55 45 45 0 40 0 30 	'I, Ind litary Max. — — — — — — — — — 25	Militar Min. 70 50 50 0 50 0 50 0 40 	5X70 y Only Max. 	Unit ns ns ns ns ns ns ns ns ns ns
WRITE CYCLE NVC TEW TAW TAS TAS TAS TAS TAS TAS TAS TAS	Write Cycle Time         Chip Enable to End-of-Write <sup>(3)</sup> Address Valid to End-of-Write         Address Set-up Time <sup>(3)</sup> Write Pulse Width         Write Recovery Time         Data Valid to End-of-Write         Output High-Z Time <sup>(1,2)</sup> Data Hold Time <sup>(6)</sup>			Cor Mil Min. 35 30 30 0 25 0 15  0	n'i & itary Max. — — — — — — — 15	Com & M Min. 55 45 45 45 0 40 0 30  0	'I, Ind litary Max. 	Militar Min. 70 50 50 0 50 0 50 0 40  0	5X70 y Only Max. — — — — — — — 30 —	Unit Ins Ins Ins Ins Ins Ins Ins Ins
WRITE CYCLE fwc few few faw faw faw faw faw faw faw fa	Write Cycle Time         Chip Enable to End-of-Write <sup>(3)</sup> Address Valid to End-of-Write         Address Set-up Time <sup>(3)</sup> Write Pulse Width         Write Recovery Time         Data Valid to End-of-Write         Output High-Z Time <sup>(1,2)</sup> Data Hold Time <sup>(6)</sup> Write Enable to Output in High-Z <sup>(1,2)</sup>			Cor Mil Min. 35 30 30 0 25 0 25 0 15  0 	n'i & itary Max. — — — — — 15 — 15	Com & M Min. 555 45 45 0 40 0 30  0 	Ind           Max.           —           —           —           —           —           —           —           —           25           —           25           —           25           —           25	Militar Min. 50 50 0 50 0 40  0 	5X70 y Only Max. 	Unit ns ns ns ns ns ns ns ns ns ns

2683 tbl 13b

NOTES: 1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).

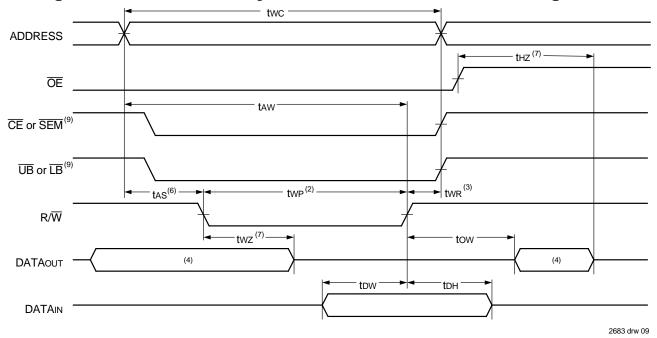
2. This parameter is guaranteed by device characterization, but is not production tested. 3. To access RAM,  $\overline{CE} = V_{IL}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ ,  $\overline{SEM} = V_{IL}$ . To access semaphore,  $\overline{CE} = V_{IH}$  or  $\overline{UB} \& \overline{LB} = V_{IH}$ , and  $\overline{SEM} = V_{IL}$ . Either condition must be valid for the entire tew time.

4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tow values will vary over voltage and temperature, the actual t\_H will always be smaller than the actual tow.

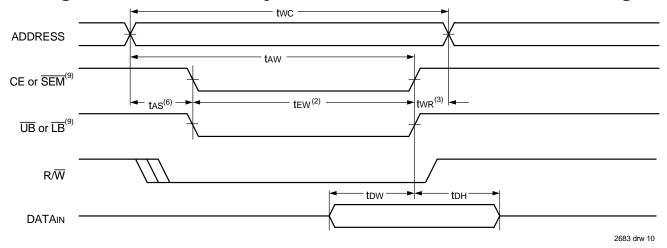
5. 'X' in part number indicates power rating (S or L).

Military, Industrial and Commercial Temperature Ranges

Timing Waveform of Write Cycle No. 1, R/W Controlled Timing<sup>(1,5,8)</sup>



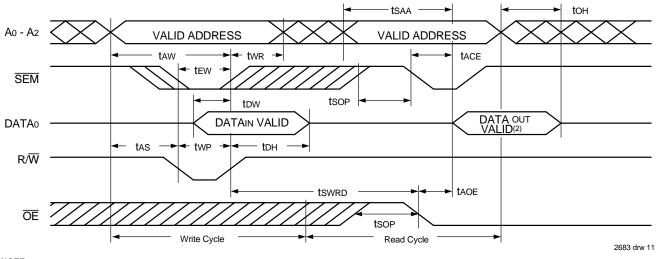
Timing Waveform of Write Cycle No. 2, CE, UB, LB Controlled Timing<sup>(1,5)</sup>



### NOTES:

- 1. R/W or  $\overline{CE}$  or  $\overline{UB} \& \overline{LB} = V_{H}$  during all address transitions.
- 2. A write occurs during the overlap (tew or twp) of a UB or LB = VIL and a CE = VIL and a RW = VIL for memory array writing cycle.
- 3. two is measured from the earlier of  $\overline{CE}$  or  $\overline{R/W}$  (or  $\overline{SEM}$  or  $\overline{R/W}$ ) going to VIH to the end-of-write cycle.
- 4. During this period, the I/O pins are in the output state and input signals must not be applied.
- 5. If the  $\overline{CE}$  or  $\overline{SEM}$  LOW = V<sub>IL</sub> transition occurs simultaneously with or after the R/W = V<sub>IL</sub> transition, the outputs remain in the HIGH impedance state. 6. Timing depends on which enable signal is asserted last,  $\overline{CE}$ , R/W, or byte control.
- 7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with Output Test Load (Figure 2).
- 8. If  $\overrightarrow{OE}$  = VIL during R/W controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If  $\overrightarrow{OE}$  = VIH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.
- 9. To access RAM, CE = VIL, UB or LB = VIL, and SEM = VIH. To access Semaphore, CE = VIH or UB & LB = VIH, and SEM = VIL. tew must be met for either condition.

# Timing Waveform of Semaphore Read after Write Timing, Either Side<sup>(1)</sup>

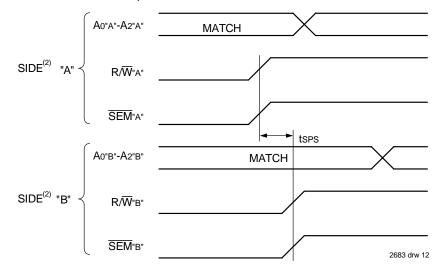


NOTE:

1.  $\overline{CE} = VIH$  or  $\overline{UB} \& \overline{LB} = VIH$  for the duration of the above timing (both write and read cycle).

2. "DATAOUT VALID" represents all I/O's (I/Oo-I/O15) equal to the semaphore value.

# Timing Waveform of Semaphore Write Contention<sup>(1,3,4)</sup>



### NOTES:

- 1. DOR = DOL = VIL,  $\overline{CE}R = \overline{CE}L = VIH$ , or both  $\overline{UB} \& \overline{LB} = VIH$ .
- 2. All timing is the same for left and right port. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 3. This parameter is measured from R/W A" or SEM A" going HIGH to R/W B" or SEM B" going HIGH.
- 4. If tsps is not satisfied, there is no guarantee which side will obtain the semaphore flag.

2683 tbl 14b

# AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range<sup>(6)</sup>

		7025X15 Com'l Ony		7025X17 Com'l Only		7025X20 Com'l, Ind & Military		7025X25 Com'l & Military		
Symbol	ymbol Parameter		Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
BUSY TIMINO	G (M/S = Vін)									
<b>t</b> BAA	BUSY Access Time from Address Match	—	15	—	17		20		20	ns
<b>t</b> BDA	BUSY Disable Time from Address Not Matched		15		17		20		20	ns
<b>t</b> BAC	BUSY Access Time from Chip Enable LOW	_	15	—	17		20		20	ns
<b>t</b> BDC	BUSY Disable Time from Chip Enable HIGH	—	15	—	17		17		17	ns
taps	Arbitration Priority Set-up Time <sup>(2)</sup>	5		5	_	5		5		ns
tBDD	BUSY Disable to Valid Data <sup>(3)</sup>	—	18	—	18		30		30	ns
twн	Write Hold After BUSY <sup>(5)</sup>	12	—	13	_	15		17		ns
BUSY TIMING	G (M/S = VIL)					-		-		-
twв	BUSY Input to Write <sup>(4)</sup>	0	—	0	_	0		0		ns
twн	Write Hold After BUSY <sup>(5)</sup>	12	—	13	_	15		17		ns
PORT-TO-PO	RT DELAY TIMING		-			-	-	-		-
twdd	Write Pulse to Data Delay <sup>(1)</sup>	—	30	—	30		45		50	ns
todd	Write Data Valid to Read Data Delay <sup>(1)</sup>		25		25		35		35	ns
	-	-	-	-	-		-		-	2683 tbl 14

		Con	5X35 n'I & itary	Com	7025X55 Com'l, Ind & Military		7025X70 Military Only	
Symbol	Parameter	Min.	Мах.	Min.	Мах.	Min.	Мах.	Unit
BUSY TIMING	і (М/S̄ = Vін)							
<b>t</b> BAA	BUSY Access Time from Address Match		20		45		45	ns
tBDA	BUSY Disable Time from Address Not Matched	-	20		40		40	ns
<b>t</b> BAC	BUSY Access Time from Chip Enable LOW	_	20		40		40	ns
tbdc	BUSY Disable Time from Chip Enable HIGH	_	20	-	35	_	35	ns
taps	Arbitration Priority Set-up Time <sup>(2)</sup>	5		5	_	5	_	ns
tBDD	BUSY Disable to Valid Data <sup>(3)</sup>	_	35	-	40	_	45	ns
twн	Write Hold After BUSY <sup>(5)</sup>	25		25	_	25		ns
BUSY TIMING	(M/S = VIL)		-					
twв	BUSY Input to Write <sup>(4)</sup>	0	-	0		0	_	ns
twн	Write Hold After BUSY <sup>5)</sup>	25	-	25		25		ns
PORT-TO-POF	RT DELAY TIMING							
twdd	Write Pulse to Data Delay <sup>(1)</sup>		60		80		95	ns
todd	Write Data Valid to Read Data Delay <sup>(1)</sup>		45		65		80	ns

NOTES:

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write Port-to-Port Read and BUSY (M/S = VI+)".

2. To ensure that the earlier of the two ports wins.

3. tBDD is a calculated parameter and is the greater of Ons, twDD - twp (actual) or tDDD - tDw (actual).

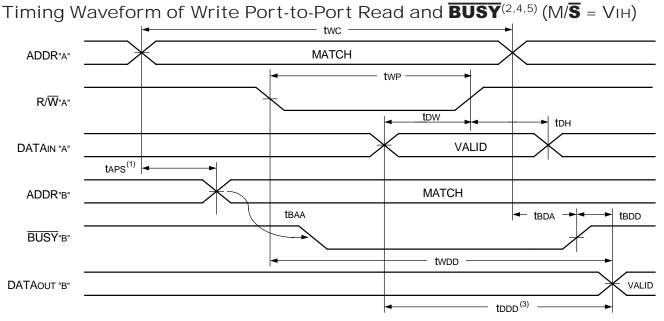
4. To ensure that the write cycle is inhibited on Port "B" during contention with Port "A".

5. To ensure that a write cycle is completed on Port "B" after contention with Port "A".

6. 'X' in part number indicates power rating (S or L).

Military, Industrial and Commercial Temperature Ranges

2683 drw 13



NOTES:

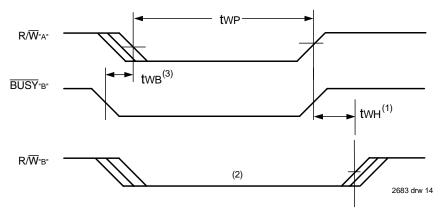
1. To ensure that the earlier of the two ports wins. taps is ignored for  $M/\overline{S} = V_{IL}$  (slave).

- 2.  $\overline{CE}_{L} = \overline{CE}_{R} = VIL.$
- 3.  $\overline{OE} = V_{IL}$  for the reading port.

4. If M/S = VIL (SLAVE), then BUSY is an input. Therefore in this example BUSY\*A\* = VIH and BUSY\*B\* input is shown.

5. All timing is the same for left and right ports. Port "A" may be either the left of right port. Port "B" is the opposite port from Port "A".

# Timing Waveform of Write with **BUSY**

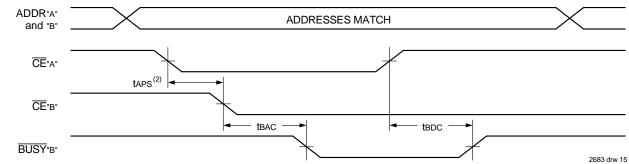


### NOTES:

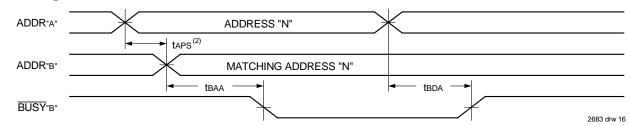
- 1. twh must be met for both  $\overline{\text{BUSY}}$  input (slave) output master.
- 2. BUSY is asserted on port "B" Blocking R/W"B", until BUSY"B" goes HIGH.
- 3. twb is only for the 'Slave' Version.

Military, Industrial and Commercial Temperature Ranges

# Waveform of **BUSY** Arbitration Controlled by $\overline{CE}$ Timing<sup>(1)</sup> (M/ $\overline{S}$ = VIH)



Waveform of **BUSY** Arbitration Cycle Controlled by Address Match Timing<sup>(1)</sup> (M/ $\overline{\mathbf{S}}$  = VIH)



### NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".

2. If taps is not satisfied, the BUSY signal will be asserted on one side or another but there is no guarantee on which side BUSY will be asserted.

# AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(1)</sup>

			7025X15 7025X Com'l Only Com'l O		'I Only C		7025X20 Com'l, Ind & Military		7025X25 Com'l & Military	
Symbol	Parameter	Min.	Max.	Min.	Мах.	Min.	Мах.	Min.	Мах.	Unit
INTERRUPT T	IMING									
tas	Address Set-up Time	0		0	_	0		0	_	ns
twr	Write Recovery Time	0	I	0	-	0	I	0	_	ns
tins	Interrupt Set Time		15	-	15		20	-	20	ns
tinr	Interrupt Reset Time	-	15		15	-	20	-	20	ns

2683 tbl 15a

		Con	5X35 n'l & itary	Com	5X55 I, Ind ilitary		5X70 'y Only	
Symbol	Parameter	Min.	Мах.	Min.	Max.	Min.	Мах.	Unit
INTERRUPT T	IMING		-				-	
tas	Address Set-up Time	0	_	0	_	0	_	ns
twR	Write Recovery Time	0	_	0	_	0	_	ns
tins	Interrupt Set Time	—	25		40	—	50	ns
tinr	Interrupt Reset Time	—	25		40		50	ns

NOTES:

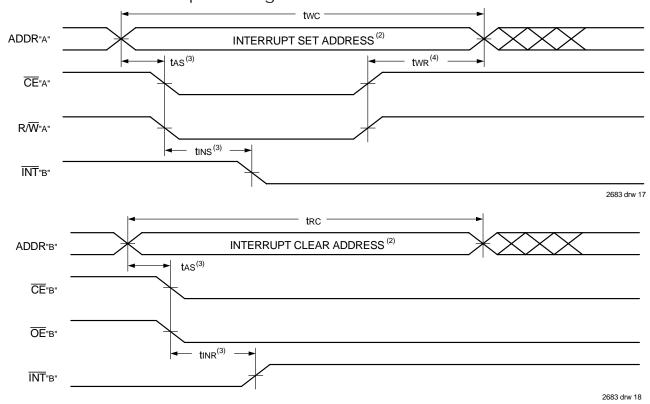
1. 'X' in part number indicates power rating (S or L).

2683 tbl 15b

### Military, Industrial and Commercial Temperature Ranges

Waveform of Interrupt Timing<sup>(1)</sup>

IDT7025S/L High-Speed 8K x 16 Dual-Port Static RAM



### NOTES:

- 1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
- 2. See Interrupt Flag Truth Table.
- 3. Timing depends on which enable signal ( $\overline{CE}$  or  $R/\overline{W}$ ) is asserted last. 4. Timing depends on which enable signal ( $\overline{CE}$  or  $R/\overline{W}$ ) is de-asserted first.

# **Truth Tables**

# Truth Table I — Interrupt Flag<sup>(1)</sup>

Left Port				Right Port						
R/₩L	CEL		A0L-A12L	ĪNT∟	R/WR	CER	<b>OE</b> R	AOR-A12R	ĪNTR	Function
L	L	Х	1FFF	Х	Х	Х	Х	Х	L <sup>(2)</sup>	Set Right INTR Flag
Х	Х	Х	Х	Х	Х	L	L	1FFF	H <sup>(3)</sup>	Reset Right INTR Flag
Х	Х	Х	Х	L <sup>(3)</sup>	L	L	Х	1FFE	Х	Set Left INTL Flag
Х	L	L	1FFE	H <sup>(2)</sup>	Х	Х	Х	Х	х	Reset Left ĪNT∟ Flag
										2689 tbl 16

### NOTES:

1. Assumes  $\overline{\text{BUSY}}_{L} = \overline{\text{BUSY}}_{R} = V_{IH}$ .

2. If  $\overline{\text{BUSY}}L = VIL$ , then no change.

# Truth Table II — Address **BUSY** Arbitration

Inputs			Out	puts	
<u>C</u> E∟	ĊĒr	Aol-A12L Aor-A12r	BUS YL <sup>(1)</sup>	BUSYR <sup>(1)</sup>	Function
Х	Х	NO MATCH	Н	Н	Normal
Η	Х	MATCH	Н	Н	Normal
Х	Н	MATCH	Н	Н	Normal
L	L	MATCH	(2)	(2)	Write Inhibit <sup>(3)</sup>

### NOTES:

2683 tbl 17

1. Pins BUSYL and BUSYR are both outputs when the part is configured as a master. BUSY are inputs when configured as a slave. BUSYx outputs on the IDT7025 are push pull, not open drain outputs. On slaves the BUSY asserted internally inhibits write.

2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either BUSYL or BUSYR = LOW will result. BUSYL and BUSYR outputs cannot be LOW simultaneously.

3. Writes to the left port are internally ignored when BUSYL outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving LOW regardless of actual logic level on the pin.

# Truth Table III — Example of Semaphore Procurement Sequence<sup>(1,2,3)</sup>

Functions	Do - D15 Left	Do - D15 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

### NOTES:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7025.

2. There are eight semaphore flags written to via I/Oo and read from all I/O's. These eight semaphores are addressed by Ao - A2.

3.  $\overline{CE} = V_{IH}$ ,  $\overline{SEM} = V_{IL}$ , to access the semaphores. Refer to the Semaphore Read/Write Truth Table.

# Functional Description

The IDT7025 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7025 has an automatic power down feature controlled by  $\overline{CE}$ . The  $\overline{CE}$  controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ( $\overline{CE} = VIH$ ). When a port is enabled, access to the entire memory array is permitted.

# Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (INTL) is asserted when the right port writes to memory location 1FFE

(HEX), where a write is defined as the  $\overline{CER} = R/\overline{WR} = VIL$  per Truth Table I. The left port clears the interrupt by an address location 1FFE access when  $\overline{CEL} = \overline{OEL} = VIL$ ,  $R/\overline{WL}$  is a "don't care". Likewise, the right port interrupt flag (INTR) is asserted when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ( $\overline{INTR}$ ), the right port must access the memory location 1FFF. The message (16 bits) at 1FFE or 1FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table If or the interrupt operation.

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## **BusyLogic**

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The BUSY pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a BUSY indication, the write signal is gated internally to prevent the write from proceeding.

The use of BUSY logic is not required or desirable for all applications. In some cases it may be useful to logically OR the BUSY outputs together and use any BUSY indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of BUSY logic is not desirable, the BUSY logic can be disabled by placing the part in slave mode with the M/S pin. Once in slave mode the BUSY pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the BUSY pins HIGH. If desired, unintended write operations can be prevented to a port by tying the BUSY pin for that port LOW.

The BUSY outputs on the IDT 7025 RAM in master mode, are pushpull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.

# Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT7025 RAM array in width while using  $\overline{BUSY}$  logic, one master part is used to decide which side of the RAM array will receive a  $\overline{BUSY}$  indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the  $\overline{BUSY}$  signal as a write inhibit signal. Thus on the IDT7025 RAM the  $\overline{BUSY}$  pin is an output if the part is used as a master (M/S pin = VIH), and the  $\overline{BUSY}$  pin is an input if the part used as a slave (M/S pin = VIL) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating  $\overline{\text{BUSY}}$  on one side of the array and another master indicating  $\overline{\text{BUSY}}$  on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The BUSY arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a  $\overline{BUSY}$  flag to be output from the master before the actual write pulse can be initiated with either the  $R/\overline{W}$  signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

## Semaphores

The IDT7025 is an extremely fast Dual-Port 8K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the

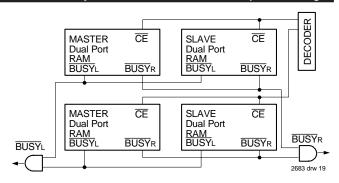


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7025 RAMs.

left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by  $\overline{CE}$ , the Dual-Port RAM enable, and  $\overline{SEM}$ , the semaphore enable. The  $\overline{CE}$  and  $\overline{SEM}$  pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table I where  $\overline{CE}$  and  $\overline{SEM}$  are both = VIH.

Systems which can best use the IDT7025 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7025's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7025 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very highspeed systems.

# How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request

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that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7025 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a LOW input on the  $\overline{SEM}$  pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address,  $\overline{OE}$ , and  $R/\overline{W}$ ) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0–A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select (SEM) and output enable ( $\overline{OE}$ ) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal (SEM or  $\overline{OE}$ ) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Truth Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

## Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7025's Dual-Port RAM. Say the 8K x 16 RAM was to be divided into two 4K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be

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variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has

been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

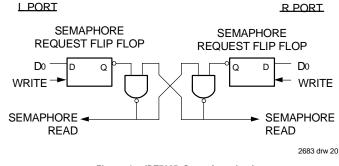
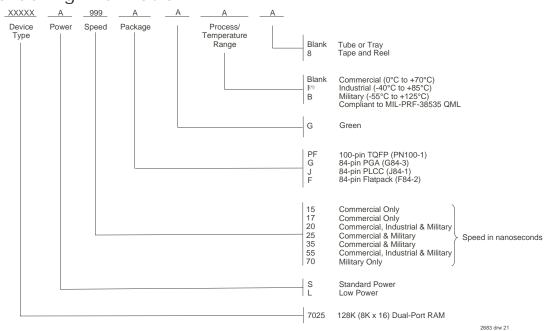


Figure 4. IDT7025 Semaphore Logic

# Ordering Information



### NOTES:

 Industrial range is available on selected PLCC packages in standard power. For other speeds, packages and powers contact your sales office. LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

# Datasheet Document History

01/13/99:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Pages 2 and 3 Added additional notes to pin configurations
05/19/99:	Page 11 Fixed typographical error
06/03/99:	Changed drawing format
	Page 1 Corrected DSC number
04/04/00:	Replaced IDT logo
	Page 7 Fixed typo in Data Retention chart
	Changed ±500mV to 0mV in notes
05/22/00:	Page 5 Increased storage temperature parameter
	Clarified TA parameter
	Page 6 DC Electrical parameters-changed wording from "open" to "disabled"
09/13/01:	Page 2 & 3 Added date revision for pin configurations
	Page 6 Added Industrial temp to the column heading for 20ns to DC Electrical Characteristics
	Pages 8,10,13&15 Added Industrial temp to the column headings for 20ns to AC Electrical Characteristics
	Pages 5,6,8,10,13&15 Removed Industrial temp footnote from all tables
	Page 21 Added Industrial temp to 20ns in ordering information
10/21/08:	Page 22 Removed "IDT" from orderable part number
07/17/12:	Page 22 Added T&R and green indicators to ordering information
03/07/18:	Product Discontinuation Notice - PDN# SP-17-02
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