ANALOG DEVICES

750 MHz, 16 × 8 Analog Crosspoint Switch

Data Sheet

ADV3224/ADV3225

FEATURES

- **16 × 8 high speed, nonblocking switch array**
- **Pinout and functionally equivalent to the AD8110/AD8111**
- **Drop-in compatible with the ADV3228/ADV3229 8 × 8 array**
- **Complete solution**
  - **Buffered inputs**
  - **Programmable high impedance outputs**
  - **8 output amplifiers, G = +1 (ADV3224), G = +2 (ADV3225)**
  - **Drives 150 Ω loads**
- **Operates on ±5 V supplies**
- **Low power: 0.5 W**
- **Excellent ac performance**
  - **−3 dB bandwidth**
    - **200 mV p-p: 1200 MHz (ADV3224), 900 MHz (ADV3225)**
    - **2 V p-p: 750 MHz (ADV3224), 850 MHz (ADV3225)**
  - **0.5 dB flatness (2 V p-p)**
    - **250 MHz (ADV3224), 235 MHz (ADV3225)**
  - **Slew rate: 2500 V/µs**
- **Serial or parallel programming of switch array**
- **72-lead LFCSP (10 mm × 10 mm)**

APPLICATIONS

- **Routing of high speed signals including**
  - **Video (NTSC, PAL, S, SECAM, YUV, RGB)**
  - **Compressed video (MPEG, wavelet)**
  - **3-level digital video (HDB3)**
- **Data communications**
- **Telecommunications**

FUNCTIONAL BLOCK DIAGRAM

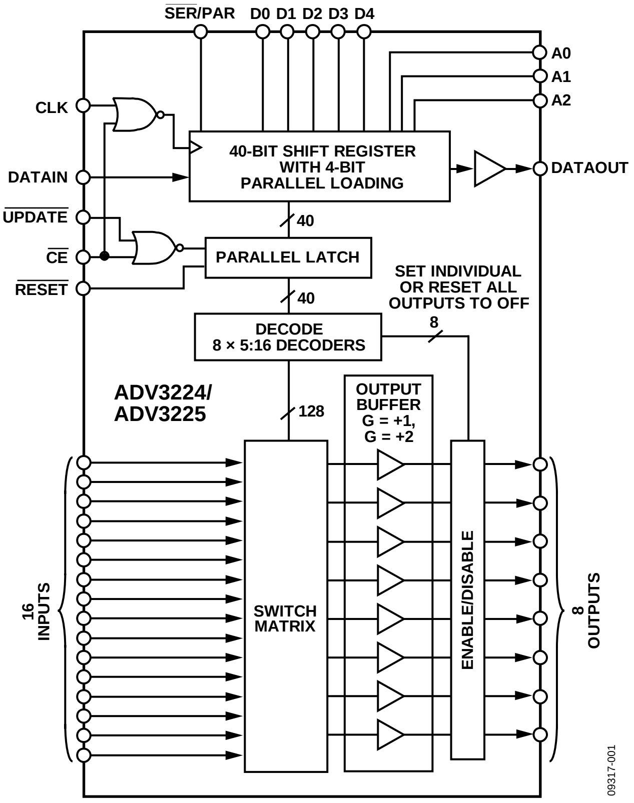

Figure 1.

GENERAL DESCRIPTION

The ADV3224/ADV3225 are high speed 16 × 8 analog crosspoint switch matrices. They offer a −3 dB signal bandwidth of greater than 750 MHz and a high slew rate of greater than 2500 V/µs.

The ADV3224/ADV3225 include eight independent output buffers that can be placed into a high impedance state for paralleling crosspoint outputs to prevent off channels from loading the output bus. The ADV3224 has a gain of +1 and the ADV3225 has a gain of +2, and they both operate on voltage supplies of ±5 V. Channel switching is performed via a serial digital control that can accommodate the daisy chaining of several devices or via a parallel control to allow updating of an individual output without reprogramming the entire array.

The ADV3224/ADV3225 are available in the 72-lead LFCSP package over the extended industrial temperature range of −40°C to +85°C.

Rev. B **Document Feedback**

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11/10—Revision 0: Initial Version

SPECIFICATIONS

$V_S = \pm 5$ V, $T_A = 25°C$, $R_L = 150\ \Omega$, unless otherwise noted.

Table 1.

			ADV3224			ADV3225		
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	200 mV p-p		1200			900		MHz
	2 V p-p		750			850		MHz
Gain Flatness	0.1 dB, 2 V p-p		55			50		MHz
	0.5 dB, 2 V p-p		250			235		MHz
Propagation Delay	2 V p-p		0.6			0.6		ns
Settling Time	1%, 2 V step		3			3		ns
Slew Rate	2 V step, peak		2500			2500		V/µs
NOISE/DISTORTION PERFORMANCE								
Differential Gain Error	NTSC or PAL		0.01			0.02		%
Differential Phase Error	NTSC or PAL		0.01			0.02		Degrees
Crosstalk, All Hostile, RTO	f = 100 MHz		−45			−45		dB
	f = 5 MHz		−87			−70		dB
Off Isolation, Input to Output	f = 100 MHz, one channel		−80			−87		dB
OIP2	f = 100 MHz, $R_L = 100\ \Omega$					38		dBm
	f = 500 MHz, $R_L = 100\ \Omega$					15		dBm
OIP3	f = 100 MHz, $R_L = 100\ \Omega$					32		dBm
	f = 500 MHz, $R_L = 100\ \Omega$					7		dBm
Output 1 dB Compression Point	f = 100 MHz, $R_L = 100\ \Omega$					19		dBm
	f = 500 MHz, $R_L = 100\ \Omega$					10		dBm
Input Voltage Noise Density	50 MHz		18			18		nV/√Hz
DC PERFORMANCE								
Gain Error			0.1	0.5		0.2	1.5	%
Gain Matching	Channel-to-channel			0.5			1.5	%
Gain Temperature Coefficient			0.5			5		ppm/°C
OUTPUT CHARACTERISTICS								
Output Resistance	DC, enabled		0.2			0.2		Ω
	DC, disabled		15			8		MΩ
Output Disabled Capacitance			2.2			2.6		pF
Output Leakage Current	Output disabled		0.5			0.5		µA
Output Voltage Range	No load		±3			±3		V
	$R_L = 150\ \Omega$		±2.8			±2.8		V
Short-Circuit Current			55			55		mA
INPUT CHARACTERISTICS								
Input Offset Voltage	Worst case (all configurations)		±5			±5		mV
Input Offset Voltage Drift			5			5		µV/°C
Input Voltage Range			±3			±1.5		V
Input Capacitance	Any switch configuration		1.8			1.8		pF
Input Resistance			2			2		MΩ
Input Bias Current	Any switch configuration		±1			±1		µA
SWITCHING CHARACTERISTICS								
Enable/Disable Time	50% $\overline{\text{UPDATE}}$ to 1% settling		20			20		ns
Switching Time, 2 V Step	50% $\overline{\text{UPDATE}}$ to 1% settling		20			20		ns
Switching Transient (Glitch)			25			50		mV p-p

Parameter	Test Conditions/Comments	ADV3224			ADV3225			Unit
		Min	Typ	Max	Min	Typ	Max	
POWER SUPPLIES								
Supply Current	AVCC, outputs enabled, no load		52	70		58	70	mA
	AVCC, outputs disabled		12	18		13	18	mA
	AVEE, outputs enabled, no load		52	70		58	70	mA
	AVEE, outputs disabled		12	18		14	18	mA
	DVCC, outputs enabled, no load		6			6		mA
Supply Voltage Range		±4.5	±5	±5.5	±4.5	±5	±5.5	V
PSRR	DC to 50 kHz, AVCC, AVEE		<−60			<−60		dB
	f = 100 kHz, AVCC, AVEE		−60			−60		dB
	f = 10 MHz, AVCC		−48			−35		dB
	f = 10 MHz, AVEE		−35			−55		dB
	f = 100 MHz, AVCC		−25			−15		dB
	f = 100 MHz, AVEE		−15			−15		dB
	f = 100 kHz, DVCC		−90			−90		dB
OPERATING TEMPERATURE RANGE								
Temperature Range	Operating (still air)	−40		+85	−40		+85	°C
θ_{JA}	Operating (still air)		29			29		°C/W

TIMING CHARACTERISTICS (SERIAL)

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Data Setup Time	t_1	10			ns
CLK Pulse Width	t_2	10			ns
Serial Data Hold Time	t_3	10			ns
CLK Pulse Separation, Serial Mode	t_4	10			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	10			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	10			ns
CLK to DATAOUT Valid, Serial Mode	t_7			50	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off			20		ns
Data Load Time, CLK = 5 MHz, Serial Mode			8		μs
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times				50	ns
$\overline{\text{RESET}}$ Time			30		ns

Timing Diagram—Serial Mode

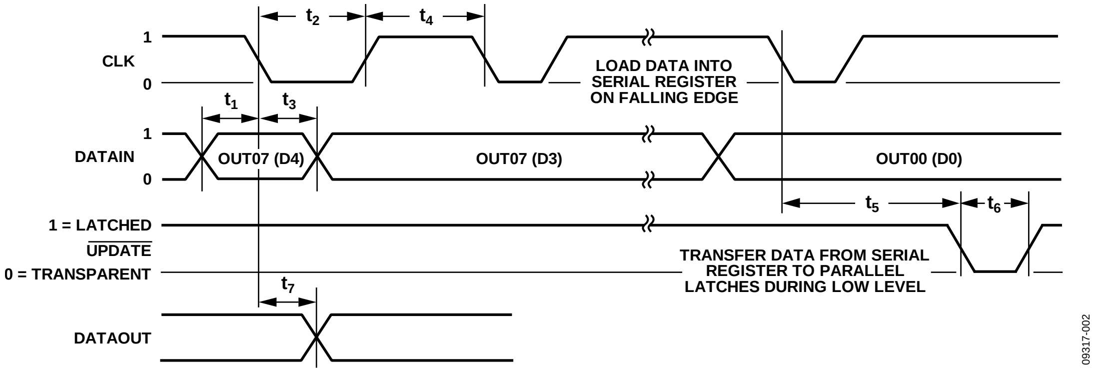


Figure 2. Timing Diagram, Serial Mode

LOGIC LEVELS

Table 3. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, DATAIN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, DATAIN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATAOUT	DATAOUT	$\overline{\text{SER}}$/PAR, CLK, DATAIN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{SER}}$/PAR, CLK, DATAIN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	DATAOUT	DATAOUT
2.0 V min	0.8 V max	2.4 V min	0.4 V max	2 μA max	2 μA max	2 μA max	300 μA max	3 mA min	1 mA min

TIMING CHARACTERISTICS (PARALLEL)

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Parallel Data Setup Time	t_{1d}	10			ns
Address Setup Time	t_{1a}	10			ns
CLK Pulse Width	t_2	10			ns
Parallel Data Hold Time	t_{3d}	10			ns
Address Hold Time	t_{3a}	10			ns
CLK Pulse Separation	t_4	20			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_5	10			ns
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times				50	ns
$\overline{\text{RESET}}$ Time			30		ns

Timing Diagram—Parallel Mode

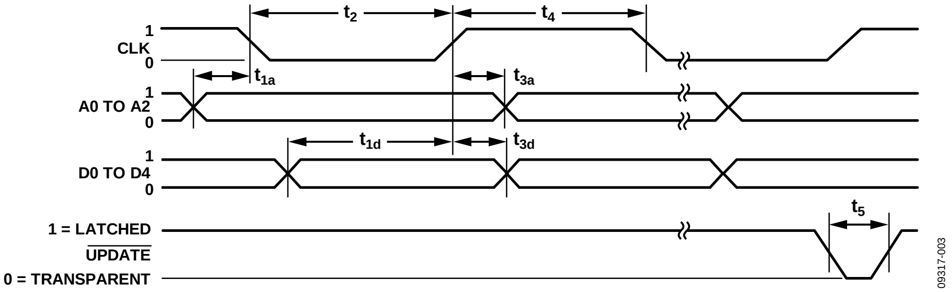


Figure 3. Timing Diagram, Parallel Mode

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Supply Voltage (AVCC to AVEE)	11 V
Digital Supply Voltage (DVCC to DGND)	6 V
Supply Potential Difference (AVCC – DVCC)	±0.5 V
Ground Potential Difference (AGND – DGND)	±0.5 V
Maximum Potential Difference (DVCC – AVEE)	11 V
Analog Input Voltage	AVEE < V_{IN} < AVCC
Digital Input Voltage	DGND < D_{IN} < DVCC
Exposed Paddle Voltage	AGND
Output Voltage (Disabled Analog Output)	AVEE < V_{OUT} < AVCC
Output Short-Circuit	
Duration	Momentary
Current	Internally limited to 55 mA
Temperature	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
72-Lead LFCSP_VQ	29	0.5	°C/W

POWER DISSIPATION

The ADV3224/ADV3225 operate with ±5 V supplies and can drive loads down to 100 Ω, resulting in a wide range of possible power dissipations. For this reason, extra care must be taken when derating the operating conditions based on ambient temperature.

Packaged in the 72-lead LFCSP, the ADV3224/ADV3225 junction-to-ambient thermal impedance (θ_{JA}) is 29°C/W. For long-term reliability, the maximum allowed junction temperature of the die should not exceed 125°C; even temporarily exceeding this limit can cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Exceeding a junction temperature of 150°C for an extended period can result in device failure. In Figure 4, the curve shows the range of allowed internal die power dissipation that meets these conditions over the −40°C to +85°C ambient temperature range. When using Figure 4, do not include the external load power in the maximum power calculation, but do include the load current dropped on the die output transistors.

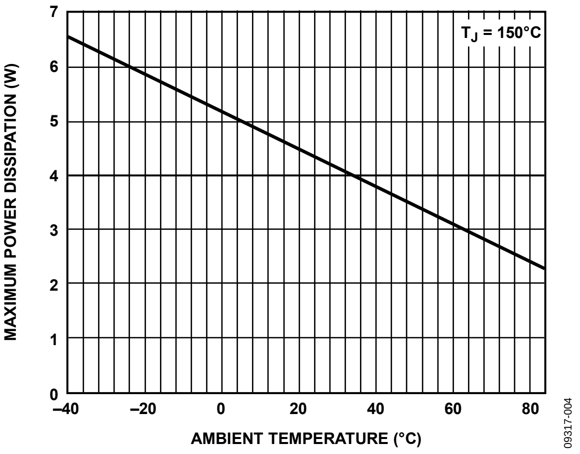
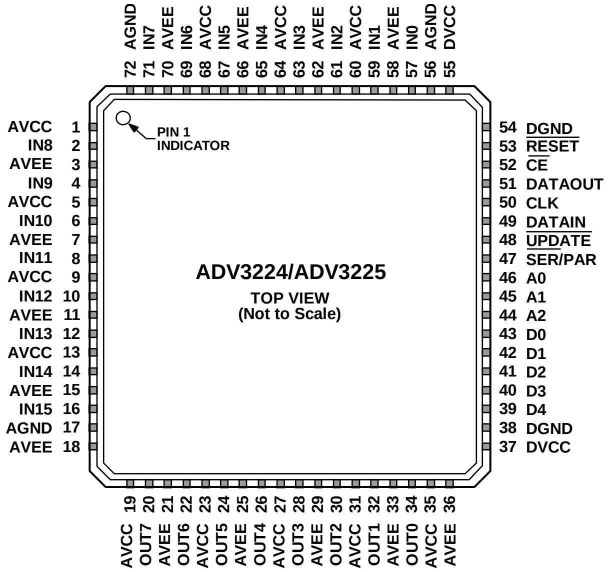


Figure 4. Maximum Die Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PADDLE. THE EXPOSED METAL PADDLE ON THE BOTTOM OF THE LFCSP PACKAGE MUST BE SOLDERED TO THE PCB AGND FOR PROPER HEAT DISSIPATION AND FOR NOISE AND MECHANICAL STRENGTH BENEFITS.

09317-005

Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 9, 13, 19, 23, 27, 31, 35, 60, 64, 68	AVCC	Analog Positive Supply.
2	IN8	Input Number 8.
3, 7, 11, 15, 18, 21, 25, 29, 33, 36, 58, 62, 66, 70	AVEE	Analog Negative Supply.
4	IN9	Input Number 9.
6	IN10	Input Number 10.
8	IN11	Input Number 11.
10	IN12	Input Number 12.
12	IN13	Input Number 13.
14	IN14	Input Number 14.
16	IN15	Input Number 15.
17, 56, 72	AGND	Analog Ground.
20	OUT7	Output Number 7.
22	OUT6	Output Number 6.
24	OUT5	Output Number 5.
26	OUT4	Output Number 4.
28	OUT3	Output Number 3.
30	OUT2	Output Number 2.
32	OUT1	Output Number 1.
34	OUT0	Output Number 0.
37, 55	DVCC	Digital Positive Supply.
38, 54	DGND	Digital Ground.
39	D4	Parallel Data Input, Output Enable.
40 to 43	D3 to D0	Parallel Data Input.
44 to 46	A2 to A0	Parallel Output Address Input.

Pin No.	Mnemonic	Description
47	$\overline{\text{SER}}$/PAR	Serial/Parallel Mode Select (Control Pin).
48	$\overline{\text{UPDATE}}$	Second Rank Write Strobe (Control Pin).
49	DATAIN	Serial Data In (Control Pin).
50	CLK	Serial Data Clock, Parallel First Rank Latch Enable (Control Pin).
51	DATAOUT	Serial Data Out.
52	$\overline{\text{CE}}$	Chip Enable (Control Pin).
53	$\overline{\text{RESET}}$	Second Rank Reset (Control Pin).
57	IN0	Input Number 0.
59	IN1	Input Number 1.
61	IN2	Input Number 2.
63	IN3	Input Number 3.
65	IN4	Input Number 4.
67	IN5	Input Number 5.
69	IN6	Input Number 6.
71	IN7	Input Number 7.
	EPAD	Exposed Paddle. The exposed metal paddle on the bottom of the LFCSP package must be soldered to the PCB AGND for proper heat dissipation and for noise and mechanical strength benefits.

TRUTH TABLE AND LOGIC DIAGRAM

Table 8. Operation Truth Table[1]

$\overline{\text{CE}}$	$\overline{\text{UPDATE}}$	CLK	DATAIN	DATAOUT	$\overline{\text{RESET}}$	$\overline{\text{SER}}$/PAR	Description
1	X	X	X	X	X	X	No change in logic.
0	X	↓	Data_{I}[2]	Data_{I-80}	X	0	The data on the serial DATAIN line is loaded into the serial register. The first bit clocked into the serial register appears at DATAOUT 40 clock cycles later.
0	X	0	D0…D4	Not applicable in parallel mode[3]	X	1	The data on the parallel data lines, D0 to D4, are loaded into the 40-bit serial shift register location addressed at A0 to A2.
0	0	X	X	X	1	X	Data in the 40-bit shift register transfers into the parallel latches that control the switch array. Latches are transparent.
X	X	X	X	X	0	X	Asynchronous operation. All outputs are disabled. Second rank latches are cleared. Remainder of logic is unchanged.

[1] X is don't care.
[2] Data_{I}: serial data.
[3] DATAOUT remains active in parallel mode and always reflects the state of the MSB of the serial shift register.

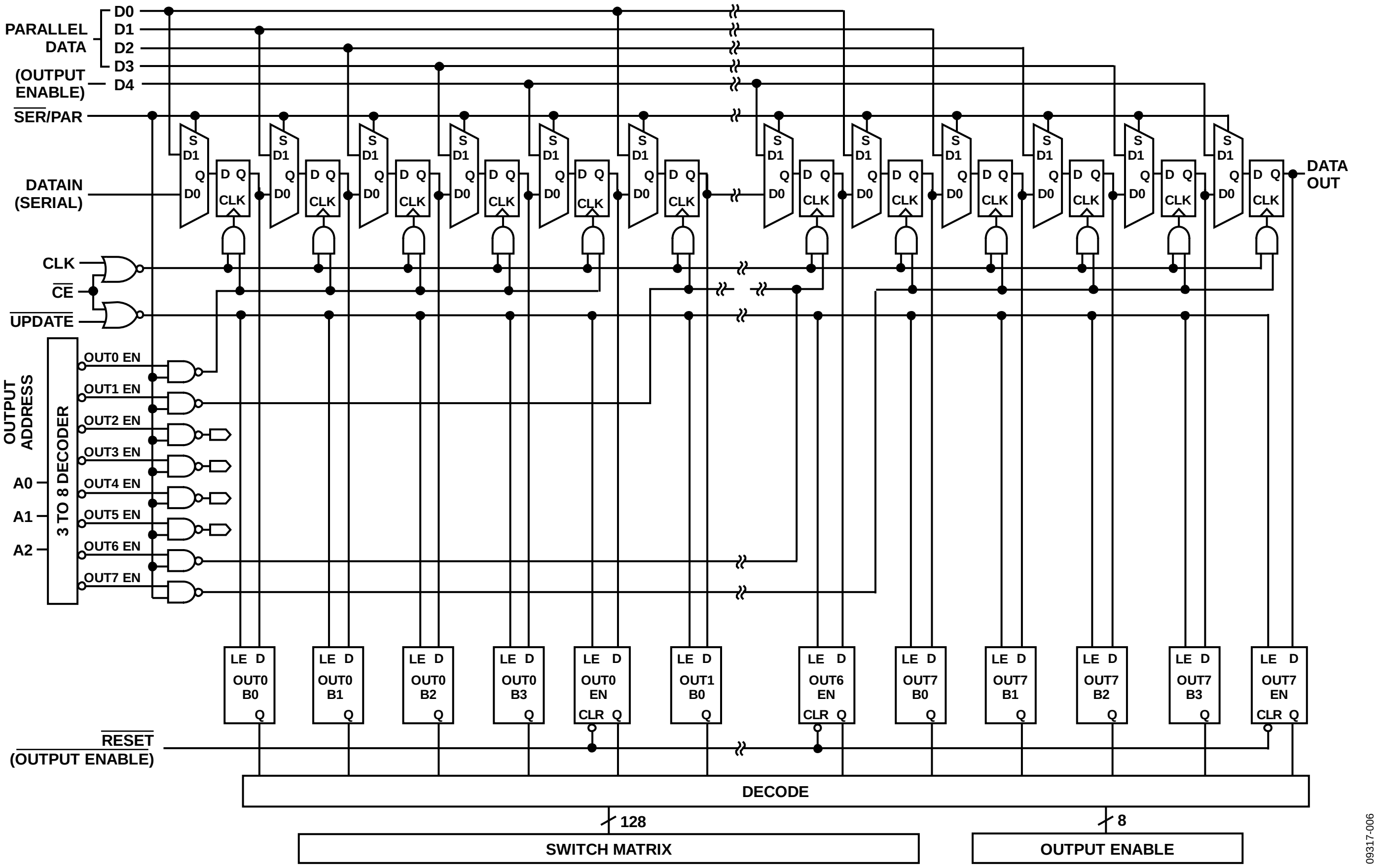


Figure 6. Logic Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm5$ V, $T_A = 25°C$, $R_L = 150\ \Omega$, unless otherwise noted. T_{MIN} to $T_{MAX} = -40°C$ to $+85°C$.

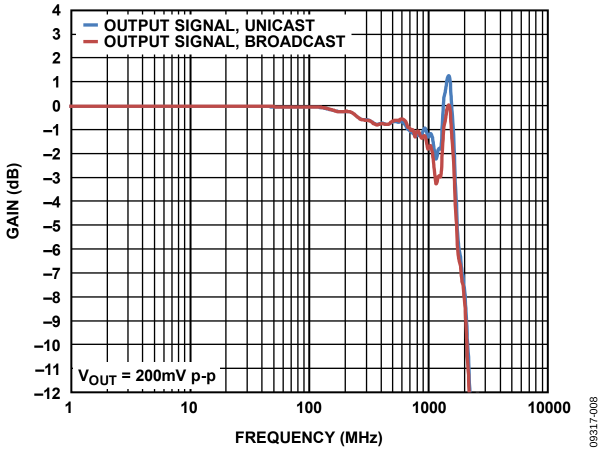


Figure 7. ADV3224 Small Signal Frequency Response

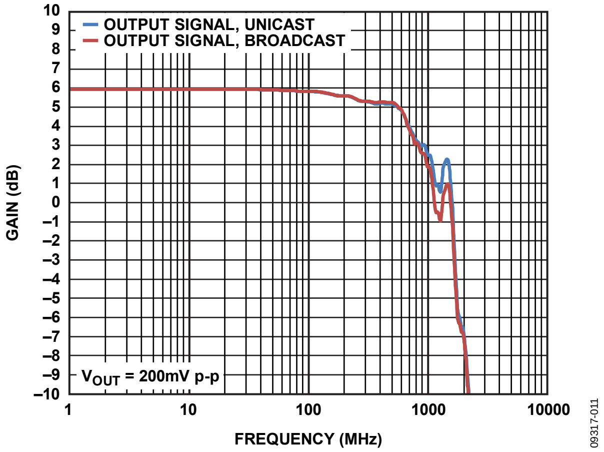


Figure 10. ADV3225 Small Signal Frequency Response

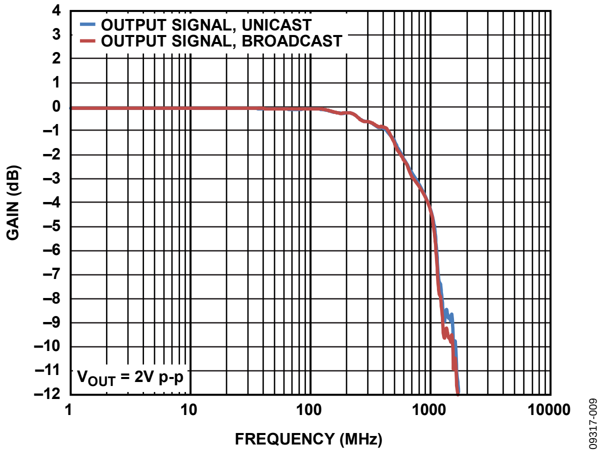


Figure 8. ADV3224 Large Signal Frequency Response

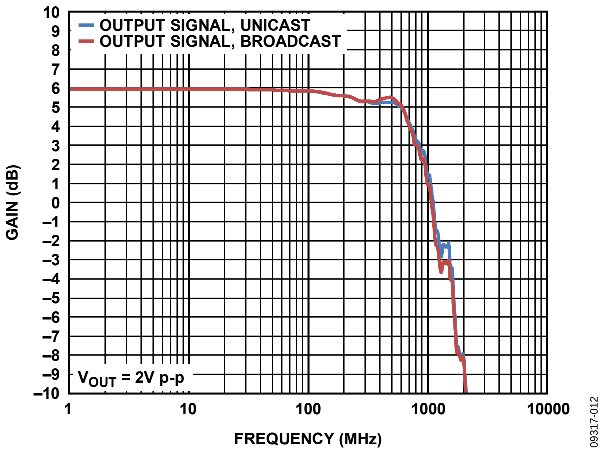


Figure 11. ADV3225 Large Signal Frequency Response

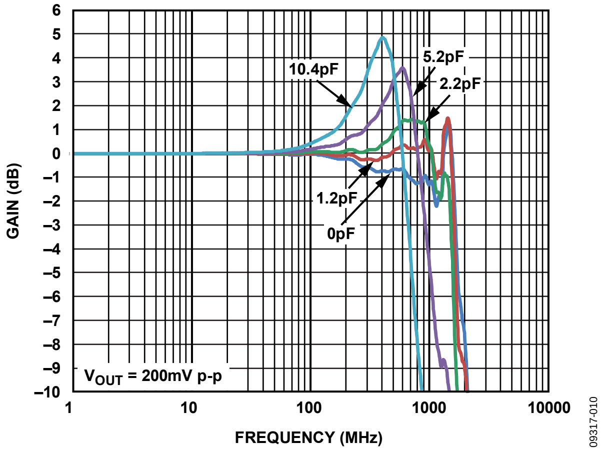


Figure 9. ADV3224 Small Signal Frequency Response with Capacitive Loads

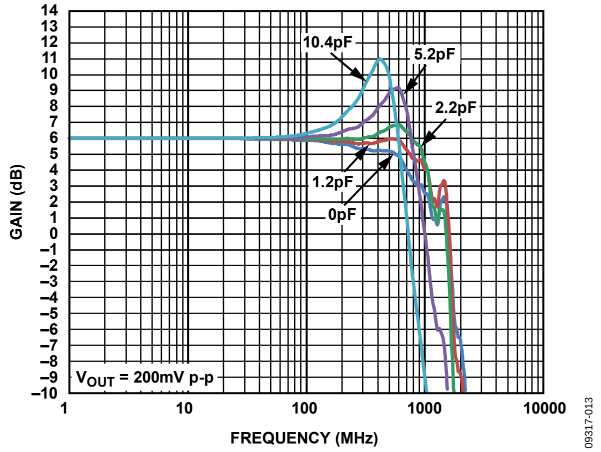


Figure 12. ADV3225 Small Signal Frequency Response with Capacitive Loads

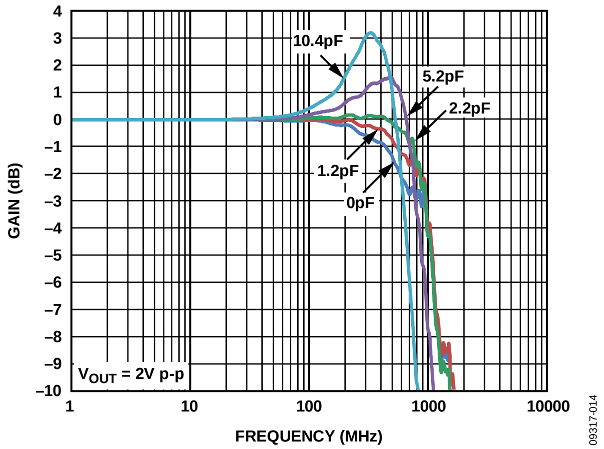


Figure 13. ADV3224 Large Signal Frequency Response with Capacitive Loads

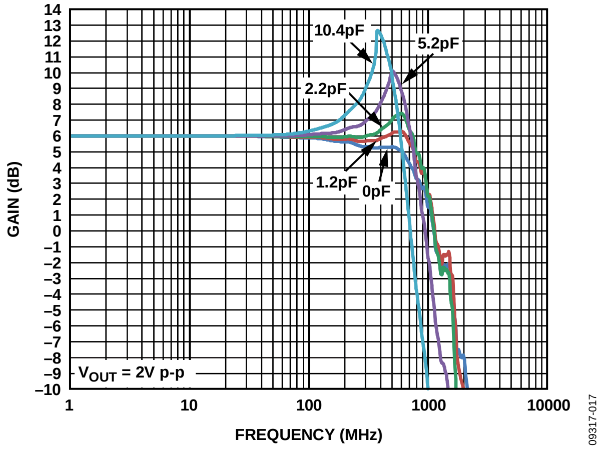


Figure 16. ADV3225 Large Signal Frequency Response with Capacitive Loads

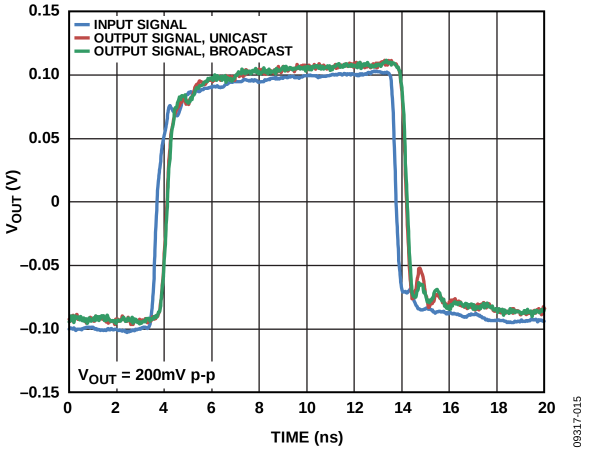


Figure 14. ADV3224 Small Signal Pulse Response

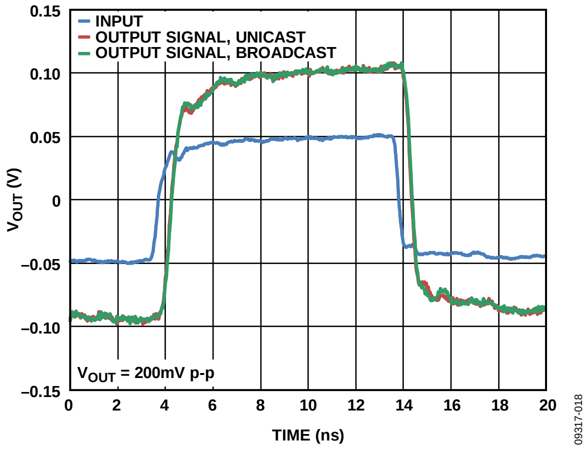


Figure 17. ADV3225 Small Signal Pulse Response

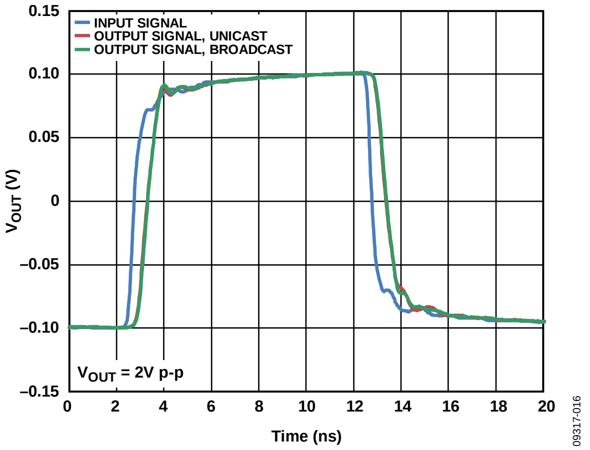


Figure 15. ADV3224 Large Signal Pulse Response

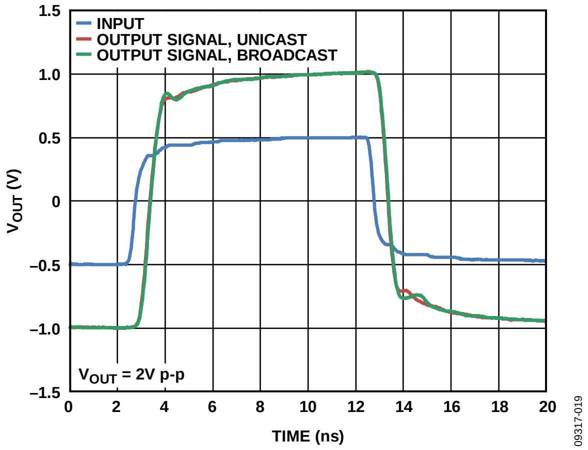


Figure 18. ADV3225 Large Signal Pulse Response

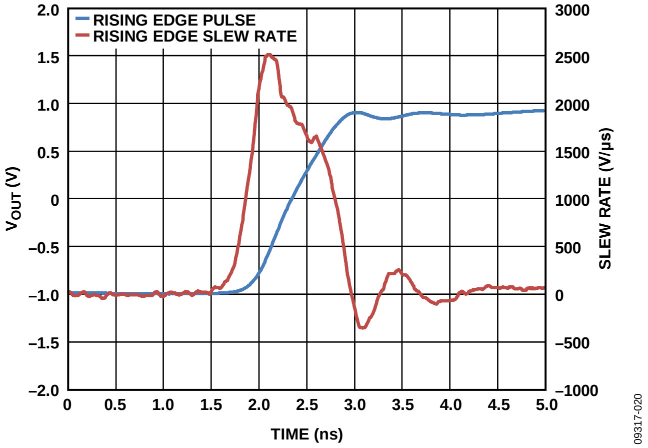


Figure 19. ADV3224 Rising Edge Slew Rate

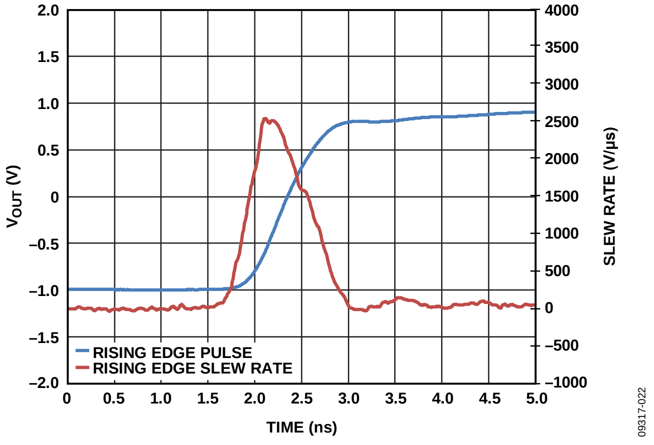


Figure 22. ADV3225 Rising Edge Slew Rate

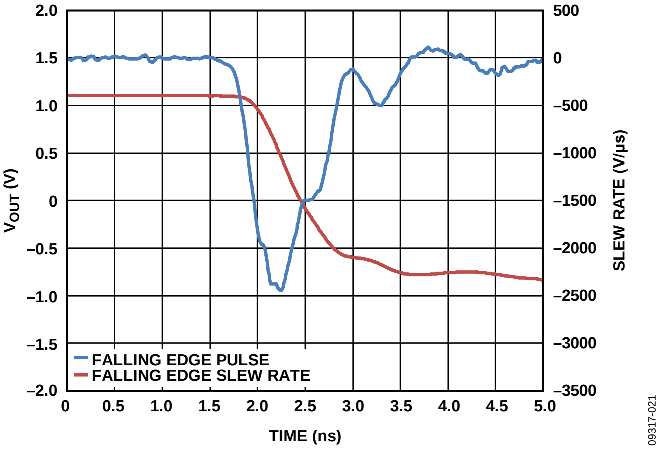


Figure 20. ADV3224 Falling Edge Slew Rate

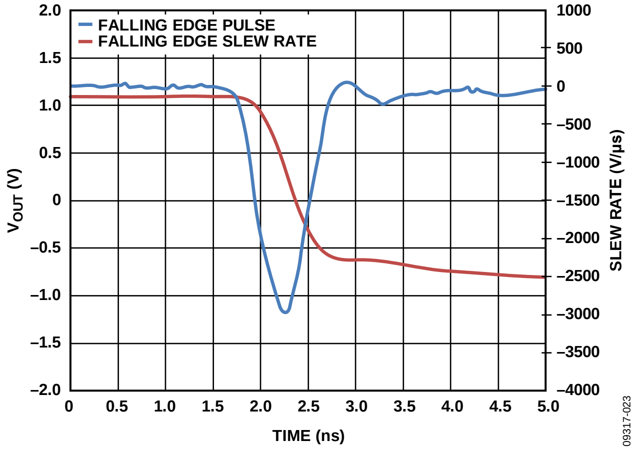


Figure 23. ADV3225 Falling Edge Slew Rate

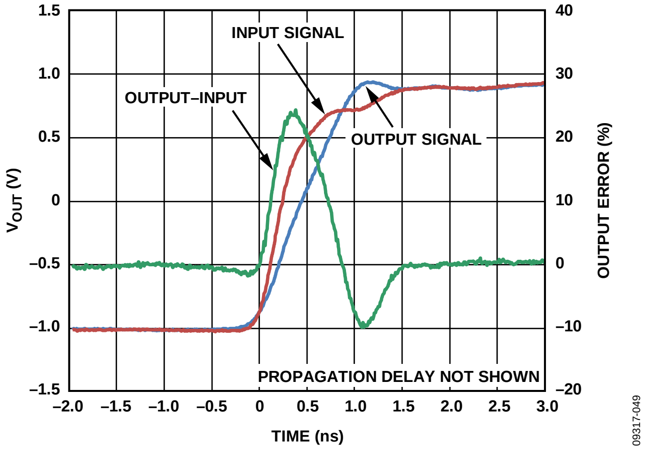


Figure 21. ADV3224 Settling Time

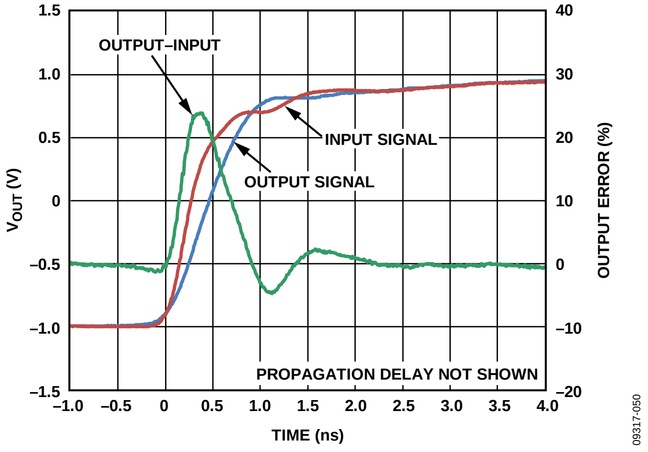


Figure 24. ADV3225 Settling Time

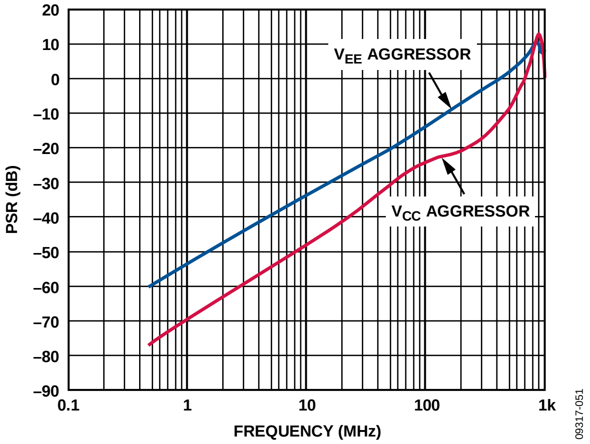


Figure 25. ADV3224 Power Supply Rejection

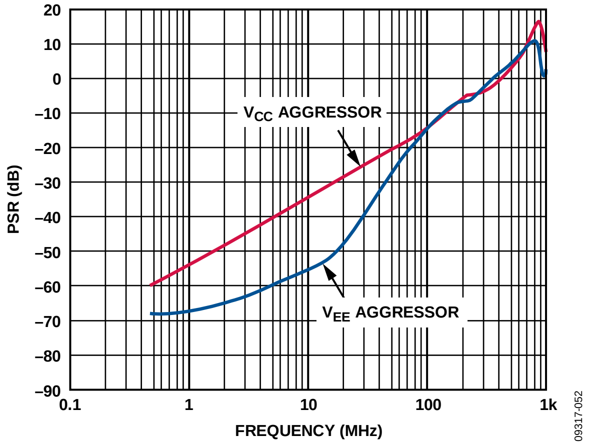


Figure 28. ADV3225 Power Supply Rejection

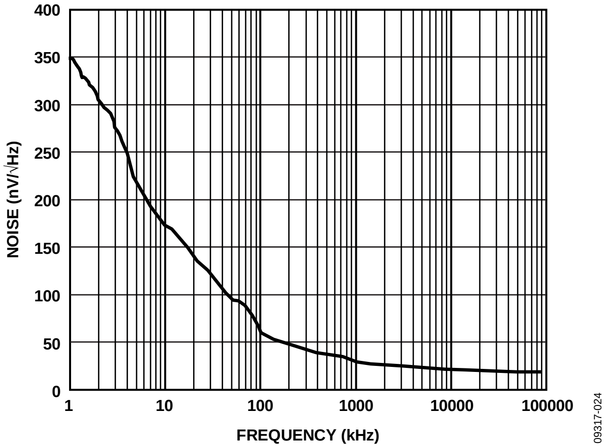


Figure 26. ADV3224 Output Noise Density, 100 Ω Load

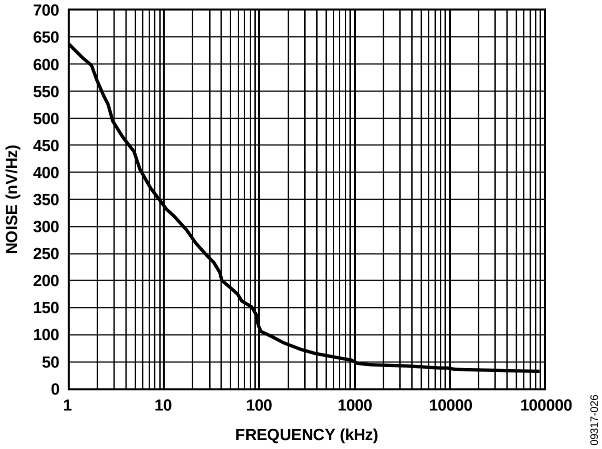


Figure 29. ADV3225 Output Noise Density, 100 Ω Load

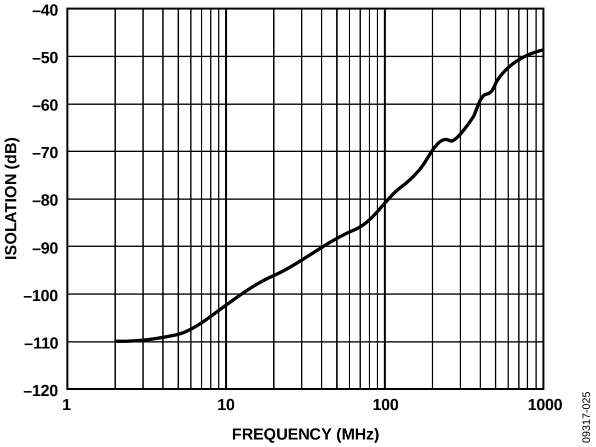


Figure 27. ADV3224 Off Isolation

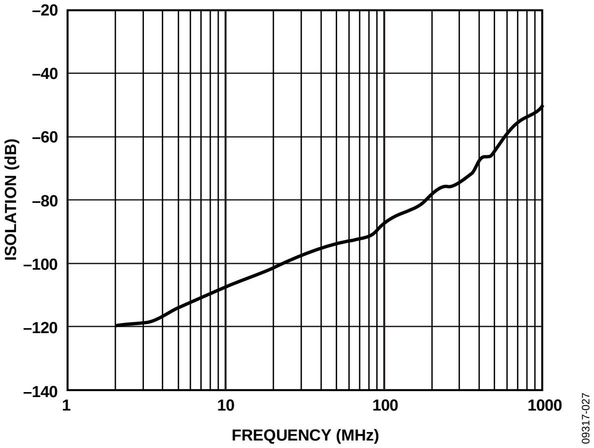


Figure 30. ADV3225 Off Isolation

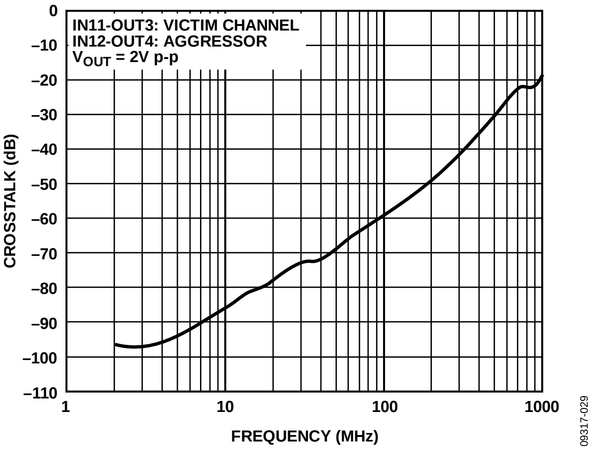


Figure 31. ADV3224 Crosstalk, One Adjacent Channel, RTO

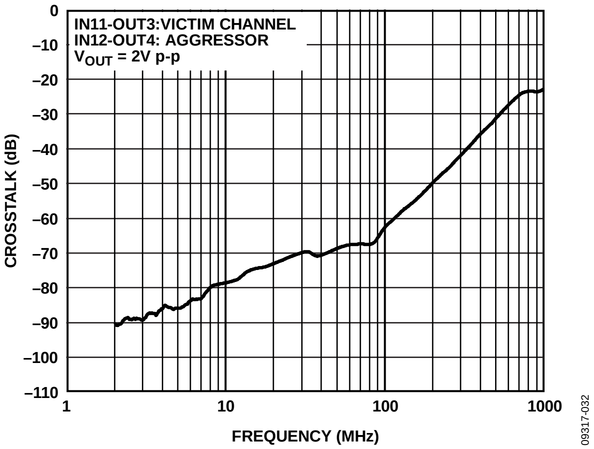


Figure 34. ADV3225 Crosstalk, One Adjacent Channel, RTO

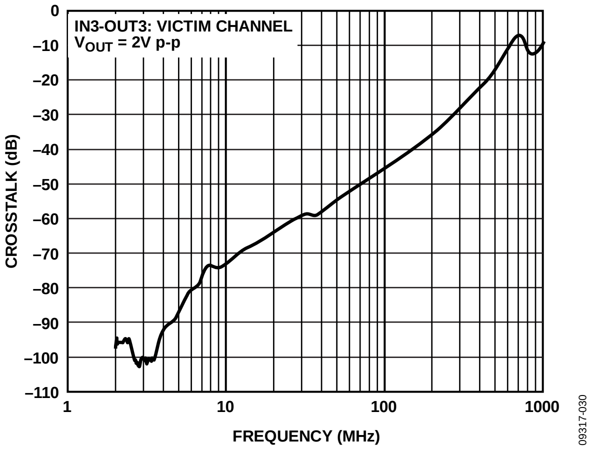


Figure 32. ADV3224 Crosstalk, All Hostile, RTO

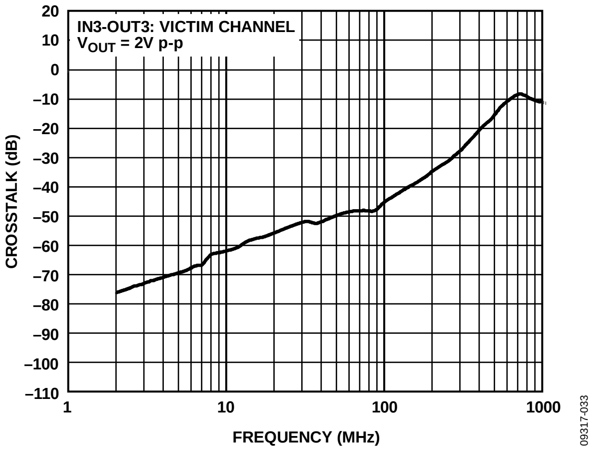


Figure 35. ADV3225 Crosstalk, All Hostile, RTO

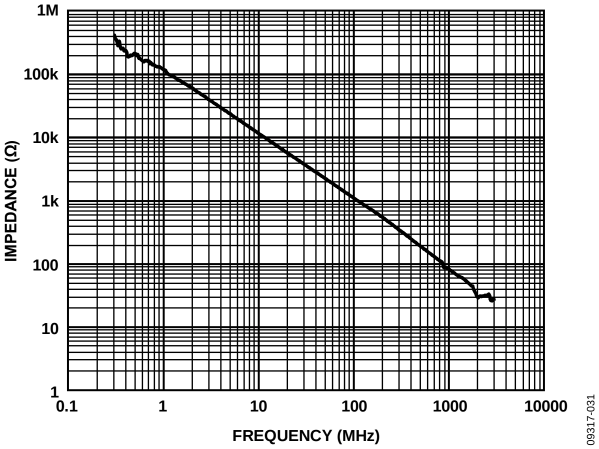


Figure 33. ADV3224 Input Impedance

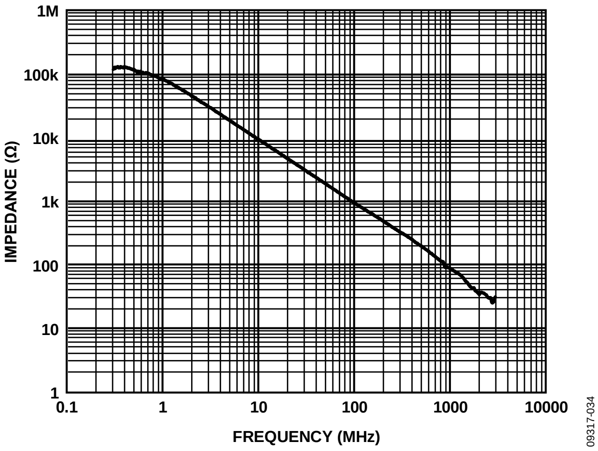


Figure 36. ADV3225 Input Impedance

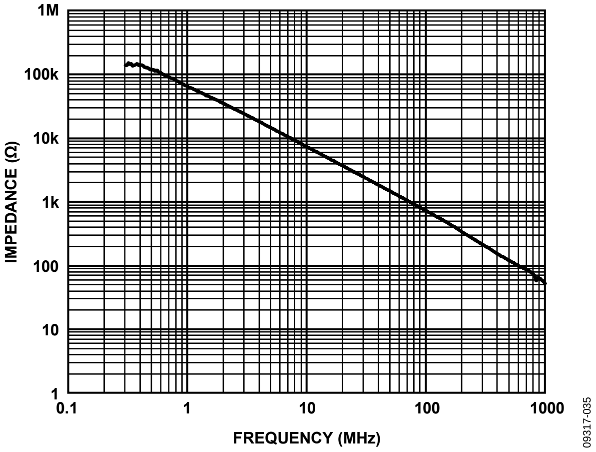


Figure 37. ADV3224 Output Impedance, Disabled

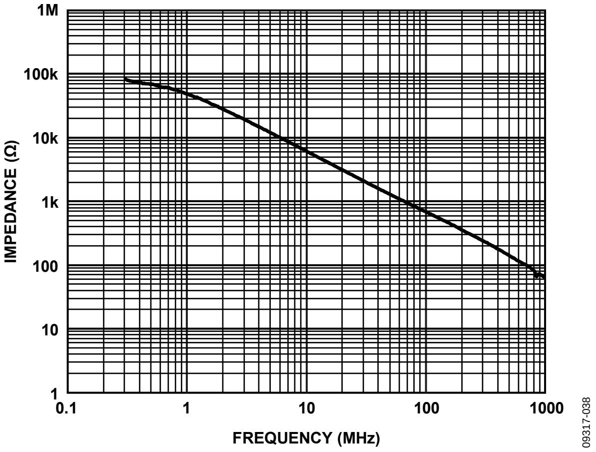


Figure 40. ADV3225 Output Impedance, Disabled

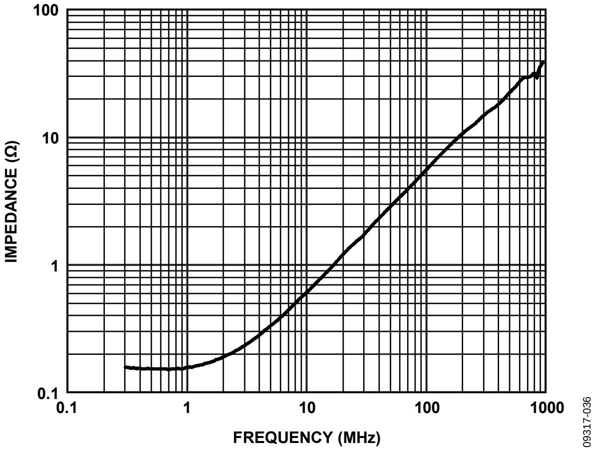


Figure 38. ADV3224 Output Impedance, Enabled

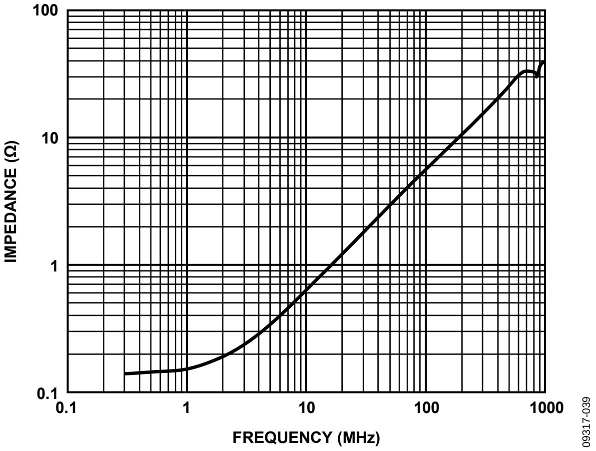


Figure 41. ADV3225 Output Impedance, Enabled

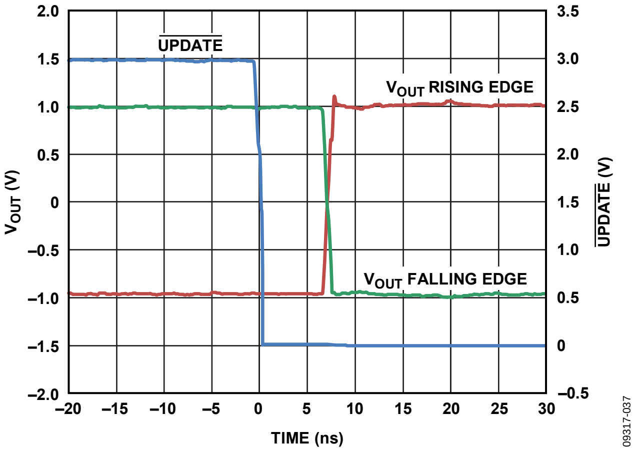


Figure 39. ADV3224 Switching Time

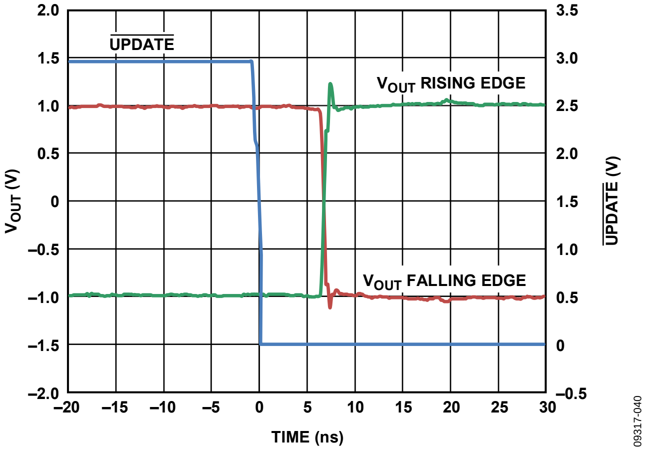


Figure 42. ADV3225 Switching Time

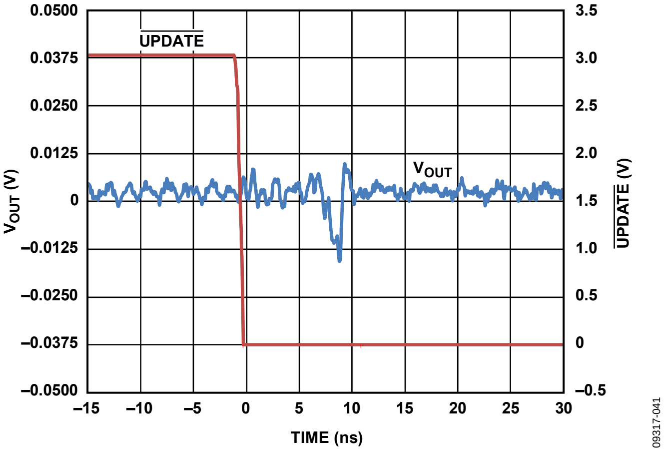


Figure 43. ADV3224 Switching Glitch

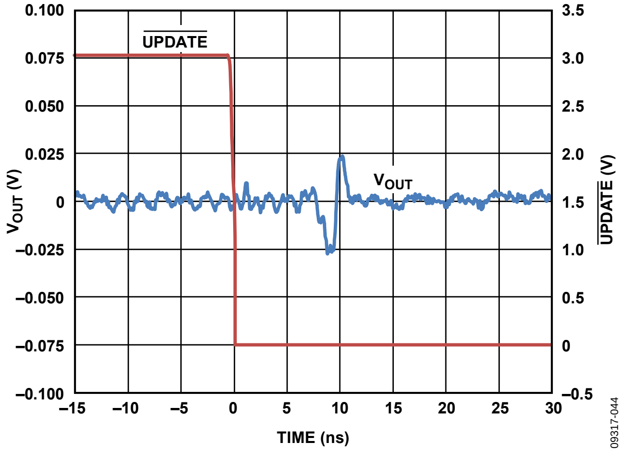


Figure 46. ADV3225 Switching Glitch

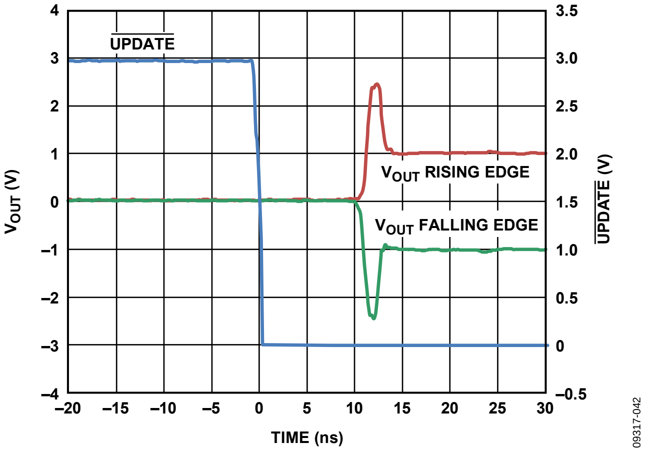


Figure 44. ADV3224 Enable Time

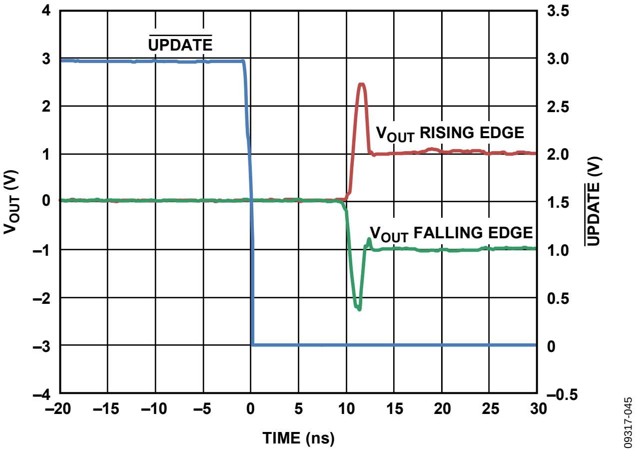


Figure 47. ADV3225 Enable Time

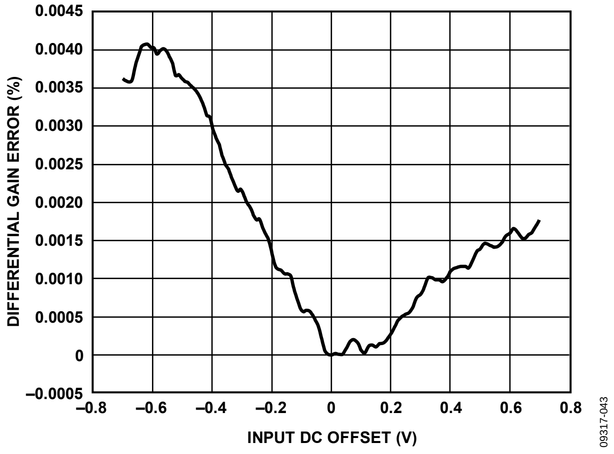


Figure 45. ADV3224 Differential Gain Error

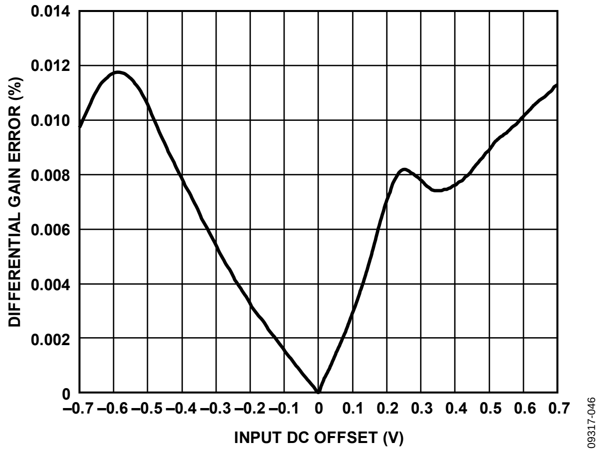


Figure 48. ADV3225 Differential Gain Error

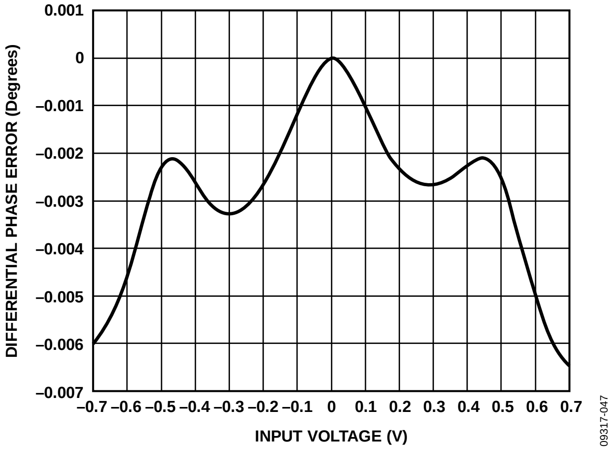


Figure 49. ADV3224 Differential Phase Error

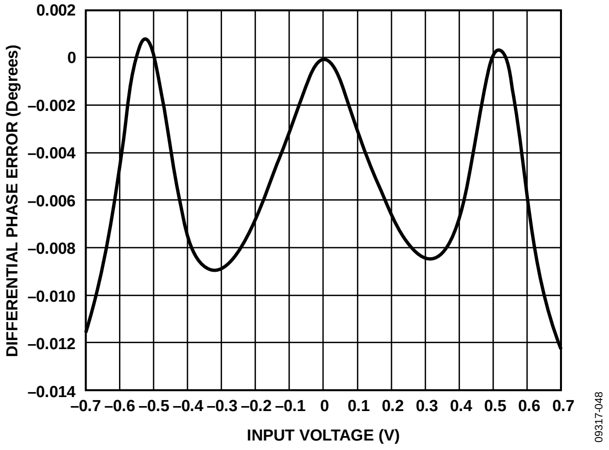


Figure 52. ADV3225 Differential Phase Error

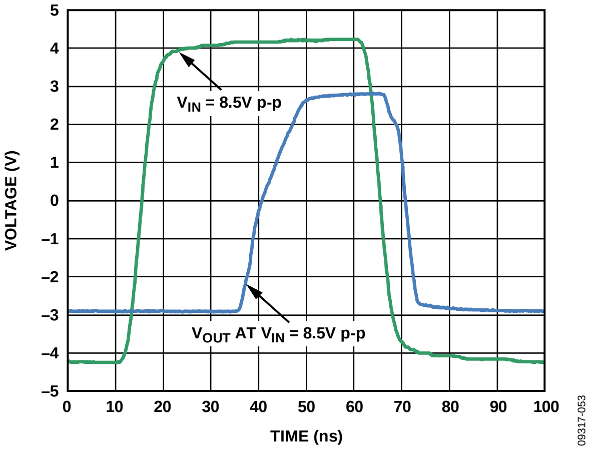


Figure 50. ADV3224 Overdrive Recovery

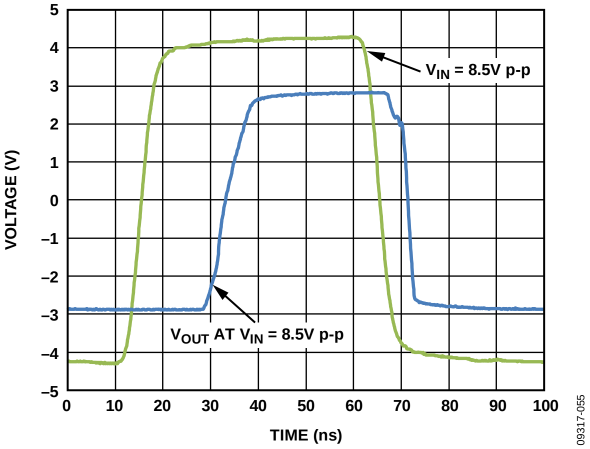


Figure 53. ADV3225 Overdrive Recovery

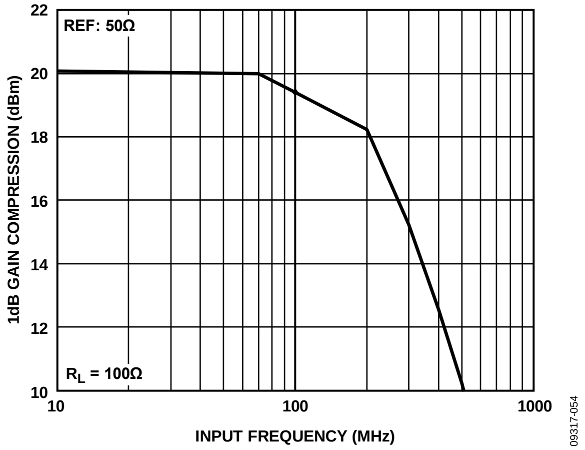


Figure 51. ADV3225 1 dB Gain Compression, 100 Ω Load

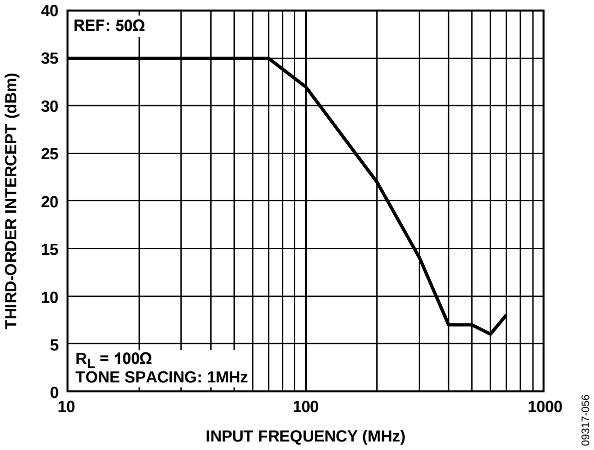


Figure 54. ADV3225 Output Third-Order Intercept, 100 Ω Load

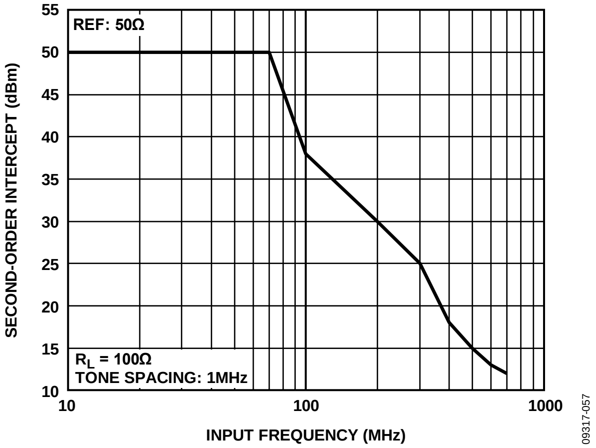


Figure 55. ADV3225 Output Second-Order Intercept, 100 Ω Load

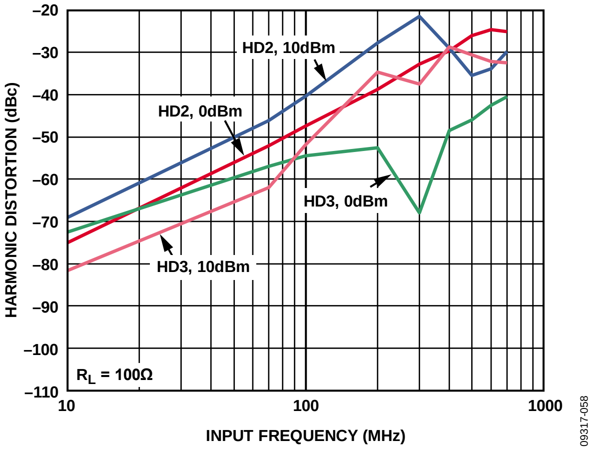


Figure 57. ADV3225 Harmonic Distortion, 100 Ω Load

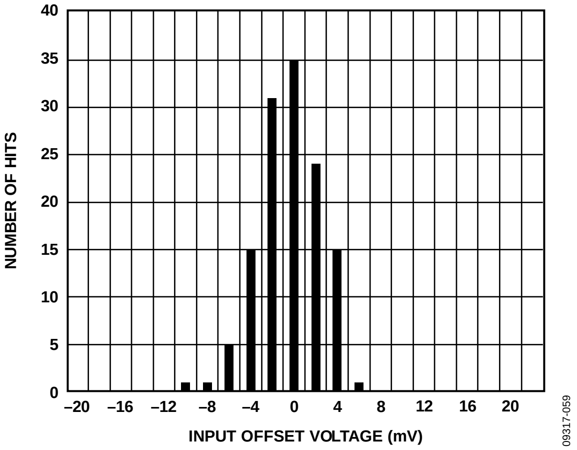


Figure 56. ADV3224 and ADV3225, Input V_{OS} Distribution

CIRCUIT DIAGRAMS

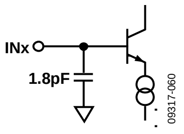


Figure 58. Analog Input

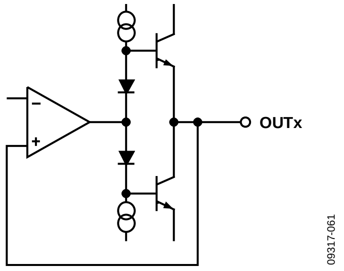


Figure 59. Analog Output Enabled

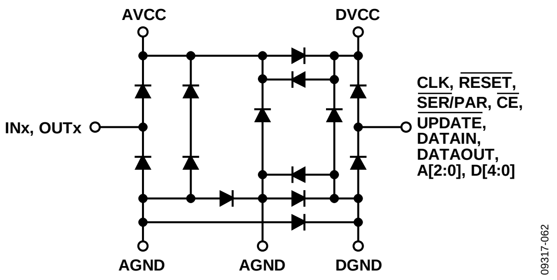


Figure 60. ESD Map

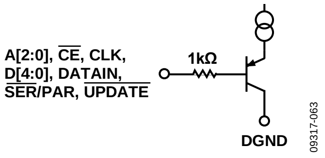


Figure 61. Logic Input

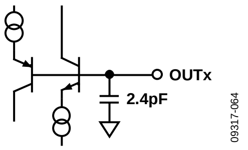


Figure 62. Analog Output Disabled

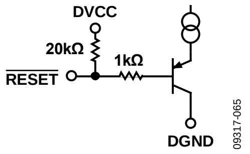


Figure 63. Reset Input

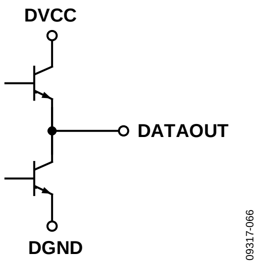


Figure 64. Logic Output

THEORY OF OPERATION

The ADV3224 (G = +1) and ADV3225 (G = +2) are crosspoint arrays with eight outputs, each of which can be connected to any one of 16 inputs. Organized by output row, 16 switchable input transconductance stages are connected to each output buffer to form 16-to-1 multiplexers. There are eight of these multiplexers, each with its inputs wired in parallel, for a total array of 128 transconductance stages forming a multicast-capable crosspoint switch. Each input is buffered and is not loaded by the outputs, simplifying the construction of larger arrays using the ADV3224 or ADV3225 as a building block.

Decoding logic for each output selects one (or none) of the transconductance stages to drive the output stage. The enabled transconductance stage drives the output stage, and feedback forms a closed-loop amplifier. A mask programmable feedback network sets the closed-loop signal gain. For the ADV3224, this gain is +1, and for the ADV3225, this gain is +2.

The output stage of the ADV3224 or ADV3225 is designed for low differential gain and phase error when driving composite video signals. It also provides slew current for a fast pulse response when driving component video signals. Unlike many multiplexer designs, these requirements are balanced such that large signal bandwidth is very similar to small signal bandwidth. The design load is 150 Ω, but provisions are made to drive loads as low as 100 Ω when on-chip power dissipation limits are not exceeded.

The outputs of the ADV3224/ADV3225 can be disabled to minimize on-chip power dissipation. When disabled, there is no feedback network loading the output. This high disabled output impedance allows multiple ICs to be bussed together without additional buffering. Take care to reduce output capacitance, which results in more overshoot and frequency domain peaking.

A series of internal amplifiers drives internal nodes such that a wideband high impedance is presented at the disabled output, even while the output bus is under large signal swings. To keep these internal amplifiers in their linear range of operation when the outputs are disabled and driven externally, do not allow the voltage applied to them to exceed the valid output swing range for the ADV3224/ADV3225. If the disabled outputs are left floating, they may exhibit high enable glitches. If necessary, the disabled output can be kept from drifting out of range by applying an output load resistor to ground.

The connection of the ADV3224/ADV3225 is controlled by a flexible TTL-compatible logic interface. Either parallel or serial loading into a first rank of latches preprograms each output. A global update signal moves the programming data into the second rank of latches, simultaneously updating all outputs. In serial mode, a serial output pin allows devices to be daisy-chained together for single pin programming of multiple ICs. A power-on reset pin is available to avoid bus conflicts by disabling all outputs. This power-on reset clears the second rank of latches but does not clear the first rank of latches. In serial mode, pre-programming individual inputs is not possible and the entire shift register must be flushed.

To easily interface to ground referenced video signals, the ADV3224/ADV3225 operate on split ±5 V supplies. The logic inputs and output run on a single 5 V supply, and the logic inputs switch at approximately 1.6 V for compatibility with a variety of logic families. The serial output buffer is a rail-to-rail output stage with 5 mA of drive capability.

APPLICATIONS INFORMATION

The ADV3224/ADV3225 have two options for changing the programming of the crosspoint matrix. In the first option, a serial word of 40 bits can be provided, which updates the entire matrix each time the 40-bit word is shifted into the device. The second option allows for changing the programming of a single output via a parallel interface. The serial option requires fewer signals but more time (clock cycles) for changing the programming, whereas the parallel programming technique requires more signals but can change a single output at a time and requires fewer clock cycles to complete the programming.

SERIAL PROGRAMMING

The serial programming mode uses the $\overline{\text{CE}}$, CLK, DATAIN, $\overline{\text{UPDATE}}$, and $\overline{\text{SER}}$/PAR pins. The first step is to assert a low on $\overline{\text{SER}}$/PAR to enable the serial programming mode. $\overline{\text{CE}}$ must be low to allow data to be clocked into the device. The $\overline{\text{CE}}$ signal can be used to address an individual device when devices are connected in parallel.

The $\overline{\text{UPDATE}}$ signal should be high during the time that data is shifted into the serial port of the device. Although the data still shifts in when $\overline{\text{UPDATE}}$ is low, the transparent, asynchronous latches allow the shifting data to reach the matrix, which causes the matrix to try to update to every intermediate state as defined by the shifting data.

The data at DATAIN is clocked in at every falling edge of CLK, and a total of 40 bits must be shifted in to complete the programming. For each of the eight outputs, there are four bits (D0 to D3) that determine the source of its input. The MSB is shifted in first. A fifth bit (D4) precedes the four input select bits and determines the enabled state of the output. If D4 is low (output disabled), the four associated bits (D0 to D3) do not matter because no input switches to that output.

The most significant output address data is shifted in first, and the remaining addresses follow in sequence until the least significant output address data is shifted in. At this point, $\overline{\text{UPDATE}}$ can be taken low, which programs the device according to the data that was just shifted in. The update registers are asynchronous, and when $\overline{\text{UPDATE}}$ is low (and $\overline{\text{CE}}$ is low), they are transparent.

If more than one ADV3224/ADV3225 device is to be serially programmed in a system, the DATAOUT signal from one device can be connected to the DATAIN of the next device to form a serial chain. Connect all of the CLK, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$, and $\overline{\text{SER}}$/PAR pins in parallel and operate them as described previously in this section. The serial data is input to the DATAIN pin of the first device of the chain, and it ripples through to the last. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence (40 bits) is multiplied by the number of devices in the chain.

PARALLEL PROGRAMMING

When using the parallel programming mode, it is not necessary to reprogram the entire device when making changes to the matrix. Parallel programming allows the modification of a single output at a time. Because this takes only one CLK/$\overline{\text{UPDATE}}$ cycle, significant time savings can be realized by using parallel programming.

An important consideration in using parallel programming is that the $\overline{\text{RESET}}$ signal does not reset all registers in the ADV3224/ADV3225. When taken low, the $\overline{\text{RESET}}$ signal sets each output to the disabled state. This is helpful during power-up to ensure that two parallel outputs are not active at the same time.

After initial power-up, the internal registers in the device generally contain random data, even though the $\overline{\text{RESET}}$ signal was asserted. If parallel programming is used to program one output, that output is properly programmed, but the rest of the device has a random program state depending on the internal register content at power-up. Therefore, when using parallel programming, it is essential that all outputs be programmed to a desired state after power-up to ensure that the programming matrix is always in a known state. From this point, parallel programming can be used to modify either a single output or multiple outputs at one time.

Similarly, if both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ are taken low after initial power-up, the random power-up data in the shift register is programmed into the matrix. Therefore, to prevent programming the crosspoint into an unknown state, do not apply low logic levels to both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ after power is initially applied. To eliminate the possibility of programming the matrix to an unknown state, after initial power-up, program the full shift register one time to a desired state using either serial or parallel programming.

To change the programming of an output via parallel programming, take the $\overline{\text{SER}}$/PAR and $\overline{\text{UPDATE}}$ pins high, and take the $\overline{\text{CE}}$ pin low. The CLK signal should be in the high state. Place the 3-bit address of the output to be programmed on A0 to A2.

The first four data bits (D0 to D3) contain the information that identifies the input that is programmed to the addressed output. The fifth data bit (D4) determines the enabled state of the output. If D4 is low (output disabled), the data on D0 to D3 does not matter.

After the address and data signals are established, they can be latched into the shift register by pulling the CLK signal low; however, the matrix is not programmed until the $\overline{\text{UPDATE}}$ signal is taken low. In this way, it is possible to latch in new data for several or all of the outputs first via successive negative transitions of CLK while $\overline{\text{UPDATE}}$ is held high and then have all the new data take effect when $\overline{\text{UPDATE}}$ goes low. Use this technique when programming the device for the first time after power-up when using parallel programming. In parallel mode, the CLK pin is level sensitive, whereas in serial mode, it is edge triggered.

POWER-ON RESET

When powering up the ADV3224/ADV3225, it is usually desirable to have the outputs come up in the disabled state. When taken low, the $\overline{\text{RESET}}$ pin causes all outputs to be in the disabled state. However, the $\overline{\text{RESET}}$ signal does not reset all registers in the ADV3224/ADV3225. This is important when operating in the parallel programming mode. Refer to the Parallel Programming section for information about programming internal registers after power-up. Serial programming programs the entire matrix each time; therefore, no special considerations apply.

Because the data in the shift register is random after power-up, it should not be used to program the matrix, or the matrix can enter unknown states. To prevent the matrix from entering unknown states, do not apply logic low signals to both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ initially after power-up. Instead, first load the shift register with the data and then take $\overline{\text{UPDATE}}$ low to program the device.

The $\overline{\text{RESET}}$ pin has a 20 kΩ pull-up resistor to DVCC that can be used to create a simple power-up reset circuit. A capacitor from $\overline{\text{RESET}}$ to ground holds the $\overline{\text{RESET}}$ pin low for a period during which the rest of the device stabilizes. The low condition causes all of the outputs to be disabled. The capacitor then charges through the pull-up resistor to the high state, thereby, allowing full programming capability of the device.

GAIN SELECTION

The 16 × 8 crosspoints come in two versions, depending on the gain of the analog circuit path. The ADV3224 device is unity gain and can be used for analog logic switching and other applications where unity gain is desired. The ADV3224 outputs have very high impedance when their outputs are disabled.

The ADV3225 can be used for devices that drive a terminated cable with its outputs. This device has a built-in gain of +2 that eliminates the need for a gain of +2 buffer to drive a video line. Its high output disabled impedance minimizes signal degradation when paralleling additional outputs of other crosspoint devices.

CREATING LARGER CROSSPOINT ARRAYS

The ADV3224/ADV3225 are high density building blocks for creating crosspoint arrays of dimensions larger than 16 × 8. Various features, such as output disable, chip enable, and gain of +1 and gain of +2 options, are useful for creating larger arrays.

The first consideration in constructing a larger crosspoint is to determine the minimum number of devices that is required. The 16 × 8 architecture of the ADV3224/ADV3225 contains 128 points, which is a factor of 32 greater than a 4 × 1 crosspoint (or multiplexer). The benefits realized in PCB area used, power consumption, and design effort are readily apparent when compared to using multiples of these smaller 4 × 1 devices.

To obtain the minimum number of required points for a nonblocking crosspoint, multiply the number of inputs by the number of outputs. Nonblocking requires that the programming of a given input to one or more outputs not restrict the availability of that input to be a source for any other outputs. Some nonblocking crosspoint architectures require more than this minimum. In addition, there are blocking architectures that can be constructed with fewer devices than this minimum. These systems have connectivity available on a statistical basis that is determined when designing the overall system.

The basic concept in constructing larger crosspoint arrays is to connect inputs in parallel in a horizontal direction and to wire-OR the outputs together in the vertical direction. The wire-OR connection can be viewed as a tristate multiplex of the two outputs in that only one output is enabled and the other is in a high-Z state. The meaning of horizontal and vertical can best be understood by referring to Figure 65, which illustrates this concept for a 32 × 16 crosspoint array that uses four ADV3224 or ADV3225 devices.

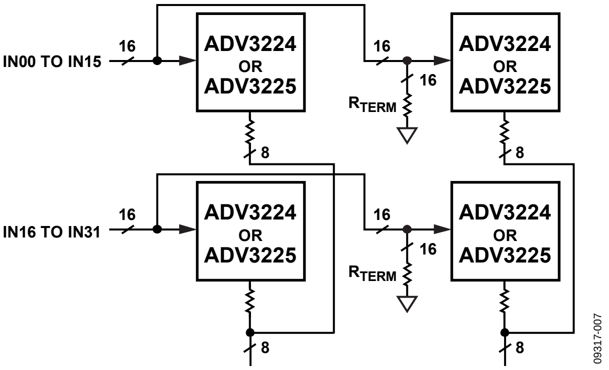
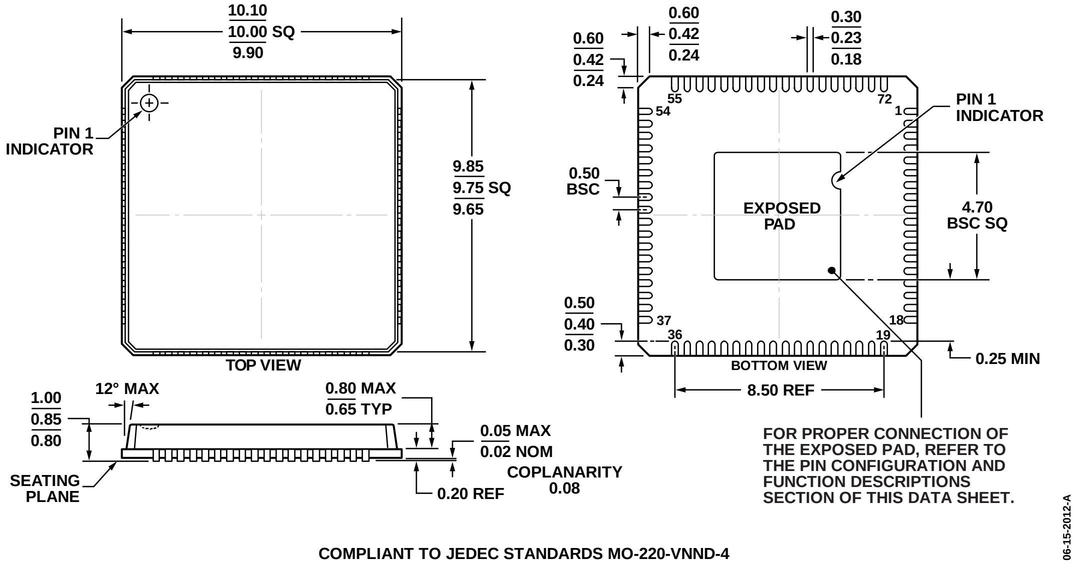


Figure 65. A 32 × 16 Nonblocking Crosspoint Switch Array

Each input is uniquely assigned to each of the 32 inputs of the two devices and terminated appropriately. The outputs are wired-OR'ed together in pairs. Enable the output from only one wire-OR'ed pair at any given time. The device programming software must be properly written to prevent multiple connected outputs from being enabled at the same time.

Also available are 32 × 16 arrays in a single package: AD8104, AD8105, ADV3202, and ADV3203. More expansion options are possible using the ADV3226 and ADV3227 wideband 16 × 16 arrays. For a complete 32 × 32 array in a single device, use the AD8117 and AD8118 for wide bandwidth or the ADV3200 and ADV3201 for less bandwidth.

OUTLINE DIMENSIONS



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 66. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADV3224ACPZ	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-1
ADV3224-EVALZ		Evaluation Board	
ADV3225ACPZ	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-1
ADV3225-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D09317-0-1/16(B)

LifeElectronics
Живое партнерство

ООО "ЛайфЭлектроникс" **"LifeElectronics" LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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