Data Sheet | November 18, 2004 | FN4725.5

Dual Slot PCI Hot Plug Controllers

The HIP1011D, HIP1011E are the first ICs available for independent control of two PCI Hot-Plug slots. The HIP1011D has all the features and functionality of two single PCI Hot-Plug slot controllers such as the HIP1011A but in the same foot print area. Like the single slot HIP1011B, the HIP1011E does not monitor output voltage nor respond to undervoltage conditions.

The HIP1011D, HIP1011E are designed to be physically placed in close proximity to two adjacent PCI slots thus reducing layout complexity and placement costs in assembly. The HIP1011D, HIP1011E provides independent power control to each slot and the addition of discrete power MOSFETs and a few passive components creates two complete power control solutions. The IC integrates the +12V and -12V current sensing switches for each slot. Overcurrent (OC) protection is provided by sensing the voltage across external current-sense resistors. In addition, on-chip references are used to monitor the +5V, +3.3V and +12V outputs for undervoltage (UV) conditions *. The two PWRON inputs control the state of the switches, one each for slot A and slot B outputs. During an OC condition on any output, or a UV condition on the +5V, +3.3V or +12V outputs *, a LOW (0V) is asserted on the associated FLTN output and all associated switches are latched-off. The outputs servicing the adjacent slot are unaffected.

The time to FLTN signal going LOW and MOSFET latch off is user determined by a single capacitor from each FLTN pin to ground. This added feature enables the HIP1011D, HIP1011E to ignore system noise transients. The FLTN latch is cleared when the PWRON input is toggled low again. During initial power-up of the main VCC supply (+12V), the PWRON input is inhibited from turning on the switches, and the latch is held in the Reset state until the VCC input is greater than 10V.

User programmability of the overcurrent threshold and turn-on slew rate is provided. A resistor connected to the OCSET pin programs the overcurrent threshold for both slots. Capacitors connected to the gate pins set the turn-on rate.

* UV references do not apply to HIP1011E.

Features

- Independent Power Control of 2 PCI Slots
- Turn-Off Delay Time Adjustability
- Internal MOSFET Switches for +12V and -12V Outputs
- μP Interface for On/Off Control and Fault Reporting
- Adjustable Overcurrent Protection for All Eight Supplies
- Provides Fault Isolation
- Adjustable Turn-On Slew Rate
- Minimum Parts Count Solution
- No Charge Pump
- 100ns Response Time to Overcurrent
- Pb-Free Available (RoHS Compliant)

Applications

- PCI Hot-Plug

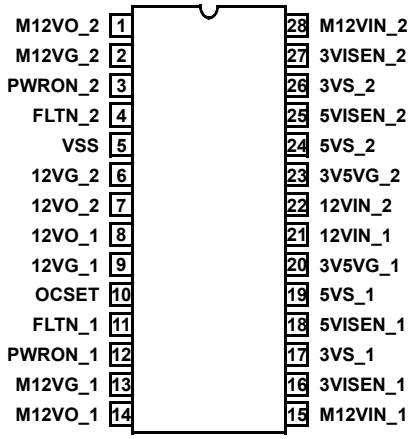
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP1011DCA*	0 to 70	28 Ld SSOP	M28.15
HIP1011DCAZA* (See Note)	0 to 70	28 Ld SSOP (Pb-free)	M28.15
HIP1011ECA*	0 to 70	28 Ld SSOP	M28.15
HIP1011ECAZA* (See Note)	0 to 70	28 Ld SSOP (Pb-free)	M28.15

* Add "-T" suffix for tape and reel option.
NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Pinout

HIP1011D, HIP1011E (SSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Typical Application

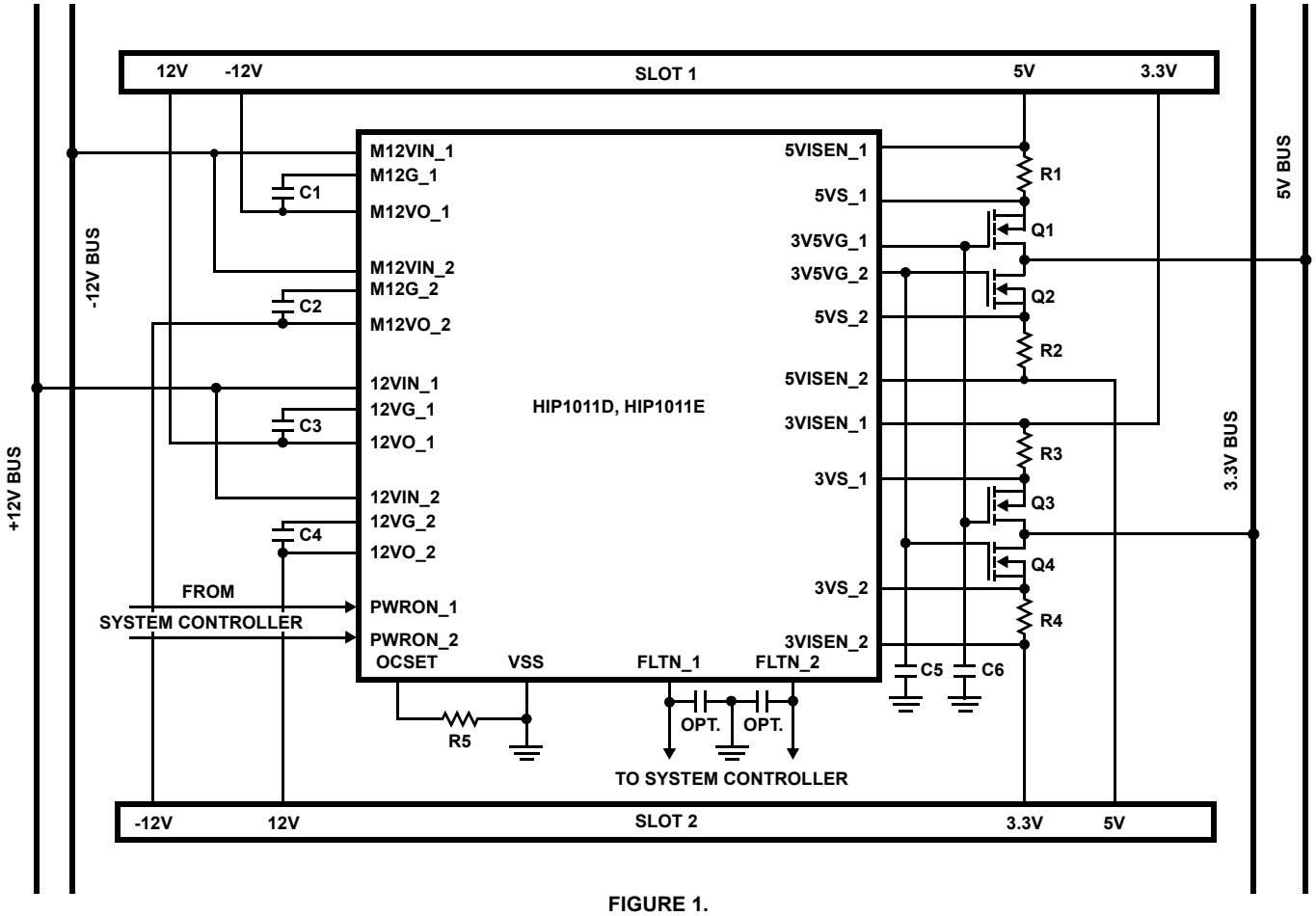


FIGURE 1.

Simplified Schematic (1/2 HIP1011D, HIP1011E)

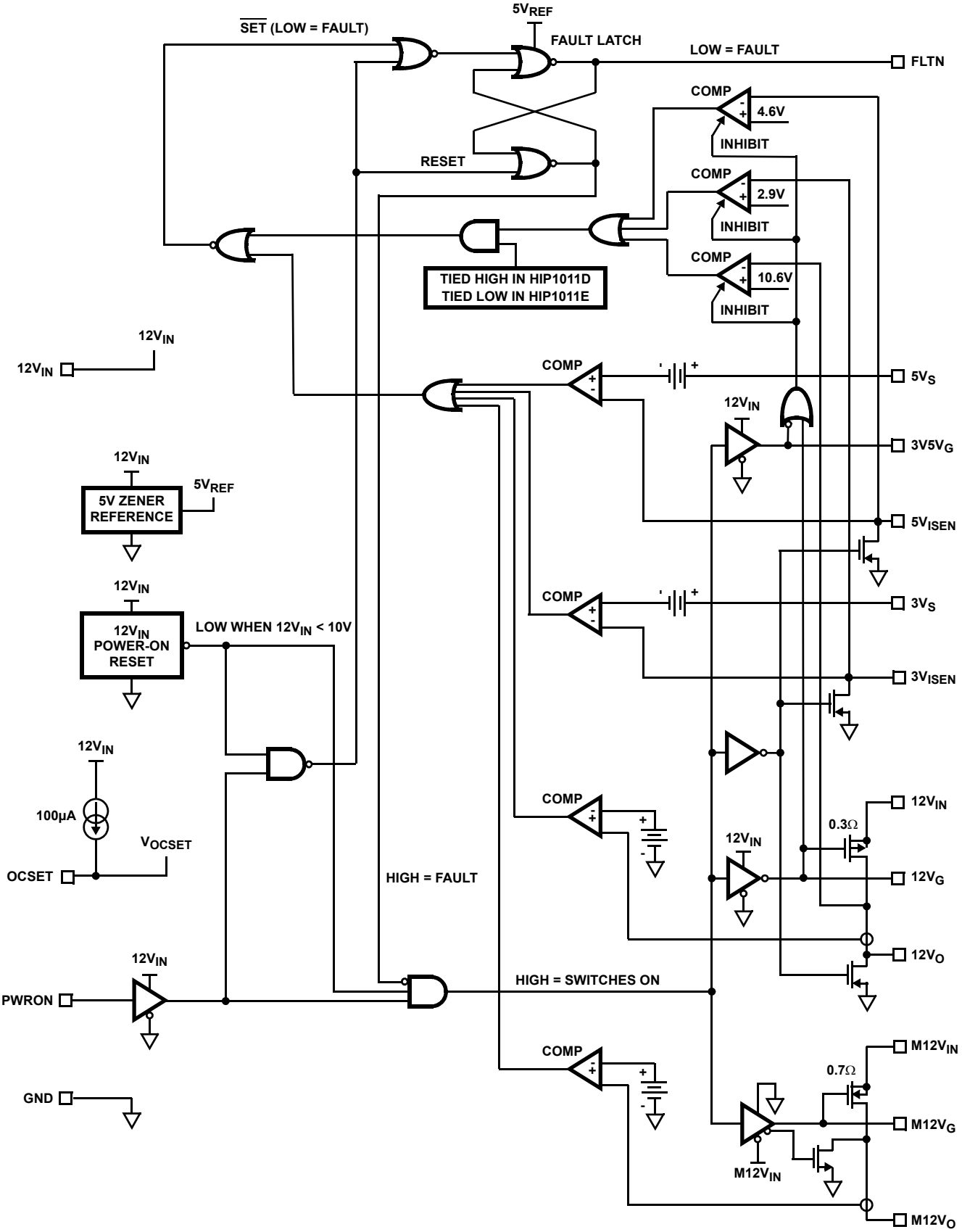


FIGURE 2.

Pin Descriptions

PIN NO.	DESIGNATOR	FUNCTION	DESCRIPTION
15, 28	M12VIN	-12V Input	-12V Supply Input. Also provides power to the -12V overcurrent circuitry.
4, 11	FLTN	Fault Output	5V CMOS Fault Output; LOW = FAULT. An optional capacitor may be placed from this pin to ground to provide additional immunity from power supply glitches.
20, 23	3V5VG	3.3V/5V Gate Output	Drive the gates of the 3.3V and 5V MOSFETs. Connect a capacitor to ground to set the startup ramp. During turn on, this capacitor is charged with a 25μA current source. HIP1011D UV comparator disabled when this pin is below 9.6V nominal.
21, 22	12VIN	12V Input	12V supply input for IC and 12VO. Both 12VIns to be connected to a single +12V supply.
16, 27	3VISEN	3.3V Current Sense	Connect to the load side of the current sense resistor in series with source of external 3.3V MOSFET.
17, 26	3VS	3.3V Source	Connect to source of 3.3V MOSFET. This connection along with (3VISEN) senses the voltage drop across the sense resistor.
19, 24	5VS	5V Source	Connect to source of 5V MOSFET switch. This connection along with (5VISEN) senses the voltage drop across the sense resistor.
18, 25	5VISEN	5V Current Sense	Connect to the load side of the current sense resistor in series with source of external 5V MOSFET.
3, 12	PWRON	Power On Control	Controls all four switches. High to turn switches ON, Low to turn them OFF.
6, 9	12VG	Gate of Internal PMOS	Connect a capacitor between 12VG and 12VO to set the startup ramp for the +12V supply. This capacitor is charged with a 25μA current source during startup. HIP1011D UV comparator disabled when this pin >1.4V nominal.
7, 8	12VO	Switched 12V Output	Switched 12V output. Rated for 0.5A.
2, 13	M12VG	Gate of Internal NMOS	Connect a capacitor between M12VG and M12VO to set the startup ramp for the M12V supply. This capacitor is charged with 25μA during startup.
1, 14	M12VO	Switched -12V Output	Switched -12V Output. Rated for 0.1A.
10	OCSET	Overcurrent Set	Connect a resistor from this pin to ground to set the overcurrent trip point of all eight switches. All eight overcurrent trips can be programmed by changing the value of this resistor. The default (6.04kΩ, 1%) is compatible with the maximum allowable currents as outlined in the PCI specification.
5	VSS	Ground	Connect to common of power supplies.

Absolute Maximum Ratings

12VIN . . . . . -0.5V to +14.0V
12VO, 12VG, 3V5VG . . . . . -0.5V to 12VIN+0.5V
M12VIN . . . . . -14.0V to +0.5V
M12VO, M12VG. . . . . V_{M12VIN}-0.5V to +0.5V
3VISEN, 5VISEN . . . . . -0.5V to the Lesser of 12VIN or +7.0V
Voltage, Any Other Pin. . . . . -0.5V to +7.0V
12VO Output Current 3A
M12VO Output Current 0.8A
ESD Classification . . . . . .2KeV (HBM)

Operating Conditions

12VIN Supply Voltage Range . . . . . .+10.8V to +13.2V
5V and 3.3V Input Supply Tolerances. . . . . .±10%
12VO Output Current . . . . . .0 to +0.5A
M12VO Output Current . . . . . .0 to +0.1A
Temperature Range (T_A) . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SSOP Package	77

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

Nominal 5.0V and 3.3V Input Supply Voltages,
$12V_{IN}$ = 12V, $M12V_{IN}$ = -12V, $T_A = T_J$ = 0 to 70°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V/3.3V SUPPLY CONTROL						
5V Overcurrent Threshold	I_{OC5V}	See Figure 24, Typical Application	-	8	-	A
5V Overcurrent Threshold Voltage	V_{OC5V_1}	V_{OCSET} = 0.6V	33	42	50	mV
5V Overcurrent Threshold Voltage	V_{OC5V_2}	V_{OCSET} = 1.2V	70	80	90	mV
5V Undervoltage Trip Threshold	V_{5VUV}	(HIP1011D only)	4.42	4.65	4.8	V
5V Undervoltage Fault Response Time	t_{5VUV}	(HIP1011D only)	-	110	160	ns
5V Turn-On Time (PWRON High to 5VOUT = 4.75V)	t_{ON5V}	C_{3V5VG} = 0.022µF, C_{5VOUT} = 2000µF, R_L = 1Ω	-	6.5	-	ms
3V Overcurrent Threshold	I_{OC3V}	See Figure 24, Typical Application	-	10	-	A
3V Overcurrent Threshold Voltage	V_{OC3V_1}	V_{OCSET} = 0.6V	41	52	62	mV
3V Overcurrent Threshold Voltage	V_{OC3V_2}	V_{OCSET} = 1.2V	89	98	108	mV
3V Undervoltage Trip Threshold	V_{3VUV}	(HIP1011D Only)	2.74	2.86	2.98	V
3V Undervoltage Fault Response Time	t_{3VUV}	(HIP1011D Only)	-	110	160	ns
3V5VG Undervoltage Enable Threshold Voltage	$V_{3V5VGENVth}$	(HIP1011D Only)	-	9.6	-	V
3V Turn-On Time (PWRON High to $3V_{OUT}$ = 3.00V)	t_{ON3V}	C_{3V5VG} = 0.022µF, C_{3VOUT} = 2000µF, R_L = 0.43Ω	-	6.5	-	ms
3V5VG V_{OUT} High	Vout_hi_35VG	PWRON = High, FLTN = High	11.5	11.8	-	V
Gate Output Charge Current	IC_{3V5VG}	PWRON = High, V_{3V+5VG} = 4V	19	25.0	29	µA
Gate Turn-On Time (PWRON High to 3V5VG = 11V)	t_{ON3V5V}	C_{3V5VG} = 0.033µF, 3V5VG Rising 10% to 90%	-	280	-	µs
Gate Turn-Off Time	$t_{OFF3V5V}$	C_{3V5VG} = 0.033µF, 3V5VG Falling 90% to 10%	-	2	-	µs

Electrical Specifications Nominal 5.0V and 3.3V Input Supply Voltages, $12V_{IN}$ = 12V, $M12V_{IN}$ = -12V, $T_A = T_J$ = 0 to 70°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
+12V SUPPLY CONTROL						
On Resistance of Internal PMOS	$r_{DS(ON)12}$	PWRON = High, I_D = 0.5A $T_A = T_J$ = 25°C	-	0.3	0.35	Ω
		$T_A = T_J$ = 70°C	-	0.35	0.50	Ω
Overcurrent Threshold	I_{OC12V_1}	V_{OCSET} = 0.6V	0.5	0.6	0.9	A
Overcurrent Threshold	I_{OC12V_2}	V_{OCSET} = 1.2V	1.2	1.4	1.8	A
12V Undervoltage Trip Threshold	V_{12VUV}	(HIP1011D only)	10.25	10.6	10.8	V
Undervoltage Fault Response Time	t_{12VUV}	(HIP1011D only)	-	110	-	ns
Gate Charge Current	IC_{12VG}	PWRON = High, V_{12VG} = 10V	19	25.0	29	µA
Turn-On Time (PWRON High to 12VG = 1V)	t_{ON12V}	C_{12VG} = 0.033µF, 12VG Falling 90% - 10%	-	16	-	ms
Turn-Off Time	t_{OFF12V}	C_{12VG} = 0.022µF, 12VG Rising 10% - 90%	-	3	-	µs
-12V SUPPLY CONTROL						
On Resistance of Internal NMOS	$r_{DS(ON)M12}$	PWRON = High, I_D = 0.1A $T_A = T_J$ = 25°C	-	0.7	1	Ω
		$T_A = T_J$ = 70°C	-	1.0	1.3	Ω
Overcurrent Threshold	I_{OC12V_1}	V_{OCSET} = 0.6V	0.13	0.17	0.25	A
Overcurrent Threshold	I_{OC12V_2}	V_{OCSET} = 1.2V	0.23	0.36	0.52	A
Gate Output Charge Current	IC_{M12VG}	PWRON = High, V_{3VG} = -10V	19	25	29	µA
Turn-On Time (PWRON High to M12VO = -10.8V)	t_{ONM12V}	C_{M12VG} = 0.033µF, C_{M12VO} = 50µF, R_L = 120Ω	-	16	-	ms
Turn-Off Time	$t_{OFFM12V}$	C_{M12VG} = 0.033µF, M12VG Falling 90% to 10%	-	3	-	µs
M12VIN Input Bias Current	IB_{M12VIN}	PWRON = High	-	2.5	5	mA
CONTROL I/O PINS						
Supply Current	I_{VCC}		-	5.3	8	mA
OCSET Current	I_{OCSET}		93	100	107	µA
Overcurrent Fault Response Time	t_{OC}		-	500	960	ns
PWRON Threshold Voltage	$V_{THPWRON}$		1.0	1.6	2.1	V
FLTN Output Low Voltage	$V_{FLTN,OL}$	I_{FLTN} = 0.9mA	-	0.25	0.4	V
FLTN Output High Voltage	$V_{FLTN,OH}$	I_{FLTN} = 0 to -4mA	3.5	4.3	-	V
FLTN Output Latch Threshold	$V_{FLTN, TH}$	FLTN High to Low Transition	1.8	2.3	3	V
12V Power On Enable Threshold	$V_{POR, THrise}$	V_{CC} Voltage Rising	9.4	10	10.2	V
12V Power On Reset Threshold	$V_{POR, THfall}$	V_{CC} Voltage Falling	8.9	9.3	9.6	V

Introduction

The HIP1011D and HIP1011E are the first dual PCI slot IC devices designed to provide control and protection of the four PCI power supplies independently to two PCI slots. Like the widely used HIP1011 this device complies with the PCI Hot Plug specification facilitating the service, upgrading or expansion of PCI based servers without the need to power down the server. The HIP1011D protects against overcurrent (OC) for the -12V, +12V, +3.3V, +5V and undervoltage (UV) conditions for the +12V, +3.3V, +5V supplies. The HIP1011E only responds to OC conditions.

Figure 1 illustrates the typical implementation of the HIP1011D, HIP1011E. Additional components for optimizing performance for particular applications, or desired features may be necessary.

Key Feature Description and Operation

The HIP1011D/E, four power MOSFETs and a few passive components as configured in Figure 1, create a small yet complete power control solution for two PCI slots. It provides an OC trip level greater than the maximum PCI specified current for each supply to each slot. OC monitoring and protection for the 3.3V and 5V supplies is provided by sensing the voltage across external current-sense resistors. For the +12V and -12V inputs, OC protection is provided internally. On-chip references in the HIP1011D are used to monitor the +5V, +3.3V and +12V outputs for UV conditions. During an OC condition on any output, or a UV condition on the +5V, +3.3V or +12V outputs (HIP1011D only), all slot specific MOSFETs are immediately latched-off and a LOW (0V) is presented to the appropriate FLTN output. During initial power-up of the main V_{CC} supply (+12V), the $\overline{\text{PWRON}}$ inputs are inhibited from turning on the switches, and the latch is held in the reset state until the V_{CC} input is greater than 10V. After a fault has been asserted and FLTN is latched low cycling PWRON low then high will clear the FLTN latch. User programming of the OC thresholds for both controlled slots is provided by a single resistor connected to the OCSET pin along with R_{SENSE}. In addition delay time to latch off after a fault condition can be increased by increasing the FLTN to ground capacitance and the turn-on ramp rate can be increased by increasing the gate pin capacitance.

Customizing Circuit Performance

OverCurrent (OC) Set Functionality and Resistor Choice

The HIP1011D/E allows easy custom programming of the OC levels of all 4 supplies simultaneously for both PCI slots by simply changing the resistor value between OCSET, (pin 10), and ground. The R_{OCSET} value and the OCSET 100µA current source sets a voltage that is used in each of eight comparators, (one for each supply for both slots). The voltages developed across the 3.3V and 5V sense resistors are applied to the inputs of their respective comparators. The +12V and -12V currents are sensed internally with pilot devices. Once any comparator trips, that output is fed through logic circuits resulting in the appropriate FLTN, (pin 4 or pin 11), going low, indicating a fault condition on that particular slot. Because of the internal current monitoring of the +12V and -12V switches, their programming flexibility is limited to R_{OCSET} changes. The 3.3V and 5V overcurrent trip points depend on both R_{OCSET} and the value chosen for each sense resistor.

See Table 1 to determine OC protection levels relative to choice of R_{OCSET} and R_{SENSE} values.

Overcurrent design guidelines and recommendations are as follows:

1. For PCI applications, set R_{OCSET} to 6.04kΩ, and use 5mΩ 1% sense resistors (see Figure 24).
2. For non PCI specified applications, the following precautions and limitations apply:

A. **Do not** exceed the maximum power of the integrated NMOS and PMOS. High power dissipation must be coupled with effective thermal management. The integrated PMOS has an $r_{DS(ON)}$ of 0.3Ω. Thus, with 1A of steady load current on each of the PMOS devices the power dissipation is 0.6W. The thermal impedance of the package is 95 degrees Celsius per watt, limiting the average DC current on the 12V supply to about 1A on each slot and imposing an upper limit on the R_{OCSET} resistor. **Do not** use an R_{OCSET} resistor greater than 15kΩ.

The average current on the -12V supply should not exceed 0.7A. Since the thermal restrictions on the +12V supply are more severe, the +12V supply restricts the use of the HIP1011 to applications where the ±12V supplies draw relatively little current. Since both supplies only have one degree of freedom, the value of R_{OCSET}, the flexibility of programming is quite limited. For applications where more power is required on the +12V supply, contact your local Intersil sales representative for information on other Hot Plug solutions.

B. **Do not** try to sense voltages across the external sense resistors that are less than 33mV. Spurious faults due to noise and comparator input sensitivity may result. The minimum recommended R_{OCSET} value is 6kΩ. This will set the nominal OC voltage thresholds at 52mV and 42mV for the 3.3V and 5V comparators respectively. This is the voltage level at which the OC fault (I_{OUT} x R_{SENSE}) will occur.

C. Minimize V_{RSENSE} so as to not significantly reduce the voltage delivered to the adapter card. Remember PCB trace and connector distribution voltage losses also need to be considered. Make sure that the R_{SENSE} resistor can adequately handle the dissipated power. For best results use a 1% precision resistor with a low temperature coefficient.

D. Minimize external FET $r_{DS(ON)}$. Low $r_{DS(ON)}$ or multiple MOSFETs in parallel are recommended. See Intersil for a complete selection of MOSFET offerings.

TABLE 1.

SUPPLY	HOW TO DETERMINE +25c NOMINAL (±10%) I_{OC} FOR EACH SUPPLY
+3.3V I_{OC}	((100µA x R_{OCSET})/11.5)/R_{RSENSE}
+5.0V I_{OC}	((100µA x R_{OCSET})/14.5)/R_{RSENSE}
+12V I_{OC}	(100µA x R_{OCSET})/1
-12V I_{OC}	(100µA x R_{OCSET})/3.4

Time Delay to Latch-Off

Time delay to latch-off allows for a predetermined delay from an OC or UV in the HIP1011D or an OC in the HIP1011E event to the simultaneous latch-off of all four supply switches of the affected slot. This delay period is set by the capacitance value to ground from the FLTN pins for each slot. This capacitance value tailors the FLTN signal going low ramp rate. This provides a delay to the fault signal latch-off threshold voltage, FLTN, Vth. By increasing this time, the HIP1011D/E delays immediate latch-off of the bus supply switches, thus ignoring transient faults. See additional information in the “Using the HIP1011DEVAL1 Platform” section of this data sheet. The HIP1011E has all features of the HIP1011D but it does not respond to UV events.

Caution: The primary purpose of a protection device such as the HIP1011D/E is to quickly isolate a faulted card from the voltage bus. Delaying the time to latch-off works against this primary concern so care must be taken when using this feature. Ensure adequate sizing of external FETs to carry additional current during time out period. Understand that voltage bus disruptions must be minimized for the time delay period in the event of a crow bar failure.

Devices using an unadjustable preset delay to latch-off time present the user with the inability to eliminate these concerns increasing cost and the chance of additional ripple through failures.

HIP1011D, HIP1011E Soft Start and Turn-Off Considerations

The HIP1011D/E does allow the user to select the rate of ramp up on the voltage supplies. This startup ramp minimizes in-rush current at startup while the on card bulk capacitors charge. The ramp is created by placing capacitors on M12VG to M12VO, 12VG to 12VO and 3V5VG to ground. These capacitors are each charged up by a nominal 25µA current during turn on. The same value for all gate timing capacitors is recommended. A recommended minimum value of 0.033µF as a smaller value may cause overcurrent faults at power up. This recommendation results in a nominal gate voltage ramp rate of 0.76V/ms. The gate capacitors must be discharged when a fault is detected to turn off the power FETs. Thus, larger caps slow the response time. If the gate capacitors are too large the HIP1011D/E may not be able to adequately protect the bus or the power FETs. The HIP1011D/E have internal discharge FETs to discharge the load when disabled. Upon turn-off these internal switches on each output discharge the load capacitance pulling the output to GND. These switches are also on when PWRON is low thus an open slot is held at the GND level.

Decoupling Precautions and Recommendations

For the HIP1011D/E proper decoupling is a particular concern during the normal switching operation and especially during a card crowbar failure. If a card experiences a crow bar short to ground, the supply to the other card will experience transients until the faulted card is isolated from the bus. In addition the common IC nodes between the two sides can fluctuate unpredictably resulting in a false latch-off of the second slot. Additionally to the mother board bulk capacitance, it is recommended that 10µF capacitors be placed on both the +12V and -12V lines of the HIP1011D/E as close to the chip as possible.

Recommended PCB Layout Design Best Practices

To ensure accurate current sensing, PCB traces that connect each of the current sense resistors to the HIP1011D/E **must not** carry any load current. This can be accomplished by two dedicated PCB kelvin traces directly from the sense resistors to the HIP1011D/E (see examples of correct and incorrect layouts below in Figure 3). To reduce parasitic inductance and resistance effects, maximize the width of the high-current PCB traces.

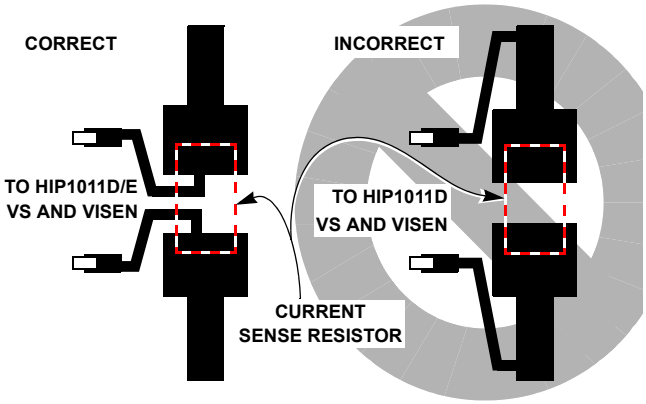


FIGURE 3. SENSE RESISTOR PCB LAYOUT

Typical Performance Curves

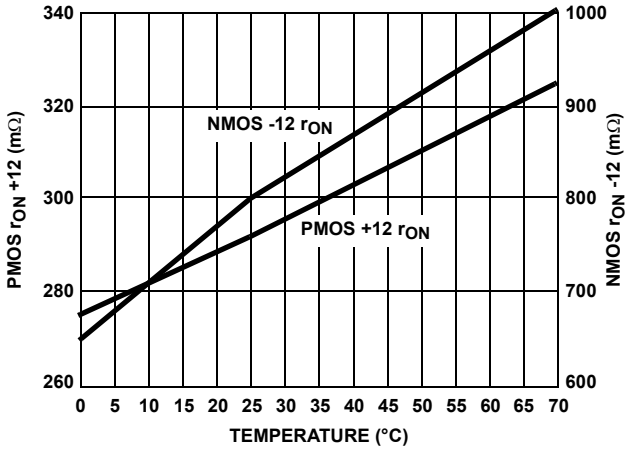


FIGURE 4. r_{ON} vs TEMPERATURE

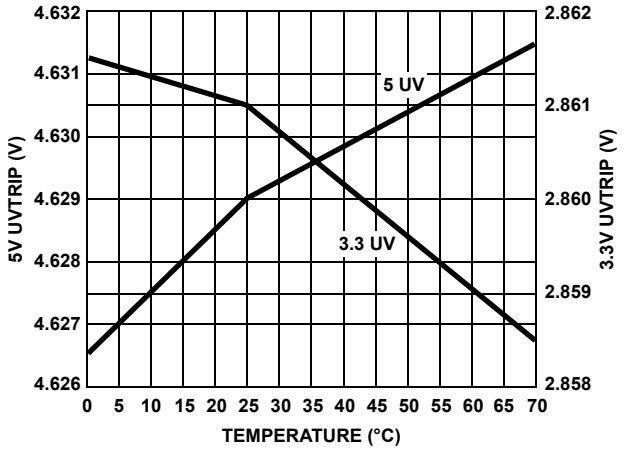


FIGURE 5. UV TRIP vs TEMPERATURE (HIP1011D only)

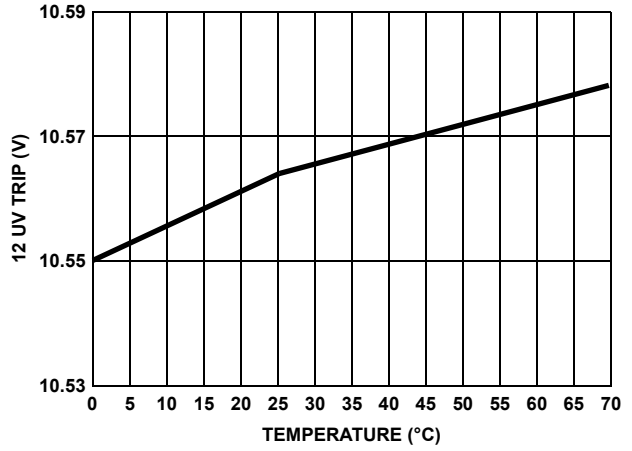


FIGURE 6. 12 UV TRIP vs TEMPERATURE (HIP1011D only)

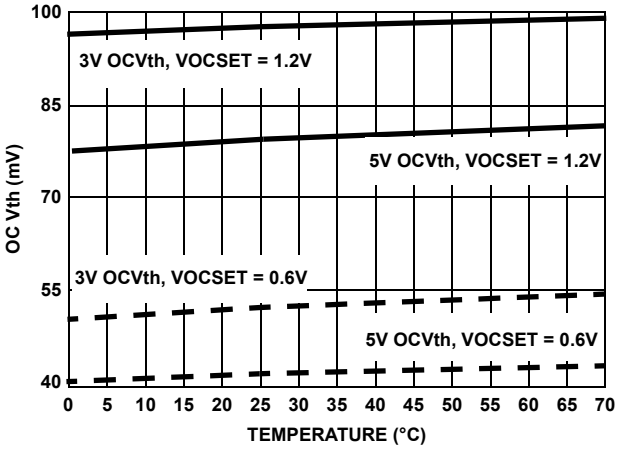


FIGURE 7. OC Vth vs TEMPERATURE

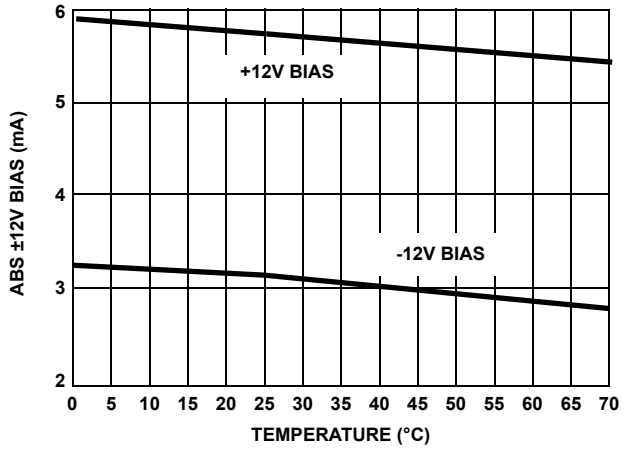


FIGURE 8. BIAS CURRENT vs TEMPERATURE

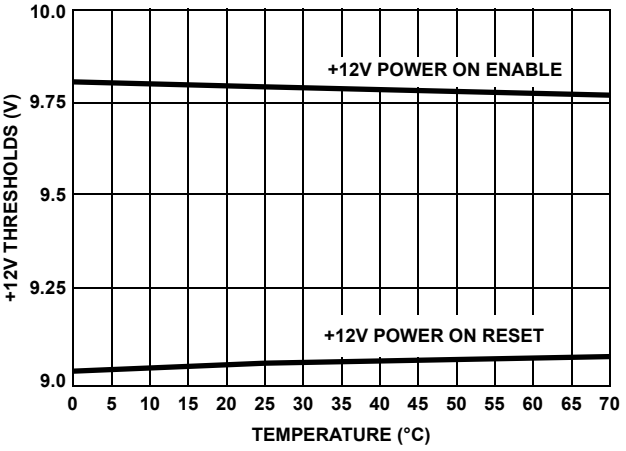


FIGURE 9. 12V ENABLE AND RESET THRESHOLD VOLTAGES vs TEMPERATURE

Typical Performance Curves (Continued)

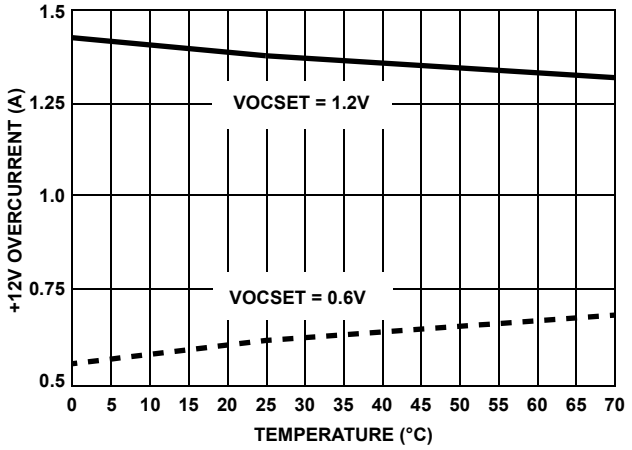


FIGURE 10. +12V OVERCURRENT LEVEL vs TEMPERATURE

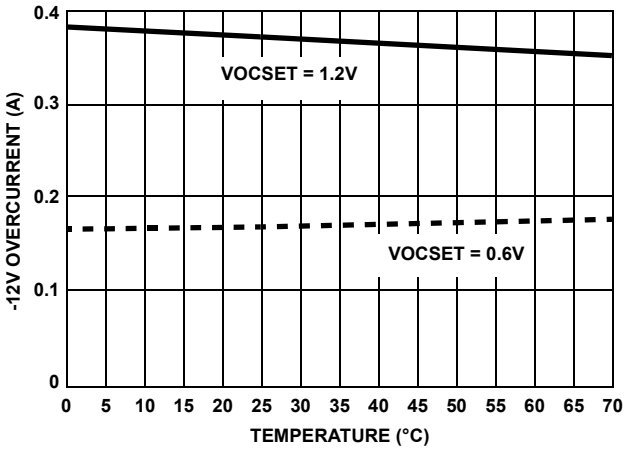


FIGURE 11. -12V OVERCURRENT vs TEMPERATURE

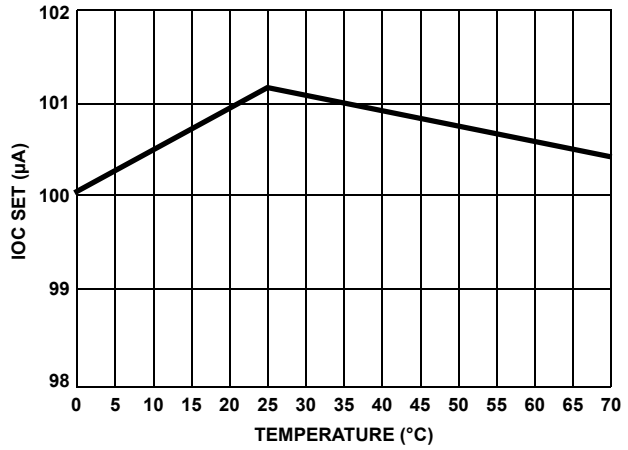


FIGURE 12. OCSET CURRENT vs TEMPERATURE

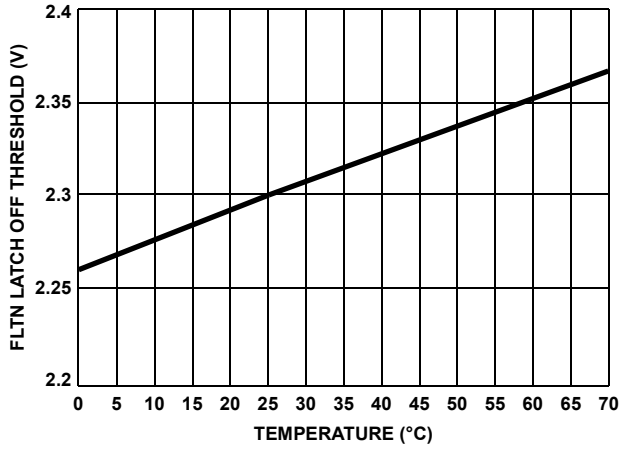


FIGURE 13. FLTN LATCH-OFF THRESHOLD VOLTAGE vs TEMPERATURE

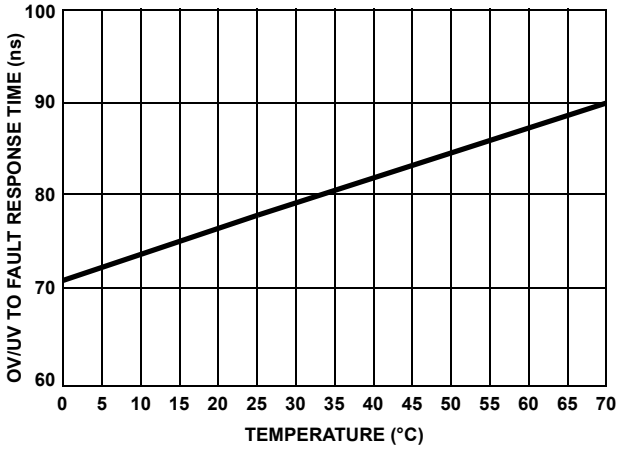


FIGURE 14. OVERCURRENT AND UNDERVOLTAGE TO FLTN RESPONSE TIME vs TEMPERATURE

Using the HIP1011DEVAL1 Platform

General and Biasing Information

The HIP1011DEVAL1 platform (Figure 24) comes as a three part set consisting of 1 motherboard emulator and 2 load cards. This evaluation platform allows a designer to evaluate and modify the performance and functionality of the HIP1011D or HIP1011E in a simple environment.

Test point numbers (TP#) correspond to the HIP1011D/E device (U5) pin numbers. Thus TP3 and TP12 are PWRON_2 and PWRON_1 respectively. These 2 pins are the HIP1011D/E control inputs for each of the 2 integrated but independent PCI power controllers in the HIP1011D/E.

On the HIP1011DEVAL1 platform are 4 HUF76132SK8, (11.5mΩ, 30V, 11.5A) N-Channel power MOSFETs, (Q1- Q4) these are used as the external switches for the +5V and +3.3V supplies to the load card connectors, P1 and P2.

Current sensing is facilitated by the four 5mΩ 1W metal strip resistors (R1-R4), the voltages developed across the sense resistors are compared to references on board the HIP1011D/E.

The HIP1011DEVAL1 platform is powered through the J1 to J5 connector jacks near the top of the board (see Table 2 for bias voltage assignments.)

TABLE 2. HIP1011DEVAL1 BIAS ASSIGNMENTS

J1	J2	J3	J4	J5
GND	+5V	-12V	+12V	+3.3V

After properly biasing the HIP1011D/E and ensuring there is an adequate ground return from the HIP1011DEVAL1 platform to the power supplies, (otherwise anomalous and unpredictable results will occur) signal the PWRON inputs low then insert the load cards as shown in Figure 15. Signaling either or both PWRON pins high (>2.4V) will turn on the appropriate FET switches and apply voltage to the load cards.

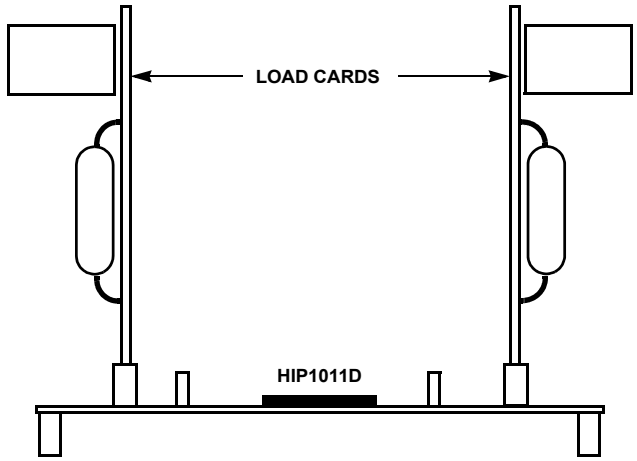


FIGURE 15. CORRECT INSTALLATION OF LOAD CARDS

* The HIP1011DEVAL board is supplied with a HIP1011D installed and in addition a loose packed HIP1011E.

Evaluating Time Delay to Latch-Off

Provided for delay to latch-off evaluation are 2 locations for SMD capacitors, C7 and C8. Filling these locations places a capacitor to ground from each of the HIP1011D/E FLTN pins thus tailoring the FLTN signal going low ramp rate. This provides a delay to the fault signal latch-off threshold voltage, FLTN Vth. By increasing this time the HIP1011D delays immediate latch-off of the bus supply switches, thus ignoring transient OC and UV conditions. See Table 3 illustrating the time it takes for switch gate turn-off from the FLTN start of response to an OC or UV condition. The FLTN response to an OC or UV condition is 110ns. See Figures 20 through 23 for waveforms.

The intent of any protection device is to isolate the supply quickly so a faulty card does not drag down a supply. A longer latch-off delay results in less isolation from a faulty card to supply.

TABLE 3.

C7 AND C8 VALUE	OPEN	0.001µF	0.01µF	0.1µF
FLTN to Gate Response	0.1µs	0.44µs	2.9µs	28µs

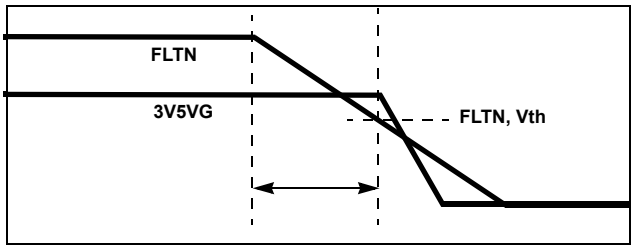


FIGURE 16. TIMING DIAGRAM

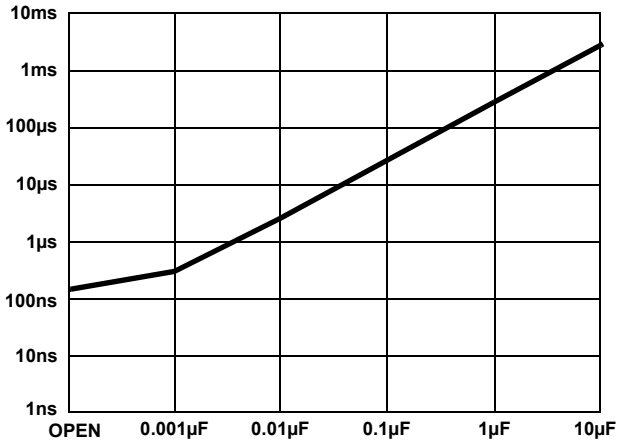


FIGURE 17. TYPICAL OC/UV TO VG RESPONSE vs FLTN CAP

Typical Performance Curves (Continued)

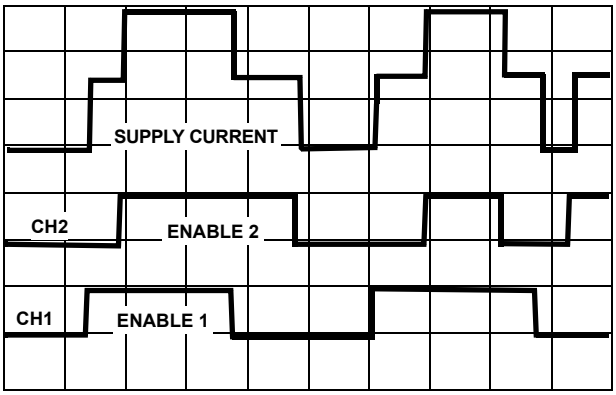


FIGURE 18. HIP1011DEVAL1 3.3V SUPPLY CURRENT AS EACH SLOT CONTROLLER TURNS ON INTO LOAD CARD

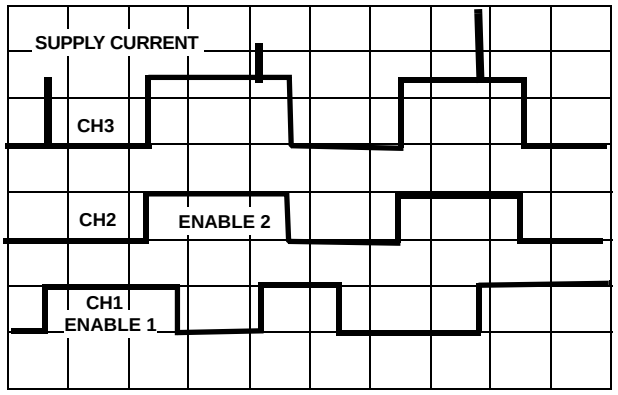


FIGURE 19. HIP1011DEVAL1 3.3V SUPPLY CURRENT AS CONTROLLER 1 TURNS ON INTO SHORTED LOAD CARD

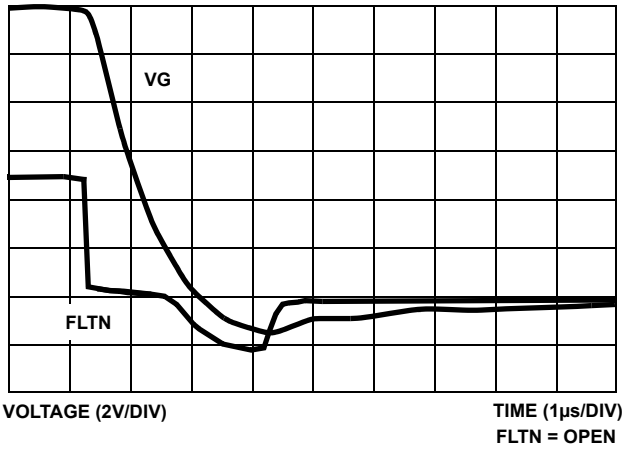


FIGURE 20. FLTN TO 35VG DELAY

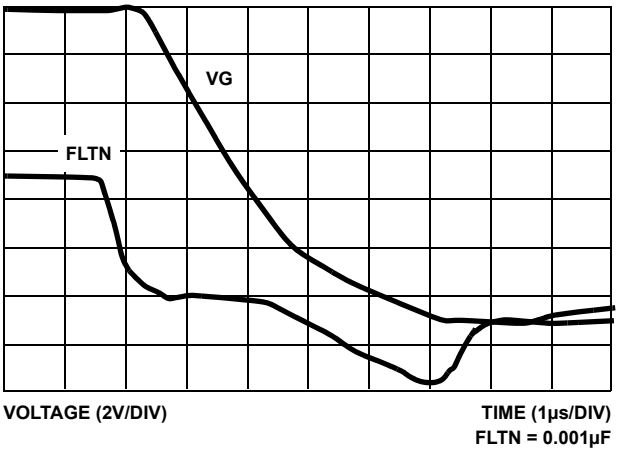


FIGURE 21. FLTN TO 35VG DELAY

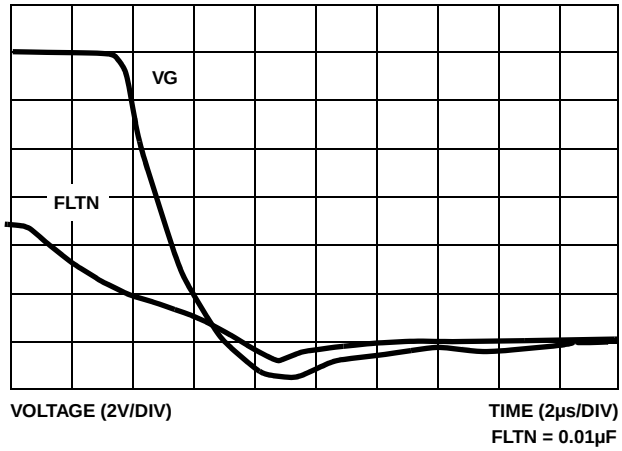


FIGURE 22. FLTN TO 35VG DELAY

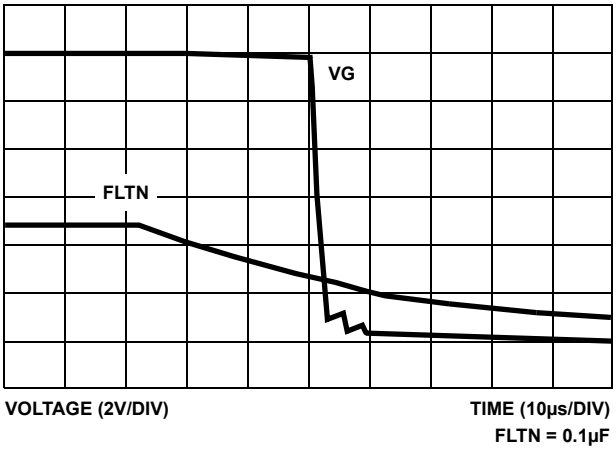


FIGURE 23. FLTN TO 35VG DELAY

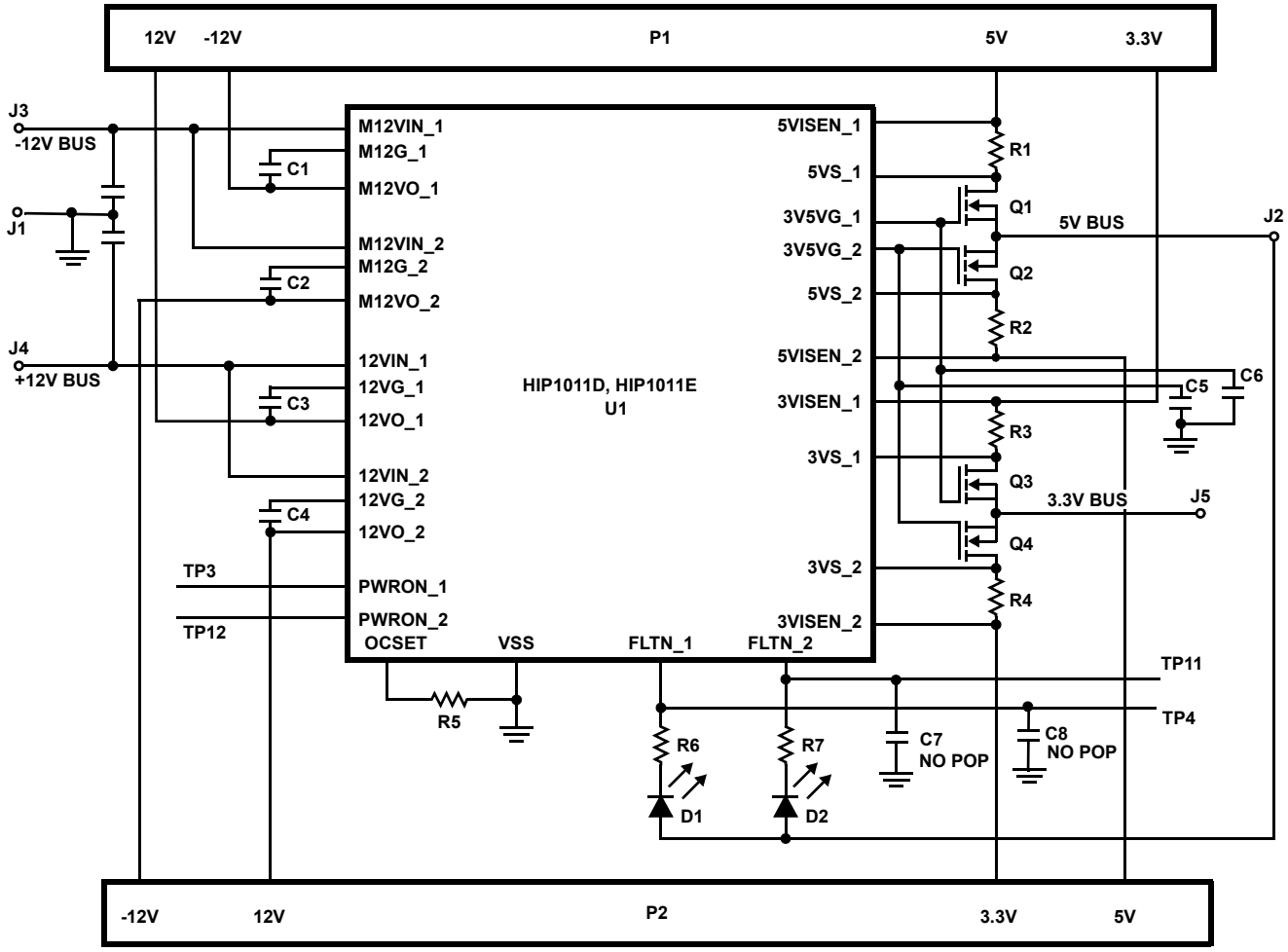


FIGURE 24.

TABLE 4. HIP1011DEVAL1 BOARD COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
U1	HIP1011DCB or HIP1011ECB Dual PCI HotPlug Controller	Intersil, HIP1011DCB or HIP1011ECB Dual PCI HotPlug Controller
Q1, Q2, Q3, Q4	HUF76132SK8 (or equivalent)	HUF76132SK8 (or equivalent), 11.5mΩ, 30V, 11.5A Logic Level N-Channel MOSFET
R1 - R4	Sense Resistor for 3.3V and 5V Supplies	Dale, WSL-2512 5mΩ Metal Strip Resistor
C1 - C6	Gate Timing Capacitors	0.033µF 805 Chip Capacitor
R5	Overcurrent Set Resistor	6kΩ 805 Chip Resistor
C7, C8 (Not Provided)	Latch-Off Delay Capacitors	Place provided for 805 Chip Cap
R6, R7	LED Series Resistors	470Ω 805 Chip Resistors
D1, D2	Fault Indicating LED	Green SMD LED
TP1 - TP28	Test Point for Corresponding Device Pin Number	
P1, P2	Connectors for Load Cards	Sullins EZM06DRXH

TABLE 4. HIP1011DEVAL1 BOARD COMPONENT LISTING (Continued)

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
RL1	3.3V Load Board Resistor	1.1Ω, 10W
RL2	5.0V Load Board Resistor	2.5Ω, 10W
RL3	+12V Load Board Resistor	47Ω, 5W
RL4	-12V Load Board Resistor	240Ω, 2W
CL1, CL2	+3.3V and +5.0V Load Board Capacitors	2200μF
CL3, CL4	+12V and -12V Load Board Capacitors	100μF

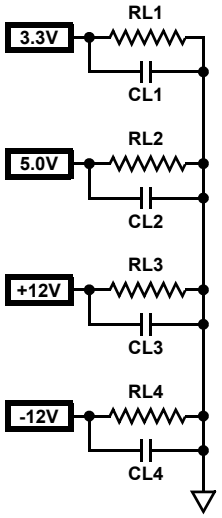
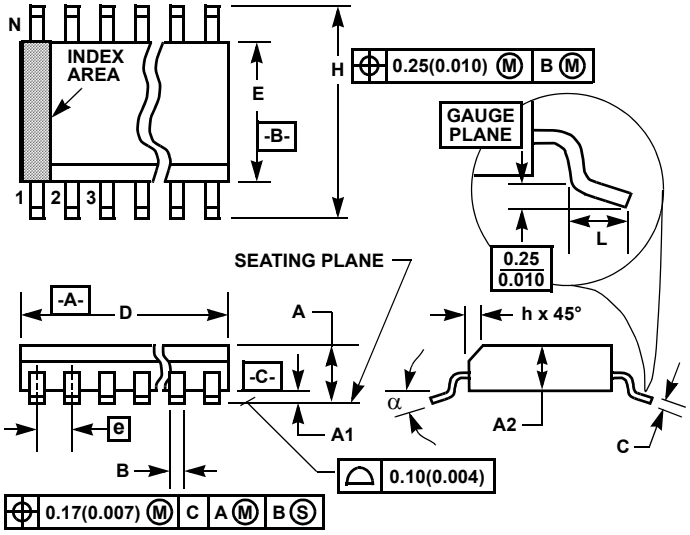


FIGURE 25. LOAD BOARD (2x)

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M28.15

28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 1 6/04

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