



Second Generation Intel® Xeon® Scalable Processors

Datasheet, Volume One: Electrical

April 2019



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Revision History

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§



1 Introduction

The Datasheet Volume 1 provides configuration space registers (CSRs).

This document is distributed as a part of the complete datasheets consisting of two volumes.

Note: Unless specified otherwise, “processor” will represent the following processors throughout the rest of the document.

- Intel® Xeon® Bronze 3XXX processor
- Intel® Xeon® Gold 6XXF processor
- Intel® Xeon® Platinum 6XXF processor
- Intel® Xeon® Platinum 8XXF processor
- Intel® Xeon® Silver 4XXX processor
- Intel® Xeon® Gold 5XXX processor
- Intel® Xeon® Platinum 6XXX processor
- Intel® Xeon® Platinum 8XXX processor

The Second Generation Intel® Xeon® Scalable Processors is the next generation of 64-bit, multi-core server processor built on 14-nm process technology. The processor supports up to 46 bits of physical address space and 48 bits of virtual address space. The processor is designed for a platform consisting of at least one Second Generation Intel® Xeon® Scalable Processors and the Platform Controller Hub (PCH). Included in this family of processors are integrated memory controller (IMC) and an Integrated I/O (IIO) on a single silicon die.

Note: Features within this document may not be available on all platform segments, processor types, and processor SKUs.

For supported processor configurations refer to:

- Second Generation Intel® Xeon® Scalable Processors Datasheet: Volume 2 - Registers, 338846

1.1 Electrical Specification Introduction

This volume provides DC electrical specifications, signal integrity, differential signaling specifications, and land and signal definitions of the processor.

This document may be used by system test engineers, board designers, and BIOS developers.



1.2 Related Publications

See the following documents for additional information.

Table 1-1. Related Publications

| Document | Document Number / Location |
|--|---|
| <ul style="list-style-type: none"> Second Generation Intel® Xeon® Scalable Processors Datasheet: Volume 2 - Registers | 338846 |
| <ul style="list-style-type: none"> Second Generation Intel® Xeon® Scalable Processors Specification Update | 338848 |
| <ul style="list-style-type: none"> Second Generation Intel® Xeon® Scalable Processors Thermal Mechanical Design Guidelines | 338847 |
| <ul style="list-style-type: none"> Intel® C620 Series Chipset Datasheet | 336067 |
| <ul style="list-style-type: none"> Intel® C620 Series Chipset Thermal Mechanical Design Guidelines | 336068 |
| <i>Intel® 64 and IA-32 Architectures Software Developer's Manuals</i> Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide Intel® 64 and IA-32 Architectures Optimization Reference Manual | 325462 http://www.intel.com/products/processor/manuals/index.htm |
| <i>Intel® Virtualization Technology Specification for Directed I/O Architecture Specification</i> | http://www.intel.com/content/www/us/en/intelligent-systems/intel-technology/vt-directed-io-spec.html |
| <i>Intel® Trusted Execution Technology Software Development Guide</i> | http://www.intel.com/technology/security/ |

1.3 Terminology

| Term | Description |
|-------|--|
| ASPM | Active State Power Management |
| BMC | Baseboard Management Controller |
| CA | Coherency Agent. In some cases this is referred to as a Caching Agent though a CA is not actually required to have a cache. It is a term used for the internal logic providing mesh interface to LLC and Core. |
| CHA | The functional module that includes the CA (Coherency Agent) and HA (Home Agent). |
| DDR4 | Fourth generation Double Data Rate SDRAM memory technology. |
| DDR-T | DDR-T (transactional) protocol which enables Apache Pass. Communication to far memory protocol running on the DDR4 physical layer. |
| DMA | Direct Memory Access |
| DMI3 | Direct Media Interface Gen3 operating at PCI Express 3.0 speed. |
| DTLB | Data Translation Look-aside Buffer; part of the processor core architecture. |



| Term | Description |
|--|--|
| DTS | Digital Thermal Sensor |
| ECC | Error Correction Code |
| Enhanced Intel SpeedStep®Technology | Allows the operating system to reduce power consumption when performance is not needed. |
| Execute Disable Bit | The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the <i>Intel® 64 and IA-32 Architectures Software Developer's Manuals</i> for more detailed information. |
| FLIT | Flow Control Unit. The Intel® Ultra Path Interconnect (Intel® UPI) Link layer's unit of transfer. A FLIT is made of multiple PHITS. A Flit is always a fixed amount of information (192 bits). |
| Functional Operation | Refers to the normal operating conditions in which all processor specifications, including DC, system bus, signal quality, mechanical, and thermal, are satisfied. |
| GSSE | Extension of the SSE/SSE2 (Streaming SIMD Extensions) floating point instruction set to 256b operands. |
| HA | A Home Agent (HA) orders read and write requests to a piece of coherent memory. The HA is implemented in the CHA logic. |
| ICU | Instruction Cache Unit. Part of the processor core architecture. |
| IFU | Instruction Fetch Unit. Part of the processor core. |
| IIO | Integrated I/O Controller. An I/O controller that is integrated in the processor die. The IIO consists of the DMI3 module, PCIe modules, and MCP modules (Intel Xeon processor-F SKUs only). |
| IMC | Integrated Memory Controller. A Memory Controller that is integrated in the processor die. |
| IQ | Instruction Queue. Part of the core architecture. |
| Intel® ME | Intel® Management Engine |
| Intel® QuickData Technology | Intel® QuickData Technology is a platform solution designed to maximize the throughput of server data traffic across a broader range of configurations and server environments to achieve faster, scalable, and more reliable I/O. |
| Intel® Ultra Path Interconnect (Intel® UPI) | A cache-coherent, link-based Interconnect specification for Intel processors. Also known as Intel® UPI. |
| Intel® 64Technology | 64-bit memory extensions to the IA-32 architecture. Further details on Intel 64 architecture and programming model can be found at http://developer.intel.com/technology/intel64/ . |
| Intel® Turbo Boost Technology | A feature that opportunistically enables the processor to run a faster frequency. This results in increased performance of both single and multi-threaded applications. |
| Intel® TXT | Intel® Trusted Execution Technology |
| Intel® Virtualization Technology (Intel® VT) | Processor Virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform. |
| Intel® VT-d | Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device Virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d. |



| Term | Description |
|--------------------------------|--|
| Integrated Heat Spreader (IHS) | A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface. |
| IOV | I/O Virtualization |
| IVR | Integrated Voltage Regulation (IVR): The processor supports several integrated voltage regulators. |
| Intel UPI | Intel® Ultra Path Interconnect (Intel® UPI) Agent. An internal logic block providing interface between internal mesh and external Intel® UPI. |
| LLC | Last Level Cache |
| LRDIMM | Load Reduced Dual In-line Memory Module |
| LRU | Least Recently Used. A term used in conjunction with cache allocation policy. |
| M2M | Mesh to Memory. Logic in the IMC which interfaces the IMC to the mesh. |
| M2PCIE | The logic in the IIO modules which interface the modules to the mesh. |
| MESH | The on die interconnect which connects modules in the processor. |
| MESI | Modified/Exclusive/Shared/Invalid. States used in conjunction with cache coherency |
| MLC | Mid Level Cache |
| NCTF | Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality. |
| NID \ NodeID | Node ID (NID) or NodeID (NID). The processor implements up to 4-bits of NodeID (NID). |
| Pcode | Pcode is microcode which is run on the dedicated microcontroller within the PCU. |
| PCH | Platform Controller Hub. The next generation chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features. |
| PCU | Power Control Unit. |
| PCI Express 3.0 | The third generation PCI Express specification that operates at twice the speed of PCI Express 2.0 (8 Gb/s); PCI Express 3.0 is completely backward compatible with PCI Express 1.0 and 2.0. |
| PCI Express 2.0 | PCI Express* Generation 2.0 |
| PECI | Platform Environment Control Interface |
| Phit | The data transfer unit on Intel® UPI at the Physical layer is called a phit (physical unit). A Phit will be either 20 bits, or 8 bits depending on the number of active lanes. |
| Processor | Includes the 64-bit cores, uncore, I/Os and package |
| Processor Core | The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache and data cache and MLC cache. All execution cores share the L3 cache. |
| Rank | A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DDR4 DIMM. |



| Term | Description |
|--------------------------------|---|
| RDIMM \ LRDIMM | Registered Dual In-line Memory Module \ Load Reduced DIMM |
| RTID | Request Transaction IDs are credits issued by the CHA to track outstanding transaction, and the RTIDs allocated to a CHA are topology dependent. |
| SCI | System Control Interrupt. Used in ACPI protocol. |
| SKU | Stock Keeping Unit (SKU) is a subset of a processor type with specific features, electrical, power and thermal specifications. Not all features are supported on all SKUs. A SKU is based on specific use condition assumption. |
| SSE | Intel® Streaming SIMD Extensions (Intel®SSE) |
| SMBus | System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. |
| Storage Conditions | A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material. |
| TAC | Thermal Averaging Constant |
| TDP | Thermal Design Power |
| TSOD | Temperature Sensor On DIMM |
| UDIMM | Unbuffered Dual In-line Memory Module |
| Uncore | The portion of the processor comprising the shared LLC cache, CHA, IMC, PCU, Ubox, IIO and Intel® UPI modules. |
| Unit Interval | Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances $t_1, t_2, t_n, \dots, t_n$ then the UI at instance "n" is defined as: $UI_n = t_n - t_{n-1}$ |
| Volume Management Device (VMD) | Volume Management Device (VMD) is a new technology used to improve PCIe management. VMD maps the PCIe configuration space for child devices/adapters for a particular PCIe x16 module into its own address space, controlled by a VMD driver. |
| VCCIN | Primary voltage input to the voltage regulators integrated into the processor. |
| VSS | Processor ground |
| VSSA | System agent supply for Intel UPI and PCIe |
| VCCIO | IO voltage supply input |
| VCCD | DDR power rail |
| x1, x4, x8, x16 | Refers to a Link or Port with one, two, four or eight Physical Lane(s) |

1.4 Statement of Volatility (SOV)

Second Generation Intel® Xeon® Scalable Processors do not retain any end-user data when powered down and/or the processor is physically removed from the socket.







2 Electrical Specifications

This chapter describes processor signaling, DC and AC specifications, and signal quality. References to various interfaces (memory, PCIe*, Intel® Ultra Path Interconnect [Intel® UPI], PECEI, and so forth) are also described.

2.1 Integrated Voltage Regulation

The platform voltage regulator is integrated into the processor. Due to this integration, the processor has one main voltage rail (V_{CCIN}) and a voltage rail for the memory interface (V_{CCD012} , V_{CCD345} - one for each memory channel pair). The V_{CCIN} voltage rail will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the cores, cache, and system agents. This integration allows the processor to better control on-die voltages to optimize for both performance and power savings. The processor V_{CCIN} rail will remain a VID -based voltage with a loadline similar to the core voltage rail (called V_{CC}) in previous processors. In addition to the above, the processor has voltage rails V_{CCIO} for IO, V_{CCSA} for the System Agent, and V_{CC33} for PIROM.

2.2 Processor Signaling

The Second Generation Intel® Xeon® Scalable Processors includes 3647 lands, which use various signaling technologies. Signals are grouped by electrical characteristics and buffer type into various signal groups. These include DDR4 (Reference Clock, Command, Control, and Data), PCI Express*, DMI3, Intel® Ultra Path Interconnect (Intel® UPI), Platform Environmental Control Interface (PECEI), System Reference Clock, SMBus, JTAG and Test Access Port (TAP), SVID Interface, Processor Asynchronous Sideband, Miscellaneous, and Power/ Other signals. See [Table 2-7, "Signal Groups"](#) for details.

Intel strongly recommends performing analog simulations of all interfaces. Please refer to [Section 1.2](#) for signal integrity model availability.

2.2.1 System Memory Interface Signal Groups

The system memory interface utilizes DDR4 technology, which consists of numerous signal groups. These include: Reference Clocks, Command Signals, Control Signals, and Data Signals. Each group consists of numerous signals, which may utilize various signaling technologies. See [Table 2-7, "Signal Groups"](#) for further details.

Throughout this chapter the system memory interface may be referred to as DDR4.

2.2.2 PCI Express* Signals

The PCI Express Signal Group consists of PCI Express* ports 1, 2, and 3, and PCI Express miscellaneous signals. See [Table 2-7, "Signal Groups"](#) for further details.



2.2.3 DMI3/PCI Express Signals

The Direct Media Interface Gen 3(DMI3) sends and receives packets and/or commands to the PCH. The DMI3 is an extension of the standard PCI Express Specification. The DMI3/PCI Express Signals consist of DMI3 receive and transmit input/output signals and a control signal to select DMI3 or PCIe* 3.0 operation for port 0. See [Table 2-7, "Signal Groups"](#) for further details.

2.2.4 Intel® Ultra Path Interconnect (Intel® UPI)

Second Generation Intel® Xeon® Scalable Processors two socket provides two Intel® Ultra Path Interconnect (Intel® UPI) ports for high-speed serial transfer between other processors, whereas the Second Generation Intel® Xeon® Scalable Processors four socket and above provides three Intel® UPI links. Each port consists of two uni-directional links (for transmit and receive). A differential signaling scheme is utilized, which consists of opposite-polarity (DP, DN) signal pairs. See [Table 2-7, "Signal Groups"](#) for further details.

2.2.5 Platform Environmental Control Interface (PECI)

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external system management logic and thermal monitoring devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics.

The PECI interface operates at a nominal voltage. The set of DC electrical specifications shown in [Section 2.8.3.2, "PECI DC Specifications"](#) is used with devices normally operating from a PECI interface supply.

2.2.5.1 Input Device Hysteresis

The PECI client and host input buffers must use a Schmitt-triggered input design for improved noise immunity. Please refer to the following image and [Section 2.8.3.2, "PECI DC Specifications."](#)

Figure 2-1. Input Device Hysteresis





2.2.6 System Reference Clocks (BCLK{0/1/2}_DP, BCLK{0/1/2}_DN)

The processor Core, processor Uncore, Intel® UPI, PCI Express* and DDR4 memory interface frequencies are generated from BCLK{0/1/2}_DP and BCLK{0/1/2}_DN signals. There is no direct link between core frequency and Intel UPI link frequency (e.g., no core frequency to Intel® UPI multiplier). The processor maximum core frequency, Intel® UPI link frequency and DDR memory frequency are set during manufacturing. It is possible to override the processor core frequency setting using software. This permits operation at lower core frequencies than the factory set maximum core frequency.

The processor core frequency is configured during reset by using values stored within the device during manufacturing. The stored value sets the lowest core multiplier at which the particular processor can operate. If higher speeds are desired, the appropriate ratio can be configured via the IA32_PERF_CTL MSR (MSR 199h); Bits [14:0]. For details of operation at core frequencies lower than the maximum rated processor speed.

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK{0/1/2}_DP, BCLK{0/1/2}_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK{0/1/2}_DP, BCLK{0/1/2}_DN inputs are provided in [Section 2.8.3.7, "Processor Asynchronous Sideband DC Specifications."](#)

These specifications must be met while also meeting the associated signal quality specifications outlined in [Section 2.10, "Signal Quality."](#)

Details regarding BCLK{0/1/2}_DP, BCLK{0/1/2}_DN driver specifications are provided in the CK420BQ Clock Synthesizer/Driver Specification.

2.2.7 JTAG and Test Access Port (TAP) Signals

Due to the voltage levels supported by other components in the JTAG and Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. Please refer to the *Second Generation Intel® Xeon® Scalable Processors Boundary Scan Description Language (BSDL)* file more details. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

2.2.8 Processor Sideband Signals

Second Generation Intel® Xeon® Scalable Processors includes asynchronous sideband signals that provide asynchronous input, output or I/O signals between the processor and the platform or Platform Controller Hub. Details can be found in [Table 2-7](#).

All Processor Asynchronous Sideband input signals are required to be asserted/deasserted for a defined number of BCLKs in order for the processor to recognize the proper signal state, these are outlined in [Section 2.8.3.7, "Processor Asynchronous Sideband DC Specifications"](#). Refer to [Section 2.10, "Signal Quality"](#) for applicable signal integrity specifications.



2.2.9 Power, Ground and Sense Signals

Processors also include various other signals including power/ground and sense points. Details can be found in [Table 2-7, "Signal Groups."](#)

2.2.9.1 Power and Ground Lands

All V_{CCD}, V_{CCIN}, and V_{CCSA}, and V_{CC33} lands must be connected to their respective processor power planes, while all V_{SS} lands must be connected to the system ground plane. Refer to the PDG for decoupling, voltage plane and routing guidelines for each power supply voltage.

For clean on-chip power distribution, processors include lands for all required voltage supplies. These are listed in the following table.

Table 2-1. Power and Ground Lands

| Power and Ground Lands | Comments |
|--|---|
| CD_VCC_CORE, CD_VPP CD_VCC_IN, CD_VCCP, | Power supplies for Second Generation Intel® Xeon® Scalable Processors-F SKU |
| V _{CCIN} | Each V _{CCIN} land must be supplied with the voltage determined by the SVID Bus signals. VR 13.0 defines the voltage level associated with each core SVID pattern. |
| V _{CCD012} V _{CCD345} | Each V _{CCD} land is connected to a switchable 1.20 V supply, provide power to the processor DDR4 interface. V _{CCD} is also controlled by the SVID Bus. V _{CCD} is the generic term for V _{CCD012} and V _{CCD345} . |
| V _{CCSA} | IO voltage supply input |
| V _{CC33} | Power supply for PIROM. |
| V _{SS} | Ground |
| V _{CCIO} | IO voltage supply input |

2.2.9.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Large electrolytic bulk capacitors (CBULK), help maintain the output voltage during current transients, for example coming out of an idle condition. Care must be taken in the baseboard design to ensure that the voltages provided to the processor remain within the specifications listed in [Table 2-13, "Voltage Specification."](#) Failure to do so can result in timing violations or reduced lifetime of the processor.

2.2.9.3 Voltage Identification (VID)

The Voltage Identification (VID) specification for the V_{CCIN}, V_{SA}, CD_VCC_CORE voltage is defined by the VR13.0 PWM: Server VR Vendor PWM Enabling Specification. The reference voltage or the VID setting is set via the SVID communication bus between the processor and the voltage regulator controller chip. The VID settings are the nominal voltages to be delivered to the processor's lands. The VR 13.0 Reference Code Voltage Identification Table specifies the reference voltage level corresponding to the VID value transmitted over serial VID. The VID codes will change due to temperature and/or current load changes in order to minimize the power and to maximize the performance of the part. The specifications are set so that a voltage regulator can operate with all supported frequencies.



Individual processor VID values may be calibrated during manufacturing such that two processor units with the same core frequency may have different default VID settings.

The processor uses voltage identification signals to support automatic selection of a power supply voltage. If the processor socket is empty (SKTOCC_N high), or a “not supported” response is received from the SVID bus, then the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself or not power on. Vout MAX register (30h) is programmed by the processor to set the maximum supported VID code and if the programmed VID code is higher than the VID supported by the VR, then VR will respond with a “not supported” acknowledgment. See the VR13.0 PWM: Server VR Vendor PWM Enabling Specification for further details.

2.2.9.4 SVID Commands

The processor provides the ability to operate while transitioning to a new VID setting and its associated processor voltage rail. This is represented by a DC shift. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target voltage. Transitions above the maximum specified VID are not supported. The processor supports the following VR commands:

- SetVID_Fast (25 mV/μs for VCCIN, 10mV for VSA,VCCIO and CD_VCC_CORE)
- SetVID_Slow is 1/4 of SetVID_Fast
- SetVID_Decay (downward voltage only and it's a function of the output capacitance's time constant) commands. The VR 13.0 Reference Code Voltage Identification Table includes SVID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in [Table 2-13, “Voltage Specification.”](#) This is a CSR configuration option.

The VRM or EVRD utilized must be capable of regulating its output to the value defined by the new VID. The VR13.0 PWM: Server VR Vendor PWM Enabling Specification contains further details.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

2.2.9.5 SetWP Working Point Command

The SetWP is a command that invokes a look up table for VID set points. During the initial power on phase the CPU will program the WPx registers (WP0=3Ah..WP7=41h) on a per rail address basis. When use with the AllCall address, SetWP acts as a group command that moves all voltage rails on the bus to new voltages in the look up table index. The SetWP command can also be used with an individual VR rail address and that rail moves to the voltage in the loop up table index. Each VR domain address has registers WP0-WPx (3Ah..41h) which stores the VID code for that domain's work points.

The Work Point command is encoded to support up to 8 VID targets, slew rate for the command, and alert function. The PWM should use its auto power state or auto-phase shedding functions to select appropriate # phases, CCM/DCM operation, and so forth. based on output load current after the SetWP command target has been reached.

Typical SetWP usage will be:

1. Processor writes VID codes to WP registers WP0 (3Ah) -WP4 (3Dh) in each VR domain. Normally done during SVID enumeration phase of system boot.



2. If a WP0-7 register is not programmed by the CPU, the VR stays at its present VID setting when it receives a SetWP (WPn) command.
3. Processor sends SetWP (WPn) command to one of the AllCall addresses 0Eh or 0Fh. See PWM guideline for more information on AllCall address mapping.
4. Voltage rails change VID to their corresponding VID code stored in their WPx register
5. CPU polls each VR addresses reading stutus1 to clear the alerts from the VRs
6. SVID error handling

WP0 = State 0, programed by master

WP1 = State 1, programmed by master

WP2 = State 2, programmed by master

WP3 = State 3, programmed by master

WP4 = State 4, programmed by master

...

WP7 = State 7

2.2.9.6 SetVID Fast Command

The SetVID_Fast command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a fast slew rate as defined in the slew rate data register. It is minimum of 25 mV/μs for VCCIN and 10 mV/μs for other rails, depending on the amount of decoupling capacitance.

The SetVID_Fast command is preemptive. The VR interrupts its current processes and moves to the new VID. The SetVID_Fast command operates on 1 VR address at a time. This command is used in the processor for package C6 fast exit.

2.2.9.7 SetVID Slow

The SetVID_Slow command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a "slow" slew rate as defined in the slow slew rate data register. The SetVID_Slow is nominally 4x slower than the SetVID_Fast slew rate.

The SetVID_Slow command is preemptive, the VR interrupts its current processes and moves to the new VID. This is the instruction used for normal P-state voltage change. This command is used in the processor for the Intel Enhanced SpeedStep® Technology transitions.

2.2.9.8 SetVID Decay

The SetVID_Decay command is the slowest of the DVID transitions. It is only used for VID down transitions. The VR does not control the slew rate, the output voltage declines with the output load current only.

The SetVID_Decay command is preemptive, the VR interrupts its current processes and moves to the new VID. This command is used in the processor for package C6 entry, allowing capacitor discharge by the leakage, thus saving energy. This command is only used in VID down direction in the processor package C6 entry.



2.2.9.9 SVID Voltage Rail Addressing

The processor addresses 4 different voltage rail control segments within VR13.0 (VCCIN, VCCD, VCCSA, VCCIO and CD_VCC_CORE). The SVID data packet contains a 4-bit addressing code:

Table 2-2. SVID Address Usage Bus 1

| PWM Address (HEX) | Protocol ID | Second Generation Intel® Xeon® Scalable |
|-------------------|----------------|---|
| 00 | 04H(10 mV VID) | VCCIN |
| 01 | 07H(5 mV VID) | VCCSA |
| 02 | 07H(5 mV VID) | VCCIO |
| 03 | 07H(5 mV VID) | CD_VCC_CORE |
| 04 | | Reserved for optional rail |
| 05 | | Reserved for optional rail |

Notes:

1. Check with VR vendors for determining the physical address assignment method for their controllers.
2. VR addressing is assigned on a per voltage rail basis.
3. Dual VR controllers will have two addresses with the lowest order address, always being the higher phase count.
4. For future platform flexibility, the VR controller should include an address offset, as shown with +1 not used.

Table 2-3. SVID Address Usage Bus 2

| PWM Address (HEX) | Protocol ID | Second Generation Intel® Xeon® Scalable |
|-------------------|----------------------------------|---|
| 00 | 04H(10mV VID) or 07H(5mV VID) | VCCD012 |
| 01 | | NA |
| 02 | 04H(10mV VID) or 07H(5mV VID) | VCCD345 |
| 03 | | NA |

Notes:

1. Check with VR vendors for determining the physical address assignment method for their controllers.
2. VR addressing is assigned on a per voltage rail basis.
3. Dual VR controllers will have two addresses with the lowest order address, always being the higher phase count.

Table 2-4. VR13.0 Reference Code VCCIN Voltage Identification (VID) (Sheet 1 of 2)

| HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN |
|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|
| 00 | 0.00 | 20 | 0.81 | 40 | 1.13 | 60 | 1.45 | 80 | 1.77 | A0 | 2.09 | C0 | 2.41 | E0 | 2.73 |
| 01 | 0.50 | 21 | 0.82 | 41 | 1.14 | 61 | 1.46 | 81 | 1.78 | A1 | 2.10 | C1 | 2.42 | E1 | 2.74 |
| 02 | 0.51 | 22 | 0.83 | 42 | 1.15 | 62 | 1.47 | 82 | 1.79 | A2 | 2.11 | C2 | 2.43 | E2 | 2.75 |
| 03 | 0.52 | 23 | 0.84 | 43 | 1.16 | 63 | 1.48 | 83 | 1.80 | A3 | 2.12 | C3 | 2.44 | E3 | 2.76 |
| 04 | 0.53 | 24 | 0.85 | 44 | 1.17 | 64 | 1.49 | 84 | 1.81 | A4 | 2.13 | C4 | 2.45 | E4 | 2.77 |
| 05 | 0.54 | 25 | 0.86 | 45 | 1.18 | 65 | 1.50 | 85 | 1.82 | A5 | 2.14 | C5 | 2.46 | E5 | 2.78 |
| 06 | 0.55 | 26 | 0.87 | 46 | 1.19 | 66 | 1.51 | 86 | 1.83 | A6 | 2.15 | C6 | 2.47 | E6 | 2.79 |
| 07 | 0.56 | 27 | 0.88 | 47 | 1.20 | 67 | 1.52 | 87 | 1.84 | A7 | 2.16 | C7 | 2.48 | E7 | 2.80 |
| 08 | 0.57 | 28 | 0.89 | 48 | 1.21 | 68 | 1.53 | 88 | 1.85 | A8 | 2.17 | C8 | 2.49 | E8 | 2.81 |
| 09 | 0.58 | 29 | 0.90 | 49 | 1.22 | 69 | 1.54 | 89 | 1.86 | A9 | 2.18 | C9 | 2.50 | E9 | 2.82 |
| 0A | 0.59 | 2A | 0.91 | 4A | 1.23 | 6A | 1.55 | 8A | 1.87 | AA | 2.19 | CA | 2.51 | EA | 2.83 |



Table 2-4. VR13.0 Reference Code VCCIN Voltage Identification (VID) (Sheet 2 of 2)

| HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN | HEX | VCCIN |
|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|
| 0B | 0.60 | 2B | 0.92 | 4B | 1.24 | 6B | 1.56 | 8B | 1.88 | AB | 2.20 | CB | 2.52 | EB | 2.84 |
| 0C | 0.61 | 2C | 0.93 | 4C | 1.25 | 6C | 1.57 | 8C | 1.89 | AC | 2.21 | CC | 2.53 | EC | 2.85 |
| 0D | 0.62 | 2D | 0.94 | 4D | 1.26 | 6D | 1.58 | 8D | 1.90 | AD | 2.22 | CD | 2.54 | ED | 2.86 |
| 0E | 0.63 | 2E | 0.95 | 4E | 1.27 | 6E | 1.59 | 8E | 1.91 | AE | 2.23 | CE | 2.55 | EE | 2.87 |
| 0F | 0.64 | 2F | 0.96 | 4F | 1.28 | 6F | 1.60 | 8F | 1.92 | AF | 2.24 | CF | 2.56 | EF | 2.88 |
| 10 | 0.65 | 30 | 0.97 | 50 | 1.29 | 70 | 1.61 | 90 | 1.93 | B0 | 2.25 | D0 | 2.57 | F0 | 2.89 |
| 11 | 0.66 | 31 | 0.98 | 51 | 1.30 | 71 | 1.62 | 91 | 1.94 | B1 | 2.26 | D1 | 2.58 | F1 | 2.90 |
| 12 | 0.67 | 32 | 0.98 | 52 | 1.31 | 72 | 1.63 | 92 | 1.95 | B2 | 2.27 | D2 | 2.59 | F2 | 2.91 |
| 13 | 0.68 | 33 | 1.00 | 53 | 1.32 | 73 | 1.64 | 93 | 1.96 | B3 | 2.28 | D3 | 2.60 | F3 | 2.92 |
| 14 | 0.69 | 34 | 1.01 | 54 | 1.33 | 74 | 1.65 | 94 | 1.97 | B4 | 2.29 | D4 | 2.61 | F4 | 2.93 |
| 15 | 0.70 | 35 | 1.02 | 55 | 1.34 | 75 | 1.66 | 95 | 1.98 | B5 | 2.30 | D5 | 2.62 | F5 | 2.94 |
| 16 | 0.71 | 36 | 1.03 | 56 | 1.35 | 76 | 1.67 | 96 | 1.99 | B6 | 2.31 | D6 | 2.63 | F6 | 2.95 |
| 17 | 0.72 | 37 | 1.04 | 57 | 1.36 | 77 | 1.68 | 97 | 2.00 | B7 | 2.32 | D7 | 2.64 | F7 | 2.96 |
| 18 | 0.73 | 38 | 1.05 | 58 | 1.37 | 78 | 1.69 | 98 | 2.01 | B8 | 2.33 | D8 | 2.65 | F8 | 2.97 |
| 19 | 0.74 | 39 | 1.06 | 59 | 1.38 | 79 | 1.70 | 99 | 2.02 | B9 | 2.34 | D9 | 2.66 | F9 | 2.98 |
| 1A | 0.75 | 3A | 1.07 | 5A | 1.39 | 7A | 1.71 | 9A | 2.03 | BA | 2.35 | DA | 2.67 | FA | 2.99 |
| 1B | 0.76 | 3B | 1.08 | 5B | 1.40 | 7B | 1.72 | 9B | 2.04 | BB | 2.36 | DB | 2.68 | FB | 3.00 |
| 1C | 0.77 | 3C | 1.09 | 5C | 1.41 | 7C | 1.73 | 9C | 2.05 | BC | 2.37 | DC | 2.69 | FC | 3.01 |
| 1D | 0.78 | 3D | 1.10 | 5D | 1.42 | 7D | 1.74 | 9D | 2.06 | BD | 2.38 | DD | 2.70 | FD | 3.02 |
| 1E | 0.79 | 3E | 1.11 | 5E | 1.43 | 7E | 1.75 | 9E | 2.07 | BE | 2.39 | DE | 2.71 | FE | 3.03 |
| 1F | 0.80 | 3F | 1.12 | 5F | 1.44 | 7F | 1.76 | 9F | 2.08 | BF | 2.40 | DF | 2.72 | FF | 3.04 |

Notes:

- 00h = Off State
- VID Range HEX 65-97 are used by the Intel® Xeon® processor E5-1600 and E5-2600 v5 product families
- VCCD can use Protocol ID of 10 mV or 5 mV.
- VCCD can use Table 2-4, "VR13.0 Reference Code VCCIN Voltage Identification (VID)" or VID Table 2-5, "VSA, VCCIO, CD_VCC_CORE or VCCD VID Table."

Table 2-5. VSA, VCCIO, CD_VCC_CORE or VCCD VID Table (Sheet 1 of 8)

| HEX | 5 mV step mode voltage | 5 mV step recommended accuracy | 10 mV step mode voltage | 10 mV step mode recommended accuracy | 10 mV mode market segment |
|-----|------------------------|--------------------------------|-------------------------|--------------------------------------|---------------------------|
| 0 0 | 0 | NA | 0 | NA | All |
| 0 1 | 0.25 | ±8 mV | 0.5 | ±10 mV | All |
| 0 2 | 0.255 | ±8 mV | 0.51 | ±10 mV | All |
| 0 3 | 0.26 | ±8 mV | 0.52 | ±10 mV | All |
| 0 4 | 0.265 | ±8 mV | 0.53 | ±10 mV | All |
| 0 5 | 0.27 | ±8 mV | 0.54 | ±10 mV | All |
| 0 6 | 0.275 | ±8 mV | 0.55 | ±10 mV | All |
| 0 7 | 0.28 | ±8 mV | 0.56 | ±10 mV | All |
| 0 8 | 0.285 | ±8 mV | 0.57 | ±10 mV | All |
| 0 9 | 0.29 | ±8 mV | 0.58 | ±10 mV | All |
| 0 A | 0.295 | ±8 mV | 0.59 | ±10 mV | All |
| 0 B | 0.3 | ±8 mV | 0.6 | ±10 mV | All |
| 0 C | 0.305 | ±8 mV | 0.61 | ±10 mV | All |



Table 2-5. VSA, VCCIO, CD_VCC_CORE or VCCD VID Table (Sheet 2 of 8)

| HEX | 5 mV step mode voltage | 5 mV step recommended accuracy | 10 mV step mode voltage | 10 mV step mode recommended accuracy | 10 mV mode market segment |
|-----|------------------------|--------------------------------|-------------------------|--------------------------------------|---------------------------|
| 0 D | 0.31 | ±8 mV | 0.62 | ±10 mV | All |
| 0 E | 0.315 | ±8 mV | 0.63 | ±10 mV | All |
| 0 F | 0.32 | ±8 mV | 0.64 | ±10 mV | All |
| 1 0 | 0.325 | ±8 mV | 0.65 | ±10 mV | All |
| 1 1 | 0.33 | ±8 mV | 0.66 | ±10 mV | All |
| 1 2 | 0.335 | ±8 mV | 0.67 | ±10 mV | All |
| 1 3 | 0.34 | ±8 mV | 0.68 | ±10 mV | All |
| 1 4 | 0.345 | ±8 mV | 0.69 | ±10 mV | All |
| 1 5 | 0.35 | ±8 mV | 0.7 | ±10 mV | All |
| 1 6 | 0.355 | ±8 mV | 0.71 | ±10 mV | All |
| 1 7 | 0.36 | ±8 mV | 0.72 | ±10 mV | All |
| 1 8 | 0.365 | ±8 mV | 0.73 | ±10 mV | All |
| 1 9 | 0.37 | ±8 mV | 0.74 | ±10 mV | All |
| 1 A | 0.375 | ±8 mV | 0.75 | ±10 mV | All |
| 1 B | 0.38 | ±8 mV | 0.76 | ±10 mV | All |
| 1 C | 0.385 | ±8 mV | 0.77 | ±10 mV | All |
| 1 D | 0.39 | ±8 mV | 0.78 | ±10 mV | All |
| 1 E | 0.395 | ±8 mV | 0.79 | ±10 mV | All |
| 1 F | 0.4 | ±8 mV | 0.8 | ±10 mV | All |
| 2 0 | 0.405 | ±8 mV | 0.81 | ±10 mV | All |
| 2 1 | 0.41 | ±8 mV | 0.82 | ±10 mV | All |
| 2 2 | 0.415 | ±8 mV | 0.83 | ±10 mV | All |
| 2 3 | 0.42 | ±8 mV | 0.84 | ±10 mV | All |
| 2 4 | 0.425 | ±8 mV | 0.85 | ±10 mV | All |
| 2 5 | 0.43 | ±8 mV | 0.86 | ±10 mV | All |
| 2 6 | 0.435 | ±8 mV | 0.87 | ±10 mV | All |
| 2 7 | 0.44 | ±8 mV | 0.88 | ±10 mV | All |
| 2 8 | 0.445 | ±8 mV | 0.89 | ±10 mV | All |
| 2 9 | 0.45 | ±8 mV | 0.9 | ±10 mV | All |
| 2 A | 0.455 | ±8 mV | 0.91 | ±10 mV | All |
| 2 B | 0.46 | ±8 mV | 0.92 | ±10 mV | All |
| 2 C | 0.465 | ±8 mV | 0.93 | ±10 mV | All |
| 2 D | 0.47 | ±8 mV | 0.94 | ±10 mV | All |
| 2 E | 0.475 | ±8 mV | 0.95 | ±10 mV | All |
| 2 F | 0.48 | ±8 mV | 0.96 | ±10 mV | All |
| 3 0 | 0.485 | ±8 mV | 0.97 | ±10 mV | All |
| 3 1 | 0.49 | ±8 mV | 0.98 | ±10 mV | All |
| 3 2 | 0.495 | ±8 mV | 0.99 | ±10 mV | All |



Table 2-5. VSA, VCCIO, CD_VCC_CORE or VCCD VID Table (Sheet 3 of 8)

| HEX | 5 mV step mode voltage | 5 mV step recommended accuracy | 10 mV step mode voltage | 10 mV step mode recommended accuracy | 10 mV mode market segment |
|-----|------------------------|--------------------------------|-------------------------|--------------------------------------|---------------------------|
| 3 3 | 0.5 | ±8 mV | 1 | ±8 mV | All |
| 3 4 | 0.505 | ±8 mV | 1.01 | ±8 mV | All |
| 3 5 | 0.51 | ±8 mV | 1.02 | ±8 mV | All |
| 3 6 | 0.515 | ±8 mV | 1.03 | ±8 mV | All |
| 3 7 | 0.52 | ±8 mV | 1.04 | ±8 mV | All |
| 3 8 | 0.525 | ±8 mV | 1.05 | ±8 mV | All |
| 3 9 | 0.53 | ±8 mV | 1.06 | ±8 mV | All |
| 3 A | 0.535 | ±8 mV | 1.07 | ±8 mV | All |
| 3 B | 0.54 | ±8 mV | 1.08 | ±8 mV | All |
| 3 C | 0.545 | ±8 mV | 1.09 | ±8 mV | All |
| 3 D | 0.55 | ±8 mV | 1.1 | ±8 mV | All |
| 3 E | 0.555 | ±8 mV | 1.11 | ±8 mV | All |
| 3 F | 0.56 | ±8 mV | 1.12 | ±8 mV | All |
| 4 0 | 0.565 | ±8 mV | 1.13 | ±8 mV | All |
| 4 1 | 0.57 | ±8 mV | 1.14 | ±8 mV | All |
| 4 2 | 0.575 | ±8 mV | 1.15 | ±8 mV | All |
| 4 3 | 0.58 | ±8 mV | 1.16 | ±8 mV | All |
| 4 4 | 0.585 | ±8 mV | 1.17 | ±8 mV | All |
| 4 5 | 0.59 | ±8 mV | 1.18 | ±8 mV | All |
| 4 6 | 0.595 | ±8 mV | 1.19 | ±8 mV | All |
| 4 7 | 0.6 | ±8 mV | 1.2 | ±8 mV | All |
| 4 8 | 0.605 | ±8 mV | 1.21 | ±8 mV | All |
| 4 9 | 0.61 | ±8 mV | 1.22 | ±8 mV | All |
| 4 A | 0.615 | ±8 mV | 1.23 | ±8 mV | All |
| 4 B | 0.62 | ±8 mV | 1.24 | ±8 mV | All |
| 4 C | 0.625 | ±8 mV | 1.25 | ±8 mV | All |
| 4 D | 0.63 | ±8 mV | 1.26 | ±8 mV | All |
| 4 E | 0.635 | ±8 mV | 1.27 | ±8 mV | All |
| 4 F | 0.64 | ±8 mV | 1.28 | ±8 mV | All |
| 5 0 | 0.645 | ±8 mV | 1.29 | ±8 mV | All |
| 5 1 | 0.65 | ±8 mV | 1.3 | ±8 mV | All |
| 5 2 | 0.655 | ±8 mV | 1.31 | ±8 mV | All |
| 5 3 | 0.66 | ±8 mV | 1.32 | ±8 mV | All |
| 5 4 | 0.665 | ±8 mV | 1.33 | ±8 mV | All |
| 5 5 | 0.67 | ±8 mV | 1.34 | ±8 mV | All |
| 5 6 | 0.675 | ±8 mV | 1.35 | ±8 mV | All |



Table 2-5. VSA, VCCIO, CD_VCC_CORE or VCCD VID Table (Sheet 4 of 8)

| HEX | 5 mV step mode voltage | 5 mV step recommended accuracy | 10 mV step mode voltage | 10 mV step mode recommended accuracy | 10 mV mode market segment |
|-----|------------------------|--------------------------------|-------------------------|--------------------------------------|---------------------------|
| 5 7 | 0.68 | ±8 mV | 1.36 | ±8 mV | All |
| 5 8 | 0.685 | ±8 mV | 1.37 | ±8 mV | All |
| 5 9 | 0.69 | ±8 mV | 1.38 | ±8 mV | All |
| 5 A | 0.695 | ±8 mV | 1.39 | ±8 mV | All |
| 5 B | 0.7 | ±8 mV | 1.4 | ±8 mV | All |
| 5 C | 0.705 | ±8 mV | 1.41 | ±8 mV | All |
| 5 D | 0.71 | ±8 mV | 1.42 | ±8 mV | All |
| 5 E | 0.715 | ±8 mV | 1.43 | ±8 mV | All |
| 5 F | 0.72 | ±8 mV | 1.44 | ±8 mV | All |
| 6 0 | 0.725 | ±8 mV | 1.45 | ±8 mV | All |
| 6 1 | 0.73 | ±8 mV | 1.46 | ±8 mV | All |
| 6 2 | 0.735 | ±8 mV | 1.47 | ±8 mV | All |
| 6 3 | 0.74 | ±8 mV | 1.48 | ±8 mV | All |
| 6 4 | 0.745 | ±8 mV | 1.49 | ±8 mV | All |
| 6 5 | 0.75 | ±8 mV | 1.5 | ±0.5% of VID | All |
| 6 6 | 0.755 | ±8 mV | 1.51 | ±0.5% of VID | All |
| 6 7 | 0.76 | ±8 mV | 1.52 | ±0.5% of VID | All |
| 6 8 | 0.765 | ±8 mV | 1.53 | ±0.5% of VID | All |
| 6 9 | 0.77 | ±8 mV | 1.54 | ±0.5% of VID | All |
| 6 A | 0.775 | ±8 mV | 1.55 | ±0.5% of VID | All |
| 6 B | 0.78 | ±8 mV | 1.56 | ±0.5% of VID | All |
| 6 C | 0.785 | ±8 mV | 1.57 | ±0.5% of VID | All |
| 6 D | 0.79 | ±8 mV | 1.58 | ±0.5% of VID | All |
| 6 E | 0.795 | ±8 mV | 1.59 | ±0.5% of VID | All |
| 6 F | 0.8 | ±5 mV | 1.6 | ±0.5% of VID | All |
| 7 0 | 0.805 | ±5 mV | 1.61 | ±0.5% of VID | All |
| 7 1 | 0.81 | ±5 mV | 1.62 | ±0.5% of VID | All |
| 7 2 | 0.815 | ±5 mV | 1.63 | ±0.5% of VID | All |
| 7 3 | 0.82 | ±5 mV | 1.64 | ±0.5% of VID | All |
| 7 4 | 0.825 | ±5 mV | 1.65 | ±0.5% of VID | All |
| 7 5 | 0.83 | ±5 mV | 1.66 | ±0.5% of VID | All |
| 7 6 | 0.835 | ±5 mV | 1.67 | ±0.5% of VID | All |
| 7 7 | 0.84 | ±5 mV | 1.68 | ±0.5% of VID | All |
| 7 8 | 0.845 | ±5 mV | 1.69 | ±0.5% of VID | All |
| 7 9 | 0.85 | ±5 mV | 1.7 | ±0.5% of VID | All |
| 7 A | 0.855 | ±5 mV | 1.71 | ±0.5% of VID | All |



Table 2-5. VSA, VCCIO, CD_VCC_CORE or VCCD VID Table (Sheet 5 of 8)

| HEX | 5 mV step mode voltage | 5 mV step recommended accuracy | 10 mV step mode voltage | 10 mV step mode recommended accuracy | 10 mV mode market segment |
|-----|------------------------|--------------------------------|-------------------------|--------------------------------------|---------------------------|
| 7 B | 0.86 | ±5 mV | 1.72 | ±0.5% of VID | All |
| 7 C | 0.865 | ±5 mV | 1.73 | ±0.5% of VID | All |
| 7 D | 0.87 | ±5 mV | 1.74 | ±0.5% of VID | All |
| 7 E | 0.875 | ±5 mV | 1.75 | ±0.5% of VID | All |
| 7 F | 0.88 | ±5 mV | 1.76 | ±0.5% of VID | All |
| 8 0 | 0.885 | ±5 mV | 1.77 | ±0.5% of VID | All |
| 8 1 | 0.89 | ±5 mV | 1.78 | ±0.5% of VID | All |
| 8 2 | 0.895 | ±5 mV | 1.79 | ±0.5% of VID | All |
| 8 3 | 0.9 | ±5 mV | 1.8 | ±0.5% of VID | All |
| 8 4 | 0.905 | ±5 mV | 1.81 | ±0.5% of VID | All |
| 8 5 | 0.91 | ±5 mV | 1.82 | ±0.5% of VID | All |
| 8 6 | 0.915 | ±5 mV | 1.83 | ±0.5% of VID | All |
| 8 7 | 0.92 | ±5 mV | 1.84 | ±0.5% of VID | All |
| 8 8 | 0.925 | ±5 mV | 1.85 | ±0.5% of VID | All |
| 8 9 | 0.93 | ±5 mV | 1.86 | ±0.5% of VID | All |
| 8 A | 0.935 | ±5 mV | 1.87 | ±0.5% of VID | All |
| 8 B | 0.94 | ±5 mV | 1.88 | ±0.5% of VID | All |
| 8 C | 0.945 | ±5 mV | 1.89 | ±0.5% of VID | All |
| 8 D | 0.95 | ±5 mV | 1.9 | ±0.5% of VID | All |
| 8 E | 0.955 | ±5 mV | 1.91 | ±0.5% of VID | All |
| 8 F | 0.96 | ±5 mV | 1.92 | ±0.5% of VID | All |
| 9 0 | 0.965 | ±5 mV | 1.93 | ±0.5% of VID | All |
| 9 1 | 0.97 | ±5 mV | 1.94 | ±0.5% of VID | All |
| 9 2 | 0.975 | ±5 mV | 1.95 | ±0.5% of VID | All |
| 9 3 | 0.98 | ±5 mV | 1.96 | ±0.5% of VID | All |
| 9 4 | 0.985 | ±5 mV | 1.97 | ±0.5% of VID | All |
| 9 5 | 0.99 | ±5 mV | 1.98 | ±0.5% of VID | All |
| 9 6 | 0.995 | ±5 mV | 1.99 | ±0.5% of VID | All |
| 9 7 | 1 | ±0.5% of VID | 2 | ±0.5% of VID | All |
| 9 8 | 1.005 | ±0.5% of VID | 2.01 | ±0.5% of VID | Optional |
| 9 9 | 1.01 | ±0.5% of VID | 2.02 | ±0.5% of VID | Optional |
| 9 A | 1.015 | ±0.5% of VID | 2.03 | ±0.5% of VID | Optional |
| 9 B | 1.02 | ±0.5% of VID | 2.04 | ±0.5% of VID | Optional |
| 9 C | 1.025 | ±0.5% of VID | 2.05 | ±0.5% of VID | Optional |
| 9 D | 1.03 | ±0.5% of VID | 2.06 | ±0.5% of VID | Optional |
| 9 E | 1.035 | ±0.5% of VID | 2.07 | ±0.5% of VID | Optional |



Table 2-5. VSA, VCCIO, CD_VCC_CORE or VCCD VID Table (Sheet 6 of 8)

| HEX | 5 mV step mode voltage | 5 mV step recommended accuracy | 10 mV step mode voltage | 10 mV step mode recommended accuracy | 10 mV mode market segment |
|-----|------------------------|--------------------------------|-------------------------|--------------------------------------|----------------------------------|
| 9 F | 1.04 | ±0.5% of VID | 2.08 | ±0.5% of VID | Optional |
| A 0 | 1.045 | ±0.5% of VID | 2.09 | ±0.5% of VID | Optional |
| A 1 | 1.05 | ±0.5% of VID | 2.1 | ±0.5% of VID | Optional |
| A 2 | 1.055 | ±0.5% of VID | 2.11 | ±0.5% of VID | Optional |
| A 3 | 1.06 | ±0.5% of VID | 2.12 | ±0.5% of VID | Optional |
| A 4 | 1.065 | ±0.5% of VID | 2.13 | ±0.5% of VID | Optional |
| A 5 | 1.07 | ±0.5% of VID | 2.14 | ±0.5% of VID | Optional |
| A 6 | 1.075 | ±0.5% of VID | 2.15 | ±0.5% of VID | Optional |
| A 7 | 1.08 | ±0.5% of VID | 2.16 | ±0.5% of VID | Optional |
| A 8 | 1.085 | ±0.5% of VID | 2.17 | ±0.5% of VID | Optional |
| A 9 | 1.09 | ±0.5% of VID | 2.18 | ±0.5% of VID | Optional |
| A A | 1.095 | ±0.5% of VID | 2.19 | ±0.5% of VID | Optional |
| A B | 1.1 | ±0.5% of VID | 2.2 | ±0.5% of VID | Optional |
| A C | 1.105 | ±0.5% of VID | 2.21 | ±0.5% of VID | Optional |
| A D | 1.11 | ±0.5% of VID | 2.22 | ±0.5% of VID | Optional |
| A E | 1.115 | ±0.5% of VID | 2.23 | ±0.5% of VID | Optional |
| A F | 1.12 | ±0.5% of VID | 2.24 | ±0.5% of VID | Optional |
| B 0 | 1.125 | ±0.5% of VID | 2.25 | ±0.5% of VID | Optional |
| B 1 | 1.13 | ±0.5% of VID | 2.26 | ±0.5% of VID | Optional |
| B 2 | 1.135 | ±0.5% of VID | 2.27 | ±0.5% of VID | Optional |
| B 3 | 1.14 | ±0.5% of VID | 2.28 | ±0.5% of VID | Optional |
| B 4 | 1.145 | ±0.5% of VID | 2.29 | ±0.5% of VID | Optional |
| B 5 | 1.15 | ±0.5% of VID | 2.3 | ±0.5% of VID | >2.3 not required in any segment |
| B 6 | 1.155 | ±0.5% of VID | 2.31 | ±0.5% of VID | >2.3 not required in any segment |
| B 7 | 1.16 | ±0.5% of VID | 2.32 | ±0.5% of VID | >2.3 not required in any segment |
| B 8 | 1.165 | ±0.5% of VID | 2.33 | ±0.5% of VID | >2.3 not required in any segment |
| B 9 | 1.17 | ±0.5% of VID | 2.34 | ±0.5% of VID | >2.3 not required in any segment |
| B A | 1.175 | ±0.5% of VID | 2.35 | ±0.5% of VID | >2.3 not required in any segment |
| B B | 1.18 | ±0.5% of VID | 2.36 | ±0.5% of VID | >2.3 not required in any segment |
| B C | 1.185 | ±0.5% of VID | 2.37 | ±0.5% of VID | >2.3 not required in any segment |
| B D | 1.19 | ±0.5% of VID | 2.38 | ±0.5% of VID | >2.3 not required in any segment |
| B E | 1.195 | ±0.5% of VID | 2.39 | ±0.5% of VID | >2.3 not required in any segment |
| B F | 1.2 | ±0.5% of VID | 2.4 | ±0.5% of VID | >2.3 not required in any segment |
| C 0 | 1.205 | ±0.5% of VID | 2.41 | ±0.5% of VID | >2.3 not required in any segment |
| C 1 | 1.21 | ±0.5% of VID | 2.42 | ±0.5% of VID | >2.3 not required in any segment |
| C 2 | 1.215 | ±0.5% of VID | 2.43 | ±0.5% of VID | >2.3 not required in any segment |



Table 2-5. VSA, VCCIO, CD_VCC_CORE or VCCD VID Table (Sheet 7 of 8)

| HEX | 5 mV step mode voltage | 5 mV step recommended accuracy | 10 mV step mode voltage | 10 mV step mode recommended accuracy | 10 mV mode market segment |
|-----|------------------------|--------------------------------|-------------------------|--------------------------------------|----------------------------------|
| C 3 | 1.22 | ±0.5% of VID | 2.44 | ±0.5% of VID | >2.3 not required in any segment |
| C 4 | 1.225 | ±0.5% of VID | 2.45 | ±0.5% of VID | >2.3 not required in any segment |
| C 5 | 1.23 | ±0.5% of VID | 2.46 | ±0.5% of VID | >2.3 not required in any segment |
| C 6 | 1.235 | ±0.5% of VID | 2.47 | ±0.5% of VID | >2.3 not required in any segment |
| C 7 | 1.24 | ±0.5% of VID | 2.48 | ±0.5% of VID | >2.3 not required in any segment |
| C 8 | 1.245 | ±0.5% of VID | 2.49 | ±0.5% of VID | >2.3 not required in any segment |
| C 9 | 1.25 | ±0.5% of VID | 2.5 | ±0.5% of VID | >2.3 not required in any segment |
| C A | 1.255 | ±0.5% of VID | 2.51 | ±0.5% of VID | >2.3 not required in any segment |
| C B | 1.26 | ±0.5% of VID | 2.52 | ±0.5% of VID | >2.3 not required in any segment |
| C C | 1.265 | ±0.5% of VID | 2.53 | ±0.5% of VID | >2.3 not required in any segment |
| C D | 1.27 | ±0.5% of VID | 2.54 | ±0.5% of VID | >2.3 not required in any segment |
| C E | 1.275 | ±0.5% of VID | 2.55 | ±0.5% of VID | >2.3 not required in any segment |
| C F | 1.28 | ±0.5% of VID | 2.56 | ±0.5% of VID | >2.3 not required in any segment |
| D 0 | 1.285 | ±0.5% of VID | 2.57 | ±0.5% of VID | >2.3 not required in any segment |
| D 1 | 1.29 | ±0.5% of VID | 2.58 | ±0.5% of VID | >2.3 not required in any segment |
| D 2 | 1.295 | ±0.5% of VID | 2.59 | ±0.5% of VID | >2.3 not required in any segment |
| D 3 | 1.3 | ±0.5% of VID | 2.6 | ±0.5% of VID | >2.3 not required in any segment |
| D 4 | 1.305 | ±0.5% of VID | 2.61 | ±0.5% of VID | >2.3 not required in any segment |
| D 5 | 1.31 | ±0.5% of VID | 2.62 | ±0.5% of VID | >2.3 not required in any segment |
| D 6 | 1.315 | ±0.5% of VID | 2.63 | ±0.5% of VID | >2.3 not required in any segment |
| D 7 | 1.32 | ±0.5% of VID | 2.64 | ±0.5% of VID | >2.3 not required in any segment |
| D 8 | 1.325 | ±0.5% of VID | 2.65 | ±0.5% of VID | >2.3 not required in any segment |
| D 9 | 1.33 | ±0.5% of VID | 2.66 | ±0.5% of VID | >2.3 not required in any segment |
| D A | 1.335 | ±0.5% of VID | 2.67 | ±0.5% of VID | >2.3 not required in any segment |
| D B | 1.34 | ±0.5% of VID | 2.68 | ±0.5% of VID | >2.3 not required in any segment |
| D C | 1.345 | ±0.5% of VID | 2.69 | ±0.5% of VID | >2.3 not required in any segment |
| D D | 1.35 | ±0.5% of VID | 2.7 | ±0.5% of VID | >2.3 not required in any segment |
| D E | 1.355 | ±0.5% of VID | 2.71 | ±0.5% of VID | >2.3 not required in any segment |
| D F | 1.36 | ±0.5% of VID | 2.72 | ±0.5% of VID | >2.3 not required in any segment |
| E 0 | 1.365 | ±0.5% of VID | 2.73 | ±0.5% of VID | >2.3 not required in any segment |
| E 1 | 1.37 | ±0.5% of VID | 2.74 | ±0.5% of VID | >2.3 not required in any segment |
| E 2 | 1.375 | ±0.5% of VID | 2.75 | ±0.5% of VID | >2.3 not required in any segment |
| E 3 | 1.38 | ±0.5% of VID | 2.76 | ±0.5% of VID | >2.3 not required in any segment |
| E 4 | 1.385 | ±0.5% of VID | 2.77 | ±0.5% of VID | >2.3 not required in any segment |
| E 5 | 1.39 | ±0.5% of VID | 2.78 | ±0.5% of VID | >2.3 not required in any segment |
| E 6 | 1.395 | ±0.5% of VID | 2.79 | ±0.5% of VID | >2.3 not required in any segment |



Table 2-5. VSA, VCCIO, CD_VCC_CORE or VCCD VID Table (Sheet 8 of 8)

| HEX | 5 mV step mode voltage | 5 mV step recommended accuracy | 10 mV step mode voltage | 10 mV step mode recommended accuracy | 10 mV mode market segment |
|-----|------------------------|--------------------------------|-------------------------|--------------------------------------|----------------------------------|
| E 7 | 1.4 | ±0.5% of VID | 2.8 | ±0.5% of VID | >2.3 not required in any segment |
| E 8 | 1.405 | ±0.5% of VID | 2.81 | ±0.5% of VID | >2.3 not required in any segment |
| E 9 | 1.41 | ±0.5% of VID | 2.82 | ±0.5% of VID | >2.3 not required in any segment |
| E A | 1.415 | ±0.5% of VID | 2.83 | ±0.5% of VID | >2.3 not required in any segment |
| E B | 1.42 | ±0.5% of VID | 2.84 | ±0.5% of VID | >2.3 not required in any segment |
| E C | 1.425 | ±0.5% of VID | 2.85 | ±0.5% of VID | >2.3 not required in any segment |
| E D | 1.43 | ±0.5% of VID | 2.86 | ±0.5% of VID | >2.3 not required in any segment |
| E E | 1.435 | ±0.5% of VID | 2.87 | ±0.5% of VID | >2.3 not required in any segment |
| E F | 1.44 | ±0.5% of VID | 2.88 | ±0.5% of VID | >2.3 not required in any segment |
| F 0 | 1.445 | ±0.5% of VID | 2.89 | ±0.5% of VID | >2.3 not required in any segment |
| F 1 | 1.45 | ±0.5% of VID | 2.9 | ±0.5% of VID | >2.3 not required in any segment |
| F 2 | 1.455 | ±0.5% of VID | 2.91 | ±0.5% of VID | >2.3 not required in any segment |
| F 3 | 1.46 | ±0.5% of VID | 2.92 | ±0.5% of VID | >2.3 not required in any segment |
| F 4 | 1.465 | ±0.5% of VID | 2.93 | ±0.5% of VID | >2.3 not required in any segment |
| F 5 | 1.47 | ±0.5% of VID | 2.94 | ±0.5% of VID | >2.3 not required in any segment |
| F 6 | 1.475 | ±0.5% of VID | 2.95 | ±0.5% of VID | >2.3 not required in any segment |
| F 7 | 1.48 | ±0.5% of VID | 2.96 | ±0.5% of VID | >2.3 not required in any segment |
| F 8 | 1.485 | ±0.5% of VID | 2.97 | ±0.5% of VID | >2.3 not required in any segment |
| F 9 | 1.49 | ±0.5% of VID | 2.98 | ±0.5% of VID | >2.3 not required in any segment |
| F A | 1.495 | ±0.5% of VID | 2.99 | ±0.5% of VID | >2.3 not required in any segment |
| F B | 1.5 | ±0.5% of VID | 3 | ±0.5% of VID | >2.3 not required in any segment |
| F C | 1.505 | ±0.5% of VID | 3.01 | ±0.5% of VID | >2.3 not required in any segment |
| F D | 1.51 | ±0.5% of VID | 3.02 | ±0.5% of VID | >2.3 not required in any segment |
| F E | 1.515 | ±0.5% of VID | 3.03 | ±0.5% of VID | >2.3 not required in any segment |
| F F | 1.52 | ±0.5% of VID | 3.04 | ±0.5% of VID | >2.3 not required in any segment |

Note:

1. DAC accuracy is a recommendation only. Total tolerance band must be met, that is, DAC set point + current sense AVP droop accuracy. VCCD may use 5 mV or 10 mV VID tables, this is set by selecting the protocol ID bit in the PWM controller, which is read by BIOS at boot.
2. VCCD can use VID Table 2-4, "VR13.0 Reference Code VCCIN Voltage Identification (VID)" or VID Table 2-5, "VSA, VCCIO, CD_VCC_CORE or VCCD VID Table."

2.2.10 Reserved or Unused Signals

All Reserved (RSVD) signals must not be connected. Connection of these signals to VCCIN, VCCD, Vss, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (Vss). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and



prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within $\pm 20\%$ of the impedance of the baseboard trace, unless otherwise noted in the appropriate platform design guidelines.

2.3 Signal Group Summary

Signals are grouped by buffer type and similar characteristics as listed in the following table. The buffer type indicates which signaling technology and specifications apply to the signals.

Table 2-6. Signal Description Buffer Types

| Signal | Description |
|--------------|---|
| Analog | Analog reference or output. May be used as a threshold voltage or for buffer compensation |
| Asynchronous | Signal has no timing relationship with any system reference clock. |
| CMOS | CMOS Output buffers: 1.05 V tolerant / CMOS Input buffers |
| DDR4 | CMOS Output buffers 1.2 V tolerant |
| DMI3 | Direct Media Interface Gen 3 signals. These signals are compatible with PCI Express* 3.0 Signaling Environment AC Specifications. |
| Intel® UPI | Current-mode 9.6 GT/s or 10.4 GT/s. Nominal voltage is 1.0 V. |
| Open Drain | Open Drain buffers: 1.05 V tolerant |
| PCI Express* | PCI Express interface signals. These signals are compatible with PCI Express 3.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification. |
| Reference | Voltage reference signal. |
| SSTL | Source Series Terminated Logic (JEDEC SSTL_15) |

Note: Qualifier for a buffer type.

Table 2-7. Signal Groups (Sheet 1 of 4)

| Differential/Single Ended | Buffer Type | Signal |
|------------------------------|-------------------|---|
| DDR4 Reference Clocks | | |
| Differential | SSTL Output | DDR{0/1/2/3/4/5}_CLK_D[N/P] [3:0] |
| DDR4 Command Signals | | |
| Single-ended | SSTL Output | DDR{0/1/2/3/4/5}_ACT_N DDR{0/1/2/3/4/5}_BA[1:0] DDR{0/1/2/3/4/5}_BG[1:0] DDR{0/1/2/3/4/5}_MA[17:0] DDR{0/1/2/3/4/5}_PAR |
| DDR4 Control Signals | | |
| Single-ended | SSTL Output | DDR{0/1/2/3/4/5}_CS_N[7:0] DDR{0/1/2/3/4/5}_CID[2] DDR{0/1/2/3/4/5}_ODT[3:0] DDR{0/1/2/3/4/5}_CKE[3:0] |
| DDR4 Data Signals | | |
| Differential | SSTL Input/Output | DDR{0/1/2/3/4/5}_DQS_D[N/P] [17:0] |
| Single-ended | SSTL Input/Output | DDR{0/1/2/3/4/5}_DQ[63:0] DDR{0/1/2/3/4/5}_ECC[7:0] |



Table 2-7. Signal Groups (Sheet 2 of 4)

| Differential/Single Ended | Buffer Type | Signal |
|--|--|---|
| DDR4 Miscellaneous Signals | | |
| Single-ended | SSTL Input | DDR{0/1/2/3/4/5}_ALERT_N |
| | CMOS Input Note: Input voltage from platform cannot exceed 1.2 V max. Refer to PDG for implementation details. | DDR{012,345}_DRAM_PWR_OK |
| | CMOS 1.2 V Output | DDR{012,345}_RESET_N |
| | Open Drain Output / CMOS Input | DDR[012,345]_SPDSCL DDR[012,345]_SPSDA |
| | DC Output | DDR{5:0}_CAVREF |
| | DDR Compensation resistance control | DDR{012,345}_RCOMP[2:0] |
| PCI Express* Port 1, 2, & 3 Signals | | |
| Differential | PCI Express* Input | PE{3:1}_RX_DN/DP[15:0] |
| Differential | PCI Express* Output | PE{3:1}_TX_DN/DP[15:0] |
| PCI Express* Miscellaneous Signals | | |
| Single-ended | Open Drain Output | PE_HP_SCL |
| | Open Drain Output /CMOS | PE_HP_SDA |
| DMI3/PCI Express* Signals | | |
| Differential | DMI3 Input | DMI3_RX_D[N/P][3:0] |
| | DMI3 Output | DMI3_TX_D[N/P][3:0] |
| Single-ended | DMI Miscellaneous | DMIMODE_OVERRIDE |
| Intel® UPI Signals | | |
| Differential | Intel® UPI Input Output | UPI{2:1}_RX/TX_DN/DP[19:0] |
| Single-ended | Intel® UPI Miscellaneous | UPI{01,2}_RBIAS |
| Single-ended | Intel® UPI Power | UPI{01,2}_VCCQ |
| Platform Environmental Control Interface (PECI) | | |
| Single-ended | PECI Input/Output | PECI |
| System Reference Clock (BCLK{0/1/2}) | | |
| Differential | CMOS 1.05 V Input | BCLK{0/1/2}_D[N/P] |



Table 2-7. Signal Groups (Sheet 3 of 4)

| Differential/Single Ended | Buffer Type | Signal |
|--|---------------------------------------|---|
| JTAG & TAP Signals | | |
| Single ended | CMOS Input | TCK,TDI,TMS,TRST_N,PREQ_N |
| | Open Drain Output /CMOS | BPM_N[7:0] |
| | Open Drain Output | TDO, PRDY_N |
| Serial VID Interface (SVID) Signals | | |
| Single ended | CMOS Input | SVIDALERT_N[1:0] |
| | Open Drain Output / CMOS | SVIDDATA [1:0] |
| | Open Drain Output | SVIDCLK [1:0] |
| Processor Asynchronous Sideband Signals | | |
| Single ended | CMOS Input | BIST_ENABLE, BMCINIT, DEBUG_EN_N |
| | | FRMAGENT, PWRGOOD, PMSYNC RESET_N, SAFE_MODE_BOOT, SOCKET_ID[1:0], TXT_AGENT TXT_PLTEN |
| | CMOS Output | FIVR_FAULT |
| | Open Drain Output / CMOS Input | CATERR_N, MEM_HOT_C01_N, MEM_HOT_C23_N, MSMI_N, PM_FAST_WAKE_N, PROCHOT_N |
| | Open Drain Output | ERROR_N[2:0], THERMTRIP_N |
| Miscellaneous Signals | | |
| | CMOS Input | EAR_N,LEGACY_SKT,NMI,PMSYNCPMSY NC_CLK,PROCDIS_N, PWR_DEBUG_N,SOCKET_ID2 |
| | Open Drain Output / CMOS Input | TSC_SYNC |
| | Not connected to Silicon | SKTOCC_N,PKGID[2:0], PROC_ID[1:0] |
| Intel Omni-Path Host Fabric Interface (Intel® OP HFI) Signals | | |
| | Open Drain Output / CMOS 2.5 Input | CD_HFI[1:0]_I2CCLK, CD_HFI[1:0]_I2CDAT |
| | CMOS 2.5V Input | CD_HFI[1:0]_INT_N, CD_HFI[1:0]_MODPRST_N |
| | CMOS 1.8V Input | CD_TCLK, CD_TDI, CD_TMS, CD_TRST_N |
| | Open Drain Output | CD_HFI[1:0]_RESET_N, CD_HFI[1:0]_LED_N |
| | CMOS 1.8V Output | CD_TDO |
| | CMOS Input | CD_HFI_REFCLK_DN/DP |
| | | CD_POR_N |
| | | MCP01_RBIAS |



Table 2-7. Signal Groups (Sheet 4 of 4)

| Differential/Single Ended | Buffer Type | Signal |
|----------------------------|----------------|--|
| Power/Other Signals | | |
| | Power / Ground | VCCIN, VCCD_012, VCCD_345, VCCIO, VCC33, VCC33, VSS |
| | Sense Points | VCCIN_SENSE, VCCIO_SENSE, VCCSA_SENSE, VSS_VCCIN_SENSE, VSS_VCCIO_SENSE, VSS_VCCSA_SENSE, VCCIN_PMAX, VSENSEPMAX |

Notes:

1. Refer to Chapter 4, "Signal Descriptions" for signal description details.
2. DDR{0/1/2/3/4/5} refers to DDR4 Channel 0, DDR4 Channel 1, DDR4 Channel 2, DDR4 Channel 3, DDR4 Channel 4, "Signal Descriptions" and DDR4 Chapter 5, "PIROM."

Table 2-8. Signals with On-Die Weak PU/PD

| Signal Name | Pull Up/Pull Down | Rail | Value | Units |
|------------------|-------------------|-------|-------|-------|
| BIST_ENABLE | Pull Up | VCCIO | 3K-8K | ohm |
| BMCINIT | Pull Down | VSS | 3K-8K | ohm |
| DEBUG_EN_N | Pull Up | VCCIO | 3K-8K | ohm |
| DMIMODE_OVERRIDE | Pull Up | VCCIO | 3K-8K | ohm |
| EAR_N | Pull Up | VCCIO | 3K-8K | ohm |
| FRMAGENT | Pull Down | VSS | 3K-8K | ohm |
| LEGACY_SKT | Pull Down | VSS | 3K-8K | ohm |
| MSMI_N | Pull Up | VCCIO | 3K-8K | ohm |
| NMI | Pull Down | VSS | 3K-8K | ohm |
| PM_FAST_WAKE_N | Pull Up | VCCIO | 3K-8K | ohm |
| PROCDIS_N | Pull Up | VCCIO | 3K-8K | ohm |
| SAFE_MODE_BOOT | Pull Down | VSS | 3K-8K | ohm |
| SOCKET_ID[2:0] | Pull Down | VSS | 3K-8K | ohm |
| TCK | Pull Down | VSS | 3K-8K | ohm |
| TDI | Pull Up | VCCIO | 3K-8K | ohm |
| TMS | Pull Up | VCCIO | 3K-8K | ohm |
| TRST_N | Pull Up | VCCIO | 3K-8K | ohm |
| TXT_AGENT | Pull Down | VSS | 3K-8K | ohm |
| TXT_PLTEN | Pull Up | VCCIO | 3K-8K | ohm |

2.4 Fault Resilient Booting (FRB)

FRB is a RASM (Reliability, Availability, Serviceability, and Manageability) feature and this section describes the processor implementation.



The processor supports both socket and core level Fault Resilient Booting (FRB), which provides the ability to boot the system as long as there is one processor functional in the system. One limitation to socket level FRB is that the system cannot boot if the legacy socket that connects to an active PCH becomes unavailable since this is the path to the system BIOS. See the table below for a list of output tri-state FRB signals.

Socket level FRB will tri-state processor outputs via the PROCDIS_N signal. Assertion of the PROCDIS_N signal through RESET_N de-assertion will tri-state processor outputs. Note, that individual core disabling is also supported for those cases where disabling the entire package is not desired.

The processor extends the FRB capability to the core granularity by maintaining a register in the Uncore so that BIOS or another entity can disable one or more specific processor cores.

Table 2-9. Fault Resilient Booting (Output Tri-State) Signals

| Output Tri-State Signal Groups | Tri-State Signals |
|--------------------------------|---|
| Intel® UPI | KTI{2:1}TX_DN/DP[19:0] |
| PCI Express* | PE_TX_DN[15:0] PE_TX_DP[15:0] PE_HP_SCL PE_HP_SDA |
| DDR4 | Control, Address and DQ, DDR4 RESET_N asserted |
| DMI3 | DMI_TX_DN[3:0] DMI_TX_DP[3:0] |
| SMBus (SPD) | DDR[012,345]_SPDSCL DDR[012,345]_SPDSDA |
| Processor Sideband | CATERR_N, ERROR_N[2:0], BPM_N[7:0], THERMTRIP_N, PROCHOT_N, PECCI, PM_FAST_WAKE_N, MSMI_N, TSC_SYNC, FIVR_FAULT |
| SVID | SVIDCLK, SVIDDATA |

2.4.1 Power-On Configuration (POC) Options

Several configuration options can be configured by hardware. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET_N, or upon assertion of PWRGOOD (inactive-to-active transition). For specifics on these options, please see the following table.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset transition of the latching signal (RESET_N or PWRGOOD).

Table 2-10. Power-On Configuration Option Lands (Sheet 1 of 2)

| Configuration Option | Land Name | Notes |
|--|-------------|-------|
| Output tri state | PROCDIS_N | 1 |
| Execute BIST (Built-In Self Test) | BIST_ENABLE | 2 |
| Enable Service Processor Boot Mode | BMCINIT | 3 |
| Power-up Sequence Halt | EAR_N | 3 |
| Enable Intel® Trusted Execution Technology (Intel® TXT) Platform | TXT_PLTEN | 3 |
| Enable Bootable Firmware Agent | FRMAGENT | 3 |
| Enable Intel Trusted Execution Technology (Intel TXT) Agent | TXT_AGENT | 3 |



Table 2-10. Power-On Configuration Option Lands (Sheet 2 of 2)

| Configuration Option | Land Name | Notes |
|---------------------------|----------------|-------|
| Enable Safe Mode Boot | SAFE_MODE_BOOT | 3 |
| Configure Socket ID | SOCKET_ID[1:0] | 3 |
| Enable legacy socket boot | LEGACY_SKT | 3 |

Notes:

1. Output tri-state option enables Fault Resilient Booting (FRB), for FRB details see the Fault Resilient Booting (FRB) Section. The signal used to latch PROCDIS_N for enabling FRB mode is RESET_N.
2. BIST_ENABLE is sampled at RESET_N de-assertion
3. This signal is sampled after PWRGOOD assertion.

2.5 Mixing Processors

Intel supports and validates two and four processor configurations only where all processors operate with the same Intel® UPI frequency, core frequency, power segment, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel. Combining processors from different power segments is also not supported.

Note: All processors within a system must run at a common maximum non-Turbo ratio. The system BIOS may be required to program the FLEX_RATIO register if mixed frequency processors are populated.

Not all operating systems can support dual processors with mixed frequencies. Mixing processors of different steppings but the same model (as per CPUID instruction) is supported, provided there is no more than one stepping delta between the processors, for example, S and S+1.

S and S+1 is defined as mixing of two CPU steppings in the same platform where one CPU is S (stepping) = CPUID.(EAX=01h):EAX[3:0], and the other is S+1 = CPUID.(EAX=01h):EAX[3:0]+1. The stepping ID is found in EAX[3:0] after executing the CPUID instruction with Function 01h. Details regarding the CPUID instruction are provided in the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set Reference, A-M*.

2.6 Flexible Motherboard Guidelines (FMB)

The Flexible Motherboard (FMB) guidelines are estimates of the maximum values the processor will have over certain time periods. The values are only estimates and actual specifications for future processors may differ. Processors may or may not have specifications equal to the FMB value in the foreseeable future. System designers should meet the FMB values to ensure their systems will be compatible with future processors.

2.7 Absolute Maximum and Minimum Ratings

The table below specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and



minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 2-11. Processor Absolute Minimum and Maximum Ratings

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|------|------|------|
| V _{CCIN} | Processor input voltage with respect to V _{SS} | -0.3 | 2.15 | V |
| V _{CCD} | Processor IO supply voltage for DDR4 (standard voltage) with respect to V _{SS} | -0.3 | 1.50 | V |
| V _{CCIO} | IO voltage supply input with respect to V _{SS} | -0.3 | 1.45 | V |
| V _{CCSA} | IO voltage supply input with respect to V _{SS} | -0.3 | 1.45 | V |

Notes:

- For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.
- Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in [Section 2.10.5, "Overshoot/Undershoot Tolerance."](#) Excessive Overshoot or undershoot on any signal will likely result in permanent damage to the processor.

2.7.1 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed to while being stored in a Moisture Barrier Bag. The specified storage conditions are for component level prior to board attach (see notes in the following table for post board attach limits).

The table below specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality and reliability may be affected.

Table 2-12. Storage Condition Ratings

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|----------|-----|-------|
| T _{absolute storage} | The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time. | -25 | 125 | °C |
| T _{sustained storage} | The minimum/maximum device storage temperature for a sustained period of time. | -5 | 40 | °C |
| T _{short term storage} | The ambient storage temperature (in shipping media) for a short period of time. | -20 | 85 | °C |
| RH _{sustained storage} | The maximum device storage relative humidity for a sustained period of time. Unopened bag, includes 6 months storage time by customer. | 60% @ 24 | | °C |
| T _{imeshort term storage} | A short period of time (in shipping media). | 0 | 72 | hours |



Notes:

1. Storage conditions are applicable to storage environments only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
2. These ratings apply to the Intel component and do not include the tray or packaging.
3. Failure to adhere to this specification can affect the long-term reliability of the processor.
4. Non-operating storage limits post board attach: Storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component level certification assessments post board attach given the multitude of attach methods, socket types and board types used by customers. Provided as general guidance only, Intel board products are specified and certified to meet the following temperature and humidity limits (Non-Operating Temperature Limit: -40C to 70C & Humidity: 50% to 90%, non condensing with a maximum wet bulb of 28°C).
5. Device storage temperature qualification methods follow JEDEC High and Low Temperature Storage Life Standards: *JESD22-A119* (low temperature) and *JESD22-A103* (high temperature).

2.8 DC Specifications

DC specifications are defined at the processor pads, unless otherwise noted.

DC specifications are only valid while meeting specifications for case temperature (TCASE specified in the *Second Generation Intel® Xeon® Scalable Processors Thermal/Mechanical Specification and Design Guide (TMSDG)*), clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

2.8.1 Voltage and Current Specifications

Table 2-13. Voltage Specification (Sheet 1 of 2)

| Symbols | Parameter | Voltage Plane | Min | Nom | Max | Unit | Notes ¹ |
|---|--|-------------------|---|---|---|------|--------------------|
| V _{CCIN} | Input to Integrated Voltage Regulator (Launch - FMB) | V _{CCIN} | = VID - R _{II} *I _{out} -0.022V | = VID - R _{II} *I _{out} | = VID - R _{II} *I _{out} +0.022V | V | 2, 3, 4, 5, 8, 12 |
| V _{CCIN} VID Range | | V _{CCIN} | 1.60 | 1.80 | 1.83 | V | 2, 3, 4, 5, 8, 12 |
| V _{VID_STEP} (V _{CCIN}) | VID step size during a transition | V _{CCIN} | | 10.0 | | mV | 6 |
| V _{VID_STEP} (V _{CCD}) | VID step size during a transition | | 5 | | 10 | mV | |
| V _{CCD} (V _{CCD_012} , V _{CCD_345}) | I/O Voltage for DDR4 (Standard Voltage) | V _{CCD} | 1.17 | 1.2 | 1.26 | V | 7, 9, 10, 11 |
| V _{CCSA} | Power supply for Intel® UPI and IIO | V _{CCSA} | VID - 0.111 | VID | VID + 0.100 | V | |



Table 2-13. Voltage Specification (Sheet 2 of 2)

| Symbols | Parameter | Voltage Plane | Min | Nom | Max | Unit | Notes ¹ |
|-----------------|-------------------------|---------------|-------|------|-------|------|--------------------|
| VCCSA VID Range | | | 0.5 | 0.85 | 1.1 | V | |
| VCCIO | IO voltage supply input | | 0.937 | 1.00 | 1.057 | V | |
| VCC33 | Power supply for PIROM | | 3.14 | 3.3 | 3.47 | V | |
| CD_VCC_CO RE | | | 0.814 | 0.9 | 0.974 | V | |

Notes:

- Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on pre-silicon characterization and will be updated as further data becomes available.
- These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
- The VCCIN voltage specification requirements are measured across the remote sense pin pairs (VCCIN_SENSE and VSS_VCCIN_SENSE) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1 Mohm minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
- Refer to VCCIN Static and Transient Tolerance Second Generation Intel® Xeon® Scalable Processors and corresponding Figure 2-3, "VCCIN Static and Transient Tolerance Load Lines 1.0 mOHM." The processor should not be subjected to any static VCCIN level that exceeds the VCCIN_MAX associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
- Minimum VCCIN and maximum ICCIN are specified at the maximum processor case temperature (TCASE) shown in the Second Generation Intel® Xeon® Scalable Processors Thermal/Mechanical Specification and Design Guide (TMSDG). ICCIN_MAX is specified at the relative VCC_MAX point on the VCCIN load line. The processor is capable of drawing ICCIN_MAX for up to 2 ms.
- This specification represents the VCCIN reduction or VCCIN increase due to each VID transition. For Voltage Identification (VID) see Table 2-4, "VR13.0 Reference Code VCCIN Voltage Identification (VID)."
- Baseboard bandwidth is limited to 20 MHz.
- FMB is the flexible motherboard guidelines. See Section 2.4, "Fault Resilient Booting (FRB)" for details.
- DC + AC + Ripple = Tolerance
- VCCD tolerance at processor pins. Required in order to meet ±5% tolerance at processor die.
- The VCCD012, VCCD345 voltage specification requirements are measured across vias on the platform. Choose VCCD012 or VCCD345 vias close to the socket and measure with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using 1.5 pF maximum probe capacitance, and 1M ohm minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
- VCCIN has a Vboot setting of 1.7 V and is not included in the PWRGOOD indication. Refer to the VR13.0 PWM - Server VR Vendor PWM Enabling Specification.

Table 2-14. Current (ICCIN_MAX and ICCIN_TDC) Specification (Sheet 1 of 2)

| TDP (W) | 205 | 200 | 165 | 150 | 145 | 140 | 135 | 130 | 125 | 120 | 115 | 105 | 85 | 70 |
|------------------|---------------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Segment | Single Die Package | | | | | | | | | | | | | |
| VCCIN ICCMAX (A) | 228 | 228 | 228 | 205 | 205 | 190 | 190 | 177 | 160 | 160 | 154 | 132 | 102 | 85 |
| VCCSA ICCMAX (A) | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| VCCIO ICCMAX (A) | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 21 | 21 |
| VCCD ICCMAX (A) | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| VCC33 ICCMAX(A) | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 |
| VCCIN TDC (A) | 112 | 112 | 89 | 80 | 77 | 73 | 70 | 68 | 65 | 62 | 54 | 54 | 42 | 33 |
| VCCSA TDC (A) | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 |
| VCCIO TDC (A) | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 |
| VCCD TDC (A) | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| VCC33 TDC (A) | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 | .075 |
| Pmax Package (W) | 413 | 413 | 363 | 319 | 319 | 297 | 297 | 286 | 264 | 264 | 253 | 231 | 187 | 154 |



Table 2-14. Current (ICCN_MAX and ICCIN_TDC) Specification (Sheet 2 of 2)

| TDP (W) | 165 | 160 | 145 | 135 | 120 | 105 | 85 | | | | | | |
|------------------------|--------|------|------|------|------|------|------|------|--|--|--|--|--|
| Segment | Fabric | | | | | | | | | | | | |
| VCCIN ICCMAX (A) | 228 | 221 | 205 | 190 | 160 | 132 | 102 | | | | | | |
| VCCSA ICCMAX (A) | 16 | 16 | 16 | 16 | 16 | 16 | 16 | | | | | | |
| VCCIO ICCMAX (A) | 21 | 21 | 21 | 21 | 21 | 21 | 21 | | | | | | |
| VCCD ICCMAX (A) | 8 | 8 | 8 | 8 | 8 | 8 | 8 | | | | | | |
| VCC33 ICCMAX(A) | .075 | .075 | .075 | .075 | .075 | .075 | .075 | | | | | | |
| VCCIN TDC (A) | 89 | 86 | 77 | 70 | 62 | 54 | 42 | | | | | | |
| VCCSA TDC (A) | 15 | 15 | 15 | 15 | 15 | 15 | 15 | | | | | | |
| VCCIO TDC (A) | 14 | 14 | 14 | 14 | 14 | 14 | 14 | | | | | | |
| VCCD TDC (A) | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | | | | |
| VCC33 TDC (A) | .075 | .075 | .075 | .075 | .075 | .075 | .075 | | | | | | |
| Pmax Package (W) | 363 | 352 | 319 | 297 | 264 | 231 | 187 | | | | | | |
| CD_VCC_CORE ICCMAX (A) | | | | | | | | 10 | | | | | |
| CD_VCCIN ICCMAX (A) | | | | | | | | .01 | | | | | |
| CD_VCCP ICCMAX (A) | | | | | | | | .015 | | | | | |
| CD_VPP ICCMAX (A) | | | | | | | | 7 | | | | | |
| CD_VCC_CORE TDC (A) | | | | | | | | 9 | | | | | |
| CD_VCCIN TDC (A) | | | | | | | | .01 | | | | | |
| CD_VCCP TDC (A) | | | | | | | | .01 | | | | | |
| CD_VPP TDC (A) | | | | | | | | 6 | | | | | |

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on pre-silicon characterization and will be updated as further data becomes available.
2. FMB is the flexible motherboard guidelines. See [Section 2.6, "Flexible Motherboard Guidelines \(FMB\)"](#) for further details.
3. ICCIN_TDC (Thermal Design Current) is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator thermal assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion. Please refer to the VR13.0 PWM Server VR Vendor PWM Enabling Specification for further details.
4. Minimum VCCIN and maximum ICCIN are specified at the maximum processor case temperature (TCASE) shown in the VR13.0 PWM Server VR Vendor PWM Enabling Specification for further details. ICCIN_MAX is specified at the relative VCCIN_MAX point on the VCCIN load line. The processor is capable of drawing ICCIN_MAX for up to 2 ms.
5. Values on this table correspond to SKT-P.

Table 2-15. VCCIN Static and Transient Tolerance for 0.9LL (Sheet 1 of 2)

| ICCN (A) | VCCIN_Max (V) | VCCIN_Nom (V) | VCCIN_Min (V) | Notes |
|----------|---------------|---------------|---------------|-------|
| 0 | VID +0.022 | VID -0.000 | VID -0.022 | |
| 10 | VID +0.013 | VID -0.009 | VID -0.031 | |
| 20 | VID +0.004 | VID -0.018 | VID -0.040 | |
| 30 | VID -0.005 | VID -0.027 | VID -0.049 | |
| 40 | VID -0.014 | VID -0.036 | VID -0.058 | |
| 50 | VID -0.023 | VID -0.045 | VID -0.067 | |
| 60 | VID -0.032 | VID -0.054 | VID -0.076 | |



Table 2-15. VCCIN Static and Transient Tolerance for 0.9LL (Sheet 2 of 2)

| I _{CCIN} (A) | V _{CCIN_Max} (V) | V _{CCIN_Nom} (V) | V _{CCIN_Min} (V) | Notes |
|-----------------------|---------------------------|---------------------------|---------------------------|-------|
| 70 | VID -0.041 | VID -0.063 | VID -0.085 | |
| 80 | VID -0.050 | VID -0.072 | VID -0.094 | |
| 90 | VID -0.059 | VID -0.081 | VID -0.103 | |
| 100 | VID -0.068 | VID -0.090 | VID -0.112 | |
| 110 | VID -0.077 | VID -0.099 | VID -0.121 | |
| 120 | VID -0.086 | VID -0.108 | VID -0.130 | |
| 130 | VID -0.095 | VID -0.117 | VID -0.139 | |
| 140 | VID -0.104 | VID -0.126 | VID -0.148 | |
| 150 | VID -0.113 | VID -0.135 | VID -0.157 | |
| 160 | VID -0.122 | VID -0.144 | VID -0.166 | |
| 170 | VID -0.131 | VID -0.153 | VID -0.175 | |
| 180 | VID -0.140 | VID -0.162 | VID -0.184 | |
| 190 | VID -0.149 | VID -0.171 | VID -0.193 | |
| 200 | VID -0.158 | VID -0.180 | VID -0.202 | |
| 210 | VID -0.167 | VID -0.189 | VID -0.211 | |
| 220 | VID -0.176 | VID -0.198 | VID -0.220 | |
| 230 | VID -0.185 | VID -0.207 | VID -0.229 | |

Notes:

1. The V_{CCIN_Min} and V_{CCIN_Max} loadlines represent static and transient limits. Please see for [Section 2.8.2.1, "VCCIN Overshoot Specifications."](#)
2. This table is intended to aid in reading discrete points on graph in [Figure 2-2, "VCCIN Static and Transient Tolerance Load Lines 0.9 mOHM."](#)
3. The loadlines specify voltage limits at the die measured at the V_{CCIN_SENSE} and V_{SS_VCCIN_SENSE} lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor V_{CCIN_SENSE} and V_{SS_VCCIN_SENSE} lands. Refer to the VR13.0 PWM Server VR Vendor PWM Enabling Specification for loadline guidelines and VR implementation details.

Table 2-16. VCCIN Static and Transient Tolerance for 1.0LL (Sheet 1 of 2)

| I _{CCIN} (A) | V _{CCIN_Max} (V) | V _{CCIN_Nom} (V) | V _{CCIN_Min} (V) | Notes |
|-----------------------|---------------------------|---------------------------|---------------------------|-------|
| 0 | VID +0.022 | VID -0.000 | VID -0.022 | |
| 10 | VID +0.012 | VID -0.010 | VID -0.032 | |
| 20 | VID +0.002 | VID -0.020 | VID -0.042 | |
| 30 | VID -0.008 | VID -0.030 | VID -0.052 | |
| 40 | VID -0.018 | VID -0.040 | VID -0.062 | |
| 50 | VID -0.028 | VID -0.050 | VID -0.072 | |
| 60 | VID -0.038 | VID -0.060 | VID -0.082 | |
| 70 | VID -0.048 | VID -0.070 | VID -0.092 | |
| 80 | VID -0.058 | VID -0.080 | VID -0.102 | |
| 90 | VID -0.068 | VID -0.090 | VID -0.112 | |
| 100 | VID -0.078 | VID -0.100 | VID -0.122 | |
| 110 | VID -0.088 | VID -0.110 | VID -0.132 | |



Table 2-16. VCCIN Static and Transient Tolerance for 1.0LL (Sheet 2 of 2)

| Iccin (A) | VCCIN_Max (V) | VCCIN_Nom (V) | VCCIN_Min (V) | Notes |
|-----------|---------------|---------------|---------------|-------|
| 120 | VID -0.098 | VID -0.120 | VID -0.142 | |
| 130 | VID -0.108 | VID -0.130 | VID -0.152 | |
| 140 | VID -0.118 | VID -0.140 | VID -0.162 | |
| 150 | VID -0.128 | VID -0.150 | VID -0.172 | |
| 160 | VID -0.138 | VID -0.160 | VID -0.182 | |
| 170 | VID -0.148 | VID -0.170 | VID -0.192 | |
| 180 | VID -0.158 | VID -0.180 | VID -0.202 | |
| 190 | VID -0.168 | VID -0.190 | VID -0.212 | |
| 200 | VID -0.178 | VID -0.200 | VID -0.222 | |
| 210 | VID -0.188 | VID -0.210 | VID -0.232 | |
| 220 | VID -0.198 | VID -0.220 | VID -0.242 | |
| 230 | VID - 0.208 | VID - 0.230 | VID - 0.252 | |

Notes:

1. The VCCIN_MIN and VCCIN_MAX loadlines represent static and transient limits. Please see [Section 2.8.2.1, "VCCIN Overshoot Specifications."](#)
2. This table is intended to aid in reading discrete points on graph in [Figure 2-3, "VCCIN Static and Transient Tolerance Load Lines 1.0 mOHM."](#)
3. The loadlines specify voltage limits at the die measured at the VCCIN_SENSE and VSS_VCCIN_SENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCCIN_SENSE and VSS_VCCIN_SENSE lands. Refer to the VR13.0 PWM Server VR Vendor PWM Enabling Specification for loadline guidelines and VR implementation details.
4. The Adaptive Loadline Positioning slope is 1.00 m² (mohm) with ±22mV TOB (Tolerance of Band).

Figure 2-2. VCCIN Static and Transient Tolerance Load Lines 0.9 mOHM

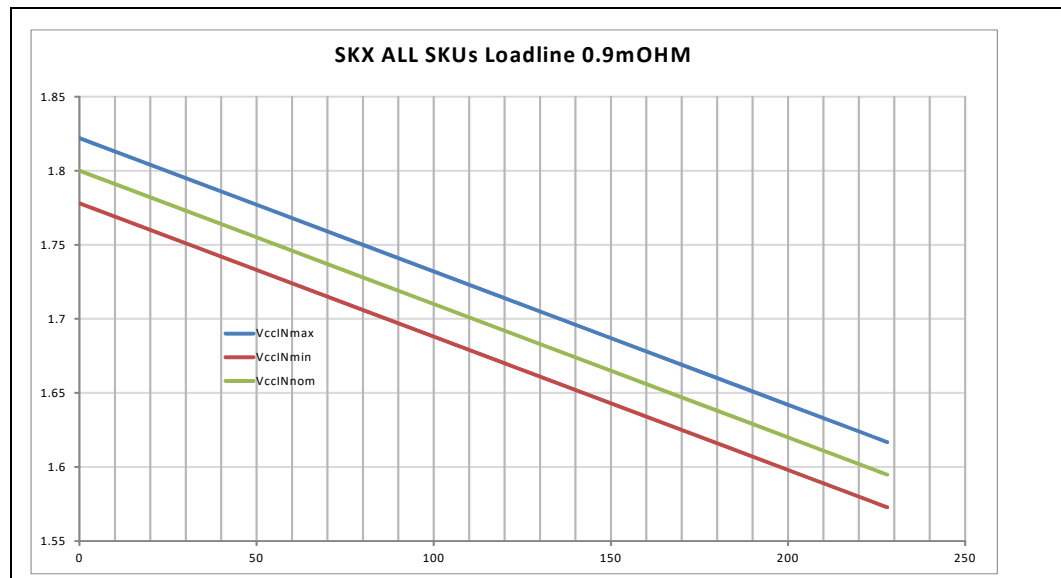




Figure 2-3. VCCIN Static and Transient Tolerance Load Lines 1.0 mOHM



2.8.2 Die Voltage Validation

Overshoot events at the processor must meet the specifications in [Table 2-17, “VCCIN Overshoot Specifications”](#) when measured across the VCCIN_SENSE and VSS_VCCIN_SENSE lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

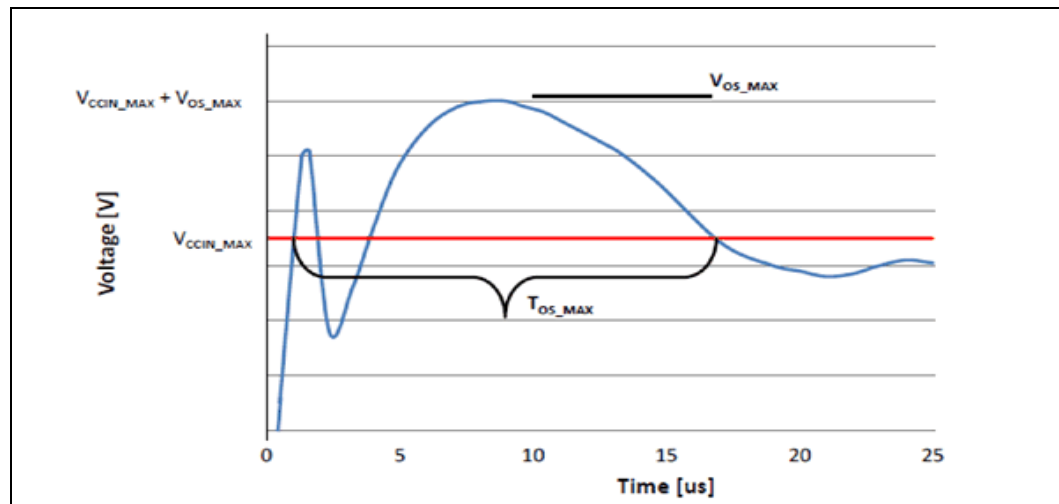
2.8.2.1 VCCIN Overshoot Specifications

The processor can tolerate short transient overshoot events where VCCIN exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + Vos_MAX (Vos_MAX is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the VCCIN_SENSE and VSS_VCCIN_SENSE lands. The processor can tolerate overshoot to phase added bumps as well.

Table 2-17. VCCIN Overshoot Specifications

| Symbol | Parameter | Min | Max | Units | Figure | Notes |
|---------|--|-----|-----------------------------|-------|----------------------------|-------|
| Vos_MAX | Magnitude of VCCIN overshoot above VID | | 92 from VID, 70 from VccMAX | mV | Figure 2-4 | |
| Tos_MAX | Time duration of VCCIN overshoot above VCCIN_Max value at the new lighter load | | 25 | µs | Figure 2-4 | |

Figure 2-4. VCCIN Overshoot Example Waveform



Notes:

1. VOS_MAX is the measured overshoot voltage above VCCIN_MAX.
2. TOS_MAX is the measured time duration above VCCIN_MAX.
3. VCCIN_MAX = VID + TOB

2.8.3 Signal DC Specifications

For additional specifications, refer to [Section 1.2, "Related Publications."](#)

2.8.3.1 DDR4 Signal DC Specifications

For the next table please use Signal Group [Table 2-7, "Signal Groups"](#) to identify which signals belong to each group.

| Symbol | Parameter | Min | Nom | Max | Units | Notes ¹ |
|--|-------------------------------------|------|---|------|-------|--------------------|
| I _{IL} | Input Leakage Current | -1.4 | | +1.4 | mA | 9 |
| Data Signals | | | | | | |
| R _{ON} | DDR4 Data Buffer On Resistance | 25.5 | 30 | 34.5 | ohm | 6 |
| Data ODT | On-Die Termination for Data Signals | 42.5 | 50 | 57.5 | ohm | 8 |
| Reference Clock and Command Signals | | | | | | |
| V _{OL} | Output Low Voltage | | $(V_{CCD} / 2) * (R_{ON} / (R_{ON} + R_{VTT_TERM}))$ | | V | 2, 7 |
| V _{OH} | Output High Voltage | | $V_{CCD} - ((V_{CCD} / 2) * (R_{ON} / (R_{ON} + R_{VTT_TERM})))$ | | V | 2, 5, 7 |
| Data Signals | | | | | | |
| V _{OL} | Output Low Voltage | | $V_{OL} = (R_{on} / (R_{on} + R_{VDD_TERM})) * V_{CCD}$ | | | 10 |
| V _{OH} | Output High Voltage | | V _{CCD} | | | |



| Symbol | Parameter | Min | Nom | Max | Units | Notes ¹ |
|-----------------------------------|--|----------------------|----------------------|----------------------|-------|--------------------|
| Reference Clock Signal | | | | | | |
| R _{ON} | DDR4 Clock Buffer On Resistance | 25.5 | 30 | 34.5 | ohm | 6 |
| Command Signals | | | | | | |
| R _{ON} | DDR4 Command Buffer On Resistance | 15.3 | 18 | 20.7 | ohm | 6,11 |
| R _{ON} | DDR4 Reset Buffer On Resistance | 76.5 | 90 | 103.5 | ohm | 6 |
| V _{OL_CMOS1.2V} | Output Low Voltage, Signals DDR_RESET_C{01/23}_N | | | 0.2*V _{CCD} | V | 1, 2 |
| V _{OH_CMOS1.2V} | Output High Voltage, Signals DDR_RESET_C{01/23}_N | 0.9*V _{CCD} | | | V | 1, 2 |
| Control Signals | | | | | | |
| R _{ON} | DDR4 Control Buffer On Resistance | 25.5 | 30 | 34.5 | ohm | 6 |
| DDR4 Miscellaneous Signals | | | | | | |
| DRAM_PWR_OK_C{01/23} | | | | | | |
| V _{IL} | Input Low Voltage | | 0.3*V _{CCD} | | mV | 2, 3 |
| V _{IH} | Input High Voltage | | 0.7*V _{CCD} | | mV | 2, 4, 5 |
| ALERT_N | | | | | | |
| V _{IL} | Input Low Voltage | V _{ref} -90 | | V _{ref} -70 | mV | 3 |
| V _{IH} | Input High Voltage | V _{ref} +70 | | V _{ref} +90 | mV | 4 |
| ODT | On Die Termination | 36 | 45 | 54 | ohms | |

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The voltage rail V_{CCD} which will be set to 1.2 V nominal depending on the voltage of all DIMMs connected to the processor.
3. V_{IL} is the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CCD}. However, input signal drivers must comply with the signal quality specifications. Refer to Section 2.10, "Signal Quality."
6. This is the pull down driver resistance. Refer to processor signal integrity models for I/V characteristics. Reset drive does not have a termination.
7. R_{VTT_TERM} is the termination on the DIMM and not controlled by the processor. Please refer to the applicable DIMM datasheet.
8. The minimum and maximum values for these signals are programmable by BIOS to one of the pairs.
9. Input leakage current is specified for all DDR4 signals.
10. Vol = Ron * [V_{CCD}/(Ron + R_{tt_Eff})], where R_{tt_Eff} is the effective pull-up resistance of all DIMMs in the system, including ODTs and series resistors on the DIMMs.
11. This Ron value is only for UDIMM, otherwise the Ron Value is 30 ohm.

2.8.3.2 PECCI DC Specifications

| Symbol | Definition and Conditions | Min | Max | Units | Figure | Notes ¹ |
|-------------------------|---|-------------------------|--------------------------|-------|------------|--------------------|
| V _{In} | Input Voltage Range | -0.15 | 0.15 + V _{CCIO} | V | | 1 |
| V _{Hysteresis} | Hysteresis | 0.1*V _{CCIO} | | V | | |
| V _N | Negative-edge threshold voltage | 0.275*V _{CCIO} | 0.500*V _{CCIO} | V | Figure 2-1 | 2 |
| V _P | Positive-edge threshold voltage | 0.550*V _{CCIO} | 0.725*V _{CCIO} | V | Figure 2-1 | 2 |
| I _{Source} | Pullup Resistance (V _{OH} = 0.75*V _{CCIO}) | -6.00 | | mA | | |



| Symbol | Definition and Conditions | Min | Max | Units | Figure | Notes ¹ |
|--------------------|---|-------------------------|------|------------------|--------|--------------------|
| I _{Leak+} | High impedance state leakage to V _{CCIO} (V _{leak} = V _{OL}) | ±50 | ±200 | μA | | 3, 4 |
| R _{ON} | High impedance leakage to GND (V _{leak} = V _{OH}) | 41 | 11 | ohm | | |
| C _{Bus} | Bus capacitance per node | | 10 | pF | | 5 |
| V _{Noise} | Signal noise immunity above 300 MHz | 0.100*V _{CCIO} | | V _{p-p} | | |
| | Output Edge Rate (50 ohm to V _{SS} , between V _{IL} and V _{IH}) | 5 | 15 | V/ns | | |

Notes:

1. The input voltage range specifies an overshoot/undershoot that applies only to the PECl data signal and not to the V_{TT} reference itself.
2. It is expected that the PECl driver will take into account, the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits (-0.150 V to 0.275*V_{CCIO} for the low level and 0.725*V_{CCIO} to V_{CCIO}+0.150 V for the high level).
3. V_{CCIO} nominal levels will vary between processor families. All PECl devices will operate at the V_{CCIO} level determined by the processor installed in the system.
4. The leakage specification applies to powered devices on the PECl bus.
5. Excessive capacitive loading on the PECl line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.

2.8.3.3 System Reference Clock (BCLK{0/1/2}) DC Specifications

| Symbol | Parameter | Signal | Min | Max | Unit | Figure | Notes ¹ |
|---------------------------|---------------------------------|--------------|---|--|------|---------------------------|--------------------|
| V _{BCLK_diff_ih} | Differential Input High Voltage | Differential | 0.150 | N/A | V | Figure 2-5 | 9 |
| V _{BCLK_diff_il} | Differential Input Low Voltage | Differential | | -0.150 | V | Figure 2-5 | 9 |
| V _{cross (abs)} | Absolute Crossing Point | Single Ended | 0.250 | 0.550 | V | Figure 2-6 and Figure 2-7 | 2, 4, 7, 9 |
| V _{cross (rel)} | Relative Crossing Point | Single Ended | 0.250 + 0.5*(V _{Havg} - 0.700) | 0.550 + 0.5*(V _{avg} - 0.700) | V | Figure 2-6 | 3, 4, 5, 9 |
| V _{cross} | Range of Crossing Points | Single Ended | N/A | 0.140 | V | Figure 2-8 | 6, 9 |
| V _{TH} | Threshold Voltage | Single Ended | V _{cross} - 0.1 | V _{cross} + 0.1 | V | | 9 |
| I _{IL} | Input Leakage | N/A | | 1.50 | mA | | 8, 9 |
| C _{pad} | Pad Capacitance | N/A | 1.90 | 1.72 | pF | | 9 |

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
3. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
4. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
5. V_{Havg} can be measured directly using "V_{top}" on Agilent* and "High" on Tektronix oscilloscopes.
6. V_{CROSS} is defined as the total variation of all crossing voltages as defined in Note 3.
7. The rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
8. For V_{in} between 0 and V_{IH}.
9. Specifications can be validated at the pin.



Figure 2-5. BCLK{0/1/2} Differential Clock Measurement Point for Ringback



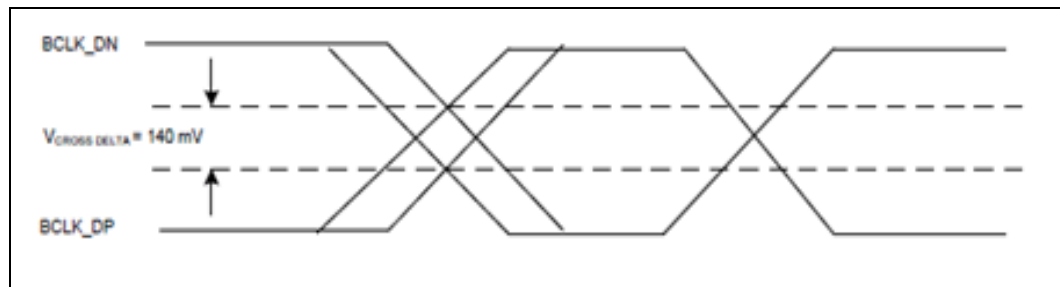
Figure 2-6. BCLK{0/1/2} Differential Clock Crosspoint Specification



Figure 2-7. BCLK{0/1/2} Single Ended Clock Measurement Points for Absolute Cross Point and Swing



Figure 2-8. BCLK{0/1/2} Single Ended Clock Measure Points for Delta Cross Point



2.8.3.4 SMBus DC Specifications

| Symbol | Parameter | Min | Max | Units | Notes |
|-------------------------|---|-----------------------|-----------------------|-------|-------|
| V _{IL} | Input Low Voltage | | 0.3*V _{CCIO} | V | |
| V _{IH} | Input High Voltage | 0.7*V _{CCIO} | | V | |
| V _{Hysteresis} | Hysteresis | 0.1*V _{CCIO} | | V | |
| V _{OL} | Output Low Voltage | | 0.2*V _{CCIO} | V | 1 |
| R _{ON} | Buffer On Resistance | 14 | 4 | ohm | |
| I _L | Leakage Current Signals | ±50 | ±200 | µA | |
| | Output Edge Rate (50 ohm to V _{CCIO} , between V _{IL} and V _{IH}) | 1.13 | 5 | V/ns | 1 |

Note:

- Value obtained through test bench with 50 ohm pull up to V_{CCIO}.

2.8.3.5 JTAG and TAP Signals DC Specifications

| Symbol | Parameter | Min | Max | Units | Notes |
|-------------------------|---|-----------------------|-----------------------|-------|-------|
| V _{IL} | Input Low Voltage | | 0.3*V _{CCIO} | V | |
| V _{IH} | Input High Voltage | 0.7*V _{CCIO} | | V | |
| V _{OL} | Output Low Voltage | | 0.2*V _{CCIO} | V | |
| V _{Hysteresis} | Hysteresis | 0.1*V _{CCIO} | | | |
| SR | Input Slew Rate: TCK0, TCK1, BPM_N[7:0], TDI | 0.05 | | V/ns | 2 |
| R _{ON} | Buffer On Resistance Signals BPM_N[7:0], TDO | 14 | 4 | ohm | |
| I _{IL} | Input Leakage Current Signals | ±50 | ±200 | µA | |
| SR | Output Edge Rate (50 ohm to V _{CCIO}) Signal: BPM_N[7:0], PRDY_N, TDO | 1.13 | 5 | V/ns | 1 |

Notes:

- These are measured between V_{IL} and V_{IH}.
- The signal edge rate must be met or the signal must transition monotonically to the asserted state.



2.8.3.6 Serial VID Interface (SVID) DC Specifications

| Symbol | Parameter | Min | Nom | Max | Units | Notes |
|-------------------------|--|------------------------|-----|------------------------|-------|-------|
| V _{CCIO} | CPU I/O Voltage | V _{CCIO} - 5% | 1.0 | V _{CCIO} + 5% | V | 1 |
| V _{IL} | Input Low Voltage Signals SVIDDATA, SVIDALERT_N | | | 0.3*V _{CCIO} | V | 1 |
| V _{IH} | Input High Voltage Signals SVIDDATA, SVIDALERT_N | 0.7*V _{CCIO} | | | V | 1 |
| V _{OL} | Output Low Voltage Signals: SVIDCLK, SVIDDATA | | | 0.2*V _{CCIO} | V | 1, 6 |
| V _{Hysteresis} | Hysteresis | 0.1*V _{CCIO} | | | V | 1 |
| R _{ON} | Buffer On Resistance Signals SVIDCLK, SVIDDATA | 14 | | 4 | ohm | 2 |
| I _{IL} | Input Leakage Current | ±50 | | ±200 | µA | 3,4 |
| | Input Edge Rate Signal: SVIDALERT_N | 0.05 | | | V/ns | 5 |
| | Output Edge Rate | 1.13 | | 5 | V/ns | 5, 6 |

Notes:

1. V_{CCIO} refers to instantaneous V_{CCIO}.
2. Measured at 0.31*V_{CCIO}.
3. Vin between 0V and V_{CCIO} (applies to SVIDDATA and SVIDALERT_N only).
4. These are measured between V_{IL} and V_{IH}.
5. Value obtained through test bench with 50? pull up to V_{CCIO}.

2.8.3.7 Processor Asynchronous Sideband DC Specifications

| Symbol | Parameter | Min | Max | Units | Notes |
|----------------------------------|-------------------------|-----------------------|-----------------------|-------|--------|
| CMOS Output Buffers | | | | | |
| I _{IL} | Input Leakage Current | ±50 | ±200 | µA | 1,2,4 |
| V _{OL} | Low Output Voltage | | 0.2*V _{CCIO} | V | 1,2,4 |
| V _{OH} | High Output Voltage | 0.9*V _{CCIO} | | V | 1,2,4 |
| R _{PD} | Pull down Resistance | | 50 | ohm | 1,2,4 |
| R _{PU} | Pull up Resistance | | 50 | ohm | 1,2,4 |
| SR | Output Edge Rate | 0.8 | 3 | V/ns | |
| CMOS Input Buffers | | | | | |
| V _{IL} | Input Low Voltage | | 0.3*V _{CCIO} | V | 1, 2,4 |
| V _{IH} | Input High Voltage | 0.7*V _{CCIO} | | V | 1, 2,4 |
| V _{Hysteresis} | Hysteresis Signals | 0.1*V _{CCIO} | | V | 1,2,4 |
| SR ₁ | Input Slew Rate | 0.005 | | V/ns | |
| SR ₂ | Input Slew Rate: PMSYNC | 0.05 | | V/ns | |
| Open Drain Output Buffers | | | | | |
| I _L | Input Leakage Current | ±50 | ±200 | µA | 1,2,4 |
| R _{ON} | Buffer On Resistance | 14 | 4 | ohm | 1, 2,4 |
| SR | Output Edge Rate | 1.13 | 5 | V/ns | 3,5 |

Notes:

1. This table applies to processor sideband and miscellaneous signals specified in Table 2-7, "Signal Groups."
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. These are measured between V_{IL} and V_{IH}.
4. In the case of bidirectional signals they use either a CMOS output /CMOS input buffer or they use Open Drain / CMOS input buffer.
5. VOL level for open drain buffers may be obtained with the Buffer ON Resistance and the external 50 ohm pull up to V_{CCIO}.



2.8.3.8 Miscellaneous Signals DC Specifications

| Symbol | Parameter | Min | Nominal | Max | Units |
|------------------------|-----------------------------|-----|---------|------|-------|
| SKTOCC_N Signal | | | | | |
| V _{O_ABS_MAX} | Output Absolute Max Voltage | | 3.30 | 3.50 | V |
| I _{OMAX} | Output Max Current | | | 1 | mA |

2.8.3.9 Intel® Omni-Path Host Fabric Interface (Intel® OP HFI) DC Specifications

| Symbol | Parameter | Min | Max | Units | Notes |
|------------------------------|-----------------------|------|------|-------|-------|
| CMOS 2.5V Inputs | | | | | |
| V _{IL} | Input Low Voltage | | 0.7 | V | |
| V _{IH} | Input High Voltage | 1.7 | | V | |
| CMOS 1.8V Inputs | | | | | |
| V _{IL} | Input Low Voltage | | 0.63 | V | |
| V _{IH} | Input High Voltage | 1.17 | | V | |
| Open Drain 2.5 Output | | | | | |
| I _L | Input Leakage Current | ±50 | ±200 | uA | |
| R _{ON} | Buffer On Resistance | 32 | 20 | ohm | |
| CMOS 1.8 Output | | | | | |
| V _{OL} | Low Output Voltage | | 0.45 | V | |
| V _{OH} | High Output Voltage | 1.3 | | V | |
| R _{PD} | Pull down Resistance | 32 | 20 | ohm | |
| R _{PU} | Pull up Resistance: | 32 | 20 | ohm | |

2.9 Package C-State Power Specifications

The table below lists the processor package C-state power specifications for the various processor SKUs.

| Die Type | C6 (W) |
|----------|--------|
| XCC | 13 |
| HCC | 12 |
| LCC | 12 |

Notes:

1. SKUs are subject to change. Please contact your Intel Field Representative to obtain the latest SKU information.
2. Package C6 power specified at T_{case} = 50°C.



2.10 Signal Quality

Data transfer requires the clean reception of data signals and clock signals. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swings will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded.

Overshoot and undershoot can also cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation. All specifications are specified at the processor die (pad measurements).

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. Therefore, proper simulation is the only way to verify proper timing and signal quality.

2.10.1 DDR Signal Quality Specifications

Various scenarios for the DDR Signals have been simulated to generate a set of layout guidelines.

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below VSS. The overshoot/undershoot specifications limit transitions beyond specified maximum voltages or VSS due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in [Table 2-18, "Processor I/O Overshoot/Undershoot Specifications"](#) ensure reliable IO performance for the lifetime of the processor.

2.10.2 PCIe Signal Quality Specifications

Signal Quality specifications for PCIe Signals are included as part of the PCIe DC specifications and PCIe AC specifications. Various scenarios have been simulated to generate a set of layout guidelines.

2.10.3 Intel® Ultra Path Interconnect (Intel® UPI) Signal Quality Specifications

Signal Quality specifications for Differential Intel® UPI Signals are included as part of the Intel® UPI defined in the Intel® Ultra Path Interconnect (Intel® UPI) Specifications.



2.10.4 Input Reference Clock Signal Quality Specifications

Overshoot/Undershoot and Ringback specifications for BCLK{0/1}_D[N/P] are found in Table 2-18, "Processor I/O Overshoot/Undershoot Specifications." Overshoot/Undershoot and Ringback specifications for the DDR4 Reference Clocks are specified by the DIMM manufacturer.

2.10.5 Overshoot/Undershoot Tolerance

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below VSS, see Figure 2-9, "Maximum Acceptable Overshoot/Undershoot Waveform." The overshoot/undershoot specifications limit transitions beyond VCCD or VSS due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in the following table will insure reliable IO performance for the lifetime of the processor.

Table 2-18. Processor I/O Overshoot/Undershoot Specifications

| Signal Group | Maximum Undershoot | Maximum Overshoot | Overshoot Duration | Undershoot Duration | Notes |
|---|------------------------|-----------------------------|---------------------|---------------------|---------|
| DDR4 | $-0.22 \cdot V_{CCD}$ | $1.22 \cdot V_{CCD}$ | $0.25 \cdot T_{CH}$ | $0.1 \cdot T_{CH}$ | 1,2,3,5 |
| Processor Asynchronous Sideband Signals, SVID, miscellaneous and JTAG/Tap Signals | $-0.35 \cdot V_{CCIO}$ | $1.35 \cdot V_{CCIO}$ | 1.25ns | 0.5ns | 1,2,5 |
| System Reference Clock (BCLK{0/1/2}) | -0.15V | 1.15V | N/A | N/A | 1,2,5 |
| PWRGOOD Signal | -0.42V | $V_{CCIO} + 0.28 \text{ V}$ | 5ns | 5ns | 1,2,4 |
| PMSYNC Signal | $-0.35 \cdot V_{CCIO}$ | $1.35 \cdot V_{CCIO}$ | 5ns | 5ns | 1,2 |
| PMSYNC_CLK Signal | -0.3V | 1.35V | 5ns | 5ns | 1,2 |
| PECI Signal | -0.35V | 1.35V | 5ns | 5ns | 1,2 |
| SVIDDATA Signal | -0.3V | 1.3V | 10ns | 10ns | 1,2 |

Notes:

1. These specifications are computer simulated at the processor pad (inside the CPU package).
2. Refer to Figure 2-9, "Maximum Acceptable Overshoot/Undershoot Waveform" for description of allowable Overshoot/Undershoot magnitude and duration.
3. T_{CH} is the minimum high pulse width duration.
4. For PWRGOOD DC specifications see Section 2.8.3.7, "Processor Asynchronous Sideband DC Specifications"
5. Refer to Table 2-7, "Signal Groups" for a list of signals under the different signal groups, except for the signals that are explicitly listed on this table.



2.10.5.1 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both are referenced to VSS. It is important to note that the overshoot and undershoot conditions are separate and their impact must be determined independently.

2.10.5.2 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage cannot be subtract the total overshoot/undershoot pulse duration.

Figure 2-9. Maximum Acceptable Overshoot/Undershoot Waveform



2.10.5.3 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the processor is not a simple single value. Instead, many factors are needed to determine the over/undershoot specification. In addition to the magnitude of the overshoot the width of the overshoot is needed. To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the signal group a particular signal falls into.
2. Determine the magnitude of the overshoot or the undershoot (relative to nominal Voltage or VSS).
3. Determine the duration of the undershoot or the overshoot.
4. Compare the values obtained with the maximum overshoot/undershoot magnitude and duration specification.



Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

2.10.5.4 Determining if a System Meets the Overshoot/Undershoot Specifications

The overshoot/undershoot specifications listed in the table specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most signals will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration and magnitude). To ensure a signal passes the overshoot and undershoot specifications, measure the worst case pulse duration and the worst case magnitude and compare the results against the specifications. If all of these worst case overshoot or undershoot events meet the specifications then the signal passes. If they do not meet the specification, please contact the Intel Representative.

§





3 Processor Land Listing

Please refer to [Appendix A, "Pin Listing."](#)

§





4 Signal Descriptions

This chapter describes the Second Generation Intel® Xeon® Scalable Processors signals. They are arranged in functional groups according to their associated interface or category.

4.1 System Memory Interface

Table 4-1. Memory Channel DDR0, DDR1, DDR2, DDR3, DDR4, DDR5

| Signal Name | Description |
|--|---|
| DDR{5:0}_ACT_N | Activate. When asserted, indicates MA[16:14] are command signals (RAS_N, CAS_N, WE_N). |
| DDR{5:0}_ALERT_N | Parity Error detected by the DIMM (one for each channel). |
| DDR{5:0}_BA[1:0] | Bank Address. Defines which bank is the destination for the current Activate, Read, Write, or Precharge command. |
| DDR{5:0}_BG[1:0] | Bank Group: Defines which bank group is the destination for the current Active, Read, Write or Precharge command. BG0 also determines which mode register is to be accessed during a MRS cycle. |
| DDR{5:0}_CID[2] | 3DS DRAM Chip ID signal |
| DDR{5:0}_CKE[3:0] | Clock Enable. |
| DDR{5:0}_CLK_DN[3:0] DDR{5:0}_CLK_DP[3:0] | Differential clocks to the DIMM. All command and control signals are valid on the rising edge of clock. |
| DDR{5:0}_CS_N[7:0] | Chip Select. Each signal selects one rank as the target of the command and address. CS_N[7:6] are MUXed with CID[4:3], respectively. CS_N[3:2] are MUXed with CID[1:0], respectively. |
| DDR{5:0}_DQ[63:0] | Data Bus. DDR4 Data bits. |
| DDR{5:0}_DQS_DP[17:0] DDR{5:0}_DQS_DN[17:0] | Data strobes. Differential pair, Data/ECC Strobe. Differential strobes latch data/ECC for each DRAM. Different numbers of strobes are used depending on whether the connected DRAMs are x4,x8. Driven with edges in center of data, receive edges are aligned with data edges. |
| DDR{5:0}_ECC[7:0] | Check bits. An error correction code is driven along with data on these lines for DIMMs that support that capability |
| DDR{5:0}_MA[17:0] | Memory Address. Selects the Row address for Reads and writes, and the column address for activates. Also used to set values for DRAM configuration registers. MA[16], MA[15], and MA[14] are multi-function and MUXed with RAS_N, CAS_N, and WE_N, respectively. <i>Note:</i> MA[17] is not used on Second Generation Intel® Xeon® Scalable Processors It is reserved for future processor implementations on the platform. The pin still requires to be routed appropriately on the board to support future drop-in compatibility. |
| DDR{5:0}_PAR | Even parity across Address and Command. |
| DDR{5:0}_ODT[3:0] | On Die Termination. Enables DRAM on die termination during Data Write or Data Read transactions. |



Table 4-2. Memory Channel Miscellaneous

| Signal Name | Description |
|--------------------------|---|
| DDR {012,345}_RESET_N | System memory reset: Reset signal from processor to DRAM devices on the DIMMs. DDR012_RESET_N is used for memory channels 0, 1 and 2 while DDR345_RESET_N is used for memory channels 3, 4 and 5. |
| DDR{012,345}_SPDSCL | SMBus clock for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SCL_C012 is used for memory channels 0, 1 and 2 while DDR_SCL_C345 is used for memory channels 3, 4 and 5. |
| DDR{012,345}_SPDSDA | SMBus data for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SDA_C012 is used for memory channels 0, 1 and 2 while DDR_SDA_C345 is used for memory channels 3, 4 and 5. |
| DDR{5:0}_CAVREF | DIMM Command address VREF signal |
| DDR{012,345}_DRAM_PWR_OK | Power good for VCCD rail used by the DRAM. This is an input signal used to indicate the VCCD power supply is stable for memory channels 0, 1, 2 and channels 3, 4, 5. |
| DDR{012,345}_RCOMP[2:0] | DDR Compensation resistance control |

4.2 PCI Express* Based Interface Signals

Note: PCI Express* Ports 1, 2 and 3 Signals are receive and transmit differential pairs.

Table 4-3. PCI Express Signals

| Signal Name | Description |
|------------------------|---------------------------|
| PE{3:1}_RX_DN/DP[15:0] | PCIe Receive Data Input |
| PE{3:1}_TX_DN/DP[15:0] | PCIe Transmit Data Output |

Table 4-4. PCI Express Miscellaneous Signals

| Signal Name | Description |
|-----------------|--|
| PE_HP_SCL | PCI Express Hot-Plug SMBus Clock: Provides PCI Express* hot-plug support via a dedicated SMBus interface. Requires an external general purpose input/output (GPIO) expansion device on the platform. |
| PE_HP_SDA | PCI Express Hot-Plug SMBus Data: Provides PCI Express* hot-plug support via a dedicated SMBus interface. Requires an external general purpose input/output (GPIO) expansion device on the platform. |
| PE{012,3}_RBIAS | 50 ohm bias resistor for PCI Express |

4.3 DMI3 Signals

Table 4-5. DMI3 Signals

| Signal Name | Description |
|-------------------|---------------------------|
| DMI_RX_DN/DP[3:0] | DMI3 Receive Data Input |
| DMI_TX_DN/DP[3:0] | DMI3 Transmit Data Output |



4.4 Intel® Ultra Path Interconnect (Intel® UPI) Signals

Table 4-6. Intel® UPI Signals

| Signal Name | Description |
|-------------------------|-------------------------------------|
| UPI{2:1}_RX_DN/DP[19:0] | Intel® UPI Receive data input. |
| UPI{2:1}_TX_DN/DP[19:0] | Intel® UPI Transmit data output. |
| UPI{01,2}_RBIAS | 50 ohm bias resistor for Intel® UPI |

4.5 PECCI Signal

Table 4-7. PECCI Signal

| Signal Name | Description |
|-------------|---|
| PECCI | PECCI (Platform Environment Control Interface) is the serial sideband interface to the processor and is used primarily for thermal, power and error management. |

4.6 System Reference Clock Signals

Table 4-8. System Reference Clock (BCLK{0/1/2}) Signals

| Signal Name | Description |
|-------------------|--|
| BCLK{0,1,2}_DN/DP | Reference Clock Differential input. These pins provide the required reference inputs to various PLLs inside the processor, such as Intel® UPI and PCIe. BCLK0, BCLK1 and BCLK2 run at 100 MHz from the same clock source. |

4.7 JTAG and TAP Signals

Table 4-9. JTAG and TAP Signals

| Signal Name | Description |
|-------------|--|
| BPM_N[7:0] | Breakpoint and Performance Monitor Signals: I/O signals from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. These are 100 MHz signals. |
| PRDY_N | Probe Mode Ready is a processor output used by debug tools to determine processor debug readiness. |
| PREQ_N | Probe Mode Request is used by debug tools to request debug operation of the processor. |
| TCK | TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port). |
| TDI | TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support. |
| TDO | TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support. |
| TMS | TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. |
| TRST_N | TRST_N (Test Reset) resets the Test Access Port (TAP) logic. TRST_N must be driven low during power on Reset. |



4.8 Serial VID Interface (SVID) Signals

Table 4-10. SVID Signals

| Signal Name | Description |
|-------------------|----------------------|
| SVIDALERT_N [1:0] | Serial VID alert. |
| SVIDCLK [1:0] | Serial VID clock. |
| SVIDDATA [1:0] | Serial VID data out. |

4.9 Processor Asynchronous Sideband and Miscellaneous Signals

Table 4-11. Processor Asynchronous Sideband Signals (Sheet 1 of 2)

| Signal Name | Description |
|----------------------|--|
| CATERR_N | Indicates that the system has experienced a fatal or catastrophic error and cannot continue to operate. The processor will assert CATERR_N for unrecoverable machine check errors and other internal unrecoverable errors. It is expected that every processor in the system will wire-OR CATERR_N for all processors. Since this is an I/O land, external agents are allowed to assert this land which will cause the processor to take a machine check exception. The CATERR_N signal can be sampled any time after 1.5 ms after the assertion of PWRGOOD. On Second Generation Intel® Xeon® Scalable Processors, CATERR_N is used for signaling the following types of errors: <ul style="list-style-type: none"> Legacy MCERR's, CATERR_N is asserted for 16 BCLKs. |
| ERROR_N[2:0] | Error status signals for integrated I/O (IIO) unit: 0 = Hardware correctable error (no operating system or firmware action necessary) 1 = Non-fatal error (operating system or firmware action required to contain and recover) 2 = Fatal error (system reset likely required to recover) |
| MEM_HOT_C{012/345}_N | Memory throttle control. Signals external BMC-less controller that DIMM is exceeding temperature limit and needs to increase to max fan speed. MEM_HOT_C012_N and MEM_HOT_C345_N signals have two modes of operation - input and output mode. Input mode is externally asserted and is used to detect external events such as VR_HOT# from the memory voltage regulator and causes the processor to throttle the appropriate memory channels. Output mode is asserted by the processor known as level mode. In level mode, the output indicates that a particular branch of memory subsystem is hot. MEM_HOT_C012_N is used for memory channels 0,1 & 2 while MEM_HOT_C345_N is used for memory channels 3, 4 & 5. |
| MSMI_N | Machine Check Exception (MCE) is signaled via this pin when eMCA2 is enabled. The MSMI_N signal can be sampled any time after 1.5 ms after the assertion of PWRGOOD |
| PMSYNC | Power Management Sync. A sideband signal to communicate power management status from the Platform Controller Hub (PCH) to the processor. |
| PMSYNC_CLK | 24 MHz SE Clock used for PCH PMSYNC. |
| PROCHOT_N | PROCHOT_N will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal can also be driven to the processor to activate the Thermal Control Circuit. This signal is sampled after PWRGOOD assertion. |



Table 4-11. Processor Asynchronous Sideband Signals (Sheet 2 of 2)

| Signal Name | Description |
|-------------|--|
| PWRGOOD | <p>PWRGOOD is a processor input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications.</p> <p>“Clean” implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state.</p> <p>PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. PWRGOOD transitions from inactive to active when all supplies except VCCIN are stable. The signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.</p> |
| RESET_N | <p>Global reset signal. Asserting the RESET_N signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. Note some PLL, Intel UPI and error states are not affected by reset and only PWRGOOD forces them to a known state.</p> |
| THERMTRIP_N | <p>Assertion of THERMTRIP_N (Thermal Trip) indicates one of two possible critical over-temperature conditions: One, the processor junction temperature has reached a level beyond which permanent silicon damage may occur and Two, the system memory interface has exceeded a critical temperature limit set by BIOS. Measurement of the processor junction temperature is accomplished through multiple internal thermal sensors that are monitored by the Digital Thermal Sensor (DTS). Simultaneously, the Power Control Unit (PCU) monitors external memory temperatures via the dedicated SMBus interface to the DIMMs. If any of the DIMMs exceed the BIOS defined limits, the PCU will signal THERMTRIP_N to prevent damage to the DIMMs. Once activated, the processor will stop all execution and shut down all PLLs. To further protect the processor, its core voltage (VCCIN), VCCD, VCCIO, VCCIO supplies must be removed following the assertion of THERMTRIP_N. Once activated, THERMTRIP_N remains latched until RESET_N is asserted. While the assertion of the RESET_N signal may de-assert THERMTRIP_N, if the processor's junction temperature remains at or above the trip level, THERMTRIP_N will again be asserted after RESET_N is de-asserted. This signal can also be asserted if the system memory interface has exceeded a critical temperature limit set by BIOS. The THERMTRIP_N signal can be sampled any time after 1.5 ms after the assertion of PWRGOOD</p> |

Table 4-12. Miscellaneous Signals (Sheet 1 of 3)

| Signal Name | Description |
|------------------|---|
| BIST_ENABLE | <p>BIST Enable Strap. Input which allows the platform to enable or disable built-in self test (BIST) on the processor. This signal is pulled up on the die. Refer to Table 2-8, “Signals with On-Die Weak PU/PD” for details.</p> |
| BMCINIT | <p>BMC Initialization Strap. Indicates whether Service Processor Boot Mode should be used. Used in combination with FRMAGENT and SOCKET_ID inputs.</p> <p>0 Service Processor Boot Mode Disabled. Example boot modes: Local PCH (this processor hosts a legacy PCH with firmware behind it)</p> <p>1 Service Processor Boot Mode Enabled. In this mode of operation, the processor performs the absolute minimum internal configuration and then waits for the Service Processor to complete its initialization. The socket boots after receiving a “GO” handshake signal via a firmware scratchpad register.</p> <p>This signal is pulled down on the die, refer to Table 2-8, “Signals with On-Die Weak PU/PD” for details.</p> |
| DEBUG_EN_N | <p>This pin is used to force debug to be enabled when the ITP is connected to the main board. This allows debug to occur beginning from cold boot.</p> |
| DMIMODE_OVERRIDE | <p>BMCINIT, DMIMODE_OVERRIDE, FRMAGENT, and LEGACY_SKT, whether local or remote, whether the boot PCH is attached, whether the socket is legacy and whether port0 is DMI or PCIe.</p> |



Table 4-12. Miscellaneous Signals (Sheet 2 of 3)

| Signal Name | Description |
|----------------|--|
| EAR_N | External Alignment of Reset, used to bring the processor up into a deterministic state. This signal is pulled up on the die, refer to Table 2-8, "Signals with On-Die Weak PU/PD" for details. |
| FIVR_FAULT | Indicates an internal error has occurred with the integrated voltage regulator. The FIVR_FAULT signal can be sampled any time after 1.5 ms after the assertion of PWRGOOD. FIVR_FAULT must be qualified by THERMTRIP_N assertion. |
| FRMAGENT | Bootable Firmware Agent Strap. This input configuration strap used in combination with SOCKET_ID to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI3 mode). The firmware flash ROM is located behind the local PCH attached to the processor via the DMI3 interface. This signal is pulled down on the die, refer to Table 2-8, "Signals with On-Die Weak PU/PD" for details. |
| PM_FAST_WAKE_N | Power Management Fast Wake. Enables quick package C3 - C6 exits of all sockets. Asserted if any socket detects a break from package C3 - C6 state requiring all sockets to exit the low power state to service a snoop, memory access, or interrupt. Expected to be wired-OR among all processor sockets within the platform. |
| PROC_ID [1:0] | This output can be used by the platform to determine if the installed processor is a Second Generation Intel® Xeon® Scalable Processors or a future processor. There is no connection to the processor silicon for this signal. The processor package grounds or floats the pin to set '0' or '1', respectively. Second Generation Intel® Xeon® Scalable Processors 00: Second Generation Intel® Xeon® Scalable Processors 01: Reserved 10: Reserved 11: Reserved Intel Xeon processor-W Family 00: Reserved 01: Reserved 10: Future Processor 11: Intel Xeon processor-W Family |
| RSVD | RESERVED. All signals that are RSVD must be left unconnected on the board. |
| SAFE_MODE_BOOT | Safe Mode Boot Strap. SAFE_MODE_BOOT allows the processor to wake up safely by disabling all clock gating. This allows BIOS to load registers or patches if required. This signal is sampled after PWRGOOD assertion. The signal is pulled down on the die. Refer to Table 2-8, "Signals with On-Die Weak PU/PD" for details. |
| SKTOCC_N | SKTOCC_N (Socket Occupied) is used to indicate that a processor is present. This is pulled to ground on the processor package; there is no connection to the processor silicon for this signal. |
| SOCKET_ID[2:0] | SOCKET_IDStrap. Socket identification configuration straps for establishing the PECl address and Intel UPI Node ID. This signal is used in combination with FRMAGENT to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI3 mode). Each processor socket consumes one Node ID, and there are 128 Home Agent tracker entries. This signal is pulled down on the die. Refer to Table 2-8, "Signals with On-Die Weak PU/PD" for details. SOCKET_ID[1:0] is used for 2S platforms and SOCKET_ID[2:0] is implemented on 4S/8S platforms. This is an asynchronous signal to other clocks in the processor. |
| TEST[15:1] | TEST[14:13], TEST[2:1]] must be individually connected to an appropriate power source or ground through a resistor for proper processor operation. |



Table 4-12. Miscellaneous Signals (Sheet 3 of 3)

| Signal Name | Description |
|-------------|---|
| TXT_AGENT | Intel® Trusted Execution Technology (Intel® TXT) Agent Strap. 0 = Default. The socket is not the Intel® TXT Agent. 1 = The socket is the Intel® TXT Agent. The legacy socket (identified by SOCKET_ID[1:0] = 00b) with Intel® TXT Agent should always set the TXT_AGENT to 1b. This signal is pulled down on the die, refer to Table 2-8, "Signals with On-Die Weak PU/PD" for details. |
| TXT_PLTEN | Intel® Trusted Execution Technology (Intel® TXT) Platform Enable Strap. 0 = The platform is not Intel® TXT enabled. All sockets should be set to zero. Scalable DP (sDP) platforms should choose this setting if the Node Controller does not support Intel® TXT. 1 = Default. The platform is Intel® TXT enabled. All sockets should be set to one. In a non-Scalable DP platform this is the default. When this is set, Intel® TXT functionality requires user to explicitly enable Intel® TXT via BIOS setup. This signal is pulled up on the die, refer to Table 2-8, "Signals with On-Die Weak PU/PD" for details. |
| LEGACY_SKT | BMCINIT, FRMAGENT, LEGACY_SKT together determine the boot mode (SSP, Intel® UPI Link boot modes, DCF boot), whether local or remote, whether the boot PCH is attached, whether the socket is legacy and whether port0 is DMI or PCIe (Gen1/2). With one exception, this input configuration strap indicates to the processor that it is the legacy socket. The legacy SKT must be strapped for NODE ID 0, via the SKIT ID pins. There is only 1 legacy SKT in a partition. |
| PKGID[2:0] | An indicator to the Second Generation Intel® Xeon® Scalable Processors-based platform of the Intel® Omni-Path Technology configuration. |
| PROCDIS_N | PROCDIS_N assert initiates FRB and tri-states the processor. |
| PWR_DEBUG_N | This is a debug signal for power debug using Intel® In-Target Probe on the |
| SOCKET_ID2 | Asynchronous to other clocks in the processor. |
| TSC_SYNC | Time stamp counter sync. Used to help align the time stamp counters of a newly socket to the time stamp counters of existing sockets. |

Table 4-13. PIROM Signals

| Signal Name | Description |
|-----------------|--|
| PIROM_ADDR[2:0] | Address for PIROM (Processor Information ROM/OEM scratch pad). |
| SM_WP | WP (Write Protect) can be used to write protect the Scratch EEPROM. The Scratch EEPROM is write-protected when this input is pulled high to VCCSTBY33. |
| SMBCLK | The SMBus Clock (SMBCLK) signal is an input clock which is required for operation of PIROM. This clock is driven by the SMBus controller and is asynchronous to other clocks in the processor. |
| SMBDAT | The SMBus Data (SMBDAT) signal is the data signal for the SMBus. This signal provides the single-bit mechanism for transferring data between SMBus devices. |



Table 4-14. Intel® Omni-Path Host Fabric Interface (Intel® OP HFI) Signals

| Signal Name | Description |
|-----------------------|---|
| CD_HFI[1:0]_I2CCLK | 2-wire serial interface clock |
| CD_HFI[1:0]_I2CDAT | 2-wire serial interface data |
| CD_HFI[1:0]_INT_N | Interrupt. Used to inform the CPU that the module has encountered a potential error condition |
| CD_HFI[1:0]_LED_N | Indicates activity on the link |
| CD_HFI[1:0]_MODPRST_N | Module present |
| CD_HFI[1:0]_RESET_N | Module reset |
| CD_HFI_REFCLK_DN/DP | HFI Reference Clock |
| CD_POR_N | Power on reset for HFI ASIC |
| MCP01_RBIAS | Multi-chip Bus RBIAS |

4.10 Processor Power and Ground Supplies

Table 4-15. Power and Ground Signals (Sheet 1 of 2)

| Signal Name | Description |
|--------------------------------|---|
| V _{CCIN} | 1.8 V - 1.55 V input to the Integrated Voltage Regulator (IVR) for the processor cores, lowest level caches (LLC), ring interface, PLL, IO, and home agent. It is provided by a VR 13.0 compliant motherboard voltage regulator (MBVR) for each CPU socket. The output voltage of this MBVR is controlled by the processor, using the serial voltage ID (SVID) bus. |
| VCCIN_SENSE VSS_VCCIN_SENSE | VCCIN_SENSE and VSS_VCCIN_SENSE are remote sense signals for V _{CCIN} MBVR13.0 and are used by the voltage regulator to ensure accurate voltage regulation. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage remains within specification. |
| VCCIO_SENSE VSS_VCCIO_SENSE | VCCIO_SENSE and VSS_VCCIO_SENSE are remote sense signals for VCCIO and are used by the voltage regulator to ensure accurate voltage regulation. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage remains within specification. |
| VCCSA_SENSE VSS_VCCSA_SENSE | VCCSA_SENSE and VSS_VCCSA_SENSE are remote sense signals, and are used by the voltage regulator to ensure accurate voltage regulation. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage remains within specification. |
| CD_VCC_CORE | Companion die 0.9 V core supply |
| CD_VCCP | Companion die 1.0 V IO supply. Connects to memory voltage regulator. |
| CD_VCCIN | Companion die voltage rail tied to VCCIN through filter |
| CD_VPP | Companion die 2.5 V supply |
| CD_VCCP | Companion die 1.0 V IO supply |
| VCCIO | .95V-1.0V power supply for the processor IO. |
| VCC33 | VCC33 supplies 3.3 V to PIROM/OEM Scratch ROM. This supply is required for PIROM usage. |
| VCCIO | .95 V - 1.0 V power supply for the processor IO. |
| VCCINPMAX | Pmax detect VCCIN supply through board R2 thermistor for VCCIN loadline temperature compensation |
| VCCSA | 1.05 V - 0.55 V supply for Intel® UPI and IIO |
| VSENSEPMAX | Pmax detect circuit output voltage |



Table 4-15. Power and Ground Signals (Sheet 2 of 2)

| Signal Name | Description |
|----------------------|--|
| VCCD_012 VCCD_345 | 1.2 V - 1.05 V power supply for the processor system memory interface. |
| VSS | Processor ground return. |
| VCCIO | IO voltage supply input. |

§





5 PIROM

5.1 Processor Information ROM

The Processor Information ROM (PIROM) is a memory device located on the processor and is accessible via the System Management Bus (SMBus) which contains information regarding the processor's features. These features are listed in [Table 5-1, "Processor Information ROM Table."](#)

The PIROM resides in the lower half of the memory component (addresses 00 to 7Fh), which is permanently write-protected by Intel. The upper half comprises the Scratch EEPROM (addresses 80 to FFh).

Table 5-1. Processor Information ROM Table (Sheet 1 of 3)

| Offset/Section | # of Bits | Function | Notes | Examples |
|----------------------------|-----------|-------------------------------|----------------------------------|---|
| Header | | | | |
| 00h | 8 | Data Format Revision | Two 4-bit hex digits | Start with 00h |
| 02-01h | 16 | PIROM Size | Size in bytes (LSB first) | Use a decimal to hex transfer; 128 bytes = 0080h: |
| 03h | 8 | Processor Data Address | Byte pointer, 00h if not present | 0Dh |
| 04h | 8 | Processor Core Data Address | Byte pointer, 00h if not present | 19h |
| 05h | 8 | Processor Uncore Data Address | Byte pointer, 00h if not present | 21h |
| 06h | 8 | Cache Data Address | Byte pointer, 00h if not present | 2Bh |
| 07h | 8 | Package Data Address | Byte pointer, 00h if not present | 31h |
| 08h | 8 | Voltage Data Address | Byte pointer, 00h if not present | 34h |
| 09h | 8 | Part Number Data Address | Byte pointer, 00h if not present | 56h |
| 0Ah | 8 | Thermal Data Address | Byte pointer, 00h if not present | 65h |
| 0Bh | 8 | Feature Data Address | Byte pointer, 00h if not present | 6Ch |
| 0Ch | 8 | PPIN Data Address | Byte pointer, 00h if not present | 77h |
| Processor Data | | | | |
| 0D to 12h | 48 | S-spec/QDF Number | Six 8-bit ASCII characters | |
| 13h | 7/1 | Sample/Production | First seven bits reserved | 0b = Sample, 1b = Production 00000001 = production |
| 14h | 8 | Number of Cores | Binary Coded Decimal | 24h=24 Cores |
| 15 | 7/1 | Hyper-Threading Support | First seven bits reserved | 0b = no Hyper-Threading, 1b = Hyper-Threading 00000001 = Hype- Threading |
| 17 to 16h | 16 | System Clock Speed | Binary Coded Decimal (Mhz) | 0100h = 100MHz ¹ |
| 18h | 8 | Reserved | Reserved for future use | 00000000 |
| Processor Core Data | | | | |
| 1A to 19h | 16 | CPUID | 4 bit Binary Coded Decimal | |
| 1B to 1Ch | 16 | Reserved | Reserved for future use | 0000000000000000 |
| 1E to 1Dh | 16 | Maximum P1 Core Frequency | 4 bit Binary Coded Decimal | 2500h = 2500 MHz ¹ |
| 20 to 1Fh | 16 | Maximum P0 Core Frequency | 4 bit Binary Coded Decimal | 2800h = 2800 MHz ¹ |



Table 5-1. Processor Information ROM Table (Sheet 2 of 3)

| Offset/Section | # of Bits | Function | Notes | Examples |
|------------------------------|-----------|---------------------------------------|------------------------------|--|
| Processor Uncore Data | | | | |
| 21h | 8 | Number of Intel® UPI Links | 4 bit Binary Coded Decimal | 03h=3 UPI links |
| 23 to 22h | 16 | Maximum Intel® UPI Link Transfer Rate | 4 bit Binary Coded Decimal | 1040h = 10.4 GT/s ¹ |
| 25 to 24h | 16 | Maximum PCIe Link Transfer Rate | 4 bit Binary Coded Decimal | 8000h = 8000 MT/s ¹ |
| 27 to 26h | 16 | Maximum DDR 1DPC Speed | 4 bit Binary Coded Decimal | 2666h = 2666 MT/S |
| 29 to 28h | 16 | Maximum DDR 2DPC Speed | 4 bit Binary Coded Decimal | 2400h = 2400 MT/s |
| 2Ah | 8 | Reserved | Reserved for future use | 00000000 |
| Cache Data | | | | |
| 2C to 2Bh | 16 | MLC Cache Size | Binary (KB) Per CPU Core | 0000010000000000h = 1024KB |
| 2E to 2Dh | 16 | LLC Cache Size | Binary (KB) | 011000000000h = 24576KB |
| 30 to 2Fh | 16 | NVM DIMM Max Capacity | Binary | Multiplier of 96 = 6TB |
| Package Data | | | | |
| 31h | 8 | Package Type | 4 bit Binary Coded Decimal | First 4 bits reserved Output decode is below |
| 32 to 33h | 16 | Reserved | Reserved for future use | 0000000000000000 |
| Voltage Data | | | | |
| 35 to 34h | 16 | Maximum VCCIN | 4 bit Binary Coded Decimal | 1800h = 1800 mV ¹ |
| 37 to 36h | 16 | Minimum VCCIN | 4 bit Binary Coded Decimal | 0600h = 600 mV ¹ |
| 39 to 38h | 16 | Maximum VCCSA | 4 bit Binary Coded Decimal | 1350h = 1350 mV ¹ |
| 3B to 3Ah | 16 | Minimum VCCSA | 4 bit Binary Coded Decimal | 0800h = 800 mV ¹ |
| 3D to 3Ch | 16 | VCCD | 4 bit Binary Coded Decimal | 1200h = 1200mV ¹ |
| 3F to 3Eh | 16 | VCCIO | 4 bit Binary Coded Decimal | 1000h = 1000mV ¹ |
| 40 to 43h | 32 | Reserved | Reserved for future use | 00000000000000000000000000000000 0000 |
| 45 to 44h | 16 | CD_VCC_CORE | 4 bit Binary Coded Decimal | 1000h = 1000mV ¹ |
| 47 to 46h | 16 | CD_VCCIN | 4 bit Binary Coded Decimal | 1000h = 1000mV ¹ |
| 49 to 48h | 16 | CD_VCCP | 4 bit Binary Coded Decimal | 1000h = 1000mV ¹ |
| 4B to 4A | 16 | CD_VPP | 4 bit Binary Coded Decimal | 1000h = 1000mV ¹ |
| 4D to 4C | 16 | RC_VCC_CORE | 4 bit Binary Coded Decimal | 1000h = 1000mV ¹ |
| 4F to 4Eh | 16 | RC_VCCH | 4 bit Binary Coded Decimal | 1000h = 1000 mV ¹ |
| 50 to 55h | 48 | Reserved | Reserved for future use | 00000000000000000000000000000000 000000000000000000000000 |
| Part Numbers | | | | |
| 5C to 56h | 56 | Processor Family Number | Seven 8-bit ASCII characters | CM80645 |
| 64 to 5Dh | 64 | Processor SKU Number | Eight 8-bit ASCII characters | 41272834 |
| Thermal Reference | | | | |
| 65h | 8 | Tcase Maximum | 4 bit Binary Coded Decimal | 69h = 69°C ¹ |
| 67 to 66h | 16 | Thermal Design Power | 4 bit Binary Coded Decimal | 0130h = 130 Watts ¹ |
| 69 to 68h | 16 | DTS Maximum | 4 bit Binary Coded Decimal | 102h = 102°C ¹ |
| 6B to 6Ah | 16 | Pn Limit | 4 bit Binary Coded Decimal | 53h = 53 Watts ¹ |



Table 5-1. Processor Information ROM Table (Sheet 3 of 3)

| Offset/Section | # of Bits | Function | Notes | Examples |
|-----------------|-----------|--------------------------------|---|---|
| Features | | | | |
| 6F to 6Ch | 32 | Processor Core Feature Flags | From CPUID function 1, EDX contents | 4387FBFFh |
| 70 to 71h | 16 | Processor Feature Flags | Up to 16 features - Binary 1 indicates functional feature | 0000000000001111 |
| 72 | 6/2 | Multiprocessor Support | 000b=1S, 001b = 2S, 010b=4S GLULS, 011b=S4S, 100b=Reserved, and 101b=S8S. | 00000101b=S8S |
| 73h | 4/4 | Number of Devices in TAP Chain | First four bits reserved One 4-bit hex digit - Bits | *0h ¹ |
| 74 to 75h | 16 | Reserved | Reserved for future use | 0000h |
| 76h | 8 | Static Checksum | 1 byte checksum | Add up by byte and take 2's complement. |
| Other | | | | |
| 7E to 77h | 64 | PPIN | Coded binary | See description |
| 7Fh | 8 | Reserved | Reserved for future use | 00000000 |

Notes:

1. Uses Binary Coded Decimal (BCD) translation.

5.2 Scratch EEPROM

Also available in the memory component on the processor SMBus is an EEPROM which may be used for other data at the system or processor vendor's discretion. The data in this EEPROM, once programmed, can be write-protected by asserting the active-high SM_WP signal. This signal has a weak pull-down (10 Kohm) to allow the EEPROM to be programmed in systems with no implementation of this signal. The Scratch EEPROM resides in the upper half of the memory component (addresses 80 - FFh). The lower half comprises the Processor Information ROM (addresses 00 - 7Fh), which is permanently write-protected by Intel.

5.3 PIROM and Scratch EEPROM Supported SMBus Transactions

The PIROM responds to two SMBus packet types: Read Byte and Write Byte. However, since the PIROM is write-protected, it will acknowledge a Write Byte command but ignore the data. The Scratch EEPROM responds to Read Byte and Write Byte commands. [Table 5-2, "Read Byte SMBus Packet"](#) illustrates the Read Byte command. [Table 5-3, "Write Byte SMBus Packet"](#) illustrates the Write Byte command.

In the tables, 'S' represents a SMBus start bit, 'P' represents a stop bit, 'A' represents an acknowledge (ACK), and 'N' represents a negative acknowledge (NACK). The shaded bits are transmitted by the PIROM or Scratch EEPROM, and the bits that aren't shaded are transmitted by the SMBus host controller. In the tables, the data addresses indicate 8 bits.

The SMBus host controller should transmit 8 bits with the most significant bit indicating which section of the EEPROM is to be addressed: the PIROM (MSB = 0) or the Scratch EEPROM (MSB = 1).



Table 5-2. Read Byte SMBus Packet

| S | Slave Address | Write | A | Command Code | A | S | Slave Address | Read | A | Data | /// | P |
|---|---------------|-------|---|--------------|---|---|---------------|------|---|--------|-----|---|
| 1 | 7-bits | 1 | 1 | 8-bits | 1 | 1 | 7-bits | 1 | 1 | 8-bits | 1 | 1 |

Table 5-3. Write Byte SMBus Packet

| S | Slave Address | Write | A | Command Code | A | Data | A | P |
|---|---------------|-------|---|--------------|---|--------|---|---|
| 1 | 7-bits | 1 | 1 | 8-bits | 1 | 8-bits | 1 | 1 |

5.4 SMBus Memory Component Addressing

Of the addresses broadcast across the SMBus, the memory component claims those of the form "10100XXZb". The "XX" bits are defined by pull-up and pull-down of the PIROM_ADDR[2:0] pins. These address pins are pulled down weakly (10 k) on the processor substrate to ensure that the memory components are in a known state in systems which do not support the SMBus (or only support a partial implementation). The "Z" bit is the read/write bit for the serial bus transaction.

Note that addresses of the form "0000XXXXb" are Reserved and should not be generated by an SMBus master.

Table 5-4, "Memory Device SMBus Addressing" describes the address pin connections and how they affect the addressing of the memory component.

Table 5-4. Memory Device SMBus Addressing

| Address (Hex) | Upper Address ¹ | Device Select | | | R/W |
|---------------|----------------------------|---------------|----------------|----------------|-------|
| | Bits 7-4 | SKTID[2] | SKTID[1] Bit 2 | SKTID[0] Bit 1 | Bit 0 |
| A0h/A1h | 10100 | 10100 | 0 | 0 | X |
| A2h/A3h | 10100 | 10100 | 0 | 1 | X |
| A4h/A5h | 10100 | 10100 | 1 | 0 | X |
| A6h/A7h | 10100 | 10100 | 1 | 1 | X |

Notes:

1. This addressing scheme will support up to four processors on a single SMBus.

5.4.1 Managing Data in the PIROM

The PIROM consists of the following sections:

- Header
- Processor Data
- Processor Core Data
- Processor Uncore Data
- Cache Data
- Package Data
- Part Number Data



- Thermal Reference Data
- Feature Data
- Other Data

Details on each of these sections are described below.

Note: Reserved fields or bits SHOULD be programmed to zeros. However, OEMs should not rely on this model.

5.4.2 Header

To maintain backward compatibility, the Header defines the starting address for each subsequent section of the PIROM. Software should check for the offset before reading data from a particular section of the ROM.

For example, Code looking for the processor uncore data of a processor would read offset 05h to find a value of 21. 21 is the first address within the 'Processor Uncore Data' section of the PIROM.

5.4.2.1 DFR: Data Format Revision

This location identifies the data format revision of the PIROM data structure. Writes to this register have no effect.

| Offset: 00h | |
|-------------|--|
| Bit | Description |
| 7:0 | <p>Data Format Revision The data format revision is used whenever fields within the PIROM are redefined. The initial definition will begin at a value of 1. If a field, or bit assignment within a field, is changed such that software needs to discern between the old and new definition, then the data format revision field will be incremented.</p> <p>00h: Reserved 01h: Initial definition 02h: Second revision 03h: Third revision 04h: Fourth revision 05h: Fifth revision 06h: Sixth revision 06h:Sixth revision 07h: Seventh revision (<i>Defined by this document</i>) 08h-FFh: Reserved</p> |

5.4.2.2 PISIZE: PIROM Size

This location identifies the PIROM size. Writes to this register have no effect.

| Offset: 02h-01h | |
|-----------------|---|
| Bit | Description |
| 15:0 | <p>PIROM Size The PIROM size provides the size of the device in hex bytes. The LSB is at location 01h; the MSB is at location 02h.</p> <p>0000h - 007Fh: Reserved 0080h: 128 byte PIROM size 0081- FFFFh: Reserved</p> |



5.4.2.3 PDA: Processor Data Address

This location provides the offset to the Processor Data Section. Writes to this register have no effect.

| Offset: 03h | |
|--------------------|--|
| Bit | Description |
| 7:0 | Processor Data Address Byte pointer to the Processor Data section 0Dh: Processor Data section pointer value |

5.4.2.4 PCDA: Processor Core Data Address

This location provides the offset to the Processor Core Data Section. Writes to this register have no effect.

| Offset: 04h | |
|--------------------|---|
| Bit | Description |
| 7:0 | Processor Core Data Address Byte pointer to the Processor Core Data section 19h: Processor Core Data section pointer value |

5.4.2.5 PUDA: Processor Uncore Data Address

This location provides the offset to the Processor Uncore Data Section. Writes to this register have no effect.

| Offset: 05h | |
|--------------------|---|
| Bit | Description |
| 7:0 | Processor Uncore Data Address Byte pointer to the Processor Uncore Data section 21h: Processor Uncore Data section pointer value |

5.4.2.6 CDA: Cache Data Address

This location provides the offset to the Cache Data Section. Writes to this register have no effect.

| Offset: 06h | |
|--------------------|--|
| Bit | Description |
| 7:0 | Cache Data Address Byte pointer to the Cache Data section 2Bh: Cache Data section pointer value |



5.4.2.7 PNDA: Package Data Address

This location provides the offset to the Package Data Section. Writes to this register have no effect.

| Offset: 07h | |
|--------------------|--|
| Bit | Description |
| 7:0 | Package Data Address Byte pointer to the Package Data section 31h: Package Data section pointer value |

5.4.2.8 VDA: Voltage Data Address

This location provides the offset to the Voltage Data Section. Writes to this register have no effect.

| Offset: 08h | |
|--------------------|--|
| Bit | Description |
| 7:0 | Voltage Data Address Byte pointer to the Voltage Data section 34h: Voltage Data section pointer value |

5.4.2.9 PNDA: Part Number Data Address

This location provides the offset to the Part Number Data Section. Writes to this register have no effect.

| Offset: 09h | |
|--------------------|--|
| Bit | Description |
| 7:0 | Part Number Data Address Byte pointer to the Part Number Data section 56h: Part Number Data section pointer value |

5.4.2.10 TRDA: Thermal Reference Data Address

This location provides the offset to the Thermal Reference Data Section. Writes to this register have no effect.

| Offset: 0Ah | |
|--------------------|--|
| Bit | Description |
| 7:0 | Thermal Reference Data Address Byte pointer to the Thermal Reference Data section 65h: Thermal Reference Data section pointer value |



5.4.2.11 FDA: Feature Data Address

This location provides the offset to the Feature Data Section. Writes to this register have no effect.

| Offset: 0Bh | |
|--------------------|--|
| Bit | Description |
| 7:0 | Feature Data Address Byte pointer to the Feature Data section 6Ch: Feature Data section pointer value |

5.4.2.12 PPIN: Protected Processor Inventory Number

This location provides the offset to the PPIN Data Section. Writes to this register have no effect.

| Offset: 0Ch | |
|--------------------|---|
| Bit | Description |
| 7:0 | PPIN Data Address Byte pointer to the PPIN Data section 77h: PPIN Data section pointer value |

5.4.3 Processor Data

This section contains five pieces of data:

- The S-spec/QDF of the part in ASCII format
- (1) 2-bit field to declare if the part is a preproduction sample or a production unit
- Core count
- Intel® Hyper-threading Technology support status
- The system bus speed in BCD format

5.4.3.1 SAMPROD: Sample/Production

This location contains the sample/production field, which is a two-bit field and is LSB aligned. All S-spec material will use a value of 01b. All other values are reserved. Writes to this register have no effect.

A processor with an Sxxxx mark (production unit) will use 01h at offset 14h.

| Offset: 13h | |
|--------------------|---|
| Bit | Description |
| 7:2 | RESERVED 000000b-111111b: Reserved |
| 1:0 | Sample/Production Sample or Production indicator 00b: Sample 01b: Production 10b-11b: Reserved |



5.4.3.2 Processor Core Information

This location contains information regarding the number of cores on the processor. Writes to this register have no effect. Data format is binary coded decimal.

| Offset: 14h | |
|-------------|--|
| Bit | Description |
| 7:0 | Number of cores 0000h-FFFFh: Cores |

5.4.3.3 Processor Thread Information

This location contains information regarding the number of cores and threads on the processor. Writes to this register have no effect. Data format is binary coded decimal.

| Offset: 15h | |
|-------------|---|
| Bit | Description |
| 7:0 | Number of threads per core 0000h-FFFFh: Threads |

5.4.3.4 SCS: System Clock Speed

This location contains the system clock frequency information. Systems may need to read this offset to decide if all installed processors support the same system clock speed. The data provided is the speed, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

For example, a processor with system bus speed of 100 MHz will have a value of 0100h.

| Offset: 17h-16h | |
|-----------------|---|
| Bit | Description |
| 15:0 | System Bus Speed 0000h-FFFFh: MHz |

5.4.3.5 RES1: Reserved 1

This location is reserved. Writes to this register have no effect.

| Offset: 18h | |
|-------------|--------------------------------------|
| Bit | Description |
| 7:0 | RESERVED 00h-FFh: Reserved |

5.4.4 Processor Core Data

This section contains silicon-related data relevant to the processor cores.



5.4.4.1 CPUID: CPUID

This location contains the CPUID, Processor Type, Family, Model and Stepping. The CPUID field is a copy of the results in EAX[15:0] from Function 1 of the CPUID instruction. For example, bit 15 is MSB in offset 1Ah and bit 0 is LSB in offset 19h. Writes to this register have no effect. Data format is hexadecimal.

| Offset: 1Ah-19h | | |
|-----------------|------|--|
| Bit | Byte | Description |
| 15:13 | 1Ah | Reserved 00b-11b: Reserved |
| 12:12 | | Processor Type 0b-1b: Processor Type |
| 11:8 | | Processor Family 0h-Fh: Processor Family |
| 7:4 | 19h | Processor Model 0h-Fh: Processor Model |
| 3:0 | | Processor Stepping 0h-Fh: Processor Stepping |

5.4.4.2 RES2: Reserved 2

This locations are reserved. Writes to this register have no effect.

| Offset: 1Bh-1Ch | |
|-----------------|--|
| Bit | Description |
| 15:0 | RESERVED 0000h-FFFFh: Reserved |

5.4.4.3 MP1CF: Maximum P1 Core Frequency

This location contains the maximum non-Intel® Turbo Boost Technology core frequency for the processor. The frequency should equate to the markings on the processor and/or the QDF/S-spec speed even if the parts are not limited or locked to the intended speed. Format of this field is in megahertz, rounded to a whole number, and encoded in binary coded decimal. Writes to this register have no effect.

For example, a 2.6 GHz processor will have a value of 2600h.

| Offset: 1Eh-1Dh | |
|-----------------|--|
| Bit | Description |
| 15:0 | Maximum P1 Core Frequency 0000h-FFFFh: MHz |



5.4.4.4 MPOCF: Maximum P0 Core Frequency

This location contains the maximum Intel Turbo Boost Technology core frequency for the processor. This is the maximum intended speed for the part under any functional conditions. Format of this field is in megahertz, rounded to a whole number, and encoded in binary coded decimal. Writes to this register have no effect.

For example, A processor with a maximum Intel Turbo Boost Technology frequency of 2.8 GHz will have a value of 2800h.

| Offset: 20h-1Fh | |
|-----------------|--|
| Bit | Description |
| 15:0 | Maximum P0 Core Frequency 0000h-FFFFh: MHz |

5.4.5 Processor Uncore Data

This section contains silicon-related data relevant to the processor Uncore.

5.4.5.1 UPIL: Number of Intel® UPI Links

Systems may need to read this offset to decide if the device has enough Intel® UPI Links to operate the number of processors your system is capable of supporting. The data provided is the number of links, and reflected in binary coded decimal. Writes to this register have no effect.

For example, the Second Generation Intel® Xeon® Scalable Processors supports a maximum of three links. Therefore, offset 21h could have a value of 03.

| Offset: 21h | |
|-------------|---|
| Bit | Description |
| 7:0 | Number of Intel® UPI links 00h-FFh: Links |

5.4.5.2 MAXUPI: Maximum Intel® UPI Transfer Rate

Systems may need to read this offset to decide if all installed processors support the same Intel® UPI link transfer rate. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

For example, the Second Generation Intel® Xeon® Scalable Processors supports a maximum Intel® UPI link transfer rate of 10.4 GT/s. Therefore, offset 23h-22h has a value of 1040.

| Offset: 23h-22h | |
|-----------------|--|
| Bit | Description |
| 15:0 | Maximum Intel® UPI Transfer Rate 0000h-FFFFh: 10 MHz |



5.4.5.3 MAXPCI: Maximum PCIe Transfer Rate

Systems may need to read this offset to decide if all installed processors support the same Intel PCIe Link Transfer Rate. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

For example, the Second Generation Intel® Xeon® Scalable Processors supports a maximum Intel PCIe2 link transfer rate of 8.0 GT/s. Therefore, offset 25h-24h has a value of 8000.

| Offset: 25h-24h | |
|-----------------|---|
| Bit | Description |
| 15:0 | Minimum PCIe Transfer Rate 0000h-FFFFh: MHz |

5.4.5.4 DDR1DPC: Maximum Intel DDR4 1 DPC DIMM Speed

Systems may need to read this offset to set maximum DIMM speeds supporting the 1 DPC usage. The data provided is maximum supported DIMM frequency, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

For example, the Second Generation Intel® Xeon® Scalable Processors supports a maximum DDR4 frequency of 2667Gh/s. Therefore, offset 27h-26h has a value of 2667h.

| Offset: 27h-26h | |
|-----------------|--|
| Bit | Description |
| 15:0 | Maximum Intel SMI Transfer Rate 0000h-FFFFh: MHz |

5.4.5.5 DDR2DPC: Maximum Intel DDR4 2 DPC DIMM Speed

Systems may need to read this offset to set maximum DIMM speeds supporting the 2DPC usage. The data provided is maximum supported DIMM frequency, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

| Offset: 29h-28h | |
|-----------------|--|
| Bit | Description |
| 15:0 | Minimum Intel SMI Transfer Rate 0000h-FFFFh: MHz |

5.4.5.6 RES3: Reserved 3

This locations are reserved. Writes to this register have no effect.



| Offset: 2Ah | |
|-------------|--------------------------------------|
| Bit | Description |
| 8:0 | RESERVED 00h-FFh: Reserved |

5.4.6 Processor Cache Data

This section contains silicon-related data relevant to the processor caches.

5.4.6.1 MLC: Mid Level Cache Size

This location contains the size of the level-two cache in kilobytes per core. Writes to this register have no effect. Data format is decimal.

For example, the Second Generation Intel® Xeon® Scalable Processors has a 1 MB MLC cache per core. Thus, offset 2Ch-2Bh will contain a value of 0400h, which is 1024.

| Offset: 2Ch-2Bh | |
|-----------------|--|
| Bit | Description |
| 15:0 | Mid Level Cache Size 0000h-FFFFh: KB |

5.4.6.2 LLC: Low Level Cache Size

This location contains the size of the level-three cache in megabytes per package. Writes to this register have no effect. Data format is decimal.

For example, the Second Generation Intel® Xeon® Scalable Processors has a 33 MB LLC cache. Thus, offset 2Eh-2Dh will contain a value of 8400h.

| Offset: 2Eh-2Dh | |
|-----------------|--|
| Bit | Description |
| 15:0 | Low Level Cache Size 0000h-FFFFh: KB |

5.4.6.3 RES2 and RES3: Reserved 2 and Reserved 3

This location contains NVM DIMM Max Capacity information. Bit 15:0 is binary value representation of multiplier of 64 GB to indicate NVM DIMM Max Capacity. Writes to this register have no effect.



| Offset: 30h-2Fh | |
|-----------------|--|
| Bit | Description |
| 15:8 | Offset 30h: NVM DIMM Max Capacity 00h-FFh: |
| 7:0 | Offset 2Fh: NVM DIMM Max Capacity 00h-FFh: |

5.4.7 Package Data

This section contains substrate and other package related data.

5.4.7.1 PKGT: Package Type

This location tracks the whether the part is a multi-chip package, and which type if so. 0 = non-MCP package. 1 = fabric. Writes to this register have no effect.

| Offset: 31h | |
|-------------|---------------------------------|
| Bit | Description |
| 7:0 | Package Type 00h-FFh: |

5.4.7.2 RES5: Reserved 5

This location is reserved. Writes to this register have no effect.

| Offset: 32h-33h | |
|-----------------|--|
| Bit | Description |
| 15:0 | RESERVED 0000h-FFFFh: Reserved |

5.4.8 Processor Voltage Data

This section contains silicon-related data relevant to the processor voltage rails.

5.4.8.1 MXVCCIN: MAX VCCIN VID

Offset 35h-34h is the Processor VCCIN maximum VID (Voltage Identification) field and contains the maximum voltage requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Some systems read this offset to determine if all processors support the same default VID setting. Writes to this register have no effect.

For example, a voltage of 1.800 V maximum core VID would contain 1800h in offset 35- 34h.



| Offset: 35h-34h | |
|------------------------|---|
| Bit | Description |
| 15:0 | MAX VCCIN VID 0000h-FFFFh: mV |

5.4.8.2 MNVCCIN: MIN VCCIN VID

Offset 37h-36h is the Processor Vsa minimum VID (Voltage Identification) field and contains the minimum voltage requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Some systems read this offset to determine if all processors support the same default VID setting. Writes to this register have no effect.

For example, a voltage of 0.600 V maximum core VID would contain 0600h in offset 37h- 36h.

| Offset: 37-36h | |
|-----------------------|---|
| Bit | Description |
| 15:0 | MIN VCCIN VID 0000h-FFFFh: mV |

5.4.8.3 MXSAVD: MAX VSA VID

Offset 39h-38h is the Processor Vsa maximum VID (Voltage Identification) field and contains the maximum voltage requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Some systems read this offset to determine if all processors support the same default VID setting. Writes to this register have no effect.

For example, a voltage of 1.000 V maximum core VID would contain 1000h in offset 39h- 38h.

| Offset: 39h-38h | |
|------------------------|---------------------------------------|
| Bit | Description |
| 15:0 | MAX VSA VID 0000h-FFFFh: mV |

5.4.8.4 MNSAVD: MIN VSA VID

Offset 3Bh-3Ah is the Processor Vsa minimum VID (Voltage Identification) field and contains the minimum voltage requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Some systems read this offset to determine if all processors support the same default VID setting. Writes to this register have no effect.

For example, a voltage of 0.600 V maximum core VID would contain 0600h in offset 3Bh-3Ah.



| | |
|------------------------|---------------------------------------|
| Offset: 3Bh-3Ah | |
| Bit | Description |
| 15:0 | MIN VSA VID 0000h-FFFFh: mV |

5.4.8.5 VCCD: VCCD

This field contains the voltage requested for the VCCD pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default VCCD settings. Writes to this register have no effect.

For example, a voltage of 1.200 VCCD would contain an offset 3D-3Ch value of 1200h.

| | |
|------------------------|--------------------------------|
| Offset: 3Dh-3Ch | |
| Bit | Description |
| 15:0 | VCCD 0000h-FFFFh: mV |

5.4.8.6 VCCIO: VCCIO

This field contains the voltage requested for the VccIO pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default VccIO settings. Writes to this register have no effect.

For example, a voltage of 1.000 VccIO_IN would contain an offset 3Fh-3Eh value of 1000h.

| | |
|------------------------|---------------------------------|
| Offset: 3Fh-3Eh | |
| Bit | Description |
| 15:0 | VCCIO 0000h-FFFFh: mV |

5.4.8.7 RES6: Reserved 6

This location is reserved. Writes to this register have no effect.

| | |
|------------------------|---|
| Offset: 43h-40h | |
| Bit | Description |
| 31:0 | RESERVED 00000000h-FFFFFFFFh: |

5.4.8.8 CDVCORE: CD Vcc Core

This field contains the voltage requested for the CD Vcc Core pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default CD Vcc Core settings. Writes to this register have no effect.

For example, a voltage of 1.000 CD Vcc Core would contain an offset 45-44h value of 1000h.



| Offset: 45h-44h | |
|-----------------|---------------------------------------|
| Bit | Description |
| 15:0 | CD Vcc Core 0000h-FFFFh: mV |

5.4.8.9 CDVCCIN: CD Vcc In

This field contains the voltage requested for the CD Vcc In pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default CD Vcc In settings. Writes to this register have no effect.

For example, a voltage of 1.000 VccIO_IN would contain an offset 47-46h value of 1000h.

| Offset: 47E-46h | |
|-----------------|-------------------------------------|
| Bit | Description |
| 15:0 | CD Vcc In 0000h-FFFFh: mV |

5.4.8.10 CDVCCP: CD VCCP

This field contains the voltage requested for the CDVCCP pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default CDVCCP settings. Writes to this register have no effect.

For example, a voltage of 1.000 CDVCCP would contain an offset 49h-48h value of 1000h.

| Offset: 49h-48h | |
|-----------------|----------------------------------|
| Bit | Description |
| 15:0 | CDVCCP 0000h-FFFFh: mV |

5.4.8.11 CDVPP: CD VPP

This field contains the voltage requested for the CD VPP pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default CD VPP settings. Writes to this register have no effect.

For example, a voltage of 1.000 CD VPP would contain an offset 4Bh-4Ah value of 1000h.

| Offset: 4B-4Ah | |
|----------------|----------------------------------|
| Bit | Description |
| 15:0 | CD VPP 0000h-FFFFh: mV |



5.4.8.12 RCVCORE: RC VCORE

This field contains the voltage requested for the RC VCORE pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default RC VCORE settings. Writes to this register have no effect.

For example, a voltage of 1.000 VCCD would contain an offset 4Dh-4Ch value of 1000h.

| Offset: 4Dh-4Ch | |
|------------------------|------------------------------------|
| Bit | Description |
| 15:0 | RC VCORE 0000h-FFFFh: mV |

5.4.8.13 RVCCH: RC VCCH

This field contains the voltage requested for the RC VCCH pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default RC VCCH settings. Writes to this register have no effect.

For example, a voltage of 1.000 RC VCCH would contain an offset 4Eh-4Fh value of 1000h.

| Offset: 4Fh-4Eh | |
|------------------------|-----------------------------------|
| Bit | Description |
| 15:0 | RC VCCH 0000h-FFFFh: mV |

5.4.8.14 RES7: Reserved 7

This location is reserved. Writes to this register have no effect.

| Offset: 50h-55h | |
|------------------------|---|
| Bit | Description |
| 39:0 | RESERVED 0000000000h-FFFFFFFFFh: Reserved |

5.4.9 Part Number Data

This section provides device traceability.

5.4.9.1 PFN: Processor Family Number

This location contains seven ASCII characters reflecting the Intel® family number for the processor. This number is the same on all Intel® Xeon® E7 v3 processors. Combined with the Processor SKU Number below, this is the complete processor part number. This information is typically marked on the outside of the processor. If the part number is less than 15 total characters, a leading space is inserted into the value. The part number should match the information found in the marking specification. Writes to this register have no effect.

For example, a processor with a part number of AT80604***** will have the following data found at offset 5Ch-56h: 41h, 54h, 38h, 30h, 36h, 30h, 34h.



| Offset: 5Ch-56h | |
|------------------------|---|
| Bit | Description |
| 55:48 | Character 1 ASCII character 00h-0FFh: ASCII character |
| 47:40 | Character 2 ASCII character 00h-0FFh: ASCII character |
| 39:32 | Character 3 ASCII character 00h-0FFh: ASCII character |
| 31:24 | Character 4 ASCII character 00h-0FFh: ASCII character |
| 23:16 | Character 5 ASCII character or 20h 00h-0FFh: ASCII character |
| 15:8 | Character 6 ASCII character or 20h 00h-0FFh: ASCII character |
| 7:0 | Character 7 ASCII character or 20h 00h-0FFh: ASCII character |

5.4.9.2 PSN: Processor SKU Number

This location contains eight ASCII characters reflecting the SKU number for the processor. Added to the end of the Processor Family Number above, this is the complete processor part number. This information is typically marked on the outside of the processor. If the part number is less than 15 total characters, a leading space is inserted into the value. The part number should match the information found in the marking specification. Writes to this register have no effect.

For example, a processor with a part number of *****003771AA will have the following data found at offset 64h-5Dh: 30h, 30h, 33h, 37h, 37h, 31h, 41h, 41h.

| Offset: 64h-5Dh | |
|------------------------|--|
| Bit | Description |
| 63:56 | Character 1 ASCII character 00h-0FFh: ASCII character |
| 55:48 | Character 2 ASCII character 00h-0FFh: ASCII character |
| 47:40 | Character 3 ASCII character 00h-0FFh: ASCII character |



| Offset: 64h-5Dh | |
|-----------------|---|
| Bit | Description |
| 39:32 | Character 4 ASCII character or 20h 00h-0FFh: ASCII character |
| 31:24 | Character 5 ASCII character or 20h 00h-0FFh: ASCII character |
| 23:16 | Character 6 ASCII character or 20h 00h-0FFh: ASCII character |
| 15:8 | Character 7 ASCII character or 20h 00h-0FFh: ASCII character |
| 7:0 | Character 8 ASCII character 00h-0FFh: ASCII character |

5.4.10 Thermal Reference Data

5.4.10.1 TCASE: T_{CASE} Maximum

This location provides the maximum T_{CASE} for the processor. The field reflects temperature in degrees Celsius in binary coded decimal format. The thermal specifications are specified at the case Integrated Heat Spreader (IHS). Writes to this register have no effect.

For example, a temperature of 66°C would contain a value of 66h.

| Offset: 65h | |
|-------------|---|
| Bit | Description |
| 7:0 | T_{CASE} Maximum 00h-FFh: Degrees Celsius |

5.4.10.2 TDP: Thermal Design Power

This location contains the maximum Thermal Design Power for the part. The field reflects power in watts in binary coded decimal format. Writes to this register have no effect. A zero value means that the value was not programmed.

For example, a 130 W TDP would be saved as 0130h. Offset 67h is 01h and offset 66h is 30h.

| Offset: 67h-66h | |
|-----------------|---|
| Bit | Description |
| 15:0 | Thermal Design Power 0000h-FFFFh: Watts |



5.4.10.3 DTSMAX: Digital Thermal Sensor Maximum

This location provides the Digital Thermal Sensor Maximum temperature for the processor. The field reflects temperature in degrees Celsius in binary coded decimal format. The thermal specifications are specified at the sensor nearest the CPU hot spot. Writes to this register have no effect.

For example, a temperature of 103°C would contain a value of 0103h.

| Offset: 69h-68h | |
|-----------------|---|
| Bit | Description |
| 15:0 | Digital Thermal Sensor Maximum 0000h-FFFFh: Degrees Celsius |

5.4.10.4 PN: Pn Power Limit

This location contains the maximum Pn power for the part. The field reflects power in watts in binary coded decimal format. Writes to this register have no effect. A zero value means that the value was not programmed.

For example, a 35 W would be saved as 0035h. Offset 6Ah is 00h and offset 69h is 35h.

| Offset: 6Ah-69h | |
|-----------------|---|
| Bit | Description |
| 15:0 | Pn Power Limit 0000h-FFFFh: Watts |

5.4.11 Feature Data

This section provides information on key features that the platform may need to understand without powering on the processor.

5.4.11.1 PCFF: Processor Core Feature Flags

This location contains a copy of results in EDX[31:0] from Function 1 of the CPUID instruction. These details provide instruction and feature support by product family. Writes to this register have no effect.

For example, a value of BFEFBFFh can be found at offset 6Ch - 6Fh.

| Offset: 6Ch-6Fh | |
|-----------------|--|
| Bit | Description |
| 31:0 | Processor Core Feature Flags 00000000h-FFFFFFFF: Feature Flags |

5.4.11.2 PFF: Processor Feature Flags

This location contains additional feature information from the processor. Writes to this register have no effect.



| Offset: 71h-70h | | |
|-----------------|------|---------------|
| Bit | Byte | Description |
| | 71h | Reserved |
| | | Reserved |
| | | Reserved |
| | | Reserved |
| | | Reserved |
| | | Reserved |
| | | Reserved |
| | | Reserved |
| 7 | 70h | Reserved |
| 6 | | Reserved |
| 5 | | Reserved |
| 4 | | AEP Enabled |
| 3 | | TXT Enabled |
| 2 | | EMCA2 Enabled |
| 1 | | Turbo Enabled |
| 0 | | avx512_2ndFMA |

Bits are set when a feature is present, and cleared when they are not.

5.4.11.3 MPSUP: Multiprocessor Support

This location contains 2 bits for representing the supported number of physical processors on the bus. These two bits are LSB aligned where 000b equates to non-scalable 1socket (1S) operation, 001b to non-scalable 2 socket (2S), 010b to 4 socket glueless (4S GLULS), 011b to scalable 4 socket (S4S), and 101b scalable 8 socket (S8S). The is a 1S, 2S, 4S GLULS, S4S, or S8S processor. The first six bits in this field are reserved for future use. Writes to this register have no effect.

For example, a scalable 8-socket processor will have a value of 100h at offset 72h.

| Offset: 72h | |
|-------------|---|
| Bit | Description |
| 7:3 | RESERVED 000000b-111111b: Reserved |
| 2:0 | Multiprocessor Support 1S, 2S, 4S GLULS, S4S, or S8S indicator 000b: Nonscalable, 1 Socket 001b: Nonscalable, up to 2 Socket Glueless 010b: Nonscalable, up to 4 Socket Glueless in Ring. 011b: Scalable, up to 4 Socket Glueless Fully Connected. 100b: Reserved 101b: Scalable, up to 8 Socket Glueless |



5.4.11.4 TCDC: Tap Chain Device Count

At offset 73, a 4-bit hex digit is used to tell how many devices are in the TAP Chain. A Second Generation Intel® Xeon® Scalable Processors with ten cores, this field would be set to Bh.

| Offset: 73h | |
|-------------|--|
| Bit | Description |
| 7:0 | TAP Chain Device Count 0000h-FFFFh: Reserved |

5.4.11.5 RES9: Reserved 9

This location is reserved. Writes to this register have no effect.

| Offset: 74h-75h | |
|-----------------|--|
| Bit | Description |
| 15:0 | RESERVED 0000h-FFFFh: Reserved |

5.4.11.6 STTCKS: Static Checksum

This location provides the checksum of the static values per SKU. Writes to this register have no effect.

| Offset: 76h | |
|-------------|--|
| Bit | Description |
| 7:0 | Static Checksum One-byte checksum of the Static Checksum 00h- FFh: See Section 5.4.13, "Checksums" for calculation of this value. |

5.4.12 Protected Processor Inventory Number

This section contains the Protected Processor Inventory Number.

5.4.12.1 PPIN: Protected Processor Inventory Number

This location contains a 64-bit identification number. The value in this field is the PPIN number, which will be the same value as the PPIN accessed through the BIOS MSR. Writes to this register have no effect.

| Offset: 7Eh-77h | |
|-----------------|--|
| Bit | Description |
| 63:0 | PPIN 0000000000000000h-FFFFFFFFFFFFFFFFh: PPIN |



5.4.12.2 RES10: Reserved 10

This location is reserved. Writes to this register have no effect.

| | |
|--------------------|--|
| Offset: 7Fh | |
| Bit | Description |
| 7:0 | RESERVED 00h- FFh: Reserved. |

5.4.13 Checksums

The PIROM includes checksums. The following table includes the checksum values for each section defined in the 128-byte ROM.

Table 5-5. 128-Byte ROM Checksum Values

| Section | Checksum Address |
|-----------------|------------------|
| Static Features | 76h |

Checksums are automatically calculated and programmed by Intel. The first step in calculating the checksum is to add each byte from the field to the next subsequent byte. This result is then negated to provide the checksum.

For example, for a byte string of AA445Ch, the resulting checksum will be B6h.

$$\begin{aligned}
 AA &= 10101010 & 44 &= 01000100 & 5C &= 01011100 \\
 AA + 44 + 5C &= 01001010
 \end{aligned}$$

Negate the sum: $10110101 + 1 = \mathbf{10110110 (B6h)}$





A Pin Listing

Table A-1. Pin List By Name (Sheet 1 of 90)

| Pin Name | Location | Type | I/O |
|-------------------|----------|--------|-----|
| BCLK0_DN | AU24 | CMOS | I |
| BCLK0_DP | AW24 | CMOS | I |
| BCLK1_DN | CR26 | CMOS | I |
| BCLK1_DP | CP27 | CMOS | I |
| BCLK2_DN | CT25 | CMOS | I |
| BCLK2_DP | CU26 | CMOS | I |
| BIST_ENABLE | BA20 | CMOS | I |
| BMCINIT | BD23 | CMOS | I |
| BPM_N[0] | AJ10 | ODCMOS | I/O |
| BPM_N[1] | AH11 | ODCMOS | I/O |
| BPM_N[2] | AG10 | ODCMOS | I/O |
| BPM_N[3] | AF11 | ODCMOS | I/O |
| BPM_N[4] | AA12 | ODCMOS | I/O |
| BPM_N[5] | Y11 | ODCMOS | I/O |
| BPM_N[6] | AE12 | ODCMOS | I/O |
| BPM_N[7] | AC12 | ODCMOS | I/O |
| CATERR_N | AL14 | ODCMOS | I/O |
| CD_HFI_REFCLK_DN | BE16 | CMOS | I |
| CD_HFI_REFCLK_DP | BG16 | CMOS | I |
| CD_HFI0_I2CCLK | BN22 | ODCMOS | I/O |
| CD_HFI0_I2CDAT | BP23 | ODCMOS | I/O |
| CD_HFI0_INT_N | BP19 | CMOS | I |
| CD_HFI0_LED_N | BK21 | OD | O |
| CD_HFI0_MODPRST_N | BR20 | CMOS | I |
| CD_HFI0_RESET_N | BN24 | OD | O |
| CD_HFI1_I2CCLK | BJ22 | ODCMOS | I/O |
| CD_HFI1_I2CDAT | BH23 | ODCMOS | I/O |
| CD_HFI1_INT_N | BM21 | CMOS | I |
| CD_HFI1_LED_N | BM23 | OD | O |
| CD_HFI1_MODPRST_N | BT19 | CMOS | I |
| CD_HFI1_RESET_N | BK23 | OD | O |
| CD_PE_REFCLK_DN | BU24 | CMOS | I |
| CD_PE_REFCLK_DP | BW24 | CMOS | I |
| CD_POR_N | CF25 | | |

Table A-1. Pin List By Name (Sheet 2 of 90)

| Pin Name | Location | Type | I/O |
|-------------------|----------|------|-----|
| CD_TCLK | CB23 | | |
| CD_TDI | BY21 | GTL | I |
| CD_TDO | CC22 | OD | O |
| CD_TMS | CE24 | GTL | I |
| CD_TRST_N | CD23 | GTL | I |
| CD_VCC_CORE | BD13 | PWR | |
| CD_VCC_CORE | BE12 | PWR | |
| CD_VCC_CORE | BE14 | PWR | |
| CD_VCC_CORE | BF11 | PWR | |
| CD_VCC_CORE | BF13 | PWR | |
| CD_VCC_CORE | BG12 | PWR | |
| CD_VCC_CORE | BG14 | PWR | |
| CD_VCC_CORE | BH13 | PWR | |
| CD_VCC_CORE | BJ12 | PWR | |
| CD_VCC_CORE | BJ14 | PWR | |
| CD_VCC_CORE | BK13 | PWR | |
| CD_VCC_CORE | BK15 | PWR | |
| CD_VCC_CORE | BL14 | PWR | |
| CD_VCC_CORE_SENSE | BN16 | PWR | |
| CD_VCCIN | BT27 | PWR | |
| CD_VCCIN | BU26 | PWR | |
| CD_VCCIN | BV27 | PWR | |
| CD_VCCIN | BY27 | PWR | |
| CD_VCCP | BM11 | PWR | |
| CD_VCCP | BN12 | PWR | |
| CD_VCCP | BN14 | PWR | |
| CD_VCCP | BP11 | PWR | |
| CD_VCCP | BP13 | PWR | |
| CD_VCCP | BP15 | PWR | |
| CD_VCCP | BR12 | PWR | |
| CD_VCCP | BR14 | PWR | |
| CD_VCCP | BT11 | PWR | |
| CD_VCCP | BT13 | PWR | |
| CD_VCCP | BT15 | PWR | |
| CD_VCCP | BU12 | PWR | |



Table A-1. Pin List By Name (Sheet 3 of 90)

| Pin Name | Location | Type | I/O |
|-----------------------|----------|------|-----|
| CD_VCCP | BU14 | PWR | |
| CD_VCCP | BV11 | PWR | |
| CD_VCCP | BV13 | PWR | |
| CD_VCCP | BV15 | PWR | |
| CD_VCCP_SENSE | BT17 | PWR | |
| CD_VPP | A10 | PWR | |
| CD_VPP | A12 | PWR | |
| CD_VPP | B11 | PWR | |
| CD_VSS_VCC_CORE_SENSE | BL16 | PWR | |
| CD_VSS_VCCP_SENSE | BU16 | PWR | |
| DDR0_ACT_N | J60 | SSTL | O |
| DDR0_ALERT_N | B61 | SSTL | I |
| DDR0_BA[0] | C52 | SSTL | O |
| DDR0_BA[1] | G54 | SSTL | O |
| DDR0_BG[0] | D61 | SSTL | O |
| DDR0_BG[1] | F63 | SSTL | O |
| DDR0_CAVREF | AJ64 | SSTL | O |
| DDR0_CID[2] | G46 | SSTL | O |
| DDR0_CKE[0] | C62 | SSTL | O |
| DDR0_CKE[1] | C64 | SSTL | O |
| DDR0_CKE[2] | B63 | SSTL | O |
| DDR0_CKE[3] | D63 | SSTL | O |
| DDR0_CLK_DN[0] | F55 | SSTL | O |
| DDR0_CLK_DN[1] | C54 | SSTL | O |
| DDR0_CLK_DN[2] | J56 | SSTL | O |
| DDR0_CLK_DN[3] | C56 | SSTL | O |
| DDR0_CLK_DP[0] | D55 | SSTL | O |
| DDR0_CLK_DP[1] | B55 | SSTL | O |
| DDR0_CLK_DP[2] | G56 | SSTL | O |
| DDR0_CLK_DP[3] | B57 | SSTL | O |
| DDR0_CS_N[0] | G52 | SSTL | O |
| DDR0_CS_N[1] | F49 | SSTL | O |
| DDR0_CS_N[2] | D47 | SSTL | O |
| DDR0_CS_N[3] | F47 | SSTL | O |
| DDR0_CS_N[4] | B51 | SSTL | O |
| DDR0_CS_N[5] | D49 | SSTL | O |
| DDR0_CS_N[6] | F45 | SSTL | O |
| DDR0_CS_N[7] | K45 | SSTL | O |
| DDR0_DQ[0] | AN86 | SSTL | I/O |
| DDR0_DQ[1] | AN84 | SSTL | I/O |
| DDR0_DQ[10] | L86 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 4 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| DDR0_DQ[11] | L84 | SSTL | I/O |
| DDR0_DQ[12] | AA86 | SSTL | I/O |
| DDR0_DQ[13] | AA84 | SSTL | I/O |
| DDR0_DQ[14] | N86 | SSTL | I/O |
| DDR0_DQ[15] | N84 | SSTL | I/O |
| DDR0_DQ[16] | V81 | SSTL | I/O |
| DDR0_DQ[17] | T79 | SSTL | I/O |
| DDR0_DQ[18] | N82 | SSTL | I/O |
| DDR0_DQ[19] | M81 | SSTL | I/O |
| DDR0_DQ[2] | AE86 | SSTL | I/O |
| DDR0_DQ[20] | W80 | SSTL | I/O |
| DDR0_DQ[21] | V79 | SSTL | I/O |
| DDR0_DQ[22] | R82 | SSTL | I/O |
| DDR0_DQ[23] | N80 | SSTL | I/O |
| DDR0_DQ[24] | L76 | SSTL | I/O |
| DDR0_DQ[25] | R76 | SSTL | I/O |
| DDR0_DQ[26] | M73 | SSTL | I/O |
| DDR0_DQ[27] | P73 | SSTL | I/O |
| DDR0_DQ[28] | M77 | SSTL | I/O |
| DDR0_DQ[29] | P77 | SSTL | I/O |
| DDR0_DQ[3] | AE84 | SSTL | I/O |
| DDR0_DQ[30] | L74 | SSTL | I/O |
| DDR0_DQ[31] | R74 | SSTL | I/O |
| DDR0_DQ[32] | C42 | SSTL | I/O |
| DDR0_DQ[33] | B41 | SSTL | I/O |
| DDR0_DQ[34] | C38 | SSTL | I/O |
| DDR0_DQ[35] | E38 | SSTL | I/O |
| DDR0_DQ[36] | E42 | SSTL | I/O |
| DDR0_DQ[37] | F41 | SSTL | I/O |
| DDR0_DQ[38] | B39 | SSTL | I/O |
| DDR0_DQ[39] | F39 | SSTL | I/O |
| DDR0_DQ[4] | AR86 | SSTL | I/O |
| DDR0_DQ[40] | K37 | SSTL | I/O |
| DDR0_DQ[41] | P37 | SSTL | I/O |
| DDR0_DQ[42] | L34 | SSTL | I/O |
| DDR0_DQ[43] | N34 | SSTL | I/O |
| DDR0_DQ[44] | L38 | SSTL | I/O |
| DDR0_DQ[45] | N38 | SSTL | I/O |
| DDR0_DQ[46] | K35 | SSTL | I/O |
| DDR0_DQ[47] | P35 | SSTL | I/O |
| DDR0_DQ[48] | K31 | SSTL | I/O |



Table A-1. Pin List By Name (Sheet 5 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR0_DQ[49] | P31 | SSTL | I/O |
| DDR0_DQ[5] | AR84 | SSTL | I/O |
| DDR0_DQ[50] | L28 | SSTL | I/O |
| DDR0_DQ[51] | N28 | SSTL | I/O |
| DDR0_DQ[52] | L32 | SSTL | I/O |
| DDR0_DQ[53] | N32 | SSTL | I/O |
| DDR0_DQ[54] | K29 | SSTL | I/O |
| DDR0_DQ[55] | P29 | SSTL | I/O |
| DDR0_DQ[56] | K25 | SSTL | I/O |
| DDR0_DQ[57] | P25 | SSTL | I/O |
| DDR0_DQ[58] | P23 | SSTL | I/O |
| DDR0_DQ[59] | T23 | SSTL | I/O |
| DDR0_DQ[6] | AG86 | SSTL | I/O |
| DDR0_DQ[60] | L26 | SSTL | I/O |
| DDR0_DQ[61] | N26 | SSTL | I/O |
| DDR0_DQ[62] | H23 | SSTL | I/O |
| DDR0_DQ[63] | K23 | SSTL | I/O |
| DDR0_DQ[7] | AG84 | SSTL | I/O |
| DDR0_DQ[8] | W86 | SSTL | I/O |
| DDR0_DQ[9] | W84 | SSTL | I/O |
| DDR0_DQS_DN[0] | AJ84 | SSTL | I/O |
| DDR0_DQS_DN[1] | R84 | SSTL | I/O |
| DDR0_DQS_DN[10] | U84 | SSTL | I/O |
| DDR0_DQS_DN[11] | U82 | SSTL | I/O |
| DDR0_DQS_DN[12] | K75 | SSTL | I/O |
| DDR0_DQS_DN[13] | A40 | SSTL | I/O |
| DDR0_DQS_DN[14] | J36 | SSTL | I/O |
| DDR0_DQS_DN[15] | J30 | SSTL | I/O |
| DDR0_DQS_DN[16] | J24 | SSTL | I/O |
| DDR0_DQS_DN[17] | AB67 | SSTL | I/O |
| DDR0_DQS_DN[2] | P79 | SSTL | I/O |
| DDR0_DQS_DN[3] | T75 | SSTL | I/O |
| DDR0_DQS_DN[4] | G40 | SSTL | I/O |
| DDR0_DQS_DN[5] | R36 | SSTL | I/O |
| DDR0_DQS_DN[6] | R30 | SSTL | I/O |
| DDR0_DQS_DN[7] | N24 | SSTL | I/O |
| DDR0_DQS_DN[8] | AH67 | SSTL | I/O |
| DDR0_DQS_DN[9] | AL84 | SSTL | I/O |
| DDR0_DQS_DP[0] | AH85 | SSTL | I/O |
| DDR0_DQS_DP[1] | P85 | SSTL | I/O |
| DDR0_DQS_DP[10] | V85 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 6 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR0_DQS_DP[11] | T81 | SSTL | I/O |
| DDR0_DQS_DP[12] | M75 | SSTL | I/O |
| DDR0_DQS_DP[13] | C40 | SSTL | I/O |
| DDR0_DQS_DP[14] | L36 | SSTL | I/O |
| DDR0_DQS_DP[15] | L30 | SSTL | I/O |
| DDR0_DQS_DP[16] | L24 | SSTL | I/O |
| DDR0_DQS_DP[17] | AD67 | SSTL | I/O |
| DDR0_DQS_DP[2] | R80 | SSTL | I/O |
| DDR0_DQS_DP[3] | P75 | SSTL | I/O |
| DDR0_DQS_DP[4] | E40 | SSTL | I/O |
| DDR0_DQS_DP[5] | N36 | SSTL | I/O |
| DDR0_DQS_DP[6] | N30 | SSTL | I/O |
| DDR0_DQS_DP[7] | R24 | SSTL | I/O |
| DDR0_DQS_DP[8] | AF67 | SSTL | I/O |
| DDR0_DQS_DP[9] | AM85 | SSTL | I/O |
| DDR0_ECC[0] | AC68 | SSTL | I/O |
| DDR0_ECC[1] | AG68 | SSTL | I/O |
| DDR0_ECC[2] | AD65 | SSTL | I/O |
| DDR0_ECC[3] | AF65 | SSTL | I/O |
| DDR0_ECC[4] | AD69 | SSTL | I/O |
| DDR0_ECC[5] | AF69 | SSTL | I/O |
| DDR0_ECC[6] | AC66 | SSTL | I/O |
| DDR0_ECC[7] | AG66 | SSTL | I/O |
| DDR0_MA[0] | F53 | SSTL | O |
| DDR0_MA[1] | F57 | SSTL | O |
| DDR0_MA[10] | J54 | SSTL | O |
| DDR0_MA[11] | G62 | SSTL | O |
| DDR0_MA[12] | J64 | SSTL | O |
| DDR0_MA[13] | J48 | SSTL | O |
| DDR0_MA[14] | F51 | SSTL | O |
| DDR0_MA[15] | K49 | SSTL | O |
| DDR0_MA[16] | D51 | SSTL | O |
| DDR0_MA[17] | K47 | SSTL | O |
| DDR0_MA[2] | D57 | SSTL | O |
| DDR0_MA[3] | C58 | SSTL | O |
| DDR0_MA[4] | G58 | SSTL | O |
| DDR0_MA[5] | F59 | SSTL | O |
| DDR0_MA[6] | D59 | SSTL | O |
| DDR0_MA[7] | G60 | SSTL | O |
| DDR0_MA[8] | C60 | SSTL | O |
| DDR0_MA[9] | F61 | SSTL | O |



Table A-1. Pin List By Name (Sheet 7 of 90)

| Pin Name | Location | Type | I/O |
|--------------------|----------|--------|-----|
| DDR0_ODT[0] | C50 | SSTL | O |
| DDR0_ODT[1] | C48 | SSTL | O |
| DDR0_ODT[2] | G50 | SSTL | O |
| DDR0_ODT[3] | G48 | SSTL | O |
| DDR0_PAR | D53 | SSTL | O |
| DDR012_DRAM_PWR_OK | AN30 | CMOS | I |
| DDR012_RCOMP[0] | Y43 | | |
| DDR012_RCOMP[1] | AB43 | | |
| DDR012_RCOMP[2] | AC42 | | |
| DDR012_RESET_N | U64 | CMOS | O |
| DDR012_SPDSCL | AJ18 | ODCMOS | I/O |
| DDR012_SPSDA | AF17 | ODCMOS | I/O |
| DDR1_ACT_N | T63 | SSTL | O |
| DDR1_ALERT_N | W62 | SSTL | I |
| DDR1_BA[0] | T53 | SSTL | O |
| DDR1_BA[1] | K55 | SSTL | O |
| DDR1_BG[0] | M61 | SSTL | O |
| DDR1_BG[1] | N60 | SSTL | O |
| DDR1_CAVREF | AK63 | SSTL | O |
| DDR1_CID[2] | M47 | SSTL | O |
| DDR1_CKE[0] | N62 | SSTL | O |
| DDR1_CKE[1] | R64 | SSTL | O |
| DDR1_CKE[2] | K63 | SSTL | O |
| DDR1_CKE[3] | L64 | SSTL | O |
| DDR1_CLK_DN[0] | M53 | SSTL | O |
| DDR1_CLK_DN[1] | R54 | SSTL | O |
| DDR1_CLK_DN[2] | N56 | SSTL | O |
| DDR1_CLK_DN[3] | R56 | SSTL | O |
| DDR1_CLK_DP[0] | N54 | SSTL | O |
| DDR1_CLK_DP[1] | T55 | SSTL | O |
| DDR1_CLK_DP[2] | M57 | SSTL | O |
| DDR1_CLK_DP[3] | T57 | SSTL | O |
| DDR1_CS_N[0] | K51 | SSTL | O |
| DDR1_CS_N[1] | R50 | SSTL | O |
| DDR1_CS_N[2] | N46 | SSTL | O |
| DDR1_CS_N[3] | V47 | SSTL | O |
| DDR1_CS_N[4] | J50 | SSTL | O |
| DDR1_CS_N[5] | T49 | SSTL | O |
| DDR1_CS_N[6] | M45 | SSTL | O |
| DDR1_CS_N[7] | R46 | SSTL | O |
| DDR1_DQ[0] | AV81 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 8 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| DDR1_DQ[1] | AT79 | SSTL | I/O |
| DDR1_DQ[10] | AC82 | SSTL | I/O |
| DDR1_DQ[11] | AB81 | SSTL | I/O |
| DDR1_DQ[12] | AJ80 | SSTL | I/O |
| DDR1_DQ[13] | AH79 | SSTL | I/O |
| DDR1_DQ[14] | AE82 | SSTL | I/O |
| DDR1_DQ[15] | AC80 | SSTL | I/O |
| DDR1_DQ[16] | E80 | SSTL | I/O |
| DDR1_DQ[17] | J80 | SSTL | I/O |
| DDR1_DQ[18] | F77 | SSTL | I/O |
| DDR1_DQ[19] | H77 | SSTL | I/O |
| DDR1_DQ[2] | AN82 | SSTL | I/O |
| DDR1_DQ[20] | F81 | SSTL | I/O |
| DDR1_DQ[21] | H81 | SSTL | I/O |
| DDR1_DQ[22] | E78 | SSTL | I/O |
| DDR1_DQ[23] | J78 | SSTL | I/O |
| DDR1_DQ[24] | D75 | SSTL | I/O |
| DDR1_DQ[25] | C74 | SSTL | I/O |
| DDR1_DQ[26] | D71 | SSTL | I/O |
| DDR1_DQ[27] | F71 | SSTL | I/O |
| DDR1_DQ[28] | F75 | SSTL | I/O |
| DDR1_DQ[29] | G74 | SSTL | I/O |
| DDR1_DQ[3] | AM81 | SSTL | I/O |
| DDR1_DQ[30] | C72 | SSTL | I/O |
| DDR1_DQ[31] | G72 | SSTL | I/O |
| DDR1_DQ[32] | K43 | SSTL | I/O |
| DDR1_DQ[33] | H43 | SSTL | I/O |
| DDR1_DQ[34] | L40 | SSTL | I/O |
| DDR1_DQ[35] | N40 | SSTL | I/O |
| DDR1_DQ[36] | P43 | SSTL | I/O |
| DDR1_DQ[37] | T43 | SSTL | I/O |
| DDR1_DQ[38] | K41 | SSTL | I/O |
| DDR1_DQ[39] | P41 | SSTL | I/O |
| DDR1_DQ[4] | AW80 | SSTL | I/O |
| DDR1_DQ[40] | C36 | SSTL | I/O |
| DDR1_DQ[41] | B35 | SSTL | I/O |
| DDR1_DQ[42] | C32 | SSTL | I/O |
| DDR1_DQ[43] | E32 | SSTL | I/O |
| DDR1_DQ[44] | E36 | SSTL | I/O |
| DDR1_DQ[45] | F35 | SSTL | I/O |
| DDR1_DQ[46] | B33 | SSTL | I/O |



Table A-1. Pin List By Name (Sheet 9 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR1_DQ[47] | F33 | SSTL | I/O |
| DDR1_DQ[48] | C30 | SSTL | I/O |
| DDR1_DQ[49] | B29 | SSTL | I/O |
| DDR1_DQ[5] | AV79 | SSTL | I/O |
| DDR1_DQ[50] | C26 | SSTL | I/O |
| DDR1_DQ[51] | E26 | SSTL | I/O |
| DDR1_DQ[52] | E30 | SSTL | I/O |
| DDR1_DQ[53] | F29 | SSTL | I/O |
| DDR1_DQ[54] | B27 | SSTL | I/O |
| DDR1_DQ[55] | F27 | SSTL | I/O |
| DDR1_DQ[56] | U28 | SSTL | I/O |
| DDR1_DQ[57] | AA28 | SSTL | I/O |
| DDR1_DQ[58] | V25 | SSTL | I/O |
| DDR1_DQ[59] | Y25 | SSTL | I/O |
| DDR1_DQ[6] | AR82 | SSTL | I/O |
| DDR1_DQ[60] | V29 | SSTL | I/O |
| DDR1_DQ[61] | Y29 | SSTL | I/O |
| DDR1_DQ[62] | U26 | SSTL | I/O |
| DDR1_DQ[63] | AA26 | SSTL | I/O |
| DDR1_DQ[7] | AN80 | SSTL | I/O |
| DDR1_DQ[8] | AH81 | SSTL | I/O |
| DDR1_DQ[9] | AF79 | SSTL | I/O |
| DDR1_DQS_DN[0] | AP79 | SSTL | I/O |
| DDR1_DQS_DN[1] | AD79 | SSTL | I/O |
| DDR1_DQS_DN[10] | AG82 | SSTL | I/O |
| DDR1_DQS_DN[11] | D79 | SSTL | I/O |
| DDR1_DQS_DN[12] | B73 | SSTL | I/O |
| DDR1_DQS_DN[13] | J42 | SSTL | I/O |
| DDR1_DQS_DN[14] | A34 | SSTL | I/O |
| DDR1_DQS_DN[15] | A28 | SSTL | I/O |
| DDR1_DQS_DN[16] | T27 | SSTL | I/O |
| DDR1_DQS_DN[17] | G68 | SSTL | I/O |
| DDR1_DQS_DN[2] | K79 | SSTL | I/O |
| DDR1_DQS_DN[3] | H73 | SSTL | I/O |
| DDR1_DQS_DN[4] | N42 | SSTL | I/O |
| DDR1_DQS_DN[5] | G34 | SSTL | I/O |
| DDR1_DQS_DN[6] | G28 | SSTL | I/O |
| DDR1_DQS_DN[7] | AB27 | SSTL | I/O |
| DDR1_DQS_DN[8] | N68 | SSTL | I/O |
| DDR1_DQS_DN[9] | AU82 | SSTL | I/O |
| DDR1_DQS_DP[0] | AR80 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 10 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR1_DQS_DP[1] | AE80 | SSTL | I/O |
| DDR1_DQS_DP[10] | AF81 | SSTL | I/O |
| DDR1_DQS_DP[11] | F79 | SSTL | I/O |
| DDR1_DQS_DP[12] | D73 | SSTL | I/O |
| DDR1_DQS_DP[13] | L42 | SSTL | I/O |
| DDR1_DQS_DP[14] | C34 | SSTL | I/O |
| DDR1_DQS_DP[15] | C28 | SSTL | I/O |
| DDR1_DQS_DP[16] | V27 | SSTL | I/O |
| DDR1_DQS_DP[17] | J68 | SSTL | I/O |
| DDR1_DQS_DP[2] | H79 | SSTL | I/O |
| DDR1_DQS_DP[3] | F73 | SSTL | I/O |
| DDR1_DQS_DP[4] | R42 | SSTL | I/O |
| DDR1_DQS_DP[5] | E34 | SSTL | I/O |
| DDR1_DQS_DP[6] | E28 | SSTL | I/O |
| DDR1_DQS_DP[7] | Y27 | SSTL | I/O |
| DDR1_DQS_DP[8] | L68 | SSTL | I/O |
| DDR1_DQS_DP[9] | AT81 | SSTL | I/O |
| DDR1_ECC[0] | J70 | SSTL | I/O |
| DDR1_ECC[1] | H69 | SSTL | I/O |
| DDR1_ECC[2] | J66 | SSTL | I/O |
| DDR1_ECC[3] | L66 | SSTL | I/O |
| DDR1_ECC[4] | L70 | SSTL | I/O |
| DDR1_ECC[5] | M69 | SSTL | I/O |
| DDR1_ECC[6] | H67 | SSTL | I/O |
| DDR1_ECC[7] | M67 | SSTL | I/O |
| DDR1_MA[0] | J52 | SSTL | O |
| DDR1_MA[1] | J58 | SSTL | O |
| DDR1_MA[10] | M55 | SSTL | O |
| DDR1_MA[11] | R60 | SSTL | O |
| DDR1_MA[12] | T61 | SSTL | O |
| DDR1_MA[13] | M51 | SSTL | O |
| DDR1_MA[14] | T51 | SSTL | O |
| DDR1_MA[15] | N52 | SSTL | O |
| DDR1_MA[16] | R52 | SSTL | O |
| DDR1_MA[17] | N48 | SSTL | O |
| DDR1_MA[2] | K57 | SSTL | O |
| DDR1_MA[3] | N58 | SSTL | O |
| DDR1_MA[4] | M59 | SSTL | O |
| DDR1_MA[5] | R58 | SSTL | O |
| DDR1_MA[6] | T59 | SSTL | O |
| DDR1_MA[7] | V61 | SSTL | O |



Table A-1. Pin List By Name (Sheet 11 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|------|-----|
| DDR1_MA[8] | W60 | SSTL | O |
| DDR1_MA[9] | K59 | SSTL | O |
| DDR1_ODT[0] | N50 | SSTL | O |
| DDR1_ODT[1] | R48 | SSTL | O |
| DDR1_ODT[2] | M49 | SSTL | O |
| DDR1_ODT[3] | T47 | SSTL | O |
| DDR1_PAR | K53 | SSTL | O |
| DDR2_ACT_N | AB61 | SSTL | O |
| DDR2_ALERT_N | AD61 | SSTL | I |
| DDR2_BA[0] | W52 | SSTL | O |
| DDR2_BA[1] | AE56 | SSTL | O |
| DDR2_BG[0] | AA60 | SSTL | O |
| DDR2_BG[1] | AE62 | SSTL | O |
| DDR2_CAVREF | AH63 | SSTL | O |
| DDR2_CID[2] | AB45 | SSTL | O |
| DDR2_CKE[0] | AA62 | SSTL | O |
| DDR2_CKE[1] | AD63 | SSTL | O |
| DDR2_CKE[2] | V63 | SSTL | O |
| DDR2_CKE[3] | AB63 | SSTL | O |
| DDR2_CLK_DN[0] | AA54 | SSTL | O |
| DDR2_CLK_DN[1] | W54 | SSTL | O |
| DDR2_CLK_DN[2] | AA56 | SSTL | O |
| DDR2_CLK_DN[3] | W56 | SSTL | O |
| DDR2_CLK_DP[0] | AB55 | SSTL | O |
| DDR2_CLK_DP[1] | V55 | SSTL | O |
| DDR2_CLK_DP[2] | AB57 | SSTL | O |
| DDR2_CLK_DP[3] | V57 | SSTL | O |
| DDR2_CS_N[0] | V51 | SSTL | O |
| DDR2_CS_N[1] | AB49 | SSTL | O |
| DDR2_CS_N[2] | W46 | SSTL | O |
| DDR2_CS_N[3] | AA46 | SSTL | O |
| DDR2_CS_N[4] | AB51 | SSTL | O |
| DDR2_CS_N[5] | W48 | SSTL | O |
| DDR2_CS_N[6] | T45 | SSTL | O |
| DDR2_CS_N[7] | V45 | SSTL | O |
| DDR2_DQ[0] | AR76 | SSTL | I/O |
| DDR2_DQ[1] | AN74 | SSTL | I/O |
| DDR2_DQ[10] | Y77 | SSTL | I/O |
| DDR2_DQ[11] | W76 | SSTL | I/O |
| DDR2_DQ[12] | AF75 | SSTL | I/O |
| DDR2_DQ[13] | AE74 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 12 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| DDR2_DQ[14] | AB77 | SSTL | I/O |
| DDR2_DQ[15] | Y75 | SSTL | I/O |
| DDR2_DQ[16] | W72 | SSTL | I/O |
| DDR2_DQ[17] | AA70 | SSTL | I/O |
| DDR2_DQ[18] | R70 | SSTL | I/O |
| DDR2_DQ[19] | T69 | SSTL | I/O |
| DDR2_DQ[2] | AK77 | SSTL | I/O |
| DDR2_DQ[20] | AA72 | SSTL | I/O |
| DDR2_DQ[21] | AB71 | SSTL | I/O |
| DDR2_DQ[22] | T71 | SSTL | I/O |
| DDR2_DQ[23] | V69 | SSTL | I/O |
| DDR2_DQ[24] | AM67 | SSTL | I/O |
| DDR2_DQ[25] | AT67 | SSTL | I/O |
| DDR2_DQ[26] | AN64 | SSTL | I/O |
| DDR2_DQ[27] | AR64 | SSTL | I/O |
| DDR2_DQ[28] | AN68 | SSTL | I/O |
| DDR2_DQ[29] | AR68 | SSTL | I/O |
| DDR2_DQ[3] | AJ76 | SSTL | I/O |
| DDR2_DQ[30] | AM65 | SSTL | I/O |
| DDR2_DQ[31] | AT65 | SSTL | I/O |
| DDR2_DQ[32] | U40 | SSTL | I/O |
| DDR2_DQ[33] | AA40 | SSTL | I/O |
| DDR2_DQ[34] | V37 | SSTL | I/O |
| DDR2_DQ[35] | Y37 | SSTL | I/O |
| DDR2_DQ[36] | V41 | SSTL | I/O |
| DDR2_DQ[37] | Y41 | SSTL | I/O |
| DDR2_DQ[38] | U38 | SSTL | I/O |
| DDR2_DQ[39] | AA38 | SSTL | I/O |
| DDR2_DQ[4] | AT75 | SSTL | I/O |
| DDR2_DQ[40] | U34 | SSTL | I/O |
| DDR2_DQ[41] | AA34 | SSTL | I/O |
| DDR2_DQ[42] | V31 | SSTL | I/O |
| DDR2_DQ[43] | Y31 | SSTL | I/O |
| DDR2_DQ[44] | V35 | SSTL | I/O |
| DDR2_DQ[45] | Y35 | SSTL | I/O |
| DDR2_DQ[46] | U32 | SSTL | I/O |
| DDR2_DQ[47] | AA32 | SSTL | I/O |
| DDR2_DQ[48] | AD31 | SSTL | I/O |
| DDR2_DQ[49] | AH31 | SSTL | I/O |
| DDR2_DQ[5] | AR74 | SSTL | I/O |
| DDR2_DQ[50] | AE28 | SSTL | I/O |



Table A-1. Pin List By Name (Sheet 13 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR2_DQ[51] | AG28 | SSTL | I/O |
| DDR2_DQ[52] | AE32 | SSTL | I/O |
| DDR2_DQ[53] | AG32 | SSTL | I/O |
| DDR2_DQ[54] | AD29 | SSTL | I/O |
| DDR2_DQ[55] | AH29 | SSTL | I/O |
| DDR2_DQ[56] | AD25 | SSTL | I/O |
| DDR2_DQ[57] | AH25 | SSTL | I/O |
| DDR2_DQ[58] | AE22 | SSTL | I/O |
| DDR2_DQ[59] | AG22 | SSTL | I/O |
| DDR2_DQ[6] | AM77 | SSTL | I/O |
| DDR2_DQ[60] | AE26 | SSTL | I/O |
| DDR2_DQ[61] | AG26 | SSTL | I/O |
| DDR2_DQ[62] | AD23 | SSTL | I/O |
| DDR2_DQ[63] | AH23 | SSTL | I/O |
| DDR2_DQ[7] | AK75 | SSTL | I/O |
| DDR2_DQ[8] | AE76 | SSTL | I/O |
| DDR2_DQ[9] | AC74 | SSTL | I/O |
| DDR2_DQS_DN[0] | AL74 | SSTL | I/O |
| DDR2_DQS_DN[1] | AA74 | SSTL | I/O |
| DDR2_DQS_DN[10] | AD77 | SSTL | I/O |
| DDR2_DQS_DN[11] | U72 | SSTL | I/O |
| DDR2_DQS_DN[12] | AL66 | SSTL | I/O |
| DDR2_DQS_DN[13] | T39 | SSTL | I/O |
| DDR2_DQS_DN[14] | T33 | SSTL | I/O |
| DDR2_DQS_DN[15] | AC30 | SSTL | I/O |
| DDR2_DQS_DN[16] | AC24 | SSTL | I/O |
| DDR2_DQS_DN[17] | AT71 | SSTL | I/O |
| DDR2_DQS_DN[2] | Y69 | SSTL | I/O |
| DDR2_DQS_DN[3] | AU66 | SSTL | I/O |
| DDR2_DQS_DN[4] | AB39 | SSTL | I/O |
| DDR2_DQS_DN[5] | AB33 | SSTL | I/O |
| DDR2_DQS_DN[6] | AJ30 | SSTL | I/O |
| DDR2_DQS_DN[7] | AJ24 | SSTL | I/O |
| DDR2_DQS_DN[8] | BB71 | SSTL | I/O |
| DDR2_DQS_DN[9] | AP77 | SSTL | I/O |
| DDR2_DQS_DP[0] | AM75 | SSTL | I/O |
| DDR2_DQS_DP[1] | AB75 | SSTL | I/O |
| DDR2_DQS_DP[10] | AC76 | SSTL | I/O |
| DDR2_DQS_DP[11] | V71 | SSTL | I/O |
| DDR2_DQS_DP[12] | AN66 | SSTL | I/O |
| DDR2_DQS_DP[13] | V39 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 14 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR2_DQS_DP[14] | V33 | SSTL | I/O |
| DDR2_DQS_DP[15] | AE30 | SSTL | I/O |
| DDR2_DQS_DP[16] | AE24 | SSTL | I/O |
| DDR2_DQS_DP[17] | AV71 | SSTL | I/O |
| DDR2_DQS_DP[2] | W70 | SSTL | I/O |
| DDR2_DQS_DP[3] | AR66 | SSTL | I/O |
| DDR2_DQS_DP[4] | Y39 | SSTL | I/O |
| DDR2_DQS_DP[5] | Y33 | SSTL | I/O |
| DDR2_DQS_DP[6] | AG30 | SSTL | I/O |
| DDR2_DQS_DP[7] | AG24 | SSTL | I/O |
| DDR2_DQS_DP[8] | AY71 | SSTL | I/O |
| DDR2_DQS_DP[9] | AN76 | SSTL | I/O |
| DDR2_ECC[0] | AU72 | SSTL | I/O |
| DDR2_ECC[1] | BA72 | SSTL | I/O |
| DDR2_ECC[2] | AV69 | SSTL | I/O |
| DDR2_ECC[3] | AY69 | SSTL | I/O |
| DDR2_ECC[4] | AV73 | SSTL | I/O |
| DDR2_ECC[5] | AY73 | SSTL | I/O |
| DDR2_ECC[6] | AU70 | SSTL | I/O |
| DDR2_ECC[7] | BA70 | SSTL | I/O |
| DDR2_MA[0] | AB53 | SSTL | O |
| DDR2_MA[1] | AE58 | SSTL | O |
| DDR2_MA[10] | AD55 | SSTL | O |
| DDR2_MA[11] | AG60 | SSTL | O |
| DDR2_MA[12] | AG62 | SSTL | O |
| DDR2_MA[13] | AD53 | SSTL | O |
| DDR2_MA[14] | W50 | SSTL | O |
| DDR2_MA[15] | AE54 | SSTL | O |
| DDR2_MA[16] | AA52 | SSTL | O |
| DDR2_MA[17] | AC46 | SSTL | O |
| DDR2_MA[2] | AD57 | SSTL | O |
| DDR2_MA[3] | W58 | SSTL | O |
| DDR2_MA[4] | AA58 | SSTL | O |
| DDR2_MA[5] | V59 | SSTL | O |
| DDR2_MA[6] | AB59 | SSTL | O |
| DDR2_MA[7] | AE60 | SSTL | O |
| DDR2_MA[8] | AD59 | SSTL | O |
| DDR2_MA[9] | AG58 | SSTL | O |
| DDR2_ODT[0] | AA50 | SSTL | O |
| DDR2_ODT[1] | AA48 | SSTL | O |
| DDR2_ODT[2] | V49 | SSTL | O |



Table A-1. Pin List By Name (Sheet 15 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|------|-----|
| DDR2_ODT[3] | AB47 | SSTL | O |
| DDR2_PAR | V53 | SSTL | O |
| DDR3_ACT_N | DW60 | SSTL | O |
| DDR3_ALERT_N | ED63 | SSTL | I |
| DDR3_BA[0] | EE52 | SSTL | O |
| DDR3_BA[1] | EA54 | SSTL | O |
| DDR3_BG[0] | ED61 | SSTL | O |
| DDR3_BG[1] | DW62 | SSTL | O |
| DDR3_CAVREF | CP61 | SSTL | O |
| DDR3_CID[2] | DV47 | SSTL | O |
| DDR3_CKE[0] | EE62 | SSTL | O |
| DDR3_CKE[1] | EF63 | SSTL | O |
| DDR3_CKE[2] | EA62 | SSTL | O |
| DDR3_CKE[3] | EB63 | SSTL | O |
| DDR3_CLK_DN[0] | ED55 | SSTL | O |
| DDR3_CLK_DN[1] | EF55 | SSTL | O |
| DDR3_CLK_DN[2] | DW56 | SSTL | O |
| DDR3_CLK_DN[3] | EF57 | SSTL | O |
| DDR3_CLK_DP[0] | EB55 | SSTL | O |
| DDR3_CLK_DP[1] | EE54 | SSTL | O |
| DDR3_CLK_DP[2] | EA56 | SSTL | O |
| DDR3_CLK_DP[3] | EE56 | SSTL | O |
| DDR3_CS_N[0] | EF51 | SSTL | O |
| DDR3_CS_N[1] | ED49 | SSTL | O |
| DDR3_CS_N[2] | ED47 | SSTL | O |
| DDR3_CS_N[3] | EB47 | SSTL | O |
| DDR3_CS_N[4] | EB51 | SSTL | O |
| DDR3_CS_N[5] | EB49 | SSTL | O |
| DDR3_CS_N[6] | DV45 | SSTL | O |
| DDR3_CS_N[7] | EB45 | SSTL | O |
| DDR3_DQ[0] | CN84 | SSTL | I/O |
| DDR3_DQ[1] | CN86 | SSTL | I/O |
| DDR3_DQ[10] | DV83 | SSTL | I/O |
| DDR3_DQ[11] | DY83 | SSTL | I/O |
| DDR3_DQ[12] | DD85 | SSTL | I/O |
| DDR3_DQ[13] | DE84 | SSTL | I/O |
| DDR3_DQ[14] | DR84 | SSTL | I/O |
| DDR3_DQ[15] | DV85 | SSTL | I/O |
| DDR3_DQ[16] | DM79 | SSTL | I/O |
| DDR3_DQ[17] | DK81 | SSTL | I/O |
| DDR3_DQ[18] | DT81 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 16 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| DDR3_DQ[19] | DR82 | SSTL | I/O |
| DDR3_DQ[2] | DA86 | SSTL | I/O |
| DDR3_DQ[20] | DK79 | SSTL | I/O |
| DDR3_DQ[21] | DJ80 | SSTL | I/O |
| DDR3_DQ[22] | DR80 | SSTL | I/O |
| DDR3_DQ[23] | DN82 | SSTL | I/O |
| DDR3_DQ[24] | DN76 | SSTL | I/O |
| DDR3_DQ[25] | DU76 | SSTL | I/O |
| DDR3_DQ[26] | DP73 | SSTL | I/O |
| DDR3_DQ[27] | DT73 | SSTL | I/O |
| DDR3_DQ[28] | DP77 | SSTL | I/O |
| DDR3_DQ[29] | DT77 | SSTL | I/O |
| DDR3_DQ[3] | DA84 | SSTL | I/O |
| DDR3_DQ[30] | DN74 | SSTL | I/O |
| DDR3_DQ[31] | DU74 | SSTL | I/O |
| DDR3_DQ[32] | EC40 | SSTL | I/O |
| DDR3_DQ[33] | ED39 | SSTL | I/O |
| DDR3_DQ[34] | EA36 | SSTL | I/O |
| DDR3_DQ[35] | EC36 | SSTL | I/O |
| DDR3_DQ[36] | DY39 | SSTL | I/O |
| DDR3_DQ[37] | EA40 | SSTL | I/O |
| DDR3_DQ[38] | DY37 | SSTL | I/O |
| DDR3_DQ[39] | ED37 | SSTL | I/O |
| DDR3_DQ[4] | CL84 | SSTL | I/O |
| DDR3_DQ[40] | DN36 | SSTL | I/O |
| DDR3_DQ[41] | DU36 | SSTL | I/O |
| DDR3_DQ[42] | DP33 | SSTL | I/O |
| DDR3_DQ[43] | DT33 | SSTL | I/O |
| DDR3_DQ[44] | DP37 | SSTL | I/O |
| DDR3_DQ[45] | DT37 | SSTL | I/O |
| DDR3_DQ[46] | DN34 | SSTL | I/O |
| DDR3_DQ[47] | DU34 | SSTL | I/O |
| DDR3_DQ[48] | DN30 | SSTL | I/O |
| DDR3_DQ[49] | DU30 | SSTL | I/O |
| DDR3_DQ[5] | CL86 | SSTL | I/O |
| DDR3_DQ[50] | DP27 | SSTL | I/O |
| DDR3_DQ[51] | DT27 | SSTL | I/O |
| DDR3_DQ[52] | DP31 | SSTL | I/O |
| DDR3_DQ[53] | DT31 | SSTL | I/O |
| DDR3_DQ[54] | DN28 | SSTL | I/O |
| DDR3_DQ[55] | DU28 | SSTL | I/O |



Table A-1. Pin List By Name (Sheet 17 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR3_DQ[56] | DN24 | SSTL | I/O |
| DDR3_DQ[57] | DU24 | SSTL | I/O |
| DDR3_DQ[58] | DY21 | SSTL | I/O |
| DDR3_DQ[59] | EB21 | SSTL | I/O |
| DDR3_DQ[6] | CW86 | SSTL | I/O |
| DDR3_DQ[60] | DP25 | SSTL | I/O |
| DDR3_DQ[61] | DT25 | SSTL | I/O |
| DDR3_DQ[62] | EC22 | SSTL | I/O |
| DDR3_DQ[63] | DW22 | SSTL | I/O |
| DDR3_DQ[7] | CW84 | SSTL | I/O |
| DDR3_DQ[8] | DG84 | SSTL | I/O |
| DDR3_DQ[9] | DH85 | SSTL | I/O |
| DDR3_DQS_DN[0] | CU84 | SSTL | I/O |
| DDR3_DQS_DN[1] | DN84 | SSTL | I/O |
| DDR3_DQS_DN[10] | DM85 | SSTL | I/O |
| DDR3_DQS_DN[11] | DN80 | SSTL | I/O |
| DDR3_DQS_DN[12] | DP75 | SSTL | I/O |
| DDR3_DQS_DN[13] | EA38 | SSTL | I/O |
| DDR3_DQS_DN[14] | DP35 | SSTL | I/O |
| DDR3_DQS_DN[15] | DM29 | SSTL | I/O |
| DDR3_DQS_DN[16] | DM23 | SSTL | I/O |
| DDR3_DQS_DN[17] | DB67 | SSTL | I/O |
| DDR3_DQS_DN[2] | DL82 | SSTL | I/O |
| DDR3_DQS_DN[3] | DV75 | SSTL | I/O |
| DDR3_DQS_DN[4] | EE38 | SSTL | I/O |
| DDR3_DQS_DN[5] | DV35 | SSTL | I/O |
| DDR3_DQS_DN[6] | DV29 | SSTL | I/O |
| DDR3_DQS_DN[7] | DV23 | SSTL | I/O |
| DDR3_DQS_DN[8] | DF67 | SSTL | I/O |
| DDR3_DQS_DN[9] | CR84 | SSTL | I/O |
| DDR3_DQS_DP[0] | CV85 | SSTL | I/O |
| DDR3_DQS_DP[1] | DP85 | SSTL | I/O |
| DDR3_DQS_DP[10] | DL84 | SSTL | I/O |
| DDR3_DQS_DP[11] | DP79 | SSTL | I/O |
| DDR3_DQS_DP[12] | DM75 | SSTL | I/O |
| DDR3_DQS_DP[13] | DW38 | SSTL | I/O |
| DDR3_DQS_DP[14] | DM35 | SSTL | I/O |
| DDR3_DQS_DP[15] | DP29 | SSTL | I/O |
| DDR3_DQS_DP[16] | DP23 | SSTL | I/O |
| DDR3_DQS_DP[17] | CY67 | SSTL | I/O |
| DDR3_DQS_DP[2] | DM81 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 18 of 90)

| Pin Name | Location | Type | I/O |
|--------------------|----------|------|-----|
| DDR3_DQS_DP[3] | DT75 | SSTL | I/O |
| DDR3_DQS_DP[4] | EC38 | SSTL | I/O |
| DDR3_DQS_DP[5] | DT35 | SSTL | I/O |
| DDR3_DQS_DP[6] | DT29 | SSTL | I/O |
| DDR3_DQS_DP[7] | DT23 | SSTL | I/O |
| DDR3_DQS_DP[8] | DD67 | SSTL | I/O |
| DDR3_DQS_DP[9] | CP85 | SSTL | I/O |
| DDR3_ECC[0] | DA68 | SSTL | I/O |
| DDR3_ECC[1] | DE68 | SSTL | I/O |
| DDR3_ECC[2] | DB65 | SSTL | I/O |
| DDR3_ECC[3] | DD65 | SSTL | I/O |
| DDR3_ECC[4] | DB69 | SSTL | I/O |
| DDR3_ECC[5] | DD69 | SSTL | I/O |
| DDR3_ECC[6] | DA66 | SSTL | I/O |
| DDR3_ECC[7] | DE66 | SSTL | I/O |
| DDR3_MA[0] | EB53 | SSTL | O |
| DDR3_MA[1] | ED57 | SSTL | O |
| DDR3_MA[10] | DW54 | SSTL | O |
| DDR3_MA[11] | EB61 | SSTL | O |
| DDR3_MA[12] | DT63 | SSTL | O |
| DDR3_MA[13] | DW48 | SSTL | O |
| DDR3_MA[14] | ED51 | SSTL | O |
| DDR3_MA[15] | DV49 | SSTL | O |
| DDR3_MA[16] | EA52 | SSTL | O |
| DDR3_MA[17] | EA46 | SSTL | O |
| DDR3_MA[2] | EE58 | SSTL | O |
| DDR3_MA[3] | EB57 | SSTL | O |
| DDR3_MA[4] | ED59 | SSTL | O |
| DDR3_MA[5] | EA58 | SSTL | O |
| DDR3_MA[6] | EE60 | SSTL | O |
| DDR3_MA[7] | EA60 | SSTL | O |
| DDR3_MA[8] | EB59 | SSTL | O |
| DDR3_MA[9] | EF61 | SSTL | O |
| DDR3_ODT[0] | EE50 | SSTL | O |
| DDR3_ODT[1] | EE48 | SSTL | O |
| DDR3_ODT[2] | EA50 | SSTL | O |
| DDR3_ODT[3] | EA48 | SSTL | O |
| DDR3_PAR | ED53 | SSTL | O |
| DDR345_DRAM_PWR_OK | CR28 | CMOS | I |
| DDR345_RCOMP[0] | DC48 | | |
| DDR345_RCOMP[1] | DD47 | | |



Table A-1. Pin List By Name (Sheet 19 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|--------|-----|
| DDR345_RCOMP[2] | DD49 | | |
| DDR345_RESET_N | DV63 | CMOS | O |
| DDR345_SPDSCL | AE18 | ODCMOS | I/O |
| DDR345_SPDSDA | AD17 | ODCMOS | I/O |
| DDR4_ACT_N | DR62 | SSTL | O |
| DDR4_ALERT_N | DT61 | SSTL | I |
| DDR4_BA[0] | DM53 | SSTL | O |
| DDR4_BA[1] | DV55 | SSTL | O |
| DDR4_BG[0] | DJ62 | SSTL | O |
| DDR4_BG[1] | DM61 | SSTL | O |
| DDR4_CAVREF | CT61 | SSTL | O |
| DDR4_CID[2] | DT47 | SSTL | O |
| DDR4_CKE[0] | DM63 | SSTL | O |
| DDR4_CKE[1] | DN64 | SSTL | O |
| DDR4_CKE[2] | DL64 | SSTL | O |
| DDR4_CKE[3] | DR64 | SSTL | O |
| DDR4_CLK_DN[0] | DM55 | SSTL | O |
| DDR4_CLK_DN[1] | DR54 | SSTL | O |
| DDR4_CLK_DN[2] | DM57 | SSTL | O |
| DDR4_CLK_DN[3] | DT57 | SSTL | O |
| DDR4_CLK_DP[0] | DN54 | SSTL | O |
| DDR4_CLK_DP[1] | DT53 | SSTL | O |
| DDR4_CLK_DP[2] | DN56 | SSTL | O |
| DDR4_CLK_DP[3] | DR56 | SSTL | O |
| DDR4_CS_N[0] | DV51 | SSTL | O |
| DDR4_CS_N[1] | DN50 | SSTL | O |
| DDR4_CS_N[2] | DR46 | SSTL | O |
| DDR4_CS_N[3] | DK47 | SSTL | O |
| DDR4_CS_N[4] | DW50 | SSTL | O |
| DDR4_CS_N[5] | DM49 | SSTL | O |
| DDR4_CS_N[6] | DT45 | SSTL | O |
| DDR4_CS_N[7] | DN46 | SSTL | O |
| DDR4_DQ[0] | CM79 | SSTL | I/O |
| DDR4_DQ[1] | CK81 | SSTL | I/O |
| DDR4_DQ[10] | DE80 | SSTL | I/O |
| DDR4_DQ[11] | DF81 | SSTL | I/O |
| DDR4_DQ[12] | CY79 | SSTL | I/O |
| DDR4_DQ[13] | CW80 | SSTL | I/O |
| DDR4_DQ[14] | DC82 | SSTL | I/O |
| DDR4_DQ[15] | DE82 | SSTL | I/O |
| DDR4_DQ[16] | DW80 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 20 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| DDR4_DQ[17] | EC80 | SSTL | I/O |
| DDR4_DQ[18] | DY77 | SSTL | I/O |
| DDR4_DQ[19] | EB77 | SSTL | I/O |
| DDR4_DQ[2] | CT81 | SSTL | I/O |
| DDR4_DQ[20] | DY81 | SSTL | I/O |
| DDR4_DQ[21] | EB81 | SSTL | I/O |
| DDR4_DQ[22] | DW78 | SSTL | I/O |
| DDR4_DQ[23] | EC78 | SSTL | I/O |
| DDR4_DQ[24] | ED75 | SSTL | I/O |
| DDR4_DQ[25] | EE74 | SSTL | I/O |
| DDR4_DQ[26] | EB71 | SSTL | I/O |
| DDR4_DQ[27] | ED71 | SSTL | I/O |
| DDR4_DQ[28] | EA74 | SSTL | I/O |
| DDR4_DQ[29] | EB75 | SSTL | I/O |
| DDR4_DQ[3] | CR82 | SSTL | I/O |
| DDR4_DQ[30] | EA72 | SSTL | I/O |
| DDR4_DQ[31] | EE72 | SSTL | I/O |
| DDR4_DQ[32] | DU42 | SSTL | I/O |
| DDR4_DQ[33] | DW42 | SSTL | I/O |
| DDR4_DQ[34] | DP39 | SSTL | I/O |
| DDR4_DQ[35] | DT39 | SSTL | I/O |
| DDR4_DQ[36] | DL42 | SSTL | I/O |
| DDR4_DQ[37] | DN42 | SSTL | I/O |
| DDR4_DQ[38] | DN40 | SSTL | I/O |
| DDR4_DQ[39] | DU40 | SSTL | I/O |
| DDR4_DQ[4] | CK79 | SSTL | I/O |
| DDR4_DQ[40] | EC34 | SSTL | I/O |
| DDR4_DQ[41] | ED33 | SSTL | I/O |
| DDR4_DQ[42] | EA30 | SSTL | I/O |
| DDR4_DQ[43] | EC30 | SSTL | I/O |
| DDR4_DQ[44] | DY33 | SSTL | I/O |
| DDR4_DQ[45] | EA34 | SSTL | I/O |
| DDR4_DQ[46] | DY31 | SSTL | I/O |
| DDR4_DQ[47] | ED31 | SSTL | I/O |
| DDR4_DQ[48] | EC28 | SSTL | I/O |
| DDR4_DQ[49] | ED27 | SSTL | I/O |
| DDR4_DQ[5] | CJ80 | SSTL | I/O |
| DDR4_DQ[50] | EA24 | SSTL | I/O |
| DDR4_DQ[51] | EC24 | SSTL | I/O |
| DDR4_DQ[52] | DY27 | SSTL | I/O |
| DDR4_DQ[53] | EA28 | SSTL | I/O |



Table A-1. Pin List By Name (Sheet 21 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR4_DQ[54] | DY25 | SSTL | I/O |
| DDR4_DQ[55] | ED25 | SSTL | I/O |
| DDR4_DQ[56] | DF27 | SSTL | I/O |
| DDR4_DQ[57] | DK27 | SSTL | I/O |
| DDR4_DQ[58] | DD25 | SSTL | I/O |
| DDR4_DQ[59] | DJ24 | SSTL | I/O |
| DDR4_DQ[6] | CR80 | SSTL | I/O |
| DDR4_DQ[60] | DG28 | SSTL | I/O |
| DDR4_DQ[61] | DJ28 | SSTL | I/O |
| DDR4_DQ[62] | DF25 | SSTL | I/O |
| DDR4_DQ[63] | DK25 | SSTL | I/O |
| DDR4_DQ[7] | CN82 | SSTL | I/O |
| DDR4_DQ[8] | DB79 | SSTL | I/O |
| DDR4_DQ[9] | CY81 | SSTL | I/O |
| DDR4_DQS_DN[0] | CL82 | SSTL | I/O |
| DDR4_DQS_DN[1] | DA82 | SSTL | I/O |
| DDR4_DQS_DN[10] | DC80 | SSTL | I/O |
| DDR4_DQS_DN[11] | DY79 | SSTL | I/O |
| DDR4_DQS_DN[12] | EB73 | SSTL | I/O |
| DDR4_DQS_DN[13] | DP41 | SSTL | I/O |
| DDR4_DQS_DN[14] | EA32 | SSTL | I/O |
| DDR4_DQS_DN[15] | EA26 | SSTL | I/O |
| DDR4_DQS_DN[16] | DG26 | SSTL | I/O |
| DDR4_DQS_DN[17] | DV67 | SSTL | I/O |
| DDR4_DQS_DN[2] | ED79 | SSTL | I/O |
| DDR4_DQS_DN[3] | EF73 | SSTL | I/O |
| DDR4_DQS_DN[4] | DV41 | SSTL | I/O |
| DDR4_DQS_DN[5] | EE32 | SSTL | I/O |
| DDR4_DQS_DN[6] | EE26 | SSTL | I/O |
| DDR4_DQS_DN[7] | DL26 | SSTL | I/O |
| DDR4_DQS_DN[8] | EB67 | SSTL | I/O |
| DDR4_DQS_DN[9] | CN80 | SSTL | I/O |
| DDR4_DQS_DP[0] | CM81 | SSTL | I/O |
| DDR4_DQS_DP[1] | DB81 | SSTL | I/O |
| DDR4_DQS_DP[10] | DD79 | SSTL | I/O |
| DDR4_DQS_DP[11] | DV79 | SSTL | I/O |
| DDR4_DQS_DP[12] | DY73 | SSTL | I/O |
| DDR4_DQS_DP[13] | DM41 | SSTL | I/O |
| DDR4_DQS_DP[14] | DW32 | SSTL | I/O |
| DDR4_DQS_DP[15] | DW26 | SSTL | I/O |
| DDR4_DQS_DP[16] | DE26 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 22 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR4_DQS_DP[17] | DT67 | SSTL | I/O |
| DDR4_DQS_DP[2] | EB79 | SSTL | I/O |
| DDR4_DQS_DP[3] | ED73 | SSTL | I/O |
| DDR4_DQS_DP[4] | DT41 | SSTL | I/O |
| DDR4_DQS_DP[5] | EC32 | SSTL | I/O |
| DDR4_DQS_DP[6] | EC26 | SSTL | I/O |
| DDR4_DQS_DP[7] | DJ26 | SSTL | I/O |
| DDR4_DQS_DP[8] | DY67 | SSTL | I/O |
| DDR4_DQS_DP[9] | CP79 | SSTL | I/O |
| DDR4_ECC[0] | DY69 | SSTL | I/O |
| DDR4_ECC[1] | EA68 | SSTL | I/O |
| DDR4_ECC[2] | DV65 | SSTL | I/O |
| DDR4_ECC[3] | DY65 | SSTL | I/O |
| DDR4_ECC[4] | DU68 | SSTL | I/O |
| DDR4_ECC[5] | DV69 | SSTL | I/O |
| DDR4_ECC[6] | DU66 | SSTL | I/O |
| DDR4_ECC[7] | EA66 | SSTL | I/O |
| DDR4_MA[0] | DW52 | SSTL | O |
| DDR4_MA[1] | DW58 | SSTL | O |
| DDR4_MA[10] | DT55 | SSTL | O |
| DDR4_MA[11] | DR60 | SSTL | O |
| DDR4_MA[12] | DN60 | SSTL | O |
| DDR4_MA[13] | DT51 | SSTL | O |
| DDR4_MA[14] | DM51 | SSTL | O |
| DDR4_MA[15] | DR52 | SSTL | O |
| DDR4_MA[16] | DN52 | SSTL | O |
| DDR4_MA[17] | DR48 | SSTL | O |
| DDR4_MA[2] | DV57 | SSTL | O |
| DDR4_MA[3] | DR58 | SSTL | O |
| DDR4_MA[4] | DT59 | SSTL | O |
| DDR4_MA[5] | DN58 | SSTL | O |
| DDR4_MA[6] | DM59 | SSTL | O |
| DDR4_MA[7] | DK61 | SSTL | O |
| DDR4_MA[8] | DJ60 | SSTL | O |
| DDR4_MA[9] | DV59 | SSTL | O |
| DDR4_ODT[0] | DR50 | SSTL | O |
| DDR4_ODT[1] | DN48 | SSTL | O |
| DDR4_ODT[2] | DT49 | SSTL | O |
| DDR4_ODT[3] | DM47 | SSTL | O |
| DDR4_PAR | DV53 | SSTL | O |
| DDR5_ACT_N | DC62 | SSTL | O |



Table A-1. Pin List By Name (Sheet 23 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|------|-----|
| DDR5_ALERT_N | DD61 | SSTL | I |
| DDR5_BA[0] | DJ52 | SSTL | O |
| DDR5_BA[1] | DC56 | SSTL | O |
| DDR5_BG[0] | DA62 | SSTL | O |
| DDR5_BG[1] | DF61 | SSTL | O |
| DDR5_CAVREF | CV61 | SSTL | O |
| DDR5_CID[2] | DF45 | SSTL | O |
| DDR5_CKE[0] | DG62 | SSTL | O |
| DDR5_CKE[1] | DD63 | SSTL | O |
| DDR5_CKE[2] | DK63 | SSTL | O |
| DDR5_CKE[3] | DF63 | SSTL | O |
| DDR5_CLK_DN[0] | DK55 | SSTL | O |
| DDR5_CLK_DN[1] | DF55 | SSTL | O |
| DDR5_CLK_DN[2] | DK57 | SSTL | O |
| DDR5_CLK_DN[3] | DF57 | SSTL | O |
| DDR5_CLK_DP[0] | DJ54 | SSTL | O |
| DDR5_CLK_DP[1] | DG54 | SSTL | O |
| DDR5_CLK_DP[2] | DJ56 | SSTL | O |
| DDR5_CLK_DP[3] | DG56 | SSTL | O |
| DDR5_CS_N[0] | DK51 | SSTL | O |
| DDR5_CS_N[1] | DF49 | SSTL | O |
| DDR5_CS_N[2] | DJ46 | SSTL | O |
| DDR5_CS_N[3] | DG46 | SSTL | O |
| DDR5_CS_N[4] | DF51 | SSTL | O |
| DDR5_CS_N[5] | DJ48 | SSTL | O |
| DDR5_CS_N[6] | DM45 | SSTL | O |
| DDR5_CS_N[7] | DK45 | SSTL | O |
| DDR5_DQ[0] | CR74 | SSTL | I/O |
| DDR5_DQ[1] | CN76 | SSTL | I/O |
| DDR5_DQ[10] | DH75 | SSTL | I/O |
| DDR5_DQ[11] | DJ76 | SSTL | I/O |
| DDR5_DQ[12] | DC74 | SSTL | I/O |
| DDR5_DQ[13] | DB75 | SSTL | I/O |
| DDR5_DQ[14] | DF77 | SSTL | I/O |
| DDR5_DQ[15] | DH77 | SSTL | I/O |
| DDR5_DQ[16] | DG70 | SSTL | I/O |
| DDR5_DQ[17] | DJ72 | SSTL | I/O |
| DDR5_DQ[18] | DM69 | SSTL | I/O |
| DDR5_DQ[19] | DN70 | SSTL | I/O |
| DDR5_DQ[2] | CW76 | SSTL | I/O |
| DDR5_DQ[20] | DF71 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 24 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| DDR5_DQ[21] | DG72 | SSTL | I/O |
| DDR5_DQ[22] | DK69 | SSTL | I/O |
| DDR5_DQ[23] | DM71 | SSTL | I/O |
| DDR5_DQ[24] | CN66 | SSTL | I/O |
| DDR5_DQ[25] | CU66 | SSTL | I/O |
| DDR5_DQ[26] | CP63 | SSTL | I/O |
| DDR5_DQ[27] | CT63 | SSTL | I/O |
| DDR5_DQ[28] | CP67 | SSTL | I/O |
| DDR5_DQ[29] | CT67 | SSTL | I/O |
| DDR5_DQ[3] | CV77 | SSTL | I/O |
| DDR5_DQ[30] | CN64 | SSTL | I/O |
| DDR5_DQ[31] | CU64 | SSTL | I/O |
| DDR5_DQ[32] | DD41 | SSTL | I/O |
| DDR5_DQ[33] | DG42 | SSTL | I/O |
| DDR5_DQ[34] | DE38 | SSTL | I/O |
| DDR5_DQ[35] | DG38 | SSTL | I/O |
| DDR5_DQ[36] | DA42 | SSTL | I/O |
| DDR5_DQ[37] | DE42 | SSTL | I/O |
| DDR5_DQ[38] | DD39 | SSTL | I/O |
| DDR5_DQ[39] | DH39 | SSTL | I/O |
| DDR5_DQ[4] | CN74 | SSTL | I/O |
| DDR5_DQ[40] | DF33 | SSTL | I/O |
| DDR5_DQ[41] | DK33 | SSTL | I/O |
| DDR5_DQ[42] | DG30 | SSTL | I/O |
| DDR5_DQ[43] | DJ30 | SSTL | I/O |
| DDR5_DQ[44] | DG34 | SSTL | I/O |
| DDR5_DQ[45] | DJ34 | SSTL | I/O |
| DDR5_DQ[46] | DF31 | SSTL | I/O |
| DDR5_DQ[47] | DK31 | SSTL | I/O |
| DDR5_DQ[48] | CW36 | SSTL | I/O |
| DDR5_DQ[49] | DC36 | SSTL | I/O |
| DDR5_DQ[5] | CM75 | SSTL | I/O |
| DDR5_DQ[50] | CY33 | SSTL | I/O |
| DDR5_DQ[51] | DB33 | SSTL | I/O |
| DDR5_DQ[52] | CY37 | SSTL | I/O |
| DDR5_DQ[53] | DB37 | SSTL | I/O |
| DDR5_DQ[54] | CW34 | SSTL | I/O |
| DDR5_DQ[55] | DC34 | SSTL | I/O |
| DDR5_DQ[56] | CW30 | SSTL | I/O |
| DDR5_DQ[57] | DC30 | SSTL | I/O |
| DDR5_DQ[58] | CY27 | SSTL | I/O |



Table A-1. Pin List By Name (Sheet 25 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| DDR5_DQ[59] | DB27 | SSTL | I/O |
| DDR5_DQ[6] | CV75 | SSTL | I/O |
| DDR5_DQ[60] | CY31 | SSTL | I/O |
| DDR5_DQ[61] | DB31 | SSTL | I/O |
| DDR5_DQ[62] | CW28 | SSTL | I/O |
| DDR5_DQ[63] | DC28 | SSTL | I/O |
| DDR5_DQ[7] | CT77 | SSTL | I/O |
| DDR5_DQ[8] | DE74 | SSTL | I/O |
| DDR5_DQ[9] | DC76 | SSTL | I/O |
| DDR5_DQS_DN[0] | CP77 | SSTL | I/O |
| DDR5_DQS_DN[1] | DD77 | SSTL | I/O |
| DDR5_DQS_DN[10] | DF75 | SSTL | I/O |
| DDR5_DQS_DN[11] | DJ70 | SSTL | I/O |
| DDR5_DQS_DN[12] | CP65 | SSTL | I/O |
| DDR5_DQS_DN[13] | DE40 | SSTL | I/O |
| DDR5_DQS_DN[14] | DG32 | SSTL | I/O |
| DDR5_DQS_DN[15] | CY35 | SSTL | I/O |
| DDR5_DQS_DN[16] | CY29 | SSTL | I/O |
| DDR5_DQS_DN[17] | CJ70 | SSTL | I/O |
| DDR5_DQS_DN[2] | DL72 | SSTL | I/O |
| DDR5_DQS_DN[3] | CV65 | SSTL | I/O |
| DDR5_DQS_DN[4] | DG40 | SSTL | I/O |
| DDR5_DQS_DN[5] | DL32 | SSTL | I/O |
| DDR5_DQS_DN[6] | DD35 | SSTL | I/O |
| DDR5_DQS_DN[7] | DD29 | SSTL | I/O |
| DDR5_DQS_DN[8] | CN70 | SSTL | I/O |
| DDR5_DQS_DN[9] | CT75 | SSTL | I/O |
| DDR5_DQS_DP[0] | CR76 | SSTL | I/O |
| DDR5_DQS_DP[1] | DE76 | SSTL | I/O |
| DDR5_DQS_DP[10] | DG74 | SSTL | I/O |
| DDR5_DQS_DP[11] | DH69 | SSTL | I/O |
| DDR5_DQS_DP[12] | CM65 | SSTL | I/O |
| DDR5_DQS_DP[13] | DC40 | SSTL | I/O |
| DDR5_DQS_DP[14] | DE32 | SSTL | I/O |
| DDR5_DQS_DP[15] | CV35 | SSTL | I/O |
| DDR5_DQS_DP[16] | CV29 | SSTL | I/O |
| DDR5_DQS_DP[17] | CG70 | SSTL | I/O |
| DDR5_DQS_DP[2] | DK71 | SSTL | I/O |
| DDR5_DQS_DP[3] | CT65 | SSTL | I/O |
| DDR5_DQS_DP[4] | DJ40 | SSTL | I/O |
| DDR5_DQS_DP[5] | DJ32 | SSTL | I/O |

Table A-1. Pin List By Name (Sheet 26 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|-------|-----|
| DDR5_DQS_DP[6] | DB35 | SSTL | I/O |
| DDR5_DQS_DP[7] | DB29 | SSTL | I/O |
| DDR5_DQS_DP[8] | CL70 | SSTL | I/O |
| DDR5_DQS_DP[9] | CU74 | SSTL | I/O |
| DDR5_ECC[0] | CH71 | SSTL | I/O |
| DDR5_ECC[1] | CM71 | SSTL | I/O |
| DDR5_ECC[2] | CJ68 | SSTL | I/O |
| DDR5_ECC[3] | CL68 | SSTL | I/O |
| DDR5_ECC[4] | CJ72 | SSTL | I/O |
| DDR5_ECC[5] | CL72 | SSTL | I/O |
| DDR5_ECC[6] | CH69 | SSTL | I/O |
| DDR5_ECC[7] | CM69 | SSTL | I/O |
| DDR5_MA[0] | DF53 | SSTL | O |
| DDR5_MA[1] | DC58 | SSTL | O |
| DDR5_MA[10] | DD55 | SSTL | O |
| DDR5_MA[11] | DA60 | SSTL | O |
| DDR5_MA[12] | DG60 | SSTL | O |
| DDR5_MA[13] | DD53 | SSTL | O |
| DDR5_MA[14] | DJ50 | SSTL | O |
| DDR5_MA[15] | DC54 | SSTL | O |
| DDR5_MA[16] | DG52 | SSTL | O |
| DDR5_MA[17] | DE46 | SSTL | O |
| DDR5_MA[2] | DD57 | SSTL | O |
| DDR5_MA[3] | DG58 | SSTL | O |
| DDR5_MA[4] | DJ58 | SSTL | O |
| DDR5_MA[5] | DF59 | SSTL | O |
| DDR5_MA[6] | DK59 | SSTL | O |
| DDR5_MA[7] | DC60 | SSTL | O |
| DDR5_MA[8] | DD59 | SSTL | O |
| DDR5_MA[9] | DA58 | SSTL | O |
| DDR5_ODT[0] | DG50 | SSTL | O |
| DDR5_ODT[1] | DG48 | SSTL | O |
| DDR5_ODT[2] | DK49 | SSTL | O |
| DDR5_ODT[3] | DF47 | SSTL | O |
| DDR5_PAR | DK53 | SSTL | O |
| DEBUG_EN_N | AV21 | CMOS | I/O |
| DMI_RX_DN[0] | CK9 | PCIEX | I |
| DMI_RX_DN[1] | CM11 | PCIEX | I |
| DMI_RX_DN[2] | CR12 | PCIEX | I |
| DMI_RX_DN[3] | CT11 | PCIEX | I |
| DMI_RX_DP[0] | CL10 | PCIEX | I |



Table A-1. Pin List By Name (Sheet 27 of 90)

| Pin Name | Location | Type | I/O |
|------------------|----------|--------|-----|
| DMI_RX_DP[1] | CN10 | PCIEX | I |
| DMI_RX_DP[2] | CP11 | PCIEX | I |
| DMI_RX_DP[3] | CV11 | PCIEX | I |
| DMI_TX_DN[0] | CG4 | PCIEX | O |
| DMI_TX_DN[1] | CJ4 | PCIEX | O |
| DMI_TX_DN[2] | CN4 | PCIEX | O |
| DMI_TX_DN[3] | CP5 | PCIEX | O |
| DMI_TX_DP[0] | CH5 | PCIEX | O |
| DMI_TX_DP[1] | CL4 | PCIEX | O |
| DMI_TX_DP[2] | CM3 | PCIEX | O |
| DMI_TX_DP[3] | CR4 | PCIEX | O |
| DMIMODE_OVERRIDE | AW12 | CMOS | I/O |
| EAR_N | AJ14 | CMOS | I |
| ERROR_N[0] | AJ12 | OD | O |
| ERROR_N[1] | AK11 | OD | O |
| ERROR_N[2] | AL12 | OD | O |
| FIVR_FAULT | AU14 | CMOS | O |
| FRMAGENT | AV17 | CMOS | I |
| LEGACY_SKT | AE20 | CMOS | I |
| MCP01_RBIAS | CT31 | | |
| MCP01_RBIAS | CU32 | | |
| MEM_HOT_C012_N | AH13 | ODCMOS | I/O |
| MEM_HOT_C345_N | AF13 | ODCMOS | I/O |
| MSMI_N | AN20 | CMOS | I/O |
| NMI | AP11 | CMOS | I |
| PE_HP_SCL | AM19 | ODCMOS | I/O |
| PE_HP_SDA | AL18 | ODCMOS | I/O |
| PE012_RBIAS | CL30 | | |
| PE012_RBIAS | CN30 | | |
| PE1_RX_DN[0] | CW8 | PCIEX3 | I |
| PE1_RX_DN[1] | DA8 | PCIEX3 | I |
| PE1_RX_DN[10] | DT11 | PCIEX3 | I |
| PE1_RX_DN[11] | DT13 | PCIEX3 | I |
| PE1_RX_DN[12] | DV13 | PCIEX3 | I |
| PE1_RX_DN[13] | DW14 | PCIEX3 | I |
| PE1_RX_DN[14] | DY15 | PCIEX3 | I |
| PE1_RX_DN[15] | DU16 | PCIEX3 | I |
| PE1_RX_DN[2] | DC8 | PCIEX3 | I |
| PE1_RX_DN[3] | DC10 | PCIEX3 | I |
| PE1_RX_DN[4] | DE10 | PCIEX3 | I |
| PE1_RX_DN[5] | DH9 | PCIEX3 | I |

Table A-1. Pin List By Name (Sheet 28 of 90)

| Pin Name | Location | Type | I/O |
|---------------|----------|--------|-----|
| PE1_RX_DN[6] | DK9 | PCIEX3 | I |
| PE1_RX_DN[7] | DM9 | PCIEX3 | I |
| PE1_RX_DN[8] | DM11 | PCIEX3 | I |
| PE1_RX_DN[9] | DP11 | PCIEX3 | I |
| PE1_RX_DP[0] | CU8 | PCIEX3 | I |
| PE1_RX_DP[1] | CY7 | PCIEX3 | I |
| PE1_RX_DP[10] | DR12 | PCIEX3 | I |
| PE1_RX_DP[11] | DP13 | PCIEX3 | I |
| PE1_RX_DP[12] | DU12 | PCIEX3 | I |
| PE1_RX_DP[13] | DY13 | PCIEX3 | I |
| PE1_RX_DP[14] | DV15 | PCIEX3 | I |
| PE1_RX_DP[15] | DT15 | PCIEX3 | I |
| PE1_RX_DP[2] | DB9 | PCIEX3 | I |
| PE1_RX_DP[3] | DA10 | PCIEX3 | I |
| PE1_RX_DP[4] | DD9 | PCIEX3 | I |
| PE1_RX_DP[5] | DF9 | PCIEX3 | I |
| PE1_RX_DP[6] | DJ8 | PCIEX3 | I |
| PE1_RX_DP[7] | DL10 | PCIEX3 | I |
| PE1_RX_DP[8] | DK11 | PCIEX3 | I |
| PE1_RX_DP[9] | DN10 | PCIEX3 | I |
| PE1_TX_DN[0] | DA2 | PCIEX3 | O |
| PE1_TX_DN[1] | DC2 | PCIEX3 | O |
| PE1_TX_DN[10] | DW4 | PCIEX3 | O |
| PE1_TX_DN[11] | DU6 | PCIEX3 | O |
| PE1_TX_DN[12] | DV7 | PCIEX3 | O |
| PE1_TX_DN[13] | DY7 | PCIEX3 | O |
| PE1_TX_DN[14] | EA8 | PCIEX3 | O |
| PE1_TX_DN[15] | ED9 | PCIEX3 | O |
| PE1_TX_DN[2] | DE2 | PCIEX3 | O |
| PE1_TX_DN[3] | DE4 | PCIEX3 | O |
| PE1_TX_DN[4] | DG4 | PCIEX3 | O |
| PE1_TX_DN[5] | DK3 | PCIEX3 | O |
| PE1_TX_DN[6] | DM3 | PCIEX3 | O |
| PE1_TX_DN[7] | DN4 | PCIEX3 | O |
| PE1_TX_DN[8] | DT5 | PCIEX3 | O |
| PE1_TX_DN[9] | DV3 | PCIEX3 | O |
| PE1_TX_DP[0] | CW2 | PCIEX3 | O |
| PE1_TX_DP[1] | DB1 | PCIEX3 | O |
| PE1_TX_DP[10] | DU4 | PCIEX3 | O |
| PE1_TX_DP[11] | DV5 | PCIEX3 | O |
| PE1_TX_DP[12] | DT7 | PCIEX3 | O |



Table A-1. Pin List By Name (Sheet 29 of 90)

| Pin Name | Location | Type | I/O |
|---------------|----------|--------|-----|
| PE1_TX_DP[13] | DW6 | PCIEX3 | O |
| PE1_TX_DP[14] | EB7 | PCIEX3 | O |
| PE1_TX_DP[15] | EC8 | PCIEX3 | O |
| PE1_TX_DP[2] | DD3 | PCIEX3 | O |
| PE1_TX_DP[3] | DC4 | PCIEX3 | O |
| PE1_TX_DP[4] | DF3 | PCIEX3 | O |
| PE1_TX_DP[5] | DH3 | PCIEX3 | O |
| PE1_TX_DP[6] | DL2 | PCIEX3 | O |
| PE1_TX_DP[7] | DP3 | PCIEX3 | O |
| PE1_TX_DP[8] | DR4 | PCIEX3 | O |
| PE1_TX_DP[9] | DU2 | PCIEX3 | O |
| PE2_RX_DN[0] | CT9 | PCIEX3 | I |
| PE2_RX_DN[1] | CP9 | PCIEX3 | I |
| PE2_RX_DN[10] | BV7 | PCIEX3 | I |
| PE2_RX_DN[11] | BT7 | PCIEX3 | I |
| PE2_RX_DN[12] | BR8 | PCIEX3 | I |
| PE2_RX_DN[13] | BN8 | PCIEX3 | I |
| PE2_RX_DN[14] | BL8 | PCIEX3 | I |
| PE2_RX_DN[15] | BK9 | PCIEX3 | I |
| PE2_RX_DN[2] | CP7 | PCIEX3 | I |
| PE2_RX_DN[3] | CM7 | PCIEX3 | I |
| PE2_RX_DN[4] | CK7 | PCIEX3 | I |
| PE2_RX_DN[5] | CG8 | PCIEX3 | I |
| PE2_RX_DN[6] | CE6 | PCIEX3 | I |
| PE2_RX_DN[7] | CE8 | PCIEX3 | I |
| PE2_RX_DN[8] | BY9 | PCIEX3 | I |
| PE2_RX_DN[9] | BY7 | PCIEX3 | I |
| PE2_RX_DP[0] | CR8 | PCIEX3 | I |
| PE2_RX_DP[1] | CM9 | PCIEX3 | I |
| PE2_RX_DP[10] | BU6 | PCIEX3 | I |
| PE2_RX_DP[11] | BP7 | PCIEX3 | I |
| PE2_RX_DP[12] | BP9 | PCIEX3 | I |
| PE2_RX_DP[13] | BM7 | PCIEX3 | I |
| PE2_RX_DP[14] | BJ8 | PCIEX3 | I |
| PE2_RX_DP[15] | BJ10 | PCIEX3 | I |
| PE2_RX_DP[2] | CN8 | PCIEX3 | I |
| PE2_RX_DP[3] | CL6 | PCIEX3 | I |
| PE2_RX_DP[4] | CH7 | PCIEX3 | I |
| PE2_RX_DP[5] | CF7 | PCIEX3 | I |
| PE2_RX_DP[6] | CD7 | PCIEX3 | I |
| PE2_RX_DP[7] | CC8 | PCIEX3 | I |

Table A-1. Pin List By Name (Sheet 30 of 90)

| Pin Name | Location | Type | I/O |
|---------------|----------|--------|-----|
| PE2_RX_DP[8] | BV9 | PCIEX3 | I |
| PE2_RX_DP[9] | BW8 | PCIEX3 | I |
| PE2_TX_DN[0] | CY3 | PCIEX3 | O |
| PE2_TX_DN[1] | CV3 | PCIEX3 | O |
| PE2_TX_DN[10] | CA4 | PCIEX3 | O |
| PE2_TX_DN[11] | BW4 | PCIEX3 | O |
| PE2_TX_DN[12] | BU4 | PCIEX3 | O |
| PE2_TX_DN[13] | BP5 | PCIEX3 | O |
| PE2_TX_DN[14] | BL4 | PCIEX3 | O |
| PE2_TX_DN[15] | BM5 | PCIEX3 | O |
| PE2_TX_DN[2] | CT1 | PCIEX3 | O |
| PE2_TX_DN[3] | CT3 | PCIEX3 | O |
| PE2_TX_DN[4] | CM1 | PCIEX3 | O |
| PE2_TX_DN[5] | CL2 | PCIEX3 | O |
| PE2_TX_DN[6] | CG2 | PCIEX3 | O |
| PE2_TX_DN[7] | CF3 | PCIEX3 | O |
| PE2_TX_DN[8] | CC2 | PCIEX3 | O |
| PE2_TX_DN[9] | CB3 | PCIEX3 | O |
| PE2_TX_DP[0] | CW4 | PCIEX3 | O |
| PE2_TX_DP[1] | CU2 | PCIEX3 | O |
| PE2_TX_DP[10] | BY5 | PCIEX3 | O |
| PE2_TX_DP[11] | BV3 | PCIEX3 | O |
| PE2_TX_DP[12] | BR4 | PCIEX3 | O |
| PE2_TX_DP[13] | BN4 | PCIEX3 | O |
| PE2_TX_DP[14] | BM3 | PCIEX3 | O |
| PE2_TX_DP[15] | BK5 | PCIEX3 | O |
| PE2_TX_DP[2] | CR2 | PCIEX3 | O |
| PE2_TX_DP[3] | CP3 | PCIEX3 | O |
| PE2_TX_DP[4] | CK1 | PCIEX3 | O |
| PE2_TX_DP[5] | CK3 | PCIEX3 | O |
| PE2_TX_DP[6] | CE2 | PCIEX3 | O |
| PE2_TX_DP[7] | CE4 | PCIEX3 | O |
| PE2_TX_DP[8] | CD3 | PCIEX3 | O |
| PE2_TX_DP[9] | BY3 | PCIEX3 | O |
| PE3_RBIAS | CP29 | PCIEX3 | I |
| PE3_RBIAS | CR30 | PCIEX3 | I |
| PE3_RX_DN[0] | EA18 | PCIEX3 | I |
| PE3_RX_DN[1] | DW18 | PCIEX3 | I |
| PE3_RX_DN[10] | DG12 | PCIEX3 | I |
| PE3_RX_DN[11] | DG10 | PCIEX3 | I |
| PE3_RX_DN[12] | DD13 | PCIEX3 | I |



Table A-1. Pin List By Name (Sheet 31 of 90)

| Pin Name | Location | Type | I/O |
|---------------|----------|--------|-----|
| PE3_RX_DN[13] | DB11 | PCIEX3 | I |
| PE3_RX_DN[14] | CY11 | PCIEX3 | I |
| PE3_RX_DN[15] | CV9 | PCIEX3 | I |
| PE3_RX_DN[2] | DW16 | PCIEX3 | I |
| PE3_RX_DN[3] | DT19 | PCIEX3 | I |
| PE3_RX_DN[4] | DR16 | PCIEX3 | I |
| PE3_RX_DN[5] | DR14 | PCIEX3 | I |
| PE3_RX_DN[6] | DN14 | PCIEX3 | I |
| PE3_RX_DN[7] | DL14 | PCIEX3 | I |
| PE3_RX_DN[8] | DL12 | PCIEX3 | I |
| PE3_RX_DN[9] | DJ12 | PCIEX3 | I |
| PE3_RX_DP[0] | DY17 | PCIEX3 | I |
| PE3_RX_DP[1] | DU18 | PCIEX3 | I |
| PE3_RX_DP[10] | DE12 | PCIEX3 | I |
| PE3_RX_DP[11] | DF11 | PCIEX3 | I |
| PE3_RX_DP[12] | DC12 | PCIEX3 | I |
| PE3_RX_DP[13] | DA12 | PCIEX3 | I |
| PE3_RX_DP[14] | CW10 | PCIEX3 | I |
| PE3_RX_DP[15] | CU10 | PCIEX3 | I |
| PE3_RX_DP[2] | DV17 | PCIEX3 | I |
| PE3_RX_DP[3] | DR18 | PCIEX3 | I |
| PE3_RX_DP[4] | DN16 | PCIEX3 | I |
| PE3_RX_DP[5] | DP15 | PCIEX3 | I |
| PE3_RX_DP[6] | DM13 | PCIEX3 | I |
| PE3_RX_DP[7] | DJ14 | PCIEX3 | I |
| PE3_RX_DP[8] | DK13 | PCIEX3 | I |
| PE3_RX_DP[9] | DH11 | PCIEX3 | I |
| PE3_TX_DN[0] | EE14 | PCIEX3 | O |
| PE3_TX_DN[1] | EE12 | PCIEX3 | O |
| PE3_TX_DN[10] | DL6 | PCIEX3 | O |
| PE3_TX_DN[11] | DJ4 | PCIEX3 | O |
| PE3_TX_DN[12] | DJ6 | PCIEX3 | O |
| PE3_TX_DN[13] | DD5 | PCIEX3 | O |
| PE3_TX_DN[14] | DB5 | PCIEX3 | O |
| PE3_TX_DN[15] | CY5 | PCIEX3 | O |
| PE3_TX_DN[2] | EC12 | PCIEX3 | O |
| PE3_TX_DN[3] | DY11 | PCIEX3 | O |
| PE3_TX_DN[4] | EB9 | PCIEX3 | O |
| PE3_TX_DN[5] | DW10 | PCIEX3 | O |
| PE3_TX_DN[6] | DU8 | PCIEX3 | O |
| PE3_TX_DN[7] | DR8 | PCIEX3 | O |

Table A-1. Pin List By Name (Sheet 32 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|--------|-----|
| PE3_TX_DN[8] | DM7 | PCIEX3 | O |
| PE3_TX_DN[9] | DP5 | PCIEX3 | O |
| PE3_TX_DP[0] | EC14 | PCIEX3 | O |
| PE3_TX_DP[1] | ED13 | PCIEX3 | O |
| PE3_TX_DP[10] | DK5 | PCIEX3 | O |
| PE3_TX_DP[11] | DH5 | PCIEX3 | O |
| PE3_TX_DP[12] | DG6 | PCIEX3 | O |
| PE3_TX_DP[13] | DC6 | PCIEX3 | O |
| PE3_TX_DP[14] | DA4 | PCIEX3 | O |
| PE3_TX_DP[15] | CV5 | PCIEX3 | O |
| PE3_TX_DP[2] | EB11 | PCIEX3 | O |
| PE3_TX_DP[3] | EA10 | PCIEX3 | O |
| PE3_TX_DP[4] | DY9 | PCIEX3 | O |
| PE3_TX_DP[5] | DV9 | PCIEX3 | O |
| PE3_TX_DP[6] | DT9 | PCIEX3 | O |
| PE3_TX_DP[7] | DP7 | PCIEX3 | O |
| PE3_TX_DP[8] | DN6 | PCIEX3 | O |
| PE3_TX_DP[9] | DM5 | PCIEX3 | O |
| PECI | AU12 | PECI | I/O |
| PIROM_ADDR[0] | CU58 | | I/O |
| PIROM_ADDR[1] | CV57 | | I/O |
| PIROM_ADDR[2] | CW56 | | I/O |
| PKGID[0] | DC72 | | |
| PKGID[1] | CW72 | | |
| PKGID[2] | DA72 | | |
| PM_FAST_WAKE_N | AF15 | ODCMOS | I/O |
| PMSYNC | AR14 | CMOS | I |
| PMSYNC_CLK | AT19 | CMOS | I |
| PRDY_N | AG16 | OD | O |
| PREQ_N | AR12 | GTL | I |
| PROC_ID[0] | CY71 | N/A | O |
| PROC_ID[1] | DB71 | N/A | O |
| PROCDIS_N | AB17 | CMOS | I |
| PROCHOT_N | AC16 | ODCMOS | I/O |
| PWR_DEBUG_N | AP17 | CMOS | I |
| PWRGOOD | BC24 | CMOS | I |
| RC_ENET_CLK_DN | AL26 | | |
| RC_ENET_CLK_DP | AK27 | | |
| RC_ERROR_N | Y23 | | |
| RC_GPIO[0] | AE48 | | I/O |
| RC_GPIO[1] | AG56 | | I/O |



Table A-1. Pin List By Name (Sheet 33 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| RC_GPIO[10] | AF53 | | I/O |
| RC_GPIO[11] | AE50 | | I/O |
| RC_GPIO[12] | AG48 | | I/O |
| RC_GPIO[13] | AG54 | | I/O |
| RC_GPIO[14] | AD49 | | I/O |
| RC_GPIO[15] | AE52 | | I/O |
| RC_GPIO[2] | AH55 | | |
| RC_GPIO[3] | AG50 | | I/O |
| RC_GPIO[4] | AD51 | | I/O |
| RC_GPIO[5] | AG52 | | I/O |
| RC_GPIO[6] | AK57 | | |
| RC_GPIO[7] | AJ56 | | |
| RC_GPIO[8] | AF51 | | I/O |
| RC_GPIO[9] | AF49 | | I/O |
| RC_REFCLK[0]_DN | AP27 | | |
| RC_REFCLK[0]_DP | AM27 | | |
| RC_REFCLK[1]_DN | BB25 | | |
| RC_REFCLK[1]_DP | BD25 | | |
| RC_VCC_CORE | AM21 | PWR | |
| RC_VCC_CORE | AM25 | PWR | |
| RC_VCC_CORE | AN18 | PWR | |
| RC_VCC_CORE | AN22 | PWR | |
| RC_VCC_CORE | AN24 | PWR | |
| RC_VCC_CORE | AN26 | PWR | |
| RC_VCC_CORE | AP23 | PWR | |
| RC_VCC_CORE | AP25 | PWR | |
| RC_VCC_CORE | AR20 | PWR | |
| RC_VCC_CORE | AR22 | PWR | |
| RC_VCC_CORE | AR26 | PWR | |
| RC_VCC_CORE | AT23 | PWR | |
| RC_VCC_CORE | AT25 | PWR | |
| RC_VCC_CORE | BH19 | PWR | |
| RC_VCC_CORE | BJ16 | PWR | |
| RC_VCC_CORE | BJ18 | PWR | |
| RC_VCC_CORE | BJ20 | PWR | |
| RC_VCC_CORE | BK17 | PWR | |
| RC_VCC_CORE | BL20 | PWR | |
| RC_VCC_CORE | BM19 | PWR | |
| RC_VCC_CORE | BP21 | PWR | |
| RC_VCC_CORE | BR22 | PWR | |
| RC_VCC_CORE | BR24 | PWR | |

Table A-1. Pin List By Name (Sheet 34 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| RC_VCC_CORE | BU20 | PWR | |
| RC_VCC_CORE | BU22 | PWR | |
| RC_VCC_CORE | BV19 | PWR | |
| RC_VCC_CORE | BV21 | PWR | |
| RC_VCC_CORE | BW20 | PWR | |
| RC_VCC_CORE | BY19 | PWR | |
| RC_VCC_CORE | CA22 | PWR | |
| RC_VCC_CORE | CB19 | PWR | |
| RC_VCC_CORE | CB21 | PWR | |
| RC_VCC_CORE | CC20 | PWR | |
| RC_VCC_CORE | CD19 | PWR | |
| RC_VCC_CORE | CD21 | PWR | |
| RC_VCC_CORE | CE22 | PWR | |
| RC_VCC_CORE | CF19 | PWR | |
| RC_VCC_CORE | CF21 | PWR | |
| RC_VCC_CORE | CF23 | PWR | |
| RC_VCC_CORE | CG20 | PWR | |
| RC_VCC_CORE | CG26 | PWR | |
| RC_VCC_CORE | CH21 | PWR | |
| RC_VCC_CORE | CH23 | PWR | |
| RC_VCC_CORE | CJ20 | PWR | |
| RC_VCC_CORE | CJ22 | PWR | |
| RC_VCC_CORE | CJ24 | PWR | |
| RC_VCC_CORE | CJ26 | PWR | |
| RC_VCC_CORE | CK23 | PWR | |
| RC_VCC_CORE | CK25 | PWR | |
| RC_VCC_CORE | CL24 | PWR | |
| RC_VCC_CORE | CL26 | PWR | |
| RC_VCC_CORE | CM23 | PWR | |
| RC_VCC_CORE | CM25 | PWR | |
| RC_VCC_CORE | CN24 | PWR | |
| RC_VCC_CORE | CP23 | PWR | |
| RC_VCC_CORE | CT23 | PWR | |
| RC_VCC_CORE | CU24 | PWR | |
| RC_VCC_CORE | CV23 | PWR | |
| RC_VCC_CORE | CW24 | PWR | |
| RC_VCC_CORE | CY25 | PWR | |
| RC_VCC_CORE | DA24 | PWR | |
| RC_VCCALG_R | BL18 | PWR | |
| RC_VCCALG_R | BM17 | PWR | |
| RC_VCCALG_R | BN18 | PWR | |



Table A-1. Pin List By Name (Sheet 35 of 90)

| Pin Name | Location | Type | I/O |
|----------------------|----------|------|-----|
| RC_VCCALG_R | BP17 | PWR | |
| RC_VCCALG_R | BU18 | PWR | |
| RC_VCCH | A14 | PWR | |
| RC_VCCH | A16 | PWR | |
| RC_VCCH | B13 | PWR | |
| RC_VCCH | B15 | PWR | |
| RC_VCCH | B17 | PWR | |
| RC_VCCH_SENSE_DP | AK21 | | |
| RC_VSS_VCCH_SENSE_DN | AL20 | | |
| RESET_N | AP21 | CMOS | I |
| RFID_VCC | A8 | PWR | |
| RSVD | A24 | | |
| RSVD | A6 | | |
| RSVD | AD47 | | |
| RSVD | AE46 | | |
| RSVD | AE72 | | |
| RSVD | AF19 | | |
| RSVD | AF47 | | |
| RSVD | AF71 | | |
| RSVD | AG20 | | |
| RSVD | AG72 | | |
| RSVD | AH15 | | |
| RSVD | AH19 | | |
| RSVD | AH57 | | |
| RSVD | AH71 | | |
| RSVD | AH73 | | |
| RSVD | AJ20 | | |
| RSVD | AJ58 | | |
| RSVD | AJ60 | | |
| RSVD | AJ62 | | |
| RSVD | AJ70 | | |
| RSVD | AK59 | | |
| RSVD | AK61 | | |
| RSVD | AK69 | | |
| RSVD | AL22 | | |
| RSVD | AL58 | | |
| RSVD | AL60 | | |
| RSVD | AL62 | | |
| RSVD | AM23 | | |
| RSVD | AM59 | | |
| RSVD | AM61 | | |

Table A-1. Pin List By Name (Sheet 36 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| RSVD | AN60 | | |
| RSVD | AN62 | | |
| RSVD | AP61 | | |
| RSVD | AR62 | | |
| RSVD | AT13 | | |
| RSVD | AV77 | | |
| RSVD | AW64 | | |
| RSVD | AW76 | | |
| RSVD | AY65 | | |
| RSVD | AY67 | | |
| RSVD | AY75 | | |
| RSVD | AY77 | | |
| RSVD | AY83 | | |
| RSVD | B7 | | |
| RSVD | B77 | | |
| RSVD | B81 | | |
| RSVD | BA14 | | |
| RSVD | BA16 | | |
| RSVD | BA18 | | |
| RSVD | BA22 | | |
| RSVD | BA64 | | |
| RSVD | BA66 | | |
| RSVD | BA76 | | |
| RSVD | BA78 | | |
| RSVD | BA82 | | |
| RSVD | BB13 | | |
| RSVD | BB15 | | |
| RSVD | BB17 | | |
| RSVD | BB21 | | |
| RSVD | BB65 | | |
| RSVD | BB67 | | |
| RSVD | BC14 | | |
| RSVD | BC18 | | |
| RSVD | BC20 | | |
| RSVD | BC22 | | |
| RSVD | BC64 | | |
| RSVD | BC66 | | |
| RSVD | BC68 | | |
| RSVD | BD17 | | |
| RSVD | BD19 | | |
| RSVD | BD65 | | |



Table A-1. Pin List By Name (Sheet 37 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| RSVD | BD67 | | |
| RSVD | BD69 | | |
| RSVD | BE18 | | |
| RSVD | BE20 | | |
| RSVD | BE22 | | |
| RSVD | BF21 | | |
| RSVD | BG18 | | |
| RSVD | BG20 | | |
| RSVD | BV23 | | |
| RSVD | BW10 | | |
| RSVD | BW22 | | |
| RSVD | BY25 | | |
| RSVD | C18 | | |
| RSVD | C24 | | |
| RSVD | C6 | | |
| RSVD | C82 | | |
| RSVD | CA24 | | |
| RSVD | CB25 | | |
| RSVD | CB5 | | |
| RSVD | CC6 | | |
| RSVD | CD25 | | |
| RSVD | CE78 | | |
| RSVD | CE80 | | |
| RSVD | CF79 | | |
| RSVD | CF81 | | |
| RSVD | CG10 | | |
| RSVD | CG24 | RSVD | |
| RSVD | CG78 | | |
| RSVD | CG82 | | |
| RSVD | CH25 | | |
| RSVD | CH77 | | |
| RSVD | CK19 | | |
| RSVD | CK77 | | |
| RSVD | CN22 | | |
| RSVD | CN28 | | |
| RSVD | CP31 | | |
| RSVD | CR60 | | |
| RSVD | CT5 | | |
| RSVD | CT69 | | |
| RSVD | CU6 | | |
| RSVD | CU60 | | |

Table A-1. Pin List By Name (Sheet 38 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| RSVD | CV69 | | |
| RSVD | CW22 | | |
| RSVD | CW60 | | |
| RSVD | CW62 | | |
| RSVD | CY23 | | |
| RSVD | CY39 | | |
| RSVD | CY53 | | |
| RSVD | CY57 | | |
| RSVD | CY63 | | |
| RSVD | CY73 | | |
| RSVD | D17 | | |
| RSVD | D5 | | |
| RSVD | D65 | | |
| RSVD | D83 | | |
| RSVD | DA40 | | |
| RSVD | DA52 | | |
| RSVD | DA54 | | |
| RSVD | DA56 | | |
| RSVD | DC46 | | |
| RSVD | DC52 | | |
| RSVD | DD51 | | |
| RSVD | DG36 | | |
| RSVD | DG64 | | |
| RSVD | DH65 | | |
| RSVD | DJ36 | | |
| RSVD | DJ66 | | |
| RSVD | DK15 | | |
| RSVD | DK37 | | |
| RSVD | DK65 | | |
| RSVD | DK67 | | |
| RSVD | DL38 | | |
| RSVD | DL66 | | |
| RSVD | DM67 | | |
| RSVD | DN62 | | |
| RSVD | DN66 | | |
| RSVD | DP17 | | |
| RSVD | DP65 | | |
| RSVD | DR44 | | |
| RSVD | DT71 | | |
| RSVD | DU44 | | |
| RSVD | DV61 | | |



Table A-1. Pin List By Name (Sheet 39 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| RSVD | DV71 | | |
| RSVD | DW44 | | |
| RSVD | DW46 | | |
| RSVD | DY3 | | |
| RSVD | E2 | | |
| RSVD | E24 | | |
| RSVD | E4 | | |
| RSVD | E84 | | |
| RSVD | EA4 | | |
| RSVD | EA44 | | |
| RSVD | EB3 | | |
| RSVD | EB5 | | |
| RSVD | EB85 | | |
| RSVD | EC16 | | |
| RSVD | EC4 | | |
| RSVD | EC44 | | |
| RSVD | EC84 | | |
| RSVD | ED45 | | |
| RSVD | ED5 | | |
| RSVD | ED83 | | |
| RSVD | EE16 | | |
| RSVD | EE46 | | |
| RSVD | EE6 | | |
| RSVD | EE82 | | |
| RSVD | EE84 | | |
| RSVD | EF47 | | |
| RSVD | EF77 | | |
| RSVD | EF81 | | |
| RSVD | EF83 | | |
| RSVD | F23 | | |
| RSVD | F3 | | |
| RSVD | F65 | | |
| RSVD | F83 | | |
| RSVD | G2 | | |
| RSVD | G64 | | |
| RSVD | G84 | | |
| RSVD | H1 | | |
| RSVD | H83 | | |
| RSVD | H85 | | |
| RSVD | J46 | | |
| RSVD | J62 | | |

Table A-1. Pin List By Name (Sheet 40 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|--------|-----|
| RSVD | K61 | | |
| RSVD | M63 | | |
| RSVD | P65 | | |
| RSVD | R62 | | |
| RSVD | R66 | | |
| RSVD | T67 | | |
| RSVD | U66 | | |
| RSVD | V65 | | |
| RSVD | V67 | | |
| RSVD | W66 | | |
| RSVD | Y65 | | |
| SAFE_MODE_BOOT | AR18 | CMOS | I |
| SKTOCC_N | AB13 | NA | O |
| SM_WP | CV59 | PIROM | I |
| SMBCLK | CT59 | PIROM | I/O |
| SMBDAT | CW58 | PIROM | I/O |
| SOCKET_ID[0] | AU22 | CMOS | I |
| SOCKET_ID[1] | AU16 | CMOS | I |
| SOCKET_ID2 | AU20 | CMOS | I |
| SVIDALERT_N[0] | DE44 | CMOS | I |
| SVIDALERT_N[1] | DL44 | CMOS | I |
| SVIDCLK[0] | DC44 | OD | O |
| SVIDCLK[1] | DG44 | OD | O |
| SVIDDATA[0] | DB45 | ODCMOS | I/O |
| SVIDDATA[1] | DJ44 | ODCMOS | I/O |
| TCK | AA14 | CMOS | I |
| TDI | AC14 | GTL | I |
| TDO | AE14 | OD | O |
| TEST_1 | AF45 | | |
| TEST_10 | AW22 | | |
| TEST_11 | AY13 | | |
| TEST_12 | AY19 | | |
| TEST_13 | DB51 | | |
| TEST_14 | DC50 | | |
| TEST_15 | AW14 | | |
| TEST_16 | B3 | | |
| TEST_17 | A4 | | |
| TEST_2 | AG46 | | |
| TEST_3 | AM13 | | |
| TEST_4 | AN12 | | |
| TEST_5 | AN14 | | |



Table A-1. Pin List By Name (Sheet 41 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|--------|-----|
| TEST_6 | AR16 | | |
| TEST_7 | AU18 | | |
| TEST_8 | AW16 | | |
| TEST_9 | AW20 | | |
| THERMTRIP_N | AB15 | OD | O |
| TMS | W14 | GTL | I |
| TRST_N | Y13 | GTL | I |
| TSC_SYNC | AM11 | ODCMOS | I/O |
| TXT_AGENT | AW18 | CMOS | I |
| TXT_PLTEN | AV15 | CMOS | I |
| UPI0_RX_DN[0] | AC10 | UPI | I |
| UPI0_RX_DN[1] | AA8 | UPI | I |
| UPI0_RX_DN[10] | AP7 | UPI | I |
| UPI0_RX_DN[11] | AR8 | UPI | I |
| UPI0_RX_DN[12] | AU10 | UPI | I |
| UPI0_RX_DN[13] | BA8 | UPI | I |
| UPI0_RX_DN[14] | BC6 | UPI | I |
| UPI0_RX_DN[15] | BD7 | UPI | I |
| UPI0_RX_DN[16] | AW8 | UPI | I |
| UPI0_RX_DN[17] | AY9 | UPI | I |
| UPI0_RX_DN[18] | BD9 | UPI | I |
| UPI0_RX_DN[19] | BB11 | UPI | I |
| UPI0_RX_DN[2] | AB7 | UPI | I |
| UPI0_RX_DN[3] | AD5 | UPI | I |
| UPI0_RX_DN[4] | AE6 | UPI | I |
| UPI0_RX_DN[5] | AG8 | UPI | I |
| UPI0_RX_DN[6] | AJ6 | UPI | I |
| UPI0_RX_DN[7] | AL6 | UPI | I |
| UPI0_RX_DN[8] | AK7 | UPI | I |
| UPI0_RX_DN[9] | AM9 | UPI | I |
| UPI0_RX_DP[0] | AB9 | UPI | I |
| UPI0_RX_DP[1] | AC8 | UPI | I |
| UPI0_RX_DP[10] | AN8 | UPI | I |
| UPI0_RX_DP[11] | AU8 | UPI | I |
| UPI0_RX_DP[12] | AT9 | UPI | I |
| UPI0_RX_DP[13] | AY7 | UPI | I |
| UPI0_RX_DP[14] | BB7 | UPI | I |
| UPI0_RX_DP[15] | BF7 | UPI | I |
| UPI0_RX_DP[16] | AV9 | UPI | I |
| UPI0_RX_DP[17] | BB9 | UPI | I |
| UPI0_RX_DP[18] | BC10 | UPI | I |

Table A-1. Pin List By Name (Sheet 42 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|------|-----|
| UPI0_RX_DP[19] | BA10 | UPI | I |
| UPI0_RX_DP[2] | AA6 | UPI | I |
| UPI0_RX_DP[3] | AC6 | UPI | I |
| UPI0_RX_DP[4] | AG6 | UPI | I |
| UPI0_RX_DP[5] | AF7 | UPI | I |
| UPI0_RX_DP[6] | AH7 | UPI | I |
| UPI0_RX_DP[7] | AK5 | UPI | I |
| UPI0_RX_DP[8] | AM7 | UPI | I |
| UPI0_RX_DP[9] | AL8 | UPI | I |
| UPI0_TX_DN[0] | N2 | UPI | I |
| UPI0_TX_DN[1] | P1 | UPI | I |
| UPI0_TX_DN[10] | AM3 | UPI | I |
| UPI0_TX_DN[11] | AN4 | UPI | I |
| UPI0_TX_DN[12] | AT1 | UPI | I |
| UPI0_TX_DN[13] | AT3 | UPI | I |
| UPI0_TX_DN[14] | AU4 | UPI | I |
| UPI0_TX_DN[15] | AV5 | UPI | I |
| UPI0_TX_DN[16] | BA4 | UPI | I |
| UPI0_TX_DN[17] | BB3 | UPI | I |
| UPI0_TX_DN[18] | BF3 | UPI | I |
| UPI0_TX_DN[19] | BG4 | UPI | I |
| UPI0_TX_DN[2] | V3 | UPI | I |
| UPI0_TX_DN[3] | Y1 | UPI | I |
| UPI0_TX_DN[4] | AB3 | UPI | I |
| UPI0_TX_DN[5] | AC2 | UPI | I |
| UPI0_TX_DN[6] | AG4 | UPI | I |
| UPI0_TX_DN[7] | AE2 | UPI | I |
| UPI0_TX_DN[8] | AH3 | UPI | I |
| UPI0_TX_DN[9] | AL2 | UPI | I |
| UPI0_TX_DP[0] | M1 | UPI | I |
| UPI0_TX_DP[1] | T1 | UPI | I |
| UPI0_TX_DP[10] | AK3 | UPI | I |
| UPI0_TX_DP[11] | AP3 | UPI | I |
| UPI0_TX_DP[12] | AP1 | UPI | I |
| UPI0_TX_DP[13] | AR2 | UPI | I |
| UPI0_TX_DP[14] | AR4 | UPI | I |
| UPI0_TX_DP[15] | AW4 | UPI | I |
| UPI0_TX_DP[16] | AY3 | UPI | I |
| UPI0_TX_DP[17] | BC2 | UPI | I |
| UPI0_TX_DP[18] | BD3 | UPI | I |
| UPI0_TX_DP[19] | BH3 | UPI | I |



Table A-1. Pin List By Name (Sheet 43 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|------|-----|
| UPI0_TX_DP[2] | Y3 | UPI | I |
| UPI0_TX_DP[3] | W2 | UPI | I |
| UPI0_TX_DP[4] | AA2 | UPI | I |
| UPI0_TX_DP[5] | AD1 | UPI | I |
| UPI0_TX_DP[6] | AF3 | UPI | I |
| UPI0_TX_DP[7] | AG2 | UPI | I |
| UPI0_TX_DP[8] | AJ2 | UPI | I |
| UPI0_TX_DP[9] | AK1 | UPI | I |
| UPI01_RBIAS | AP29 | UPI | I |
| UPI01_RBIAS | AT29 | UPI | I |
| UPI1_RX_DN[0] | T5 | UPI | I |
| UPI1_RX_DN[1] | P7 | UPI | I |
| UPI1_RX_DN[10] | R16 | UPI | I |
| UPI1_RX_DN[11] | P17 | UPI | I |
| UPI1_RX_DN[12] | U16 | UPI | I |
| UPI1_RX_DN[13] | W18 | UPI | I |
| UPI1_RX_DN[14] | R20 | UPI | I |
| UPI1_RX_DN[15] | U18 | UPI | I |
| UPI1_RX_DN[16] | P21 | UPI | I |
| UPI1_RX_DN[17] | V19 | UPI | I |
| UPI1_RX_DN[18] | Y21 | UPI | I |
| UPI1_RX_DN[19] | AB19 | UPI | I |
| UPI1_RX_DN[2] | V7 | UPI | I |
| UPI1_RX_DN[3] | T9 | UPI | I |
| UPI1_RX_DN[4] | P9 | UPI | I |
| UPI1_RX_DN[5] | R10 | UPI | I |
| UPI1_RX_DN[6] | U12 | UPI | I |
| UPI1_RX_DN[7] | L12 | UPI | I |
| UPI1_RX_DN[8] | N14 | UPI | I |
| UPI1_RX_DN[9] | R12 | UPI | I |
| UPI1_RX_DP[0] | R6 | UPI | I |
| UPI1_RX_DP[1] | T7 | UPI | I |
| UPI1_RX_DP[10] | T15 | UPI | I |
| UPI1_RX_DP[11] | N16 | UPI | I |
| UPI1_RX_DP[12] | W16 | UPI | I |
| UPI1_RX_DP[13] | V17 | UPI | I |
| UPI1_RX_DP[14] | P19 | UPI | I |
| UPI1_RX_DP[15] | T19 | UPI | I |
| UPI1_RX_DP[16] | T21 | UPI | I |
| UPI1_RX_DP[17] | Y19 | UPI | I |
| UPI1_RX_DP[18] | W20 | UPI | I |

Table A-1. Pin List By Name (Sheet 44 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|------|-----|
| UPI1_RX_DP[19] | AA20 | UPI | I |
| UPI1_RX_DP[2] | U8 | UPI | I |
| UPI1_RX_DP[3] | R8 | UPI | I |
| UPI1_RX_DP[4] | N10 | UPI | I |
| UPI1_RX_DP[5] | U10 | UPI | I |
| UPI1_RX_DP[6] | T11 | UPI | I |
| UPI1_RX_DP[7] | N12 | UPI | I |
| UPI1_RX_DP[8] | M13 | UPI | I |
| UPI1_RX_DP[9] | P13 | UPI | I |
| UPI1_TX_DN[0] | M3 | UPI | O |
| UPI1_TX_DN[1] | L4 | UPI | O |
| UPI1_TX_DN[10] | E12 | UPI | O |
| UPI1_TX_DN[11] | G14 | UPI | O |
| UPI1_TX_DN[12] | D15 | UPI | O |
| UPI1_TX_DN[13] | F15 | UPI | O |
| UPI1_TX_DN[14] | H17 | UPI | O |
| UPI1_TX_DN[15] | K19 | UPI | O |
| UPI1_TX_DN[16] | G18 | UPI | O |
| UPI1_TX_DN[17] | J20 | UPI | O |
| UPI1_TX_DN[18] | F21 | UPI | O |
| UPI1_TX_DN[19] | H21 | UPI | O |
| UPI1_TX_DN[2] | K5 | UPI | O |
| UPI1_TX_DN[3] | J6 | UPI | O |
| UPI1_TX_DN[4] | G6 | UPI | O |
| UPI1_TX_DN[5] | H7 | UPI | O |
| UPI1_TX_DN[6] | K9 | UPI | O |
| UPI1_TX_DN[7] | D9 | UPI | O |
| UPI1_TX_DN[8] | F11 | UPI | O |
| UPI1_TX_DN[9] | G10 | UPI | O |
| UPI1_TX_DP[0] | P3 | UPI | O |
| UPI1_TX_DP[1] | K3 | UPI | O |
| UPI1_TX_DP[10] | G12 | UPI | O |
| UPI1_TX_DP[11] | F13 | UPI | O |
| UPI1_TX_DP[12] | E14 | UPI | O |
| UPI1_TX_DP[13] | H15 | UPI | O |
| UPI1_TX_DP[14] | G16 | UPI | O |
| UPI1_TX_DP[15] | L18 | UPI | O |
| UPI1_TX_DP[16] | J18 | UPI | O |
| UPI1_TX_DP[17] | H19 | UPI | O |
| UPI1_TX_DP[18] | G20 | UPI | O |
| UPI1_TX_DP[19] | K21 | UPI | O |



Table A-1. Pin List By Name (Sheet 45 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|------|-----|
| UPI1_TX_DP[2] | M5 | UPI | O |
| UPI1_TX_DP[3] | H5 | UPI | O |
| UPI1_TX_DP[4] | F7 | UPI | O |
| UPI1_TX_DP[5] | K7 | UPI | O |
| UPI1_TX_DP[6] | J8 | UPI | O |
| UPI1_TX_DP[7] | F9 | UPI | O |
| UPI1_TX_DP[8] | E10 | UPI | O |
| UPI1_TX_DP[9] | H9 | UPI | O |
| UPI2_RBIAS | CK29 | | |
| UPI2_RBIAS | CL28 | | |
| UPI2_RX_DN[0] | DF23 | UPI | I |
| UPI2_RX_DN[1] | DE22 | UPI | I |
| UPI2_RX_DN[10] | CN20 | UPI | I |
| UPI2_RX_DN[11] | CP21 | UPI | I |
| UPI2_RX_DN[12] | CL16 | UPI | I |
| UPI2_RX_DN[13] | CJ18 | UPI | I |
| UPI2_RX_DN[14] | CH17 | UPI | I |
| UPI2_RX_DN[15] | CE16 | UPI | I |
| UPI2_RX_DN[16] | CD15 | UPI | I |
| UPI2_RX_DN[17] | CF17 | UPI | I |
| UPI2_RX_DN[18] | CB15 | UPI | I |
| UPI2_RX_DN[19] | BY17 | UPI | I |
| UPI2_RX_DN[2] | DC22 | UPI | I |
| UPI2_RX_DN[3] | DB21 | UPI | I |
| UPI2_RX_DN[4] | DD19 | UPI | I |
| UPI2_RX_DN[5] | DA20 | UPI | I |
| UPI2_RX_DN[6] | CW20 | UPI | I |
| UPI2_RX_DN[7] | CV19 | UPI | I |
| UPI2_RX_DN[8] | CT21 | UPI | I |
| UPI2_RX_DN[9] | CR18 | UPI | I |
| UPI2_RX_DP[0] | DG22 | UPI | I |
| UPI2_RX_DP[1] | DD21 | UPI | I |
| UPI2_RX_DP[10] | CP19 | UPI | I |
| UPI2_RX_DP[11] | CM21 | UPI | I |
| UPI2_RX_DP[12] | CJ16 | UPI | I |
| UPI2_RX_DP[13] | CK17 | UPI | I |
| UPI2_RX_DP[14] | CG16 | UPI | I |
| UPI2_RX_DP[15] | CF15 | UPI | I |
| UPI2_RX_DP[16] | CC14 | UPI | I |
| UPI2_RX_DP[17] | CD17 | UPI | I |
| UPI2_RX_DP[18] | BY15 | UPI | I |

Table A-1. Pin List By Name (Sheet 46 of 90)

| Pin Name | Location | Type | I/O |
|----------------|----------|------|-----|
| UPI2_RX_DP[19] | CA16 | UPI | I |
| UPI2_RX_DP[2] | DA22 | UPI | I |
| UPI2_RX_DP[3] | DC20 | UPI | I |
| UPI2_RX_DP[4] | DB19 | UPI | I |
| UPI2_RX_DP[5] | CY19 | UPI | I |
| UPI2_RX_DP[6] | CU20 | UPI | I |
| UPI2_RX_DP[7] | CW18 | UPI | I |
| UPI2_RX_DP[8] | CR20 | UPI | I |
| UPI2_RX_DP[9] | CN18 | UPI | I |
| UPI2_TX_DN[0] | DT21 | UPI | O |
| UPI2_TX_DN[1] | DM21 | UPI | O |
| UPI2_TX_DN[10] | DA16 | UPI | O |
| UPI2_TX_DN[11] | CW14 | UPI | O |
| UPI2_TX_DN[12] | CU14 | UPI | O |
| UPI2_TX_DN[13] | CM13 | UPI | O |
| UPI2_TX_DN[14] | CJ14 | UPI | O |
| UPI2_TX_DN[15] | CF13 | UPI | O |
| UPI2_TX_DN[16] | CH11 | UPI | O |
| UPI2_TX_DN[17] | CE12 | UPI | O |
| UPI2_TX_DN[18] | CC10 | UPI | O |
| UPI2_TX_DN[19] | CC12 | UPI | O |
| UPI2_TX_DN[2] | DL20 | UPI | O |
| UPI2_TX_DN[3] | DG20 | UPI | O |
| UPI2_TX_DN[4] | DH19 | UPI | O |
| UPI2_TX_DN[5] | DK17 | UPI | O |
| UPI2_TX_DN[6] | DG18 | UPI | O |
| UPI2_TX_DN[7] | DD17 | UPI | O |
| UPI2_TX_DN[8] | DF15 | UPI | O |
| UPI2_TX_DN[9] | DC16 | UPI | O |
| UPI2_TX_DP[0] | DP21 | UPI | O |
| UPI2_TX_DP[1] | DN20 | UPI | O |
| UPI2_TX_DP[10] | CW16 | UPI | O |
| UPI2_TX_DP[11] | CV13 | UPI | O |
| UPI2_TX_DP[12] | CR14 | UPI | O |
| UPI2_TX_DP[13] | CK13 | UPI | O |
| UPI2_TX_DP[14] | CH13 | UPI | O |
| UPI2_TX_DP[15] | CG12 | UPI | O |
| UPI2_TX_DP[16] | CF11 | UPI | O |
| UPI2_TX_DP[17] | CD11 | UPI | O |
| UPI2_TX_DP[18] | CB11 | UPI | O |
| UPI2_TX_DP[19] | CA12 | UPI | O |



Table A-1. Pin List By Name (Sheet 47 of 90)

| Pin Name | Location | Type | I/O |
|---------------|----------|------|-----|
| UPI2_TX_DP[2] | DK19 | UPI | O |
| UPI2_TX_DP[3] | DJ20 | UPI | O |
| UPI2_TX_DP[4] | DJ18 | UPI | O |
| UPI2_TX_DP[5] | DH17 | UPI | O |
| UPI2_TX_DP[6] | DF17 | UPI | O |
| UPI2_TX_DP[7] | DE16 | UPI | O |
| UPI2_TX_DP[8] | DD15 | UPI | O |
| UPI2_TX_DP[9] | DB15 | UPI | O |
| VCC33 | CY55 | PWR | |
| VCCD012 | AD45 | PWR | |
| VCCD012 | AF55 | PWR | |
| VCCD012 | AF57 | PWR | |
| VCCD012 | AF59 | PWR | |
| VCCD012 | AF61 | PWR | |
| VCCD012 | AF63 | PWR | |
| VCCD012 | B47 | PWR | |
| VCCD012 | B49 | PWR | |
| VCCD012 | B53 | PWR | |
| VCCD012 | B59 | PWR | |
| VCCD012 | C46 | PWR | |
| VCCD012 | D45 | PWR | |
| VCCD012 | E46 | PWR | |
| VCCD012 | E48 | PWR | |
| VCCD012 | E50 | PWR | |
| VCCD012 | E52 | PWR | |
| VCCD012 | E54 | PWR | |
| VCCD012 | E56 | PWR | |
| VCCD012 | E58 | PWR | |
| VCCD012 | E60 | PWR | |
| VCCD012 | E62 | PWR | |
| VCCD012 | E64 | PWR | |
| VCCD012 | L46 | PWR | |
| VCCD012 | L48 | PWR | |
| VCCD012 | L50 | PWR | |
| VCCD012 | L52 | PWR | |
| VCCD012 | L54 | PWR | |
| VCCD012 | L56 | PWR | |
| VCCD012 | L58 | PWR | |
| VCCD012 | L60 | PWR | |
| VCCD012 | L62 | PWR | |
| VCCD012 | N64 | PWR | |

Table A-1. Pin List By Name (Sheet 48 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VCCD012 | U46 | PWR | |
| VCCD012 | U48 | PWR | |
| VCCD012 | U50 | PWR | |
| VCCD012 | U52 | PWR | |
| VCCD012 | U54 | PWR | |
| VCCD012 | U56 | PWR | |
| VCCD012 | U58 | PWR | |
| VCCD012 | U60 | PWR | |
| VCCD012 | U62 | PWR | |
| VCCD012 | W64 | PWR | |
| VCCD012 | Y45 | PWR | |
| VCCD012 | Y47 | PWR | |
| VCCD012 | Y49 | PWR | |
| VCCD012 | Y51 | PWR | |
| VCCD012 | Y53 | PWR | |
| VCCD012 | Y55 | PWR | |
| VCCD012 | Y57 | PWR | |
| VCCD012 | Y59 | PWR | |
| VCCD012 | Y61 | PWR | |
| VCCD012 | Y63 | PWR | |
| VCCD345 | DB53 | PWR | |
| VCCD345 | DB55 | PWR | |
| VCCD345 | DB57 | PWR | |
| VCCD345 | DB59 | PWR | |
| VCCD345 | DB61 | PWR | |
| VCCD345 | DB63 | PWR | |
| VCCD345 | DD45 | PWR | |
| VCCD345 | DH45 | PWR | |
| VCCD345 | DH47 | PWR | |
| VCCD345 | DH49 | PWR | |
| VCCD345 | DH51 | PWR | |
| VCCD345 | DH53 | PWR | |
| VCCD345 | DH55 | PWR | |
| VCCD345 | DH57 | PWR | |
| VCCD345 | DH59 | PWR | |
| VCCD345 | DH61 | PWR | |
| VCCD345 | DH63 | PWR | |
| VCCD345 | DJ64 | PWR | |
| VCCD345 | DL46 | PWR | |
| VCCD345 | DL48 | PWR | |
| VCCD345 | DL50 | PWR | |



Table A-1. Pin List By Name (Sheet 49 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VCCD345 | DL52 | PWR | |
| VCCD345 | DL54 | PWR | |
| VCCD345 | DL56 | PWR | |
| VCCD345 | DL58 | PWR | |
| VCCD345 | DL60 | PWR | |
| VCCD345 | DL62 | PWR | |
| VCCD345 | DU46 | PWR | |
| VCCD345 | DU48 | PWR | |
| VCCD345 | DU50 | PWR | |
| VCCD345 | DU52 | PWR | |
| VCCD345 | DU54 | PWR | |
| VCCD345 | DU56 | PWR | |
| VCCD345 | DU58 | PWR | |
| VCCD345 | DU60 | PWR | |
| VCCD345 | DU62 | PWR | |
| VCCD345 | DU64 | PWR | |
| VCCD345 | EC46 | PWR | |
| VCCD345 | EC48 | PWR | |
| VCCD345 | EC50 | PWR | |
| VCCD345 | EC52 | PWR | |
| VCCD345 | EC54 | PWR | |
| VCCD345 | EC56 | PWR | |
| VCCD345 | EC58 | PWR | |
| VCCD345 | EC60 | PWR | |
| VCCD345 | EC62 | PWR | |
| VCCD345 | EE44 | PWR | |
| VCCD345 | EF45 | PWR | |
| VCCD345 | EF49 | PWR | |
| VCCD345 | EF53 | PWR | |
| VCCD345 | EF59 | PWR | |
| VCCIN | AF43 | PWR | |
| VCCIN | AG38 | PWR | |
| VCCIN | AG40 | PWR | |
| VCCIN | AG42 | PWR | |
| VCCIN | AH37 | PWR | |
| VCCIN | AH39 | PWR | |
| VCCIN | AH41 | PWR | |
| VCCIN | AJ36 | PWR | |
| VCCIN | AK35 | PWR | |
| VCCIN | AK45 | PWR | |
| VCCIN | AK47 | PWR | |

Table A-1. Pin List By Name (Sheet 50 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VCCIN | AK49 | PWR | |
| VCCIN | AK51 | PWR | |
| VCCIN | AK53 | PWR | |
| VCCIN | AL34 | PWR | |
| VCCIN | AL46 | PWR | |
| VCCIN | AL48 | PWR | |
| VCCIN | AL50 | PWR | |
| VCCIN | AL52 | PWR | |
| VCCIN | AL54 | PWR | |
| VCCIN | AM33 | PWR | |
| VCCIN | AM53 | PWR | |
| VCCIN | AM55 | PWR | |
| VCCIN | AN32 | PWR | |
| VCCIN | AN54 | PWR | |
| VCCIN | AN56 | PWR | |
| VCCIN | AP55 | PWR | |
| VCCIN | AP57 | PWR | |
| VCCIN | AR56 | PWR | |
| VCCIN | AR58 | PWR | |
| VCCIN | AT57 | PWR | |
| VCCIN | AT59 | PWR | |
| VCCIN | AU58 | PWR | |
| VCCIN | AU60 | PWR | |
| VCCIN | AV59 | PWR | |
| VCCIN | AV61 | PWR | |
| VCCIN | AW60 | PWR | |
| VCCIN | AY61 | PWR | |
| VCCIN | BA60 | PWR | |
| VCCIN | BB61 | PWR | |
| VCCIN | BB85 | PWR | |
| VCCIN | BC60 | PWR | |
| VCCIN | BC62 | PWR | |
| VCCIN | BC84 | PWR | |
| VCCIN | BD61 | PWR | |
| VCCIN | BD73 | PWR | |
| VCCIN | BD75 | PWR | |
| VCCIN | BD77 | PWR | |
| VCCIN | BD79 | PWR | |
| VCCIN | BD81 | PWR | |
| VCCIN | BD83 | PWR | |
| VCCIN | BD85 | PWR | |



Table A-1. Pin List By Name (Sheet 51 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VCCIN | BE60 | PWR | |
| VCCIN | BE62 | PWR | |
| VCCIN | BE72 | PWR | |
| VCCIN | BE74 | PWR | |
| VCCIN | BE76 | PWR | |
| VCCIN | BE78 | PWR | |
| VCCIN | BE80 | PWR | |
| VCCIN | BE82 | PWR | |
| VCCIN | BE84 | PWR | |
| VCCIN | BF61 | PWR | |
| VCCIN | BF73 | PWR | |
| VCCIN | BF75 | PWR | |
| VCCIN | BF77 | PWR | |
| VCCIN | BF79 | PWR | |
| VCCIN | BF81 | PWR | |
| VCCIN | BF83 | PWR | |
| VCCIN | BF85 | PWR | |
| VCCIN | BG60 | PWR | |
| VCCIN | BG62 | PWR | |
| VCCIN | BG64 | PWR | |
| VCCIN | BG66 | PWR | |
| VCCIN | BG68 | PWR | |
| VCCIN | BG70 | PWR | |
| VCCIN | BG84 | PWR | |
| VCCIN | BH61 | PWR | |
| VCCIN | BH63 | PWR | |
| VCCIN | BH65 | PWR | |
| VCCIN | BH67 | PWR | |
| VCCIN | BH69 | PWR | |
| VCCIN | BH71 | PWR | |
| VCCIN | BH73 | PWR | |
| VCCIN | BH75 | PWR | |
| VCCIN | BH77 | PWR | |
| VCCIN | BH79 | PWR | |
| VCCIN | BH81 | PWR | |
| VCCIN | BH83 | PWR | |
| VCCIN | BJ60 | PWR | |
| VCCIN | BJ62 | PWR | |
| VCCIN | BJ64 | PWR | |
| VCCIN | BJ66 | PWR | |
| VCCIN | BJ68 | PWR | |

Table A-1. Pin List By Name (Sheet 52 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VCCIN | BJ70 | PWR | |
| VCCIN | BJ72 | PWR | |
| VCCIN | BJ74 | PWR | |
| VCCIN | BJ76 | PWR | |
| VCCIN | BJ78 | PWR | |
| VCCIN | BJ80 | PWR | |
| VCCIN | BJ82 | PWR | |
| VCCIN | BJ84 | PWR | |
| VCCIN | BK61 | PWR | |
| VCCIN | BK63 | PWR | |
| VCCIN | BK65 | PWR | |
| VCCIN | BK67 | PWR | |
| VCCIN | BK69 | PWR | |
| VCCIN | BK71 | PWR | |
| VCCIN | BK73 | PWR | |
| VCCIN | BK75 | PWR | |
| VCCIN | BK77 | PWR | |
| VCCIN | BK79 | PWR | |
| VCCIN | BK81 | PWR | |
| VCCIN | BK83 | PWR | |
| VCCIN | BL60 | PWR | |
| VCCIN | BL62 | PWR | |
| VCCIN | BL84 | PWR | |
| VCCIN | BM61 | PWR | |
| VCCIN | BM63 | PWR | |
| VCCIN | BM65 | PWR | |
| VCCIN | BM67 | PWR | |
| VCCIN | BM69 | PWR | |
| VCCIN | BM71 | PWR | |
| VCCIN | BM73 | PWR | |
| VCCIN | BM75 | PWR | |
| VCCIN | BM77 | PWR | |
| VCCIN | BM79 | PWR | |
| VCCIN | BM81 | PWR | |
| VCCIN | BM83 | PWR | |
| VCCIN | BN60 | PWR | |
| VCCIN | BN62 | PWR | |
| VCCIN | BN64 | PWR | |
| VCCIN | BN66 | PWR | |
| VCCIN | BN68 | PWR | |
| VCCIN | BN70 | PWR | |

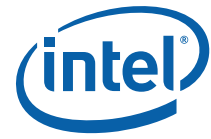


Table A-1. Pin List By Name (Sheet 53 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VCCIN | BN72 | PWR | |
| VCCIN | BN74 | PWR | |
| VCCIN | BN76 | PWR | |
| VCCIN | BN78 | PWR | |
| VCCIN | BN80 | PWR | |
| VCCIN | BN82 | PWR | |
| VCCIN | BN84 | PWR | |
| VCCIN | BP61 | PWR | |
| VCCIN | BP63 | PWR | |
| VCCIN | BP65 | PWR | |
| VCCIN | BP67 | PWR | |
| VCCIN | BP69 | PWR | |
| VCCIN | BP71 | PWR | |
| VCCIN | BP73 | PWR | |
| VCCIN | BP75 | PWR | |
| VCCIN | BP77 | PWR | |
| VCCIN | BP79 | PWR | |
| VCCIN | BP81 | PWR | |
| VCCIN | BP83 | PWR | |
| VCCIN | BR60 | PWR | |
| VCCIN | BR62 | PWR | |
| VCCIN | BR84 | PWR | |
| VCCIN | BT61 | PWR | |
| VCCIN | BT63 | PWR | |
| VCCIN | BT65 | PWR | |
| VCCIN | BT67 | PWR | |
| VCCIN | BT69 | PWR | |
| VCCIN | BT71 | PWR | |
| VCCIN | BT73 | PWR | |
| VCCIN | BT75 | PWR | |
| VCCIN | BT77 | PWR | |
| VCCIN | BT79 | PWR | |
| VCCIN | BT81 | PWR | |
| VCCIN | BT83 | PWR | |
| VCCIN | BU60 | PWR | |
| VCCIN | BU62 | PWR | |
| VCCIN | BU64 | PWR | |
| VCCIN | BU66 | PWR | |
| VCCIN | BU68 | PWR | |
| VCCIN | BU70 | PWR | |
| VCCIN | BU72 | PWR | |

Table A-1. Pin List By Name (Sheet 54 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VCCIN | BU74 | PWR | |
| VCCIN | BU76 | PWR | |
| VCCIN | BU78 | PWR | |
| VCCIN | BU80 | PWR | |
| VCCIN | BU82 | PWR | |
| VCCIN | BU84 | PWR | |
| VCCIN | BV61 | PWR | |
| VCCIN | BV63 | PWR | |
| VCCIN | BV65 | PWR | |
| VCCIN | BV67 | PWR | |
| VCCIN | BV69 | PWR | |
| VCCIN | BV71 | PWR | |
| VCCIN | BV73 | PWR | |
| VCCIN | BV75 | PWR | |
| VCCIN | BV77 | PWR | |
| VCCIN | BV79 | PWR | |
| VCCIN | BV81 | PWR | |
| VCCIN | BV83 | PWR | |
| VCCIN | BW60 | PWR | |
| VCCIN | BW62 | PWR | |
| VCCIN | BW64 | PWR | |
| VCCIN | BW66 | PWR | |
| VCCIN | BW68 | PWR | |
| VCCIN | BW70 | PWR | |
| VCCIN | BW84 | PWR | |
| VCCIN | BY61 | PWR | |
| VCCIN | BY73 | PWR | |
| VCCIN | BY75 | PWR | |
| VCCIN | BY77 | PWR | |
| VCCIN | BY79 | PWR | |
| VCCIN | BY81 | PWR | |
| VCCIN | BY83 | PWR | |
| VCCIN | CA60 | PWR | |
| VCCIN | CA62 | PWR | |
| VCCIN | CA72 | PWR | |
| VCCIN | CA74 | PWR | |
| VCCIN | CA76 | PWR | |
| VCCIN | CA78 | PWR | |
| VCCIN | CA80 | PWR | |
| VCCIN | CA82 | PWR | |
| VCCIN | CA84 | PWR | |



Table A-1. Pin List By Name (Sheet 55 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VCCIN | CB61 | PWR | |
| VCCIN | CB73 | PWR | |
| VCCIN | CB75 | PWR | |
| VCCIN | CB77 | PWR | |
| VCCIN | CB79 | PWR | |
| VCCIN | CB81 | PWR | |
| VCCIN | CB83 | PWR | |
| VCCIN | CC60 | PWR | |
| VCCIN | CC62 | PWR | |
| VCCIN | CC84 | PWR | |
| VCCIN | CD61 | PWR | |
| VCCIN | CD83 | PWR | |
| VCCIN | CD85 | PWR | |
| VCCIN | CE60 | PWR | |
| VCCIN | CE84 | PWR | |
| VCCIN | CF61 | PWR | |
| VCCIN | CF85 | PWR | |
| VCCIN | CG60 | PWR | |
| VCCIN | CG84 | PWR | |
| VCCIN | CH61 | PWR | |
| VCCIN | CH85 | PWR | |
| VCCIN | CJ60 | PWR | |
| VCCIN | CK59 | PWR | |
| VCCIN | CK61 | PWR | |
| VCCIN | CL58 | PWR | |
| VCCIN | CL60 | PWR | |
| VCCIN | CM57 | PWR | |
| VCCIN | CM59 | PWR | |
| VCCIN | CN56 | PWR | |
| VCCIN | CN58 | PWR | |
| VCCIN | CP33 | PWR | |
| VCCIN | CP55 | PWR | |
| VCCIN | CP57 | PWR | |
| VCCIN | CR34 | PWR | |
| VCCIN | CR54 | PWR | |
| VCCIN | CR56 | PWR | |
| VCCIN | CT37 | PWR | |
| VCCIN | CT39 | PWR | |
| VCCIN | CT41 | PWR | |
| VCCIN | CT53 | PWR | |
| VCCIN | CT55 | PWR | |

Table A-1. Pin List By Name (Sheet 56 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| VCCIN | CU38 | PWR | |
| VCCIN | CU40 | PWR | |
| VCCIN | CU42 | PWR | |
| VCCIN | CU52 | PWR | |
| VCCIN | CU54 | PWR | |
| VCCIN | CV51 | PWR | |
| VCCIN | CW46 | PWR | |
| VCCIN | CW48 | PWR | |
| VCCIN | CW50 | PWR | |
| VCCIN | CY47 | PWR | |
| VCCIN | CY49 | PWR | |
| VCCIN_SENSE | BA86 | PWR | |
| VCCINPMAX | AV85 | PWR | |
| VCCINPMAX | AW86 | PWR | |
| VCCIO | AA10 | PWR | |
| VCCIO | AC20 | PWR | |
| VCCIO | AC36 | PWR | |
| VCCIO | AC4 | PWR | |
| VCCIO | AD35 | PWR | |
| VCCIO | AD37 | PWR | |
| VCCIO | AE10 | PWR | |
| VCCIO | AE34 | PWR | |
| VCCIO | AE36 | PWR | |
| VCCIO | AF35 | PWR | |
| VCCIO | AF5 | PWR | |
| VCCIO | AG34 | PWR | |
| VCCIO | AH9 | PWR | |
| VCCIO | AL28 | PWR | |
| VCCIO | AM29 | PWR | |
| VCCIO | AM5 | PWR | |
| VCCIO | AN10 | PWR | |
| VCCIO | AR28 | PWR | |
| VCCIO | AT11 | PWR | |
| VCCIO | AT5 | PWR | |
| VCCIO | AT7 | PWR | |
| VCCIO | AV27 | PWR | |
| VCCIO | AW26 | PWR | |
| VCCIO | AW6 | PWR | |
| VCCIO | AY11 | PWR | |
| VCCIO | AY27 | PWR | |
| VCCIO | BA24 | PWR | |



Table A-1. Pin List By Name (Sheet 57 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VCCIO | BA26 | PWR | |
| VCCIO | BB27 | PWR | |
| VCCIO | BB5 | PWR | |
| VCCIO | BC26 | PWR | |
| VCCIO | BE24 | PWR | |
| VCCIO | BF23 | PWR | |
| VCCIO | BF27 | PWR | |
| VCCIO | BG26 | PWR | |
| VCCIO | BH25 | PWR | |
| VCCIO | BH27 | PWR | |
| VCCIO | BJ24 | PWR | |
| VCCIO | BJ26 | PWR | |
| VCCIO | BK25 | PWR | |
| VCCIO | BK27 | PWR | |
| VCCIO | BL26 | PWR | |
| VCCIO | BM27 | PWR | |
| VCCIO | BP25 | PWR | |
| VCCIO | CB13 | PWR | |
| VCCIO | CB17 | PWR | |
| VCCIO | CC26 | PWR | |
| VCCIO | CD27 | PWR | |
| VCCIO | CD9 | PWR | |
| VCCIO | CE18 | PWR | |
| VCCIO | CF27 | PWR | |
| VCCIO | CF5 | PWR | |
| VCCIO | CG14 | PWR | |
| VCCIO | CH27 | PWR | |
| VCCIO | CH9 | PWR | |
| VCCIO | CJ28 | PWR | |
| VCCIO | CK5 | PWR | |
| VCCIO | CL12 | PWR | |
| VCCIO | CL20 | PWR | |
| VCCIO | CM15 | PWR | |
| VCCIO | CN6 | PWR | |
| VCCIO | CP13 | PWR | |
| VCCIO | CU12 | PWR | |
| VCCIO | CU18 | PWR | |
| VCCIO | CV21 | PWR | |
| VCCIO | CV7 | PWR | |
| VCCIO | CY17 | PWR | |
| VCCIO | D7 | PWR | |

Table A-1. Pin List By Name (Sheet 58 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| VCCIO | DA14 | PWR | |
| VCCIO | DC18 | PWR | |
| VCCIO | DD7 | PWR | |
| VCCIO | DE14 | PWR | |
| VCCIO | DF13 | PWR | |
| VCCIO | DF21 | PWR | |
| VCCIO | DG8 | PWR | |
| VCCIO | DH7 | PWR | |
| VCCIO | DJ16 | PWR | |
| VCCIO | DK21 | PWR | |
| VCCIO | DM17 | PWR | |
| VCCIO | DN8 | PWR | |
| VCCIO | DP19 | PWR | |
| VCCIO | DR10 | PWR | |
| VCCIO | DR2 | PWR | |
| VCCIO | DU20 | PWR | |
| VCCIO | DV11 | PWR | |
| VCCIO | EA12 | PWR | |
| VCCIO | EB15 | PWR | |
| VCCIO | EE10 | PWR | |
| VCCIO | H13 | PWR | |
| VCCIO | J10 | PWR | |
| VCCIO | J2 | PWR | |
| VCCIO | K15 | PWR | |
| VCCIO | L14 | PWR | |
| VCCIO | L16 | PWR | |
| VCCIO | M11 | PWR | |
| VCCIO | M21 | PWR | |
| VCCIO | M7 | PWR | |
| VCCIO | M9 | PWR | |
| VCCIO | N18 | PWR | |
| VCCIO | P5 | PWR | |
| VCCIO | T3 | PWR | |
| VCCIO | U14 | PWR | |
| VCCIO | W10 | PWR | |
| VCCIO | W4 | PWR | |
| VCCIO | W6 | PWR | |
| VCCIO_SENSE | BH5 | PWR | |
| VCCSA | CB65 | PWR | |
| VCCSA | CB67 | PWR | |
| VCCSA | CB69 | PWR | |



Table A-1. Pin List By Name (Sheet 59 of 90)

| Pin Name | Location | Type | I/O |
|-------------|----------|------|-----|
| VCCSA | CC66 | PWR | |
| VCCSA | CC68 | PWR | |
| VCCSA | CC70 | PWR | |
| VCCSA | CD65 | PWR | |
| VCCSA | CD67 | PWR | |
| VCCSA | CD69 | PWR | |
| VCCSA | CD71 | PWR | |
| VCCSA | CE64 | PWR | |
| VCCSA | CE66 | PWR | |
| VCCSA | CE68 | PWR | |
| VCCSA | CE72 | PWR | |
| VCCSA | CE74 | PWR | |
| VCCSA | CF65 | PWR | |
| VCCSA | CF67 | PWR | |
| VCCSA | CF73 | PWR | |
| VCCSA | CF75 | PWR | |
| VCCSA | CG64 | PWR | |
| VCCSA | CG66 | PWR | |
| VCCSA | CG74 | PWR | |
| VCCSA | CH65 | PWR | |
| VCCSA | CH75 | PWR | |
| VCCSA | CJ64 | PWR | |
| VCCSA | CJ66 | PWR | |
| VCCSA_SENSE | CE76 | PWR | |
| VSENSEPMAX | AD41 | | |
| VSS | A26 | PWR | |
| VSS | A30 | PWR | |
| VSS | A32 | PWR | |
| VSS | A36 | PWR | |
| VSS | A38 | PWR | |
| VSS | A42 | PWR | |
| VSS | AA16 | PWR | |
| VSS | AA18 | PWR | |
| VSS | AA22 | PWR | |
| VSS | AA24 | PWR | |
| VSS | AA30 | PWR | |
| VSS | AA36 | PWR | |
| VSS | AA4 | PWR | |
| VSS | AA42 | PWR | |
| VSS | AA64 | PWR | |
| VSS | AA66 | PWR | |

Table A-1. Pin List By Name (Sheet 60 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | AA68 | PWR | |
| VSS | AA76 | PWR | |
| VSS | AA78 | PWR | |
| VSS | AA80 | PWR | |
| VSS | AA82 | PWR | |
| VSS | AB1 | PWR | |
| VSS | AB11 | PWR | |
| VSS | AB21 | PWR | |
| VSS | AB23 | PWR | |
| VSS | AB25 | PWR | |
| VSS | AB29 | PWR | |
| VSS | AB31 | PWR | |
| VSS | AB35 | PWR | |
| VSS | AB37 | PWR | |
| VSS | AB41 | PWR | |
| VSS | AB5 | PWR | |
| VSS | AB65 | PWR | |
| VSS | AB69 | PWR | |
| VSS | AB73 | PWR | |
| VSS | AB79 | PWR | |
| VSS | AB83 | PWR | |
| VSS | AB85 | PWR | |
| VSS | AC18 | PWR | |
| VSS | AC22 | PWR | |
| VSS | AC26 | PWR | |
| VSS | AC28 | PWR | |
| VSS | AC32 | PWR | |
| VSS | AC34 | PWR | |
| VSS | AC38 | PWR | |
| VSS | AC40 | PWR | |
| VSS | AC48 | PWR | |
| VSS | AC50 | PWR | |
| VSS | AC52 | PWR | |
| VSS | AC54 | PWR | |
| VSS | AC56 | PWR | |
| VSS | AC58 | PWR | |
| VSS | AC60 | PWR | |
| VSS | AC62 | PWR | |
| VSS | AC64 | PWR | |
| VSS | AC70 | PWR | |
| VSS | AC72 | PWR | |



Table A-1. Pin List By Name (Sheet 61 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | AC78 | PWR | |
| VSS | AC84 | PWR | |
| VSS | AC86 | PWR | |
| VSS | AD11 | PWR | |
| VSS | AD13 | PWR | |
| VSS | AD15 | PWR | |
| VSS | AD19 | PWR | |
| VSS | AD21 | PWR | |
| VSS | AD27 | PWR | |
| VSS | AD3 | PWR | |
| VSS | AD33 | PWR | |
| VSS | AD39 | PWR | |
| VSS | AD43 | PWR | |
| VSS | AD7 | PWR | |
| VSS | AD71 | PWR | |
| VSS | AD73 | PWR | |
| VSS | AD75 | PWR | |
| VSS | AD81 | PWR | |
| VSS | AD83 | PWR | |
| VSS | AD85 | PWR | |
| VSS | AD9 | PWR | |
| VSS | AE16 | PWR | |
| VSS | AE38 | PWR | |
| VSS | AE4 | PWR | |
| VSS | AE40 | PWR | |
| VSS | AE42 | PWR | |
| VSS | AE64 | PWR | |
| VSS | AE66 | PWR | |
| VSS | AE68 | PWR | |
| VSS | AE70 | PWR | |
| VSS | AE78 | PWR | |
| VSS | AE8 | PWR | |
| VSS | AF1 | PWR | |
| VSS | AF21 | PWR | |
| VSS | AF23 | PWR | |
| VSS | AF25 | PWR | |
| VSS | AF27 | PWR | |
| VSS | AF29 | PWR | |
| VSS | AF31 | PWR | |
| VSS | AF33 | PWR | |
| VSS | AF37 | PWR | |

Table A-1. Pin List By Name (Sheet 62 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | AF39 | PWR | |
| VSS | AF41 | PWR | |
| VSS | AF73 | PWR | |
| VSS | AF77 | PWR | |
| VSS | AF83 | PWR | |
| VSS | AF85 | PWR | |
| VSS | AF9 | PWR | |
| VSS | AG12 | PWR | |
| VSS | AG14 | PWR | |
| VSS | AG18 | PWR | |
| VSS | AG36 | PWR | |
| VSS | AG64 | PWR | |
| VSS | AG70 | PWR | |
| VSS | AG74 | PWR | |
| VSS | AG76 | PWR | |
| VSS | AG78 | PWR | |
| VSS | AG80 | PWR | |
| VSS | AH1 | PWR | |
| VSS | AH21 | PWR | |
| VSS | AH27 | PWR | |
| VSS | AH33 | PWR | |
| VSS | AH35 | PWR | |
| VSS | AH45 | PWR | |
| VSS | AH47 | PWR | |
| VSS | AH49 | PWR | |
| VSS | AH5 | PWR | |
| VSS | AH51 | PWR | |
| VSS | AH53 | PWR | |
| VSS | AH59 | PWR | |
| VSS | AH61 | PWR | |
| VSS | AH65 | PWR | |
| VSS | AH69 | PWR | |
| VSS | AH75 | PWR | |
| VSS | AH77 | PWR | |
| VSS | AH83 | PWR | |
| VSS | AJ22 | PWR | |
| VSS | AJ26 | PWR | |
| VSS | AJ28 | PWR | |
| VSS | AJ32 | PWR | |
| VSS | AJ34 | PWR | |
| VSS | AJ4 | PWR | |



Table A-1. Pin List By Name (Sheet 63 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | AJ46 | PWR | |
| VSS | AJ48 | PWR | |
| VSS | AJ50 | PWR | |
| VSS | AJ52 | PWR | |
| VSS | AJ54 | PWR | |
| VSS | AJ66 | PWR | |
| VSS | AJ68 | PWR | |
| VSS | AJ74 | PWR | |
| VSS | AJ78 | PWR | |
| VSS | AJ8 | PWR | |
| VSS | AJ82 | PWR | |
| VSS | AJ86 | PWR | |
| VSS | AK13 | PWR | |
| VSS | AK19 | PWR | |
| VSS | AK23 | PWR | |
| VSS | AK25 | PWR | |
| VSS | AK29 | PWR | |
| VSS | AK31 | PWR | |
| VSS | AK33 | PWR | |
| VSS | AK55 | PWR | |
| VSS | AK65 | PWR | |
| VSS | AK67 | PWR | |
| VSS | AK73 | PWR | |
| VSS | AK79 | PWR | |
| VSS | AK81 | PWR | |
| VSS | AK83 | PWR | |
| VSS | AK85 | PWR | |
| VSS | AK9 | PWR | |
| VSS | AL10 | PWR | |
| VSS | AL24 | PWR | |
| VSS | AL30 | PWR | |
| VSS | AL32 | PWR | |
| VSS | AL4 | PWR | |
| VSS | AL56 | PWR | |
| VSS | AL64 | PWR | |
| VSS | AL68 | PWR | |
| VSS | AL76 | PWR | |
| VSS | AL78 | PWR | |
| VSS | AL80 | PWR | |
| VSS | AL82 | PWR | |
| VSS | AL86 | PWR | |

Table A-1. Pin List By Name (Sheet 64 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | AM1 | PWR | |
| VSS | AM31 | PWR | |
| VSS | AM57 | PWR | |
| VSS | AM63 | PWR | |
| VSS | AM69 | PWR | |
| VSS | AM73 | PWR | |
| VSS | AM79 | PWR | |
| VSS | AM83 | PWR | |
| VSS | AN2 | PWR | |
| VSS | AN28 | PWR | |
| VSS | AN58 | PWR | |
| VSS | AN6 | PWR | |
| VSS | AN78 | PWR | |
| VSS | AP13 | PWR | |
| VSS | AP19 | PWR | |
| VSS | AP31 | PWR | |
| VSS | AP5 | PWR | |
| VSS | AP59 | PWR | |
| VSS | AP63 | PWR | |
| VSS | AP65 | PWR | |
| VSS | AP67 | PWR | |
| VSS | AP69 | PWR | |
| VSS | AP73 | PWR | |
| VSS | AP75 | PWR | |
| VSS | AP81 | PWR | |
| VSS | AP83 | PWR | |
| VSS | AP85 | PWR | |
| VSS | AP9 | PWR | |
| VSS | AR10 | PWR | |
| VSS | AR24 | PWR | |
| VSS | AR30 | PWR | |
| VSS | AR6 | PWR | |
| VSS | AR60 | PWR | |
| VSS | AR72 | PWR | |
| VSS | AR78 | PWR | |
| VSS | AT15 | PWR | |
| VSS | AT17 | PWR | |
| VSS | AT21 | PWR | |
| VSS | AT27 | PWR | |
| VSS | AT61 | PWR | |
| VSS | AT63 | PWR | |



Table A-1. Pin List By Name (Sheet 65 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | AT69 | PWR | |
| VSS | AT73 | PWR | |
| VSS | AT77 | PWR | |
| VSS | AT83 | PWR | |
| VSS | AT85 | PWR | |
| VSS | AU2 | PWR | |
| VSS | AU26 | PWR | |
| VSS | AU28 | PWR | |
| VSS | AU6 | PWR | |
| VSS | AU62 | PWR | |
| VSS | AU64 | PWR | |
| VSS | AU68 | PWR | |
| VSS | AU74 | PWR | |
| VSS | AU76 | PWR | |
| VSS | AU78 | PWR | |
| VSS | AU80 | PWR | |
| VSS | AU84 | PWR | |
| VSS | AU86 | PWR | |
| VSS | AV1 | PWR | |
| VSS | AV11 | PWR | |
| VSS | AV13 | PWR | |
| VSS | AV19 | PWR | |
| VSS | AV23 | PWR | |
| VSS | AV25 | PWR | |
| VSS | AV3 | PWR | |
| VSS | AV63 | PWR | |
| VSS | AV65 | PWR | |
| VSS | AV67 | PWR | |
| VSS | AV7 | PWR | |
| VSS | AV75 | PWR | |
| VSS | AV83 | PWR | |
| VSS | AW10 | PWR | |
| VSS | AW2 | PWR | |
| VSS | AW62 | PWR | |
| VSS | AW66 | PWR | |
| VSS | AW68 | PWR | |
| VSS | AW70 | PWR | |
| VSS | AW72 | PWR | |
| VSS | AW74 | PWR | |
| VSS | AW78 | PWR | |
| VSS | AW82 | PWR | |

Table A-1. Pin List By Name (Sheet 66 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|-------|-----|
| VSS | AW84 | PWR | |
| VSS | AY15 | PWR | |
| VSS | AY17 | PWR | |
| VSS | AY21 | PWR | |
| VSS | AY23 | PWR | |
| VSS | AY25 | PWR | |
| VSS | AY5 | PWR | |
| VSS | AY63 | PWR | |
| VSS | AY79 | PWR | |
| VSS | AY81 | PWR | |
| VSS | B25 | PWR | |
| VSS | B31 | PWR | |
| VSS | B37 | PWR | |
| VSS | B43 | PWR | |
| VSS | B5 | PWR | |
| VSS | B71 | PWR | |
| VSS | B75 | PWR | |
| VSS | B79 | PWR | |
| VSS | B9 | POWER | |
| VSS | BA12 | PWR | |
| VSS | BA2 | PWR | |
| VSS | BA6 | PWR | |
| VSS | BA62 | PWR | |
| VSS | BA68 | PWR | |
| VSS | BA74 | PWR | |
| VSS | BA80 | PWR | |
| VSS | BA84 | PWR | |
| VSS | BB19 | PWR | |
| VSS | BB23 | PWR | |
| VSS | BB63 | PWR | |
| VSS | BB69 | PWR | |
| VSS | BB73 | PWR | |
| VSS | BB75 | PWR | |
| VSS | BB77 | PWR | |
| VSS | BB79 | PWR | |
| VSS | BB81 | PWR | |
| VSS | BB83 | PWR | |
| VSS | BC12 | PWR | |
| VSS | BC16 | PWR | |
| VSS | BC4 | PWR | |
| VSS | BC70 | PWR | |



Table A-1. Pin List By Name (Sheet 67 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | BC72 | PWR | |
| VSS | BC74 | PWR | |
| VSS | BC76 | PWR | |
| VSS | BC78 | PWR | |
| VSS | BC8 | PWR | |
| VSS | BC80 | PWR | |
| VSS | BC82 | PWR | |
| VSS | BD11 | PWR | |
| VSS | BD15 | PWR | |
| VSS | BD21 | PWR | |
| VSS | BD27 | PWR | |
| VSS | BD5 | PWR | |
| VSS | BD63 | PWR | |
| VSS | BD71 | PWR | |
| VSS | BE10 | PWR | |
| VSS | BE26 | PWR | |
| VSS | BE4 | PWR | |
| VSS | BE6 | PWR | |
| VSS | BE64 | PWR | |
| VSS | BE66 | PWR | |
| VSS | BE68 | PWR | |
| VSS | BE70 | PWR | |
| VSS | BE8 | PWR | |
| VSS | BF15 | PWR | |
| VSS | BF17 | PWR | |
| VSS | BF19 | PWR | |
| VSS | BF25 | PWR | |
| VSS | BF63 | PWR | |
| VSS | BF65 | PWR | |
| VSS | BF67 | PWR | |
| VSS | BF69 | PWR | |
| VSS | BF71 | PWR | |
| VSS | BF9 | PWR | |
| VSS | BG10 | PWR | |
| VSS | BG22 | PWR | |
| VSS | BG24 | PWR | |
| VSS | BG6 | PWR | |
| VSS | BG72 | PWR | |
| VSS | BG74 | PWR | |
| VSS | BG76 | PWR | |
| VSS | BG78 | PWR | |

Table A-1. Pin List By Name (Sheet 68 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | BG8 | PWR | |
| VSS | BG80 | PWR | |
| VSS | BG82 | PWR | |
| VSS | BH11 | PWR | |
| VSS | BH15 | PWR | |
| VSS | BH17 | PWR | |
| VSS | BH21 | PWR | |
| VSS | BH7 | PWR | |
| VSS | BH9 | PWR | |
| VSS | BJ4 | PWR | |
| VSS | BJ6 | PWR | |
| VSS | BK11 | PWR | |
| VSS | BK19 | PWR | |
| VSS | BK3 | PWR | |
| VSS | BK7 | PWR | |
| VSS | BL10 | PWR | |
| VSS | BL12 | PWR | |
| VSS | BL22 | PWR | |
| VSS | BL24 | PWR | |
| VSS | BL6 | PWR | |
| VSS | BL64 | PWR | |
| VSS | BL66 | PWR | |
| VSS | BL68 | PWR | |
| VSS | BL70 | PWR | |
| VSS | BL72 | PWR | |
| VSS | BL74 | PWR | |
| VSS | BL76 | PWR | |
| VSS | BL78 | PWR | |
| VSS | BL80 | PWR | |
| VSS | BL82 | PWR | |
| VSS | BM13 | PWR | |
| VSS | BM15 | PWR | |
| VSS | BM25 | PWR | |
| VSS | BM9 | PWR | |
| VSS | BN10 | PWR | |
| VSS | BN20 | PWR | |
| VSS | BN26 | PWR | |
| VSS | BN6 | PWR | |
| VSS | BP27 | PWR | |
| VSS | BP3 | PWR | |
| VSS | BR10 | PWR | |



Table A-1. Pin List By Name (Sheet 69 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | BR16 | PWR | |
| VSS | BR18 | PWR | |
| VSS | BR26 | PWR | |
| VSS | BR6 | PWR | |
| VSS | BR64 | PWR | |
| VSS | BR66 | PWR | |
| VSS | BR68 | PWR | |
| VSS | BR70 | PWR | |
| VSS | BR72 | PWR | |
| VSS | BR74 | PWR | |
| VSS | BR76 | PWR | |
| VSS | BR78 | PWR | |
| VSS | BR80 | PWR | |
| VSS | BR82 | PWR | |
| VSS | BT21 | PWR | |
| VSS | BT23 | PWR | |
| VSS | BT25 | PWR | |
| VSS | BT3 | PWR | |
| VSS | BT5 | PWR | |
| VSS | BT9 | PWR | |
| VSS | BU10 | PWR | |
| VSS | BU8 | PWR | |
| VSS | BV17 | PWR | |
| VSS | BV25 | PWR | |
| VSS | BV5 | PWR | |
| VSS | BW12 | PWR | |
| VSS | BW14 | PWR | |
| VSS | BW16 | PWR | |
| VSS | BW18 | PWR | |
| VSS | BW26 | PWR | |
| VSS | BW6 | PWR | |
| VSS | BW72 | PWR | |
| VSS | BW74 | PWR | |
| VSS | BW76 | PWR | |
| VSS | BW78 | PWR | |
| VSS | BW80 | PWR | |
| VSS | BW82 | PWR | |
| VSS | BY11 | PWR | |
| VSS | BY13 | PWR | |
| VSS | BY23 | PWR | |
| VSS | BY63 | PWR | |

Table A-1. Pin List By Name (Sheet 70 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | BY65 | PWR | |
| VSS | BY67 | PWR | |
| VSS | BY69 | PWR | |
| VSS | BY71 | PWR | |
| VSS | C10 | PWR | |
| VSS | C12 | PWR | |
| VSS | C14 | PWR | |
| VSS | C16 | PWR | |
| VSS | C4 | PWR | |
| VSS | C76 | PWR | |
| VSS | C78 | PWR | |
| VSS | C8 | PWR | |
| VSS | C80 | PWR | |
| VSS | CA10 | PWR | |
| VSS | CA14 | PWR | |
| VSS | CA18 | PWR | |
| VSS | CA2 | PWR | |
| VSS | CA20 | PWR | |
| VSS | CA26 | PWR | |
| VSS | CA6 | PWR | |
| VSS | CA64 | PWR | |
| VSS | CA66 | PWR | |
| VSS | CA68 | PWR | |
| VSS | CA70 | PWR | |
| VSS | CA8 | PWR | |
| VSS | CB27 | PWR | |
| VSS | CB63 | PWR | |
| VSS | CB7 | PWR | |
| VSS | CB71 | PWR | |
| VSS | CB9 | PWR | |
| VSS | CC16 | PWR | |
| VSS | CC18 | PWR | |
| VSS | CC24 | PWR | |
| VSS | CC4 | PWR | |
| VSS | CC64 | PWR | |
| VSS | CC72 | PWR | |
| VSS | CC74 | PWR | |
| VSS | CC76 | PWR | |
| VSS | CC78 | PWR | |
| VSS | CC80 | PWR | |
| VSS | CC82 | PWR | |



Table A-1. Pin List By Name (Sheet 71 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | CD13 | PWR | |
| VSS | CD5 | PWR | |
| VSS | CD63 | PWR | |
| VSS | CD73 | PWR | |
| VSS | CD75 | PWR | |
| VSS | CD77 | PWR | |
| VSS | CD79 | PWR | |
| VSS | CD81 | PWR | |
| VSS | CE10 | PWR | |
| VSS | CE14 | PWR | |
| VSS | CE20 | PWR | |
| VSS | CE26 | PWR | |
| VSS | CE62 | PWR | |
| VSS | CE70 | PWR | |
| VSS | CE82 | PWR | |
| VSS | CF63 | PWR | |
| VSS | CF69 | PWR | |
| VSS | CF71 | PWR | |
| VSS | CF77 | PWR | |
| VSS | CF83 | PWR | |
| VSS | CF9 | PWR | |
| VSS | CG18 | PWR | |
| VSS | CG22 | PWR | |
| VSS | CG6 | PWR | |
| VSS | CG62 | PWR | |
| VSS | CG68 | PWR | |
| VSS | CG72 | PWR | |
| VSS | CG80 | PWR | |
| VSS | CH1 | PWR | |
| VSS | CH15 | PWR | |
| VSS | CH19 | PWR | |
| VSS | CH3 | PWR | |
| VSS | CH63 | PWR | |
| VSS | CH67 | PWR | |
| VSS | CH73 | PWR | |
| VSS | CH79 | PWR | |
| VSS | CH81 | PWR | |
| VSS | CH83 | PWR | |
| VSS | CJ10 | PWR | |
| VSS | CJ12 | PWR | |
| VSS | CJ2 | PWR | |

Table A-1. Pin List By Name (Sheet 72 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | CJ6 | PWR | |
| VSS | CJ62 | PWR | |
| VSS | CJ74 | PWR | |
| VSS | CJ76 | PWR | |
| VSS | CJ78 | PWR | |
| VSS | CJ8 | PWR | |
| VSS | CJ82 | PWR | |
| VSS | CJ84 | PWR | |
| VSS | CJ86 | PWR | |
| VSS | CK11 | PWR | |
| VSS | CK15 | PWR | |
| VSS | CK21 | PWR | |
| VSS | CK27 | PWR | |
| VSS | CK63 | PWR | |
| VSS | CK65 | PWR | |
| VSS | CK67 | PWR | |
| VSS | CK69 | PWR | |
| VSS | CK71 | PWR | |
| VSS | CK73 | PWR | |
| VSS | CK75 | PWR | |
| VSS | CK83 | PWR | |
| VSS | CK85 | PWR | |
| VSS | CL14 | PWR | |
| VSS | CL18 | PWR | |
| VSS | CL22 | PWR | |
| VSS | CL62 | PWR | |
| VSS | CL64 | PWR | |
| VSS | CL66 | PWR | |
| VSS | CL74 | PWR | |
| VSS | CL76 | PWR | |
| VSS | CL78 | PWR | |
| VSS | CL8 | PWR | |
| VSS | CL80 | PWR | |
| VSS | CM19 | PWR | |
| VSS | CM27 | PWR | |
| VSS | CM29 | PWR | |
| VSS | CM31 | PWR | |
| VSS | CM5 | PWR | |
| VSS | CM61 | PWR | |
| VSS | CM63 | PWR | |
| VSS | CM67 | PWR | |



Table A-1. Pin List By Name (Sheet 73 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | CM73 | PWR | |
| VSS | CM77 | PWR | |
| VSS | CM83 | PWR | |
| VSS | CM85 | PWR | |
| VSS | CN12 | PWR | |
| VSS | CN14 | PWR | |
| VSS | CN2 | PWR | |
| VSS | CN26 | PWR | |
| VSS | CN32 | PWR | |
| VSS | CN60 | PWR | |
| VSS | CN62 | PWR | |
| VSS | CN68 | PWR | |
| VSS | CN78 | PWR | |
| VSS | CP1 | PWR | |
| VSS | CP25 | PWR | |
| VSS | CP59 | PWR | |
| VSS | CP69 | PWR | |
| VSS | CP73 | PWR | |
| VSS | CP75 | PWR | |
| VSS | CP81 | PWR | |
| VSS | CP83 | PWR | |
| VSS | CR10 | PWR | |
| VSS | CR22 | PWR | |
| VSS | CR24 | PWR | |
| VSS | CR32 | PWR | |
| VSS | CR58 | PWR | |
| VSS | CR6 | PWR | |
| VSS | CR62 | PWR | |
| VSS | CR64 | PWR | |
| VSS | CR66 | PWR | |
| VSS | CR68 | PWR | |
| VSS | CR78 | PWR | |
| VSS | CR86 | PWR | |
| VSS | CT13 | PWR | |
| VSS | CT19 | PWR | |
| VSS | CT27 | PWR | |
| VSS | CT29 | PWR | |
| VSS | CT33 | PWR | |
| VSS | CT35 | PWR | |
| VSS | CT57 | PWR | |
| VSS | CT7 | PWR | |

Table A-1. Pin List By Name (Sheet 74 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | CT73 | PWR | |
| VSS | CT79 | PWR | |
| VSS | CT83 | PWR | |
| VSS | CT85 | PWR | |
| VSS | CU22 | PWR | |
| VSS | CU28 | PWR | |
| VSS | CU30 | PWR | |
| VSS | CU34 | PWR | |
| VSS | CU36 | PWR | |
| VSS | CU4 | PWR | |
| VSS | CU56 | PWR | |
| VSS | CU62 | PWR | |
| VSS | CU68 | PWR | |
| VSS | CU76 | PWR | |
| VSS | CU78 | PWR | |
| VSS | CU80 | PWR | |
| VSS | CU82 | PWR | |
| VSS | CU86 | PWR | |
| VSS | CV1 | PWR | |
| VSS | CV17 | PWR | |
| VSS | CV25 | PWR | |
| VSS | CV27 | PWR | |
| VSS | CV31 | PWR | |
| VSS | CV33 | PWR | |
| VSS | CV37 | PWR | |
| VSS | CV39 | PWR | |
| VSS | CV41 | PWR | |
| VSS | CV53 | PWR | |
| VSS | CV55 | PWR | |
| VSS | CV63 | PWR | |
| VSS | CV67 | PWR | |
| VSS | CV73 | PWR | |
| VSS | CV79 | PWR | |
| VSS | CV81 | PWR | |
| VSS | CV83 | PWR | |
| VSS | CW12 | PWR | |
| VSS | CW26 | PWR | |
| VSS | CW32 | PWR | |
| VSS | CW38 | PWR | |
| VSS | CW40 | PWR | |
| VSS | CW42 | PWR | |



Table A-1. Pin List By Name (Sheet 75 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | CW52 | PWR | |
| VSS | CW54 | PWR | |
| VSS | CW6 | PWR | |
| VSS | CW64 | PWR | |
| VSS | CW66 | PWR | |
| VSS | CW68 | PWR | |
| VSS | CW74 | PWR | |
| VSS | CW78 | PWR | |
| VSS | CW82 | PWR | |
| VSS | CY1 | PWR | |
| VSS | CY13 | PWR | |
| VSS | CY15 | PWR | |
| VSS | CY21 | PWR | |
| VSS | CY41 | PWR | |
| VSS | CY45 | PWR | |
| VSS | CY51 | PWR | |
| VSS | CY59 | PWR | |
| VSS | CY61 | PWR | |
| VSS | CY65 | PWR | |
| VSS | CY69 | PWR | |
| VSS | CY75 | PWR | |
| VSS | CY77 | PWR | |
| VSS | CY83 | PWR | |
| VSS | CY85 | PWR | |
| VSS | CY9 | PWR | |
| VSS | D11 | PWR | |
| VSS | D13 | PWR | |
| VSS | D25 | PWR | |
| VSS | D27 | PWR | |
| VSS | D29 | PWR | |
| VSS | D3 | PWR | |
| VSS | D31 | PWR | |
| VSS | D33 | PWR | |
| VSS | D35 | PWR | |
| VSS | D37 | PWR | |
| VSS | D39 | PWR | |
| VSS | D41 | PWR | |
| VSS | D43 | PWR | |
| VSS | D77 | PWR | |
| VSS | D81 | PWR | |
| VSS | DA18 | PWR | |

Table A-1. Pin List By Name (Sheet 76 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | DA26 | PWR | |
| VSS | DA28 | PWR | |
| VSS | DA30 | PWR | |
| VSS | DA32 | PWR | |
| VSS | DA34 | PWR | |
| VSS | DA36 | PWR | |
| VSS | DA38 | PWR | |
| VSS | DA44 | PWR | |
| VSS | DA46 | PWR | |
| VSS | DA48 | PWR | |
| VSS | DA50 | PWR | |
| VSS | DA6 | PWR | |
| VSS | DA64 | PWR | |
| VSS | DA70 | PWR | |
| VSS | DA74 | PWR | |
| VSS | DA76 | PWR | |
| VSS | DA78 | PWR | |
| VSS | DA80 | PWR | |
| VSS | DB13 | PWR | |
| VSS | DB17 | PWR | |
| VSS | DB23 | PWR | |
| VSS | DB25 | PWR | |
| VSS | DB3 | PWR | |
| VSS | DB39 | PWR | |
| VSS | DB41 | PWR | |
| VSS | DB47 | PWR | |
| VSS | DB49 | PWR | |
| VSS | DB7 | PWR | |
| VSS | DB73 | PWR | |
| VSS | DB77 | PWR | |
| VSS | DB83 | PWR | |
| VSS | DB85 | PWR | |
| VSS | DC14 | PWR | |
| VSS | DC24 | PWR | |
| VSS | DC26 | PWR | |
| VSS | DC32 | PWR | |
| VSS | DC38 | PWR | |
| VSS | DC42 | PWR | |
| VSS | DC64 | PWR | |
| VSS | DC66 | PWR | |
| VSS | DC68 | PWR | |



Table A-1. Pin List By Name (Sheet 77 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | DC70 | PWR | |
| VSS | DC78 | PWR | |
| VSS | DC84 | PWR | |
| VSS | DC86 | PWR | |
| VSS | DD11 | PWR | |
| VSS | DD23 | PWR | |
| VSS | DD27 | PWR | |
| VSS | DD31 | PWR | |
| VSS | DD33 | PWR | |
| VSS | DD37 | PWR | |
| VSS | DD71 | PWR | |
| VSS | DD73 | PWR | |
| VSS | DD75 | PWR | |
| VSS | DD81 | PWR | |
| VSS | DD83 | PWR | |
| VSS | DE18 | PWR | |
| VSS | DE20 | PWR | |
| VSS | DE24 | PWR | |
| VSS | DE28 | PWR | |
| VSS | DE30 | PWR | |
| VSS | DE34 | PWR | |
| VSS | DE36 | PWR | |
| VSS | DE48 | PWR | |
| VSS | DE50 | PWR | |
| VSS | DE52 | PWR | |
| VSS | DE54 | PWR | |
| VSS | DE56 | PWR | |
| VSS | DE58 | PWR | |
| VSS | DE6 | PWR | |
| VSS | DE60 | PWR | |
| VSS | DE62 | PWR | |
| VSS | DE64 | PWR | |
| VSS | DE70 | PWR | |
| VSS | DE72 | PWR | |
| VSS | DE78 | PWR | |
| VSS | DE8 | PWR | |
| VSS | DF19 | PWR | |
| VSS | DF29 | PWR | |
| VSS | DF35 | PWR | |
| VSS | DF37 | PWR | |
| VSS | DF39 | PWR | |

Table A-1. Pin List By Name (Sheet 78 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | DF41 | PWR | |
| VSS | DF5 | PWR | |
| VSS | DF65 | PWR | |
| VSS | DF69 | PWR | |
| VSS | DF7 | PWR | |
| VSS | DF73 | PWR | |
| VSS | DF79 | PWR | |
| VSS | DF83 | PWR | |
| VSS | DF85 | PWR | |
| VSS | DG14 | PWR | |
| VSS | DG16 | PWR | |
| VSS | DG2 | PWR | |
| VSS | DG24 | PWR | |
| VSS | DG66 | PWR | |
| VSS | DG68 | PWR | |
| VSS | DG76 | PWR | |
| VSS | DG78 | PWR | |
| VSS | DG80 | PWR | |
| VSS | DG82 | PWR | |
| VSS | DH13 | PWR | |
| VSS | DH15 | PWR | |
| VSS | DH21 | PWR | |
| VSS | DH23 | PWR | |
| VSS | DH25 | PWR | |
| VSS | DH27 | PWR | |
| VSS | DH29 | PWR | |
| VSS | DH31 | PWR | |
| VSS | DH33 | PWR | |
| VSS | DH35 | PWR | |
| VSS | DH37 | PWR | |
| VSS | DH41 | PWR | |
| VSS | DH67 | PWR | |
| VSS | DH71 | PWR | |
| VSS | DH73 | PWR | |
| VSS | DH79 | PWR | |
| VSS | DH81 | PWR | |
| VSS | DH83 | PWR | |
| VSS | DJ10 | PWR | |
| VSS | DJ2 | PWR | |
| VSS | DJ22 | PWR | |
| VSS | DJ38 | PWR | |



Table A-1. Pin List By Name (Sheet 79 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | DJ42 | PWR | |
| VSS | DJ68 | PWR | |
| VSS | DJ74 | PWR | |
| VSS | DJ78 | PWR | |
| VSS | DJ82 | PWR | |
| VSS | DJ84 | PWR | |
| VSS | DK23 | PWR | |
| VSS | DK29 | PWR | |
| VSS | DK35 | PWR | |
| VSS | DK39 | PWR | |
| VSS | DK41 | PWR | |
| VSS | DK7 | PWR | |
| VSS | DK73 | PWR | |
| VSS | DK75 | PWR | |
| VSS | DK77 | PWR | |
| VSS | DK83 | PWR | |
| VSS | DK85 | PWR | |
| VSS | DL16 | PWR | |
| VSS | DL18 | PWR | |
| VSS | DL22 | PWR | |
| VSS | DL24 | PWR | |
| VSS | DL28 | PWR | |
| VSS | DL30 | PWR | |
| VSS | DL34 | PWR | |
| VSS | DL36 | PWR | |
| VSS | DL4 | PWR | |
| VSS | DL40 | PWR | |
| VSS | DL68 | PWR | |
| VSS | DL70 | PWR | |
| VSS | DL74 | PWR | |
| VSS | DL76 | PWR | |
| VSS | DL78 | PWR | |
| VSS | DL8 | PWR | |
| VSS | DL80 | PWR | |
| VSS | DM15 | PWR | |
| VSS | DM19 | PWR | |
| VSS | DM25 | PWR | |
| VSS | DM27 | PWR | |
| VSS | DM31 | PWR | |
| VSS | DM33 | PWR | |
| VSS | DM37 | PWR | |

Table A-1. Pin List By Name (Sheet 80 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | DM39 | PWR | |
| VSS | DM65 | PWR | |
| VSS | DM73 | PWR | |
| VSS | DM77 | PWR | |
| VSS | DM83 | PWR | |
| VSS | DN12 | PWR | |
| VSS | DN18 | PWR | |
| VSS | DN2 | PWR | |
| VSS | DN22 | PWR | |
| VSS | DN26 | PWR | |
| VSS | DN32 | PWR | |
| VSS | DN38 | PWR | |
| VSS | DN44 | PWR | |
| VSS | DN68 | PWR | |
| VSS | DN72 | PWR | |
| VSS | DN78 | PWR | |
| VSS | DP45 | PWR | |
| VSS | DP47 | PWR | |
| VSS | DP49 | PWR | |
| VSS | DP51 | PWR | |
| VSS | DP53 | PWR | |
| VSS | DP55 | PWR | |
| VSS | DP57 | PWR | |
| VSS | DP59 | PWR | |
| VSS | DP61 | PWR | |
| VSS | DP63 | PWR | |
| VSS | DP67 | PWR | |
| VSS | DP69 | PWR | |
| VSS | DP71 | PWR | |
| VSS | DP81 | PWR | |
| VSS | DP83 | PWR | |
| VSS | DP9 | PWR | |
| VSS | DR20 | PWR | |
| VSS | DR22 | PWR | |
| VSS | DR24 | PWR | |
| VSS | DR26 | PWR | |
| VSS | DR28 | PWR | |
| VSS | DR30 | PWR | |
| VSS | DR32 | PWR | |
| VSS | DR34 | PWR | |
| VSS | DR36 | PWR | |



Table A-1. Pin List By Name (Sheet 81 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | DR38 | PWR | |
| VSS | DR40 | PWR | |
| VSS | DR42 | PWR | |
| VSS | DR6 | PWR | |
| VSS | DR66 | PWR | |
| VSS | DR68 | PWR | |
| VSS | DR70 | PWR | |
| VSS | DR72 | PWR | |
| VSS | DR74 | PWR | |
| VSS | DR76 | PWR | |
| VSS | DR78 | PWR | |
| VSS | DT17 | PWR | |
| VSS | DT3 | PWR | |
| VSS | DT65 | PWR | |
| VSS | DT69 | PWR | |
| VSS | DT79 | PWR | |
| VSS | DT83 | PWR | |
| VSS | DT85 | PWR | |
| VSS | DU10 | PWR | |
| VSS | DU14 | PWR | |
| VSS | DU22 | PWR | |
| VSS | DU26 | PWR | |
| VSS | DU32 | PWR | |
| VSS | DU38 | PWR | |
| VSS | DU70 | PWR | |
| VSS | DU72 | PWR | |
| VSS | DU78 | PWR | |
| VSS | DU80 | PWR | |
| VSS | DU82 | PWR | |
| VSS | DU84 | PWR | |
| VSS | DV19 | PWR | |
| VSS | DV21 | PWR | |
| VSS | DV25 | PWR | |
| VSS | DV27 | PWR | |
| VSS | DV31 | PWR | |
| VSS | DV33 | PWR | |
| VSS | DV37 | PWR | |
| VSS | DV39 | PWR | |
| VSS | DV73 | PWR | |
| VSS | DV77 | PWR | |
| VSS | DV81 | PWR | |

Table A-1. Pin List By Name (Sheet 82 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | DW12 | PWR | |
| VSS | DW2 | PWR | |
| VSS | DW20 | PWR | |
| VSS | DW24 | PWR | |
| VSS | DW28 | PWR | |
| VSS | DW30 | PWR | |
| VSS | DW34 | PWR | |
| VSS | DW36 | PWR | |
| VSS | DW40 | PWR | |
| VSS | DW64 | PWR | |
| VSS | DW66 | PWR | |
| VSS | DW68 | PWR | |
| VSS | DW70 | PWR | |
| VSS | DW72 | PWR | |
| VSS | DW74 | PWR | |
| VSS | DW76 | PWR | |
| VSS | DW8 | PWR | |
| VSS | DW82 | PWR | |
| VSS | DW84 | PWR | |
| VSS | DY19 | PWR | |
| VSS | DY23 | PWR | |
| VSS | DY29 | PWR | |
| VSS | DY35 | PWR | |
| VSS | DY41 | PWR | |
| VSS | DY45 | PWR | |
| VSS | DY47 | PWR | |
| VSS | DY49 | PWR | |
| VSS | DY5 | PWR | |
| VSS | DY51 | PWR | |
| VSS | DY53 | PWR | |
| VSS | DY55 | PWR | |
| VSS | DY57 | PWR | |
| VSS | DY59 | PWR | |
| VSS | DY61 | PWR | |
| VSS | DY63 | PWR | |
| VSS | DY71 | PWR | |
| VSS | DY75 | PWR | |
| VSS | DY85 | PWR | |
| VSS | E16 | PWR | |
| VSS | E18 | PWR | |
| VSS | E20 | PWR | |



Table A-1. Pin List By Name (Sheet 83 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | E22 | PWR | |
| VSS | E6 | PWR | |
| VSS | E66 | PWR | |
| VSS | E72 | PWR | |
| VSS | E74 | PWR | |
| VSS | E76 | PWR | |
| VSS | E8 | PWR | |
| VSS | E82 | PWR | |
| VSS | EA14 | PWR | |
| VSS | EA16 | PWR | |
| VSS | EA20 | PWR | |
| VSS | EA22 | PWR | |
| VSS | EA42 | PWR | |
| VSS | EA6 | PWR | |
| VSS | EA64 | PWR | |
| VSS | EA70 | PWR | |
| VSS | EA76 | PWR | |
| VSS | EA78 | PWR | |
| VSS | EA80 | PWR | |
| VSS | EA82 | PWR | |
| VSS | EA84 | PWR | |
| VSS | EB13 | PWR | |
| VSS | EB23 | PWR | |
| VSS | EB25 | PWR | |
| VSS | EB27 | PWR | |
| VSS | EB29 | PWR | |
| VSS | EB31 | PWR | |
| VSS | EB33 | PWR | |
| VSS | EB35 | PWR | |
| VSS | EB37 | PWR | |
| VSS | EB39 | PWR | |
| VSS | EB41 | PWR | |
| VSS | EB65 | PWR | |
| VSS | EB69 | PWR | |
| VSS | EB83 | PWR | |
| VSS | EC10 | PWR | |
| VSS | EC42 | PWR | |
| VSS | EC6 | PWR | |
| VSS | EC70 | PWR | |
| VSS | EC72 | PWR | |
| VSS | EC74 | PWR | |

Table A-1. Pin List By Name (Sheet 84 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | EC76 | PWR | |
| VSS | EC82 | PWR | |
| VSS | ED11 | PWR | |
| VSS | ED15 | PWR | |
| VSS | ED23 | PWR | |
| VSS | ED29 | PWR | |
| VSS | ED35 | PWR | |
| VSS | ED41 | PWR | |
| VSS | ED69 | PWR | |
| VSS | ED7 | PWR | |
| VSS | ED77 | PWR | |
| VSS | ED81 | PWR | |
| VSS | EE24 | PWR | |
| VSS | EE28 | PWR | |
| VSS | EE30 | PWR | |
| VSS | EE34 | PWR | |
| VSS | EE36 | PWR | |
| VSS | EE40 | PWR | |
| VSS | EE70 | PWR | |
| VSS | EE76 | PWR | |
| VSS | EE78 | PWR | |
| VSS | EE8 | PWR | |
| VSS | EE80 | PWR | |
| VSS | EF71 | PWR | |
| VSS | EF75 | PWR | |
| VSS | EF79 | PWR | |
| VSS | F17 | PWR | |
| VSS | F19 | PWR | |
| VSS | F25 | PWR | |
| VSS | F31 | PWR | |
| VSS | F37 | PWR | |
| VSS | F43 | PWR | |
| VSS | F5 | PWR | |
| VSS | F67 | PWR | |
| VSS | F69 | PWR | |
| VSS | G22 | PWR | |
| VSS | G24 | PWR | |
| VSS | G26 | PWR | |
| VSS | G30 | PWR | |
| VSS | G32 | PWR | |
| VSS | G36 | PWR | |



Table A-1. Pin List By Name (Sheet 85 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | G38 | PWR | |
| VSS | G4 | PWR | |
| VSS | G42 | PWR | |
| VSS | G66 | PWR | |
| VSS | G70 | PWR | |
| VSS | G76 | PWR | |
| VSS | G78 | PWR | |
| VSS | G8 | PWR | |
| VSS | G80 | PWR | |
| VSS | G82 | PWR | |
| VSS | H11 | PWR | |
| VSS | H25 | PWR | |
| VSS | H27 | PWR | |
| VSS | H29 | PWR | |
| VSS | H3 | PWR | |
| VSS | H31 | PWR | |
| VSS | H33 | PWR | |
| VSS | H35 | PWR | |
| VSS | H37 | PWR | |
| VSS | H39 | PWR | |
| VSS | H41 | PWR | |
| VSS | H45 | PWR | |
| VSS | H47 | PWR | |
| VSS | H49 | PWR | |
| VSS | H51 | PWR | |
| VSS | H53 | PWR | |
| VSS | H55 | PWR | |
| VSS | H57 | PWR | |
| VSS | H59 | PWR | |
| VSS | H61 | PWR | |
| VSS | H63 | PWR | |
| VSS | H65 | PWR | |
| VSS | H71 | PWR | |
| VSS | H75 | PWR | |
| VSS | J12 | PWR | |
| VSS | J14 | PWR | |
| VSS | J16 | PWR | |
| VSS | J22 | PWR | |
| VSS | J26 | PWR | |
| VSS | J28 | PWR | |
| VSS | J32 | PWR | |

Table A-1. Pin List By Name (Sheet 86 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | J34 | PWR | |
| VSS | J38 | PWR | |
| VSS | J4 | PWR | |
| VSS | J40 | PWR | |
| VSS | J72 | PWR | |
| VSS | J74 | PWR | |
| VSS | J76 | PWR | |
| VSS | J82 | PWR | |
| VSS | J84 | PWR | |
| VSS | J86 | PWR | |
| VSS | K1 | PWR | |
| VSS | K11 | PWR | |
| VSS | K13 | PWR | |
| VSS | K17 | PWR | |
| VSS | K27 | PWR | |
| VSS | K33 | PWR | |
| VSS | K39 | PWR | |
| VSS | K65 | PWR | |
| VSS | K67 | PWR | |
| VSS | K69 | PWR | |
| VSS | K71 | PWR | |
| VSS | K73 | PWR | |
| VSS | K77 | PWR | |
| VSS | K81 | PWR | |
| VSS | K83 | PWR | |
| VSS | K85 | PWR | |
| VSS | L10 | PWR | |
| VSS | L2 | PWR | |
| VSS | L20 | PWR | |
| VSS | L22 | PWR | |
| VSS | L6 | PWR | |
| VSS | L72 | PWR | |
| VSS | L78 | PWR | |
| VSS | L8 | PWR | |
| VSS | L80 | PWR | |
| VSS | L82 | PWR | |
| VSS | M15 | PWR | |
| VSS | M17 | PWR | |
| VSS | M19 | PWR | |
| VSS | M23 | PWR | |
| VSS | M25 | PWR | |



Table A-1. Pin List By Name (Sheet 87 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | M27 | PWR | |
| VSS | M29 | PWR | |
| VSS | M31 | PWR | |
| VSS | M33 | PWR | |
| VSS | M35 | PWR | |
| VSS | M37 | PWR | |
| VSS | M39 | PWR | |
| VSS | M41 | PWR | |
| VSS | M43 | PWR | |
| VSS | M65 | PWR | |
| VSS | M71 | PWR | |
| VSS | M79 | PWR | |
| VSS | M83 | PWR | |
| VSS | M85 | PWR | |
| VSS | N20 | PWR | |
| VSS | N22 | PWR | |
| VSS | N4 | PWR | |
| VSS | N6 | PWR | |
| VSS | N66 | PWR | |
| VSS | N70 | PWR | |
| VSS | N72 | PWR | |
| VSS | N74 | PWR | |
| VSS | N76 | PWR | |
| VSS | N78 | PWR | |
| VSS | N8 | PWR | |
| VSS | P11 | PWR | |
| VSS | P15 | PWR | |
| VSS | P27 | PWR | |
| VSS | P33 | PWR | |
| VSS | P39 | PWR | |
| VSS | P45 | PWR | |
| VSS | P47 | PWR | |
| VSS | P49 | PWR | |
| VSS | P51 | PWR | |
| VSS | P53 | PWR | |
| VSS | P55 | PWR | |
| VSS | P57 | PWR | |
| VSS | P59 | PWR | |
| VSS | P61 | PWR | |
| VSS | P63 | PWR | |
| VSS | P67 | PWR | |

Table A-1. Pin List By Name (Sheet 88 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | P69 | PWR | |
| VSS | P71 | PWR | |
| VSS | P81 | PWR | |
| VSS | P83 | PWR | |
| VSS | R14 | PWR | |
| VSS | R18 | PWR | |
| VSS | R2 | PWR | |
| VSS | R22 | PWR | |
| VSS | R26 | PWR | |
| VSS | R28 | PWR | |
| VSS | R32 | PWR | |
| VSS | R34 | PWR | |
| VSS | R38 | PWR | |
| VSS | R4 | PWR | |
| VSS | R40 | PWR | |
| VSS | R68 | PWR | |
| VSS | R72 | PWR | |
| VSS | R78 | PWR | |
| VSS | R86 | PWR | |
| VSS | T13 | PWR | |
| VSS | T17 | PWR | |
| VSS | T25 | PWR | |
| VSS | T29 | PWR | |
| VSS | T31 | PWR | |
| VSS | T35 | PWR | |
| VSS | T37 | PWR | |
| VSS | T41 | PWR | |
| VSS | T65 | PWR | |
| VSS | T73 | PWR | |
| VSS | T77 | PWR | |
| VSS | T83 | PWR | |
| VSS | T85 | PWR | |
| VSS | U2 | PWR | |
| VSS | U20 | PWR | |
| VSS | U22 | PWR | |
| VSS | U24 | PWR | |
| VSS | U30 | PWR | |
| VSS | U36 | PWR | |
| VSS | U4 | PWR | |
| VSS | U42 | PWR | |
| VSS | U6 | PWR | |

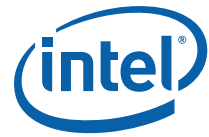


Table A-1. Pin List By Name (Sheet 89 of 90)

| Pin Name | Location | Type | I/O |
|----------|----------|------|-----|
| VSS | U68 | PWR | |
| VSS | U70 | PWR | |
| VSS | U74 | PWR | |
| VSS | U76 | PWR | |
| VSS | U78 | PWR | |
| VSS | U80 | PWR | |
| VSS | U86 | PWR | |
| VSS | V1 | PWR | |
| VSS | V11 | PWR | |
| VSS | V13 | PWR | |
| VSS | V15 | PWR | |
| VSS | V21 | PWR | |
| VSS | V23 | PWR | |
| VSS | V43 | PWR | |
| VSS | V5 | PWR | |
| VSS | V73 | PWR | |
| VSS | V75 | PWR | |
| VSS | V77 | PWR | |
| VSS | V83 | PWR | |
| VSS | V9 | PWR | |
| VSS | W12 | PWR | |
| VSS | W22 | PWR | |
| VSS | W24 | PWR | |
| VSS | W26 | PWR | |
| VSS | W28 | PWR | |
| VSS | W30 | PWR | |
| VSS | W32 | PWR | |
| VSS | W34 | PWR | |
| VSS | W36 | PWR | |
| VSS | W38 | PWR | |
| VSS | W40 | PWR | |
| VSS | W42 | PWR | |
| VSS | W68 | PWR | |
| VSS | W74 | PWR | |
| VSS | W78 | PWR | |
| VSS | W8 | PWR | |
| VSS | W82 | PWR | |
| VSS | Y15 | PWR | |
| VSS | Y17 | PWR | |
| VSS | Y5 | PWR | |
| VSS | Y67 | PWR | |

Table A-1. Pin List By Name (Sheet 90 of 90)

| Pin Name | Location | Type | I/O |
|-----------------|----------|------|-----|
| VSS | Y7 | PWR | |
| VSS | Y71 | PWR | |
| VSS | Y73 | PWR | |
| VSS | Y79 | PWR | |
| VSS | Y81 | PWR | |
| VSS | Y83 | PWR | |
| VSS | Y85 | PWR | |
| VSS | Y9 | PWR | |
| VSS_VCCIN_SENSE | AY85 | PWR | |
| VSS_VCCIO_SENSE | BF5 | PWR | |
| VSS_VCCSA_SENSE | CG76 | PWR | |
| | | | |



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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru