SX1250

Multi-band Sub-GHz RF Front End

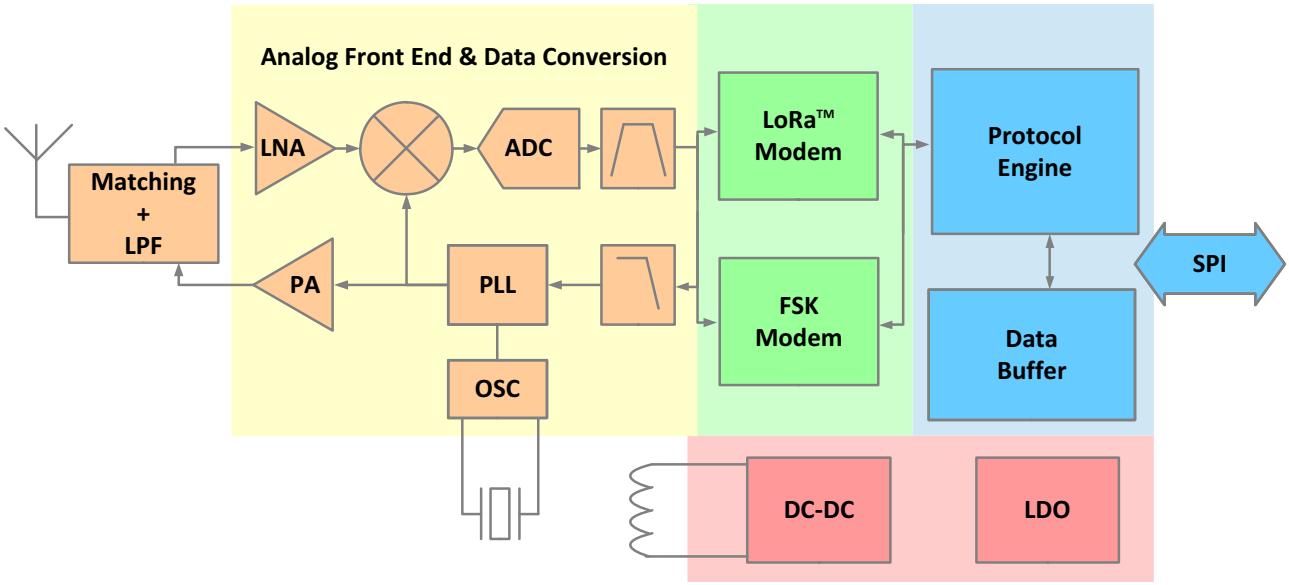

Figure A: SX1250 Block Diagram

General Description

The SX1250 is a sub-GHz RF Front End device designed to work along with Semtech's SX1302 baseband engine, to design a high-performing LoRa® or LoRaWAN gateway.

It covers any frequency band below 1 GHz, making it the perfect candidate to support any license-free band used in today's IOT use cases.

The device supports up to +22 dBm output power on-chip. This embedded high-power capability can be leveraged to reduce the bill of material cost when designing a gateway. As far as receiver, the Noise Figure of the system is also extremely low, eliminating the need for an external high-end and power-consuming Low Noise amplifier, if the goal is to come up with a cheaper and median-spec gateway.

Applications

- LoRa® and LoRaWAN gateways

Regional Support

- Europe 868 MHz
- India 866 MHz
- North America 915 MHz
- APAC 920 MHz
- Asia 923 MHz
- Lower UHF bands 169 and 433 or 490 MHz

Ordering Information

Part Number	Delivery	Minimum Order Quantity
SX1250IMLTRT	Tape & Reel	3'000 pieces

QFN 24 Package, Pb-free, Halogen free, RoHS/WEEE compliant product

Revision History

Version	ECO	Date	Modifications
1.0	ECO-047284	June 2019	First Internal Release
1.1	ECO-047548	July 2019	First External Release

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1. Architecture

The SX1250 is a half-duplex RF to IQ transceiver capable of low power operation in the 150-960 MHz ISM frequency bands. The radio comprises four main blocks:

1. **Analog Front End**: the transmit and receive chains, as well as the data converter interface to ensuing digital blocks. The SX1250 transceiver is capable of delivering up to +22 dBm under the battery supply. Details on both the transmit and receive parts of the chips are given in Section 4. "Analog Circuit Description" on page 14
2. **Baseband Interface:** after down-conversion and digitization, I/Q samples are made available to the companion baseband chip, over a 32 MHz digital interface, described in Section 5. "Baseband Interface" on page 18
3. **Control interface:** the SX1250 transceiver is typically controlled by its companion baseband chip, through a UART or SPI interface. Details are found in Section 6. "Control Interface" on page 19

2. Pin Connection

2.1 I/O Description

Table 2-1: SX1250 Pinout in QFN 4x4 24L

Pin Number	Pin Name	Type (I = input O = Output)	Description
0	GND	-	Exposed Ground pad
1	VR_PA	-	Regulated power amplifier supply
2	VDD_IN	I	Input voltage for power amplifier regulator, VR_PA connected to pin 1
3	XTA	-	Crystal oscillator connection, can be used to input external reference clock
4	XTB	-	Crystal oscillator connection
5	DIO3	I/O	Multi-purpose digital IO
6	VREG	O	Regulated output voltage from the internal regulator LDO / DC-DC
7	GND	-	Ground
8	DCC_SW	O	DC-DC Switcher Output
9	VBAT_RF	I	Supply for the RFIC
10	VBAT_DIO	I	Supply for the Digital I/O interface pins (except DIO3) Supply for the RFIC
11	DIO5	I/O	Multi-purpose digital IO
12	DIO2	I/O	Multi-purpose digital I/O / RF Switch control
13	DIO1	I/O	Multi-purpose digital IO
14	BUSY	O	Busy indicator
15	NRESET	I	Reset signal, active low
16	MISO	O	SPI slave output
17	MOSI	I	SPI slave input
18	SCK	I	SPI clock
19	NSS	I	SPI Slave Select
20	GND	-	Ground
21	DIO4	I/O	Multi-purpose digital IO
22	RFI_P	I	RF receiver input
23	RFI_N	I	RF receiver input
24	RFO	O	RF transmitter output

2.2 Package View

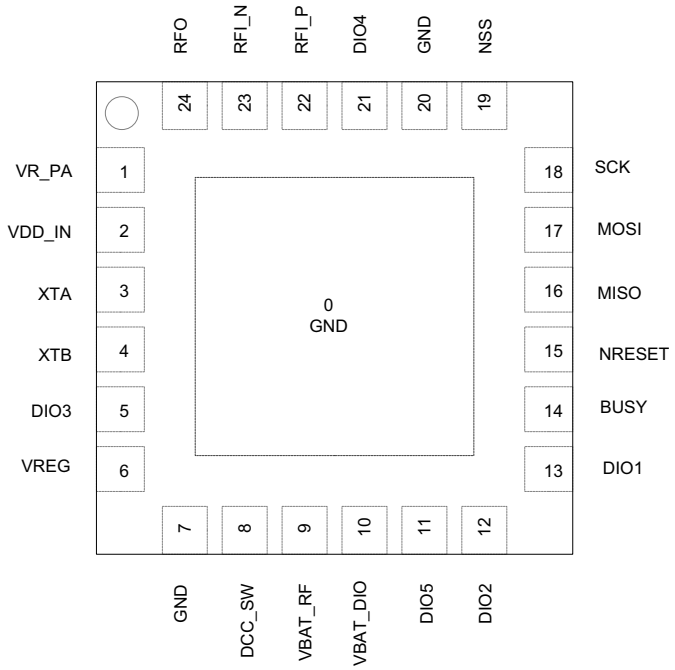


Figure 2-1: SX1250 Top View Pin Location QFN 4x4 24L

3. Specifications

3.1 ESD Notice

The SX1250 transceiver is a high-performance radio frequency device, with high ESD and latch-up resistance. The chip should be handled with all the necessary ESD precautions to avoid any permanent damage.

Table 3-1: ESD and Latch-up Notice

Symbol	Description	Min	Typ	Max	Unit
ESD_HBM	Class 2 of ANSI/ESDA/JEDEC Standard JS-001-2014 (Human Body Model)	-	-	2.0	kV
ESD_CDM	ESD Charged Device Model, JEDEC standard JESD22-C101D, class III	-	-	1000	V
LU	Latch-up, JEDEC standard JESD78 B, class I level A	-	-	100	mA

3.2 Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability, reducing product life time.

Table 3-2: Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
VDDmr	Supply voltage, applies to VBAT_RF and VBAT_DIO	-0.5	-	3.9	V
Tmr	Temperature	-55	-	125	°C
Pmr	RF Input level	-	-	10	dBm

3.3 Operating Range

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not guaranteed.

Table 3-3: Operating Range

Symbol	Description	Min	Typ	Max	Unit
VDDop	Supply voltage, applies to VBAT_RF and VBAT_DIO	3	-	3.6	V
Top	Temperature under bias	-40	-	85	°C
Clop	Load capacitance on digital ports	-	-	20	pF
ML	RF Input power	-	-	0	dBm
VSWR	Voltage Standing Wave Ratio	-	-	10:1	-

3.4 Crystal Specifications

Table 3-4: Crystal Specifications

Symbol	Description	Min	Typ	Max	Unit
FXOSC	Crystal oscillator frequency	-	32	-	MHz
CLOAD	Crystal load capacitance	-	10	-	pF
C0XTAL	Crystal shunt capacitance	0.3	0.6	2	pF
RSXTAL	Crystal series resistance	-	30	60	Ω
CMXTAL	Crystal motional capacitance	1.3	1.89	2.5	fF
DRIVE	Drive level	-	-	100	µW

Although the SX1250 can support XTAL based operation, in most applications a TCXO will be used in conjunction with this RF Front End device. For details on the TCXO operation, please see Section 4.1 "Clock References" on page 14.

3.5 Electrical Specifications

The electrical specifications are given with the following conditions unless otherwise specified:

- VBAT_DIO = VBAT_RF = 3.3 V, all current consumptions are given for VBAT_RF connected to VBAT_DIO
- Temperature = 25 °C
- FXOSC = 32 MHz
- FRF = 434/490/868/915 MHz
- All RF impedances matched
- Transmit mode output power defined in 50 Ω load
- RX/TX specifications given using default RX gain step and direct tie connection between Rx and Tx
- TCXO and RF Switch power consumption always excluded

Caution!

Throughout this document, all receiver bandwidths are expressed as “double-sided bandwidth”.

3.5.1 Power Consumption

Table 3-5: Power Consumption

Symbol	Mode	Conditions	Min	Typ	Max	Unit
IDDOFF	OFF mode	All blocks off	-	160	-	nA
IDDSL	SLEEP mode	Configuration retained	-	600	-	nA
		Configuration retained + RC64k	-	1.2	-	µA
IDDRX	Receive mode	Built-in DC-DC used	-	4.2	-	mA
	Receive mode	Built-in LDO used	-	8	-	mA

Table 3-6: Power Consumption in Transmit Mode

Symbol	Frequency Band	PA Match / Condition	Power Output	Typical	Unit
IDDTX	868/915 MHz	+22 dBm	+22 dBm	118	mA
			+20 dBm	102	mA
			+17 dBm	95	mA
			+14 dBm	90	mA
	434/490 MHz	+22 dBm	+22 dBm	107	mA
			+20 dBm	90	mA
			+17 dBm	75	mA
			+14 dBm	63	mA

3.5.2 General Specifications

Table 3-7: General Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer frequency range		150	-	960	MHz
FSTEP	Synthesizer frequency step	-	-	0.95	-	Hz
PHN	Synthesizer phase noise	1 kHz offset	-	-75	-	dBc/Hz
		10 kHz offset	-	-95	-	dBc/Hz
		100 kHz offset	-	-100	-	dBc/Hz
		1MHz offset	-	-120	-	dBc/Hz
		10 MHz offset	-	-135	-	dBc/Hz
TS_OSC	Crystal oscillator wake-up time	from STDBY_RC[1]	-	150	-	µs
VTCXO	Regulated voltage range for TCXO voltage supply	Min/Max values in typical conditions, Typ value for default setting VDDop > VTCXO + 200 mV	1.6	1.7	3.3	V

Table 3-7: General Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
ILTCXO	Load current for TCXO regulator		-	1.5	4	mA
TSVTCXO	Start-up time for TCXO regulator	From enable to regulated voltage within 25 mV from target	-	-	100	µs
IDDTCXO	Current consumption of the TCXO regulator	Quiescent current Relative to load current	- -	- 1	70 2	µA %
ATCXO	Amplitude voltage for external TCXO applied to XTA pin	provided through a 220 Ω resistor in series with a 10 pF capacitance See Section 4.1 "Clock References" on page 14	0.4	0.6	1.2	Vpk-pk

1. Wake-up time till crystal oscillator frequency is within +/- 10 ppm

3.5.3 Receive Mode Specifications

Table 3-8: Receive Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
IIP3	Input IP3	Maximum gain In-band Unwanted tones are 1 MHz and 1.96 MHz above LO	-	-5	-	dBm
IMA	Image attenuation	With IQ calibration	-	54	-	dB
BW_F	Receiver BW		-	-	500	kHz
TS_RX	Receiver wake-up time	FS to RX	-	41	-	µs

3.5.4 Transmit Mode Specifications

Table 3-9: Transmit Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
TXOP	Maximum RF output power	22 dBm setting	-	+22	-	dBm
TXPRNG	RF output power range	Programmable in 31 steps, typical value	TXOP-31	-	TXOP	dBm
TXACC	RF output power step accuracy		-	± 2	-	dB
TXRMP	Power amplifier ramping time	Programmable	10	-	3400	µs
TS_TX	Tx wake-up time	Frequency Synthesizer enabled	-	36 + PA ramping	-	µs

3.5.5 Digital I/O Specifications

Table 3-10: Digital I/O Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
VIH	Input High Voltage	-	0.7*VBAT_DIO [1]	-	VBAT_DIO [1]+0.3	V
VIL	Input Low Voltage	-	-0.3	-	0.3*VBAT_DIO [1]	V
VIL_N	Input Low Voltage for pin NRESET	-	-0.3	-	0.2*VBAT_RF	V
VOH	Output High Voltage	I_{max} = -2.5 mA	0.9*VBAT_DIO [1]	-	VBAT_DIO [1]	V
VOL	Output Low Voltage	I_{max} = 2.5 mA	0	-	0.1*VBAT_DIO [1]	V
Ileak	Digital input leakage current (NSS, MOSI, SCK)	-	-1	-	1	µA

1. excluding following pins: NRESET and DIO3, which are referred to VBAT_RF

4. Analog Circuit Description

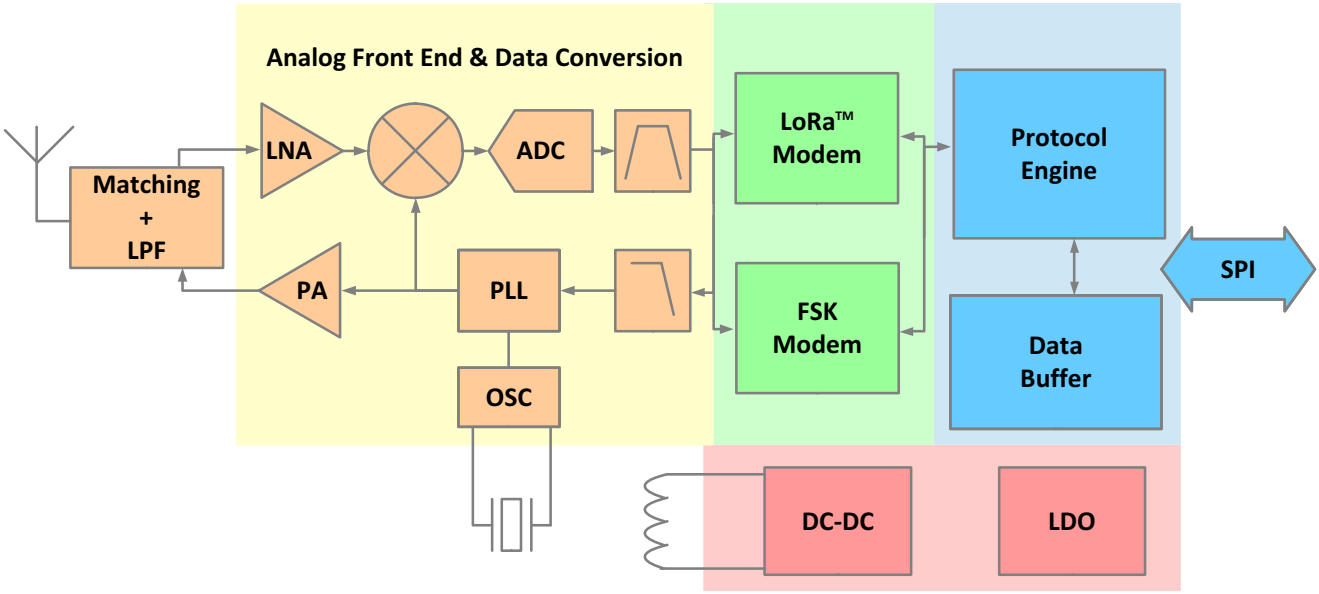


Figure 4-1: SX1250 Block Diagram

SX1250 is a half-duplex RF front-end device operating in the sub-GHz frequency bands and can handle constant envelope modulations schemes such as LoRa® or FSK.

4.1 Clock References

In gateway implementations, where the BOM cost is less sensitive, it is required to use a TCXO (Temperature Compensated Crystal Oscillator) to achieve better frequency accuracy.

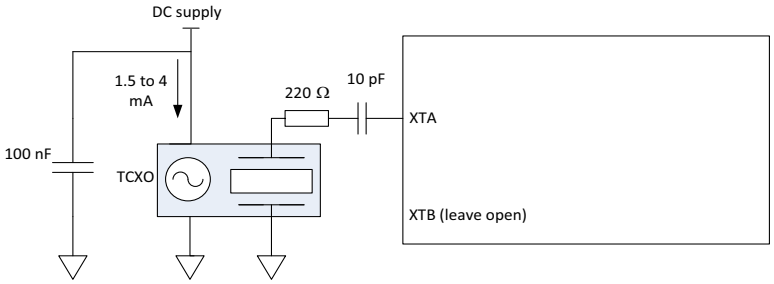


Figure 4-2: TCXO Connection

When a TCXO is used, it should be connected to pin 3 XTA, through a 220 Ω resistor and a10 pF DC-cut capacitor. Pin 4 XTB should be left open. Clipped-sine output TCXO are required, with the output amplitude not exceeding 1.2 V peak-to-peak.

4.2 Receiver

The SX1250 offers a built-in differential Low Noise Amplifier (LNA), for the benefit of common mode rejection and immunity against noise and interferers. The L-C network in front of the differential inputs serves both functions of a balun to convert the single-ended to differential signals and impedance transformation.

The optimal source impedance is the LNA is 74 + j134 Ohms at maximum gain, and the typical balun and Z-match circuit for both 868 MHz and 915 MHz operation is shown in Figure 4-3, when connectiong two SX1250, Figure 4-4 is relevant.

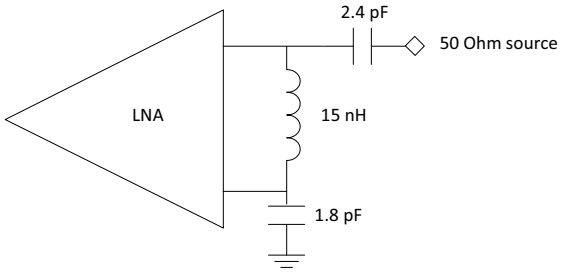


Figure 4-3: Single 868-915 MHz LNA Matching

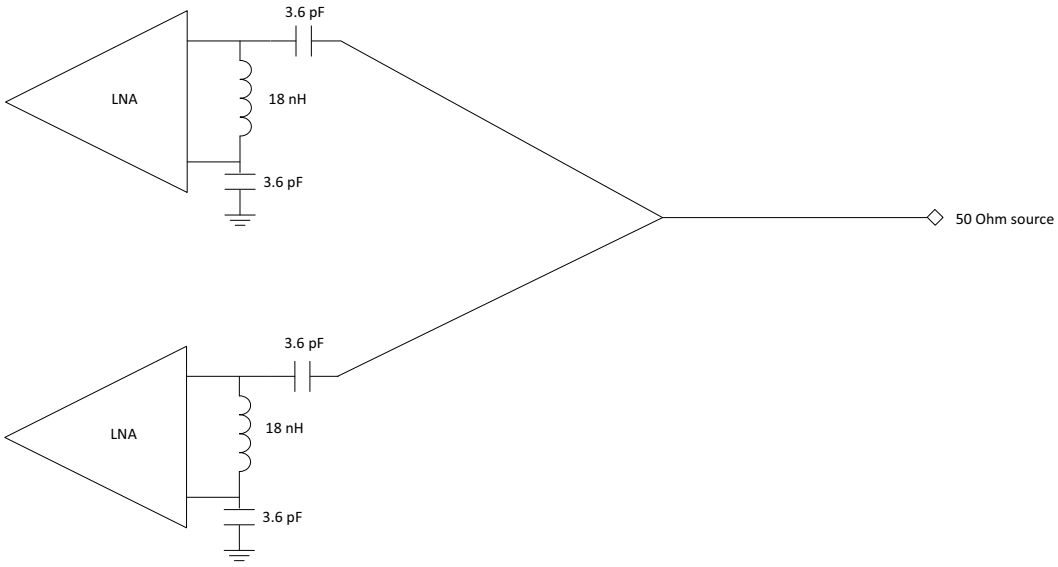


Figure 4-4: Dual 868-915 MHz LNA Matching

4.3 Transmitter

The default maximum RF output power of the transmitter is +22 dBm. The RF output power is programmable with 32 dB of dynamic range, in 1 dB steps. The power amplifier ramping time is also programmable to meet regulatory requirements.

The power amplifier is supplied by the regulator VR_PA and the connection between VR_PA and RFO is done externally to the chip. As illustrated in Figure 4-5: PA Supply Scheme,VR_PA is supplied through VDD_IN, taken directly from the battery or low-noise power supply, and in this case maximum output power is limited by supply voltage at VDD_IN.

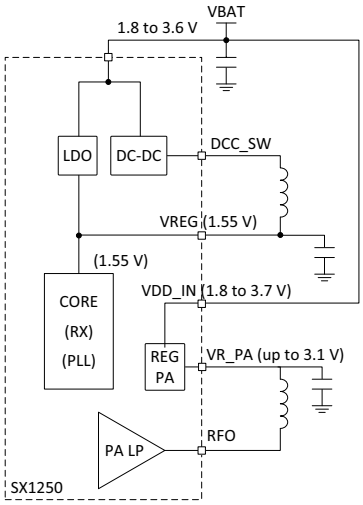


Figure 4-5: PA Supply Scheme

The following table summarizes the power amplifier optimization keys in the SX1250 transceiver:

Table 4-1: Power Amplifier Summary

PA Summary	Conditions	SX1250
Max Power	with relevant matching and settings	+ 22 dBm
IDDTX	at + 22 dBm, indicative at + 14 dBm, indicative	118 mA 90 mA
Output Power vs VBAT_RF		flat from 3.3 V to 3.6 V

The Power Amplifier impedance matching is highlighted below, and proper values, inherited from the SX1262 reference design, can be found on all our gateway reference designs:

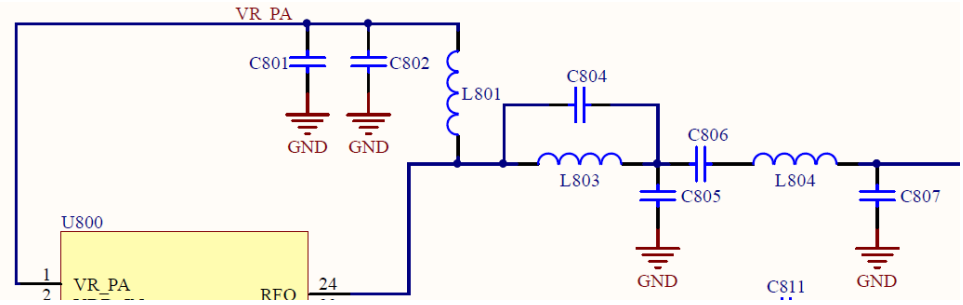


Figure 4-6: Power Amplifier Matching

4.4 Consideration on the DC-DC Inductor Selection

The selection of the inductor is essential to ensure optimal performance of the DC-DC internal block. Selecting an incorrect inductor could cause various unwanted effects ranging from ripple currents to early aging of the device, as well as a degradation of the efficiency of the DC-DC regulator.

For the SX1250, the preferred inductor will be shielded, presenting a low internal series resistance and a resonance frequency much higher than the DC-DC switching frequency. When selecting the 15 µH inductor, the user should therefore select a part with the following considerations:

- DCR (max) = 2 ohms
- Idc (min) = 100 mA
- Freq (min) = 20 MHz

Table 4-2: Typical 15 µH Inductors

Reference	Manufacturer	Value (µH)	Idc max (mA)	Freq (MHz)	DCR (ohm)	Package (L x W x H in mm)
LPS3010-153	Coilcraft	15	370	43	0.95	2.95 x 2.95 x 0.9
MLZ2012N150L	TDK	15	90	40	0.47	2 x 1.25 x 1.25
MLZ2012M150W	TDK	15	120	40	0.95	2 x 1.25 x 1.25
VLS2010ET-150M	TDK	15	440	40	1.476	2 x 2 x 1
VLS2012ET-150M	TDK	15	440	40	1.062	2 x 2 x 1.2

4.5 Flexible DIO Supply

The front-end has two power supply pins, one for the core of the transceiver called VBAT_RF and one for the host controller interface (SPI, DIOs, BUSY) called VBAT_DIO. Both power supplies can be connected together in application, but the user also can:

- use VBAT_RF at 3.3 V or higher for optimal RF performance
- directly connect VBAT_DIO to the same supply used for the micro-controller
- connect the digital IOs directly to the micro-controller DIOs.

At any time, VBAT_DIO must be lower than or equal to VBAT_RF.

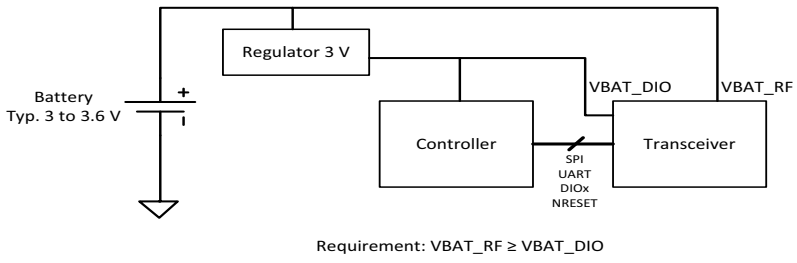


Figure 4-7: Separate DIO Supply

5. Baseband Interface

The SX1250 interfaces to, typically, the SX1302 chip, over proprietary interfaces. They are described in the following table:

Table 5-1: Baseband Interface Description

<table>
<tr><th>Pin name</th><th>SPI Control (slave)[1]</th><th>RF Rx mode</th><th>RF Tx mode</th></tr>
<tr><td>BUSY</td><td>BUSY indicator</td><td colspan="2">32 MHz system clout (output)</td></tr>
<tr><td>DIO1</td><td rowspan="5">Unused</td><td rowspan="3">I(t) digitized over 2 bits</td><td rowspan="5">PLL's Sigma-delta modulator input (over 5 bits)</td></tr>
<tr><td>DIO2</td></tr>
<tr><td>DIO3</td></tr>
<tr><td>DIO4</td><td rowspan="2">Q(t) digitized over 2 bits</td></tr>
<tr><td>DIO5</td><td rowspan="3">Proprietary dynamic RF gain control interface[2]</td></tr>
<tr><td>MISO</td><td>Slave Out</td><td>Sigma-delta clock sync (input)</td></tr>
<tr><td>MOSI</td><td>Slave In</td><td>-</td></tr>
<tr><td>SCK</td><td>SPI clock</td><td>-</td></tr>
<tr><td>NSS</td><td>Slave Select</td><td>-</td><td>-</td></tr>
</table>

1. SPI control mode overrides Rx or Tx mode, and the corresponding pins change function on-the-go when NSS toggles low.
2. The "Proprietary dynamic RF gain control interface" is designed to dynamically handle large signal variations. It consists of a clock (BUSY), a word-type synchronization (DIO5), and 3 data lines (MISO, MOSI and SCK).

6. Control Interface

The SX1250 is controlled via a serial SPI interface and a set of general purpose input/output (DIOs). At least one DIO must be used for IRQ and the BUSY line is mandatory to ensure the host controller is ready to accept the commands. The SX1250 uses an internal controller (CPU) to handle communication and chip control (mode switching, API etc...). BUSY is used as a busy signal indicating that the chip is ready for new command only if this signal is low. When BUSY is high, the host controller must wait until it goes down again before sending another command. Through SPI the application sends commands to the internal chip or access directly the data memory space.

6.1 Reset

A complete "factory reset" of the chip can be issued on request by toggling pin 15 NRESET of the SX1250. It will be automatically followed by the standard calibration procedure and any previous context will be lost. The pin should be held low for more than 50 µs (typically 100 µs) for the Reset to happen.

6.2 SPI Interface

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

An address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the beginning of the frame and goes high after the data byte.

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.

A transfer is always started by the NSS pin going low. MISO is high impedance when NSS is high.

The SPI runs on the external SCK clock to allow high speed up to 16 MHz.

6.2.1 SPI Timing When the Transceiver is in Active Mode

In this mode the chip is able to handle SPI command in a standard way i.e. no extra delay needed at the first SPI transaction.

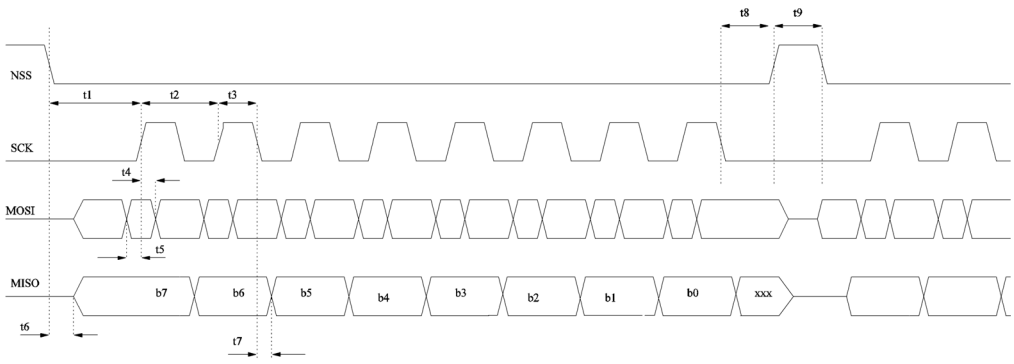


Figure 6-1: SPI Timing Diagram

All timings in following table are given for a max load cap of 10 pF.

Table 6-1: SPI Timing Requirements

Symbol	Description	Minimum	Typical	Maximum	Unit
t1	NSS falling edge to SCK setup time	32	-	-	ns
t2	SCK period	62.5	-	-	ns
t3	SCK high time	31.25	-	-	ns
t4	MOSI to SCK hold time	5	-	-	ns
t5	MOSI to SCK setup time	5	-	-	ns
t6	NSS falling to MISO delay	0	-	15	ns
t7	SCK falling to MISO delay,	0	-	15	ns
t8	SCK to NSS rising edge hold time	31.25	-	-	ns
t9	NSS high time	125	-	-	ns
t10	NSS falling edge to SCK setup time when switching from SLEEP to STDBY_RC mode	100	-	-	µs
t11	NSS falling to MISO delay when switching from SLEEP to STDBY_RC mode	0	-	150	µs

7. Host Controller Interface

Semtech has optimized the complete reference design, made of SX1250 and SX1302, and is providing a complete Hardware Abstraction Layer (HAL), self-contained, to operate a gateway. On top of the HAL, an example application using the transceiver is also posted, it is named “Packet Forwarder”.

HAL and Packet Forwarder should be used as they are, and packaged in a larger library including a rich feature set required in an industrial gateway, such as capability to upgrade remotely, or establish a secured link to a server.

Official libraries are released for public use under a revised BSD license, and can be found on our “LoRa-net” Github repository, available at https://github.com/Lora-net.

8. Application

A typical use of the SX1250 in a gateway application is proposed below.

8.1 Application Schematics

8.1.1 Corecell Design

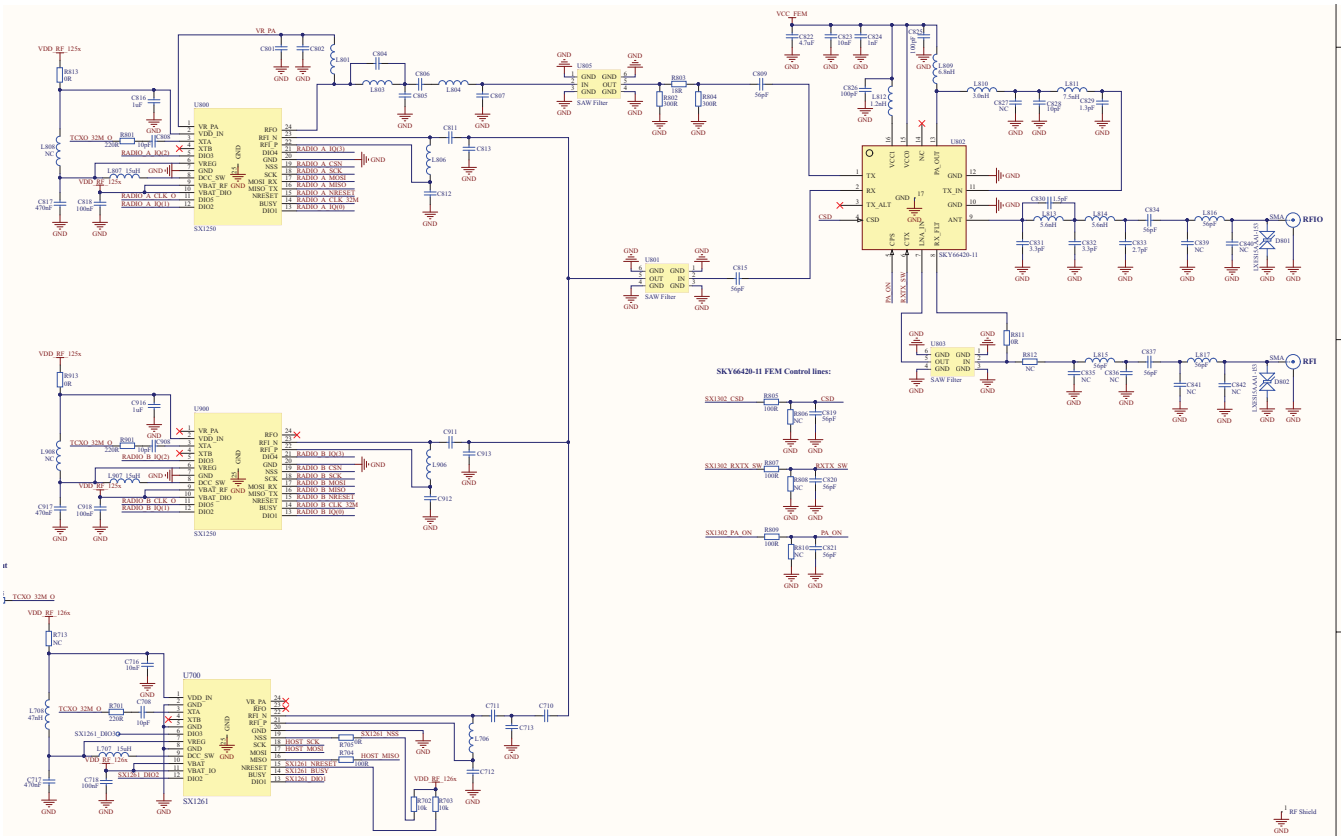
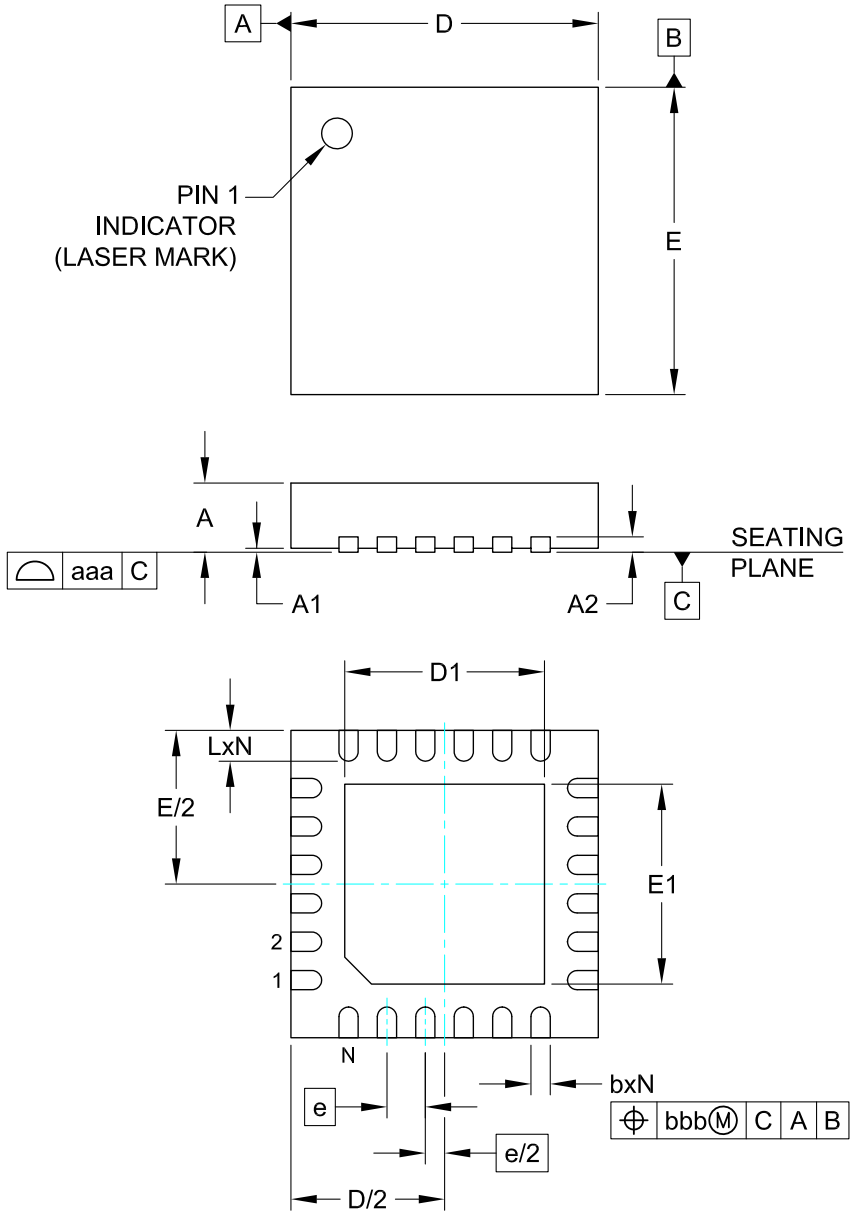


Figure 8-1: Corecell Design Extract

9. Packaging Information

9.1 Package Outline Drawing

The transceiver is delivered in a 4x4mm QFN package with 0.5 mm pitch:



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		(0.20)	
b	0.18	0.23	0.30
D	3.90	4.00	4.10
D1	2.55	2.60	2.65
E	3.90	4.00	4.10
E1	2.55	2.60	2.65
e		0.50 BSC	
L	0.35	0.40	0.45
N		24	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 9-1: QFN 4x4 Package Outline Drawing

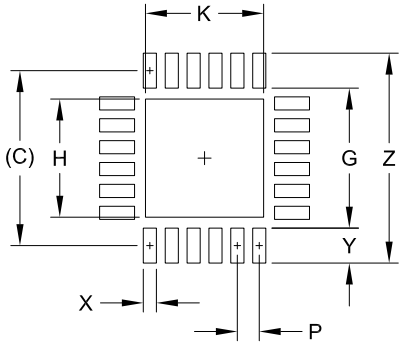
9.2 Package Marking

Marking for the 4 x 4mm MLPQ 24 Lead package:
nnnn = Part Number (Example: 1250)
yyww = Date Code (1952)
xxxxx = Semtech Lot No. (Example: E9010)

Figure 9-2: SX1250 Marking

9.3 Land Pattern

The recommended land pattern is as follows:



DIMENSIONS	
DIM	MILLIMETERS
C	(4.00)
G	3.20
H	2.70
K	2.70
P	0.50
X	0.30
Y	0.80
Z	4.80

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSE ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

Figure 9-3: QFN 4x4mm Land Pattern

9.4 Reflow Profiles

Reflow process instructions are available from the Semtech website, at the following address:

http://www.semtech.com/quality/ir_reflow_profiles.html This transceiver uses a QFN24 4x4 mm package, also named MLP package.

Glossary

List of Acronyms and their Meaning

Acronym	Meaning
ACR	Adjacent Channel Rejection
ADC	Analog-to-Digital Converter
API	Application Programming Interface
β	Modulation Index
BER	Bit Error Rate
BR	Bit Rate
BT	Bandwidth-Time bit period product
BW	BandWidth
CAD	Channel Activity Detection
CPOL	Clock Polarity
CPHA	Clock Phase
CR	Coding Rate
CRC	Cyclical Redundancy Check
CW	Continuous Wave
DIO	Digital Input / Output
DSB	Double Side Band
ECO	Engineering Change Order
FDA	Frequency Deviation
FEC	Forward Error Correction
FIFO	First In First Out
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
GDPW	Gross Die Per Wafer
IF	Intermediate Frequencies
IRQ	Interrupt Request
ISM	Industrial, Scientific and Medical (radio spectrum)
LDO	Low-Dropout
LDRO	Low Data Rate Optimization

List of Acronyms and their Meaning

Acronym	Meaning
LFSR	Linear-Feedback Shift Register
LNA	Low-Noise Amplifier
LO	Local Oscillator
LoRa®	Long Range Communication *the LoRa® Mark is a registered trademark of the Semtech Corporation*
LSB	Least Significant Bit
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSB	Most Significant Bit
MSK	Minimum-Shift Keying
NOP	No Operation (0x00)
NRZ	Non-Return-to-Zero
NSS	Slave Select active low
OCP	Over Current Protection
PA	Power Amplifier
PER	Packet Error Rate
PHY	Physical Layer
PID	Product Identification
PLL	Phase-Locked Loop
POR	Power On Reset
RC13M	13 MHz Resistance-Capacitance Oscillator
RC64k	64 kHz Resistance-Capacitance Oscillator
RFO	Radio Frequency Output
RFU	Reserved for Future Use
RTC	Real-Time Clock
SCK	Serial Clock
SF	Spreading Factor
SN	Sequence Number
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SSB	Single Side Bandwidth
STDBY	Standby

List of Acronyms and their Meaning

Acronym	Meaning
TCXO	Temperature-Compensated Crystal Oscillator
XOSC	Crystal Oscillator

Important Notice

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