



**Is Now Part of**



**ON Semiconductor®**

**To learn more about ON Semiconductor, please visit our website at**  
**[www.onsemi.com](http://www.onsemi.com)**

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (\_), the underscore (\_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (\_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at [www.onsemi.com](http://www.onsemi.com). Please email any questions regarding the system integration to [Fairchild\\_questions@onsemi.com](mailto:Fairchild_questions@onsemi.com).

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



# FAN9672

## Two-Channel Interleaved CCM PFC Controller

### Features

- Continuous Conduction Mode Control
- Two-Channel PFC Control (Maximum)
- Average Current-Mode Control
- PFC Slave Channel Management Function
- Programmable Operation Frequency Range: 18 kHz~40 kHz or 55 kHz~75 kHz
- Programmable PFC Output Voltage
- Two Current-Limit Functions
- TriFault Detect™ Protects Against Feedback Loop Failure
- SAG Protection
- Programmable Soft-Start
- Under-Voltage Lockout (UVLO)
- Differential Current Sensing
- Available in 32-Pin LQFP Package

### Applications

- High-Power AC-DC Power Supply
- DC Motor Power Supply
- White Goods; e.g. Air Conditioner Power Supply
- Server and Telecom Power Supply
- UPS
- Industrial Welding and Power Supply

### Description

The FAN9672 is an interleaved two-channel Continuous Conduction Mode (CCM) Power Factor Correction (PFC) controller IC intended for PFC pre-regulators. Incorporating circuits for leading edge, average current, and “boost”-type power factor correction; the FAN9672 enables the design of a power supply that fully complies with the IEC1000-3-2 specification. Interleaved operation provides substantial reduction in the input and output ripple currents and the conducted EMI filtering becomes simpler and cost effective.

An innovative channel-management function allows the power level of the slave channels to be loaded and unloaded smoothly according to the setting voltage on the CM pin, improving the PFC converter's load transient response.

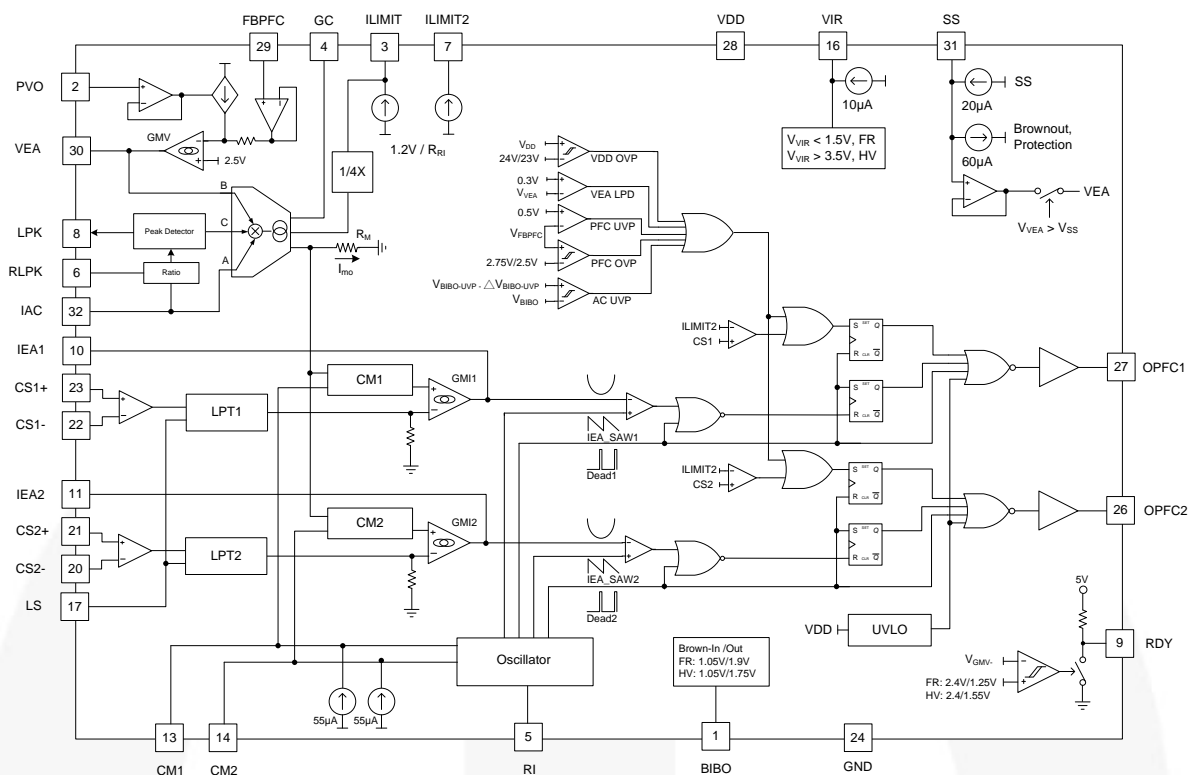
The FAN9672 also incorporates a variety of protection functions, including: peak current limiting, input voltage brownout protection, and TriFault Detect™ function.

### Ordering Information

| Part Number | Operating Temperature Range | Package   | Packing Method |
|-------------|-----------------------------|---|----------------|
| FAN9672Q    | -40°C to 105°C              | 32-Lead, Low Quad Flat Package (LQFP), JEDEC MS-026, Variation BBA, 7 mm Square | Tray           |

**Figure 1. Typical Application Diagram for Two-Channel PFC Converter**

## Block Diagram



\* FR: Full Range AC Input, AC85V~264V  
HV: High Voltage Range AC Input, AC180~264V

Figure 2. Functional Block Diagram

## Pin Configuration / Marking Information

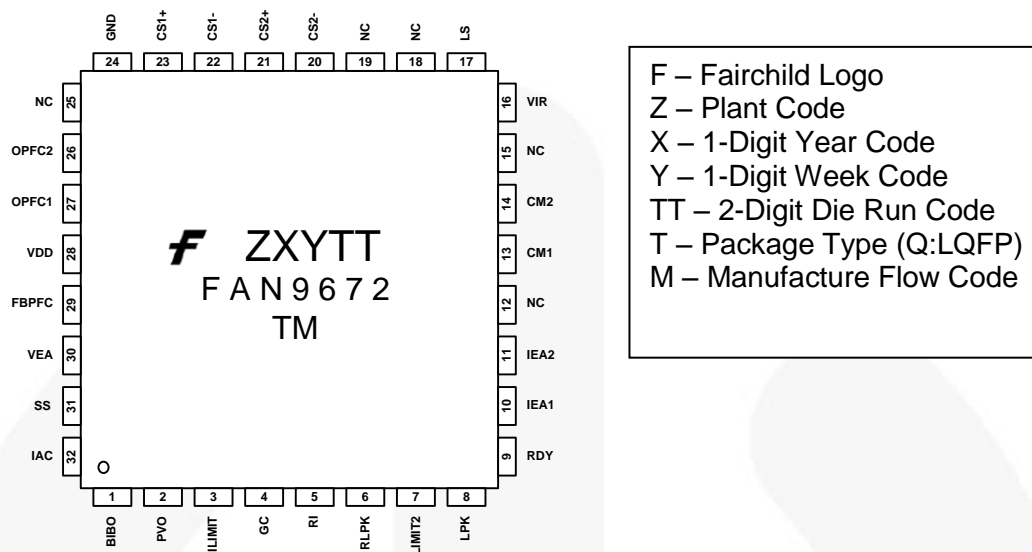


Figure 3. Pin Layout (Top View)

## Pin Definitions

| Pin # | Name    | Description   |
|-------|---------|---|
| 1     | BIBO    | <b>Brown-In /Out Level Setting.</b> This pin is used for brown in /out setting.   |
| 2     | PVO     | <b>Programmable Output Voltage.</b> DC voltage from a microcontroller (MCU) can be applied to this pin to program the output voltage level. The operation range is 3.5 V ~ 0.5 V. If $V_{PVO} < 0.5$ V, the PVO function is disabled.   |
| 3     | ILIMIT  | <b>Current Command Clamp Setting.</b> Average current mode is to control the average value of inductor current by a current command. Connecting a resistor and a capacitor to this pin can determine a limit value of the current command.  |
| 4     | GC      | <b>Setting of Gain Modulator.</b> A resistor, connected from this pin to ground, is used to adjust the output level of the gain modulator. A small capacitor connected from this pin to GND is recommended for noise filtering.   |
| 5     | RI      | <b>Oscillator Setting.</b> There are two oscillator frequency ranges: 18 k~40 kHz and 50 k~75 kHz. A resistor connected from RI to ground determines the switching frequency. A resistor value between 10.6 k ~ 44.4 kΩ is recommended.   |
| 6     | RLPK    | <b>Ratio of <math>V_{LPK}</math> and <math>V_{IN}</math>.</b> Connect a resistor and a capacitor to this pin to adjust the ratio of $V_{IN}$ peak to $V_{LPK}$ . Typical value is 12.4 kΩ (1:100 of $V_{LPK}$ and $V_{IN}$ peak). The accuracy of $V_{LPK}$ is primarily determined by the tolerance of $R_{RLPK}$ at this pin. |
| 7     | ILIMIT2 | <b>Peak Current Limit Setting.</b> Connect a resistor and a capacitor to this pin to set the over-current limit threshold and to protect power devices from damage due to inductor saturation. This pin sets the over-current threshold for cycle-by-cycle current limit.   |
| 8     | LPK     | <b>Peak of Line Voltage.</b> This pin can be used to provide information about the peak amplitude of the line voltage to an MCU.  |
| 9     | RDY     | <b>Output Ready Signal.</b> When the feedback voltage on FBPFC reaches 2.4 V, the RDY pin outputs a high $V_{RDY}$ signal to inform the MCU that the downstream power stage can start normal operation. If AC brownout is detected, the $V_{RDY}$ signal is LOW to signal to the MCU it is not ready.                           |

Continued on the following page...

## Pin Definitions (Continued)

| Pin # | Name  | Description   |
|-------|-------|---|
| 10    | IEA1  | <b>Output 1 of PFC Current Amplifier.</b> The signal from this pin is compared with an internal sawtooth to determine the pulse width for PFC gate drive 1.   |
| 11    | IEA2  | <b>Output 2 of PFC Current Amplifier.</b> The signal from this pin is compared with an internal sawtooth to determine the pulse width for PFC gate drive 2.   |
| 12    | NC    | No Connection   |
| 13    | CM1   | <b>Channel 1 Management Setting.</b> This pin is used to configure the characteristic of PFC enable / disable. The “PFC enabling” pull voltage on this pin is LOW (=0 V) to enable and HIGH (>4 V) to disable the whole PFC system.   |
| 14    | CM2   | <b>Channel 2 Management Setting.</b> There are two control methods for channel 2. The first uses an external signal to enable / disable channel 2 ( $V_{CM2} = 0\text{ V}$ / $V_{CM2} > 4\text{ V}$ ). The second is linear increase / decrease loading of channel 2 when power level, $V_{VEA}$ , triggers the setting level of $V_{CM2}$ .  |
| 15    | NC    | No Connection   |
| 16    | VIR   | <b>Input Voltage Range Setting.</b> A capacitor and a resistor are connected in parallel from this pin to GND. When $V_{VIR} > 3.5\text{ V}$ , the PFC controller only works for the high-voltage input range ( $180\text{ V}_{AC} \sim 264\text{ V}_{AC}$ ) and $R_{IAC}$ must be $12\text{ M}\Omega$ . When $V_{VIR} < 1.5\text{ V}$ , the PFC controller works for the full line voltage range ( $90\text{ V}_{AC} \sim 264\text{ V}_{AC}$ ) and $R_{IAC}$ must be $6\text{ M}\Omega$ . Voltage $1.5\text{ V}$ to $3.5\text{ V}$ is not allowed. |
| 17    | LS    | <b>Setting for Current Predict Function.</b> A resistor, connected from this pin to ground, is used to adjust the compensation of the linear predict function (LPT). A small capacitor connected from this pin to GND is recommended for noise filtering.   |
| 18    | NC    | No Connection   |
| 19    | NC    | No Connection   |
| 20    | CS2-  | <b>Negative PFC Current Sense2 Input</b>  |
| 21    | CS2+  | <b>Positive PFC Current Sense2 Input</b>  |
| 22    | CS1-  | <b>Negative PFC Current Sense1 Input</b>  |
| 23    | CS1+  | <b>Positive PFC Current Sense1 Input</b>  |
| 24    | GND   | <b>Ground</b>   |
| 25    | NC    | No Connection   |
| 26    | OPFC2 | <b>PFC Gate Drive 2.</b> The totem-pole output drive for the PWM MOSFET or IGBT. This pin has an internal 15 V clamp to protect the external power switch.  |
| 27    | OPFC1 | <b>PFC Gate Drive 1.</b> The totem-pole output drive for the PWM MOSFET or IGBT. This pin has an internal 15 V clamp to protect the external power switch.  |
| 28    | VDD   | <b>External Bias Supply for the IC.</b> The typical turn-on and turn-off threshold voltages are 12.8 V and 10.8 V, respectively.  |
| 29    | FBPFC | <b>Voltage Feedback Input for PFC.</b> Inverting input of the PFC error amplifier. This pin is connected to the PFC output through a resistor divider network.  |
| 30    | VEA   | <b>Output of PFC Voltage Amplifier.</b> The error amplifier output for the PFC voltage feedback loop. A compensation network is connected between this pin and ground.  |
| 31    | SS    | <b>Soft-Start.</b> Connect a capacitor to this pin to set the soft-start time. Pull this pin to ground to disable the gate drive outputs OPFC1 and OPFC2.   |
| 32    | IAC   | <b>Input AC Current.</b> During normal operation, this input provides a current reference for the multiplier. The recommended maximum current on IAC, $I_{AC}$ , is $100\text{ }\mu\text{A}$ .  |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol                | Parameter   |   | Min. | Max.                   | Unit |
|-----------------------|---|---|------|------------------------|------|
| V <sub>DD</sub>       | DC Supply Voltage   |   |      | 30                     | V    |
| V <sub>OPFC</sub>     | Voltage on OPFC1, OPFC2 Pins  |   | -0.3 | V <sub>DD</sub> +0.3 V | V    |
| V <sub>L</sub>        | Voltage on IAC, BIBO, LPK, RLPK, FBPFC, VEA, CS1+, CS2+, CS1-, CS2-, CM1, CM2, ILIMIT, ILIMIT2, RI, PVO, GC, LS, VIR Pins |   | -0.3 | 7.0                    | V    |
| V <sub>IEA</sub>      | Voltage on IEA1, IEA2, SS Pins  |   | 0    | 8                      | V    |
| I <sub>IAC</sub>      | Input AC Current  |   |      | 1                      | mA   |
| I <sub>PFC-OPFC</sub> | Peak PFC OPFC Current, Source or Sink   |   |      | 0.5                    | A    |
| P <sub>D</sub>        | Power Dissipation, T <sub>A</sub> < 50°C  |   |      | 1640                   | mW   |
| R <sub>θJA</sub>      | Thermal Resistance (Junction-to-Air)  |   |      | 77                     | °C/W |
| T <sub>J</sub>        | Operating Junction Temperature  |   | -40  | 150                    | °C   |
| T <sub>STG</sub>      | Storage Temperature Range   |   | -55  | 150                    | °C   |
| T <sub>L</sub>        | Lead temperature (Soldering)  |   |      | 260                    | °C   |
| ESD                   | Electrostatic Discharge Capability  | Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 |      | 4                      | kV   |
|                       |   | Charged Device Model, JESD22-C101             |      | 2                      |      |

### Notes:

1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

## Recommended Operating Conditions

The recommended operating conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol         | Parameter               | Min. | Typ. | Max. | Unit |
|----------------|-------------------------|------|------|------|------|
| $V_{DD-OP}$    | Operating Voltage       |      | 15   |      | V    |
| $L_{MISMATCH}$ | Boost Inductor Mismatch | -5   |      | +5   | %    |

## Electrical Characteristics

Unless otherwise noted,  $V_{DD} = 15\text{ V}$  and  $T_J = -40\sim 105^\circ\text{C}$ .

| Symbol                             | Parameter   | Condition   | Min. | Typ. | Max. | Unit          |
|------------------------------------|---|---|------|------|------|---------------|
| <b>VDD Section</b>                 |   |   |      |      |      |               |
| $I_{DD\text{-}ST}$                 | Startup Current   | $V_{DD} = V_{TH\text{-}ON} - 0.1\text{ V}$  |      | 30   | 80   | $\mu\text{A}$ |
| $I_{DD\text{-}OP}$                 | Operating Current   | $V_{DD} = 14\text{ V}$ ; Output Not Switching, $R_{RI} = 25\text{ k}\Omega$                         | 4    | 6    | 7    | $\text{mA}$   |
| $V_{TH\text{-}ON}$                 | Turn-On Threshold Voltage   | $V_{DD}$ Rising   |      | 12.8 |      | $\text{V}$    |
| $\Delta V_{TH}$                    | UVLO Hysteresis   |   | 2    |      | 3    | $\text{V}$    |
| $V_{DD\text{-}OVP}$                | $V_{DD}$ OVP Threshold  | OPFC1~2 Disabled, IEA1~2 and SS Pull LOW  | 23   | 24   | 25   | $\text{V}$    |
| $\Delta V_{DD\text{-}OVP}$         | $V_{DD}$ OVP Hysteresis   |   |      | 1    |      | $\text{V}$    |
| $t_{D\text{-}OVP}$                 | $V_{DD}$ OVP Debounce Time  |   |      |      | 80   | $\mu\text{s}$ |
| <b>Oscillator<sup>(3)</sup></b>    |   |   |      |      |      |               |
| $V_{RI}$                           | Voltage on RI   | $R_{RI} = 25\text{ k}\Omega$  | 1.15 | 1.20 | 1.25 | $\text{V}$    |
| $f_{OSC1}$                         | PFC Frequency of $R_{RI}=25\text{ k}\Omega$                           | $R_{RI} = 25\text{ k}\Omega$  | 30   | 32   | 34   | $\text{kHz}$  |
| $f_{OSC2}$                         | PFC Frequency of $R_{RI}=62\text{ k}\Omega$                           | $R_{RI} = 12.5\text{ k}\Omega$  | 58   | 62   | 66   | $\text{kHz}$  |
| $f_{DV}$                           | Voltage Stability   | $13\text{ V} \leq V_{DD} \leq 22\text{ V}$  |      |      | 2    | $\%$          |
| $f_{DT}$                           | Temperature Stability   |   |      |      | 2    | $\text{V}$    |
| $\Delta V_{IEA\text{-}SAW32}$      | $V_{IEA\text{-}SAW}$ of PFC Frequency=32 kHz                          | $R_{RI} = 25\text{ k}\Omega$  |      | 5    |      | $\text{V}$    |
| $\Delta V_{IEA\text{-}SAW64}$      | $V_{IEA\text{-}SAW}$ of PFC Frequency=64 kHz                          | $R_{RI} = 12.5\text{ k}\Omega$  |      | 5.15 |      | $\text{V}$    |
| $D_{PFC\text{-}MAX}$               | Maximum Duty Cycle  | $V_{IEA} > 7\text{ V}$  | 94   | 97   |      | $\%$          |
| $D_{PFC\text{-}MIN}$               | Minimum Duty Cycle  | $V_{IEA} < 1\text{ V}$  |      |      | 0    | $\%$          |
| $f_{RANGE1}$                       | Frequency Range 1 <sup>(3,6)</sup>                                    |   | 18   |      | 40   | $\text{kHz}$  |
| $f_{RANGE2}$                       | Frequency Range 2 <sup>(3,6)</sup>                                    |   | 55   |      | 75   | $\text{kHz}$  |
| $t_{DEAD\text{-}MIN}$              | Minimum Dead Time   | $R_{RI} = 10.7\text{ k}\Omega$  |      | 600  |      | $\text{ns}$   |
| <b>VIR</b>                         |   |   |      |      |      |               |
| $V_{VIR\text{-}H}$                 | Setting Level for High Voltage Input Range                            | $R_{VIR} = 500\text{ k}\Omega$ ( $V_{VIR} = 5\text{ V}$ )   | 3.5  |      |      | $\text{V}$    |
| $V_{VIR\text{-}L}$                 | Setting Level for Low Voltage Input Range or Full Voltage Input Range | $V_{VIR} = 0\text{ V}$  |      |      | 1.5  | $\text{V}$    |
| $I_{VIR}$                          | Source Current of VIR Pin   |   | 7    | 10   | 13   | $\mu\text{A}$ |
| <b>PFC Soft-Start</b>              |   |   |      |      |      |               |
| $I_{SS}$                           | Constant Current Output for Soft-Start                                | System Brown-in   |      | 22   |      | $\mu\text{A}$ |
| $V_{SS}$                           | Maximum Voltage on SS   |   | 6.8  |      |      | $\text{V}$    |
| $I_{SS\text{-}Discharge}$          | Discharge Current of SS Pin   | Brownout, SAG, CM1>4 V, $R_{RI}$ Open / Short, OTP  |      | 60   |      | $\mu\text{A}$ |
| <b>Low-Power Detect Comparator</b> |   |   |      |      |      |               |
| $V_{VEA\text{-}OFF}$               | VEA Voltage Off   | When $V_{VEA\text{-}OFF} < 0.3\text{ V}$ , $V_{OPFC1\sim 2}$ Turns Off & $V_{IEA1\sim 2}$ Pulls LOW |      | 0.3  |      | $\text{V}$    |

Continued on the following page...



## Electrical Characteristics

Unless otherwise noted,  $V_{DD} = 15\text{ V}$  and  $T_J = -40\sim 105^\circ\text{C}$ .

| Symbol                             | Parameter   | Condition  | Min. | Typ. | Max. | Unit            |
|------------------------------------|---|--|------|------|------|-----------------|
| <b>Voltage Error Amplifier</b>     |   |  |      |      |      |                 |
| $V_{REF}$                          | Reference Voltage   | $PVO = GND, T_J = 25^\circ\text{C}$  | 2.45 | 2.50 | 2.55 | V               |
| $A_V$                              | Open-Loop Gain <sup>(3)</sup>                             |  | 42   | 65   |      | dB              |
| $G_{mV}$                           | Transconductance  | $V_{NONINV} - V_{INV} = 0.5\text{ V}, T_J = 25^\circ\text{C}$  |      | 100  |      | $\mu\text{mho}$ |
| $I_{FBPFC-L}$                      | Maximum Source Current                                    | $V_{FBPFC} = 2\text{ V}, V_{VEA} = 3\text{ V}$   | 40   | 50   |      | $\mu\text{A}$   |
| $I_{FBPFC-H}$                      | Maximum Sink Current                                      | $V_{FBPFC} = 3\text{ V}, V_{VEA} = 3\text{ V}$   |      | -50  | -40  | $\mu\text{A}$   |
| $I_{BS}$                           | Input Bias Current Range                                  |  | -1   |      | 1    | $\mu\text{A}$   |
| $I_{FBPFC-FL}$                     | Pull HIGH Current for FBPFC                               | FBPFC Floating   |      | 500  |      | nA              |
| $V_{VEA-H}$                        | Output High Voltage on $V_{VEA}$                          | $V_{FBPFC} = 2\text{ V}$   | 5.7  | 6.0  |      | V               |
| $V_{VEA-L}$                        | Output Low Voltage on $V_{VEA}$                           | $V_{FBPFC} = 3\text{ V}$   |      | 0    | 0.15 | V               |
| $I_{VEA-DIS}$                      | Discharge Current   | Brownout, $R_{RI}$ Open /Short, OTP, SAG   |      | 10   |      | $\mu\text{A}$   |
| <b>Current Error Amplifier 1~2</b> |   |  |      |      |      |                 |
| $G_{mi}$                           | Transconductance  | $V_{NONINV} = V_{INV}, V_{IEA} = 4\text{ V}, V_{LIMIT} > 0.6\text{ V}, T_J = 25^\circ\text{C}$   |      | 88   |      | $\mu\text{mho}$ |
| $V_{OFFSET}$                       | Input Offset Voltage                                      | $V_{VEA} = 0.45\text{ V}, R_{IAC} = 12\text{ M}\Omega, V_{IAC} = 311\text{ V}, V_{FBPFC} = 2\text{ V}, V_{VIR} = 5\text{ V}, T_J = 25^\circ\text{C}$ |      | 0    |      | mV              |
| $V_{IEA-H}$                        | Output High Voltage                                       |  | 6.8  | 7.0  |      | V               |
| $V_{IEA-L}$                        | Output Low Voltage  |  |      | 0    | 0.4  | V               |
| $I_L$                              | Source Current  | $V_{NONINV} - V_{INV} = +0.6\text{ V}, V_{IEA} = 1\text{ V}, V_{LIMIT} > 0.6\text{ V}$   | 35   | 50   |      | $\mu\text{A}$   |
| $I_H$                              | Sink Current  | $V_{NONINV} - V_{INV} = -0.6\text{ V}, V_{IEA} = 6.5\text{ V}, V_{LIMIT} > 0.6\text{ V}$   |      | -50  | -35  | $\mu\text{A}$   |
| $A_I$                              | Open-Loop Gain <sup>(3)</sup>                             |  | 40   | 50   |      | dB              |
| $I_{IEA-LOW}$                      | IEA Pin Pull LOW Capability Protection                    | $V_{IEA} > 5\text{ V}$   | 500  |      |      | $\mu\text{A}$   |
| <b>Brown-In /Out</b>               |   |  |      |      |      |                 |
| $V_{BIBO-FL}$                      | Low Threshold of BO at Full Range AC Input                | $V_{VIR} < 1.5\text{ V}, R_{IAC} = 6\text{ M}\Omega$   | 1.00 | 1.05 | 1.10 | V               |
| $\Delta V_{BIBO-F}$                | Hysteresis  | $V_{BIBO} > V_{BIBO-FL} + \Delta V_{BIBO-F}$ , System Brown-in, Start SS   |      | 850  |      | mV              |
| $V_{BIBO-HL}$                      | Low Threshold of BO at High Voltage Single Range AC Input | $V_{VIR} > 3.5\text{ V}, R_{IAC} = 12\text{ M}\Omega$  | 1.00 | 1.05 | 1.10 | V               |
| $\Delta V_{BIBO-H}$                | Hysteresis  | $V_{BIBO} > V_{BIBO-HL} + \Delta V_{BIBO-H}$ , System Brown-in, Start SS   |      | 700  |      | mV              |
| $t_{UVP}$                          | Under-Voltage Protection Delay                            |  |      | 450  |      | ms              |
| <b>TriFault Detect™</b>            |   |  |      |      |      |                 |
| $V_{PFC-UVP}$                      | PFC Feedback Under-Voltage Protection                     |  | 0.4  | 0.5  | 0.6  | V               |
| $V_{PFC-OVP}$                      | Over-Voltage Protection                                   |  | 2.70 | 2.75 | 2.80 | V               |
| $\Delta V_{PFC-OVP}$               | PFC OVP Hysteresis  |  | 200  | 250  | 300  | mV              |
| $t_{FBPFC-OPEN}$                   | FBPFC Open Delay <sup>(3)</sup>                           | $V_{FBPFC} = V_{PFC-UVP}$ to FBPFC Open, 470 pF from FBPFC to GND  |      | 2    |      | ms              |
| $t_{FBPFC-UVP}$                    | Under-Voltage Protection Debounce Time                    |  |      | 50   |      | $\mu\text{s}$   |

Continued on the following page...

## Electrical Characteristics

Unless otherwise noted,  $V_{DD} = 15\text{ V}$  and  $T_J = -40\sim 105^\circ\text{C}$ .

| Symbol                           | Parameter  | Condition  | Min. | Typ.  | Max. | Unit          |
|----------------------------------|--|--|------|-------|------|---------------|
| <b>PFC ILIMIT2 (CS1 /CS2)</b>    |  |  |      |       |      |               |
| $V_{ILIMIT2-CS1}$                | Peak Current Limit Voltage                                 | $CS1 > V_{ILIMIT2}$ , OPFC1 Disables Cycle by Cycle Limit, $V_{IEA1\sim 2}$ Pull LOW, $R_{ILIMIT2} = 30\text{ k}\Omega$ , $R_{RI} = 25\text{ k}\Omega$ |      | 1.48  |      | V             |
| $V_{ILIMIT2-CS2}$                | Peak Current Limit Voltage                                 | $CS2 > V_{ILIMIT2}$ , OPFC2 Disables Cycle by Cycle Limit, $V_{IEA1\sim 2}$ Pull LOW, $R_{ILIMIT2} = 30\text{ k}\Omega$ , $R_{RI} = 25\text{ k}\Omega$ |      | 1.48  |      | V             |
| $I_{ILIMIT2}$                    | Output Current for Peak Current Limit Setting              | $R_{RI} = 25\text{ k}\Omega$ , $V_{RI}/R_{RI}$ , $T_J = 25^\circ\text{C}$  |      | 49.5  |      | $\mu\text{A}$ |
| $t_{PFC-Bnk1}$                   | Leading-Edge Blanking Time of ILIMIT of Channel 1          | $V_{DD} = 15\text{ V}$ , OPFC Drops to 9 V   |      | 250   |      | ns            |
| $t_{PFC-Bnk2}$                   | Leading-Edge Blanking Time of ILIMIT of Channel 2          | $V_{DD} = 15\text{ V}$ , OPFC Drops to 9 V   |      | 250   |      | ns            |
| $t_{PD1}$                        | Propagation Delay to Output of Channel 1                   |  |      | 200   | 400  | ns            |
| $t_{PD2}$                        | Propagation Delay to Output of Channel 2                   |  |      | 200   | 400  | ns            |
| $V_{LIMIT-OPEN}$                 | LIMIT Open Voltage   | OPFC1~2 Disabled and IEA1~2 Pull LOW   | 3.8  | 4.0   | 4.2  | V             |
| <b>ILIMIT (Command Limit)</b>    |  |  |      |       |      |               |
| $V_{ILIMIT-R}$                   | Input Range  |  | 0.2  |       | 0.8  | V             |
| $V_{ILIMIT}$                     | Over-Power Limit Voltage                                   | $R_{ILIMIT} = 42\text{ k}\Omega$ , $R_{RI} = 25\text{ k}\Omega$ , $V_{ILIMIT} = R_{ILIMIT} * I_{ILIMIT}/4$   |      | 0.504 |      | V             |
| $I_{ILIMIT}$                     | Source Current of ILIMIT Pin                               | $R_{RI} = 25\text{ k}\Omega$ , $V_{RI}/R_{RI}$   |      | 49    |      | $\mu\text{A}$ |
| <b>SAG Protection Section</b>    |  |  |      |       |      |               |
| $V_{SAG}$                        | SAG Voltage of BIBO  | 1. $V_{BIBO} < V_{SAG}$ & $V_{RDY}$ HIGH 33 ms, or 2. $V_{BIBO} < V_{SAG}$ & $V_{RDY}$ Low, Brownout   |      | 0.85  |      | V             |
| $t_{SAG-DT}$                     | SAG Debounce Time  | $V_{BIBO} < V_{SAG}$ & $V_{RDY}$ HIGH  |      | 33    |      | ms            |
| <b>Gain Compensation Section</b> |  |  |      |       |      |               |
| $I_{GC-L1}$                      | Mirror Current of $I_{AC}$ at Full Range AC Input          | $V_{VIR} = 0\text{ V}$ , $V_{IAC} = 127.28\text{ V}$ , $R_{IAC} = 6\text{ M}\Omega$  |      | 20.71 |      | $\mu\text{A}$ |
| $I_{GC-L2}$                      | Mirror Current of $I_{AC}$ at Full Range AC Input          | $V_{VIR} = 0\text{ V}$ , $V_{IAC} = 311.13\text{ V}$ , $R_{IAC} = 6\text{ M}\Omega$  |      | 51.86 |      | $\mu\text{A}$ |
| $I_{GC-HV}$                      | Mirror Current of $I_{AC}$ at High Voltage Single AC Input | $V_{VIR} = 5\text{ V}$ , $V_{IAC} = 311.13\text{ V}$ , $R_{IAC} = 12\text{ M}\Omega$   |      | 51.86 |      | $\mu\text{A}$ |
| $I_{GC-OPEN}$                    | Pull HIGH Current for GC Open                              |  |      | 100   |      | nA            |
| $V_{GC-OPEN}$                    | GC Open Voltage  | $V_{GC} > V_{GC-OPEN}$ $V_{IEA}$ , OPFC1, 2 Blanking   | 2.85 | 3.00  | 3.15 | V             |
| <b>LPK<sup>(7)</sup></b>         |  |  |      |       |      |               |
| $V_{LPK-H1}$                     | $V_{LPK}$ on High Voltage Input Range                      | $V_{IAC} = 311\text{ V}$ , $R_{IAC} = 12\text{ M}\Omega$ , $V_{VIR} > 3.5\text{ V}$ , $R_{LPK} = 12.4\text{ k}\Omega$ , $T_J = 25^\circ\text{C}$       |      | 3.168 |      | V             |
| $V_{LPK-H2}$                     | $V_{LPK}$ on High Voltage Input Range                      | $V_{IAC} = 373\text{ V}$ , $R_{IAC} = 12\text{ M}\Omega$ , $V_{VIR} > 3.5\text{ V}$ , $R_{LPK} = 12.4\text{ k}\Omega$ , $T_J = 25^\circ\text{C}$       |      | 3.80  |      | V             |

Continued on the following page...

## Electrical Characteristics

Unless otherwise noted,  $V_{DD} = 15\text{ V}$  and  $T_J = -40\sim 105^\circ\text{C}$ .

| Symbol                     | Parameter                                    | Condition  | Min. | Typ.                       | Max. | Unit |
|----------------------------|--|--|------|----------------------------|------|------|
| V <sub>LPK-L1</sub>        | V <sub>LPK</sub> on Full Range AC Input      | V <sub>IAC</sub> = 127 V, R <sub>IAC</sub> = 6 MΩ,<br>V <sub>VIR</sub> < 1.5 V, R <sub>LPK</sub> = 12.4 kΩ,<br>T <sub>J</sub> = 25°C |      | 1.29                       |      | V    |
| V <sub>LPK-L2</sub>        | V <sub>LPK</sub> on Full Range AC Input      | V <sub>IAC</sub> = 373 V, R <sub>IAC</sub> = 6 MΩ,<br>V <sub>VIR</sub> < 1.5 V, R <sub>LPK</sub> = 12.4 kΩ,<br>T <sub>J</sub> = 25°C |      | 3.80                       |      | V    |
| V <sub>AC-ON</sub>         | AC ON Threshold Voltage                      | R <sub>IAC</sub> = 12 MΩ, V <sub>VIR</sub> > 3.5 V   |      | V <sub>AC-OFF</sub><br>+26 |      | V    |
| RLPK                       |  |  |      |                            |      |      |
| I <sub>RLPK-OPEN</sub>     | Pull HIGH Current for RLPK Open              |  | 10   | 100                        | 250  | nA   |
| V <sub>RLPK-OPEN</sub>     | RLPK Open Voltage                            | RLPK Open  | 2.28 | 2.40                       | 2.52 | V    |
| PVO                        |  |  |      |                            |      |      |
| V <sub>PVO</sub>           | Input Range                                  |  | 0.3  |                            | 3.5  | V    |
| V <sub>PVO_DIS</sub>       | PVO Disable Voltage                          | PVO< V <sub>PVO_DIS</sub> Disable  |      | 0.2                        |      | V    |
| V <sub>PVO-CLAMPH</sub>    | PVO Limit Voltage                            | FBPFC Connected to VEA,<br>V <sub>PVO</sub> = 4 V  |      | 1.6                        |      | V    |
| V <sub>FBPFC1</sub>        | FBPFC Voltage 1                              | FBPFC Connected to VEA,<br>V <sub>PVO</sub> = 0.3 V  |      | 2.425                      |      | V    |
| V <sub>FBPFC2</sub>        | FBPFC Voltage 2                              | FBPFC Connected to VEA,<br>V <sub>PVO</sub> = 3.5 V  |      | 1.625                      |      | V    |
| I <sub>PVO-Discharge</sub> | PVO Discharge Current                        | PVO Open   |      | 1                          |      | μA   |
| OTP                        |  |  |      |                            |      |      |
| T <sub>OTP-ON</sub>        | Over-Temperature Protection <sup>(3)</sup>   |  |      | 140                        |      | °C   |
| ΔT <sub>OTP</sub>          | Hysteresis <sup>(3)</sup>                    |  |      | 30                         |      | °C   |
| CM1 Section                |  |  |      |                            |      |      |
| I <sub>CM1</sub>           | CM1 Output Current                           |  |      | 55                         |      | μA   |
| V <sub>CM1-disable</sub>   | PFC Disable Voltage                          | OPFC1~2 Disabled and IEA1~2<br>Pull LOW and SS Pull LOW<br>when I <sub>CM1</sub> · R <sub>CM1</sub> > 4 V                            |      | 4                          |      | V    |
| θ <sub>1</sub>             | Phase of OPFC1                               | When I <sub>CM1</sub> · R <sub>CM1</sub> < 4 V or Short  |      | 0                          |      | °    |
| θ <sub>2</sub>             | Phase of OPFC2                               | When I <sub>CM1</sub> · R <sub>CM1</sub> < 4 V or Short  | 170  | 180                        | 190  | °    |
| CM2 Section                |  |  |      |                            |      |      |
| I <sub>CM2</sub>           | CM2 Output Current                           |  |      | 55                         |      | μA   |
| V <sub>CM2-disable</sub>   | Channel2 Disable Voltage                     | OPFC2 Disables and IEA2<br>Pulls LOW when I <sub>CM2</sub> · R <sub>CM2</sub> ><br>4 V or CM2 Floating                               |      | 4                          |      | V    |
| V <sub>CM2-range</sub>     | Set VEA Unload Voltage                       |  | 0    |                            | 3.8  | V    |
| θ <sub>1</sub>             | Phase of OPFC1                               | When I <sub>CM2</sub> · R <sub>CM2</sub> > 4 V or CM2<br>Floating  |      | 0                          |      | °    |
| θ <sub>2</sub>             | Phase of OPFC2                               | When I <sub>CM2</sub> · R <sub>CM2</sub> > 4 V or CM2<br>Floating  | 170  | 180                        | 190  | °    |
| RDY Section                |  |  |      |                            |      |      |
| V <sub>FB-RD</sub>         | Level of V <sub>FBPFC</sub> to Pull RDY HIGH | V <sub>PVO</sub> = 0 V, Brown-in,<br>V <sub>FBPFC</sub> > V <sub>FB-RD</sub>   | 2.3  | 2.4                        | 2.5  | V    |
| ΔV <sub>FB-RD-L</sub>      | Hysteresis                                   | V <sub>PVO</sub> = 0 V, V <sub>IR</sub> < 1.5 V  |      | 1.15                       |      | V    |

Continued on the following page

## Electrical Characteristics

Unless otherwise noted,  $V_{DD} = 15\text{ V}$  and  $T_J = -40\sim 105^\circ\text{C}$ .

| Symbol                      | Parameter  | Condition  | Min. | Typ.  | Max. | Unit          |
|-----------------------------|--|--|------|-------|------|---------------|
| $\Delta V_{FB-RD-H}$        | Hysteresis   | $V_{PVO} = 0\text{ V}$ , $V_{IR} > 3.5\text{ V}$   |      | 0.85  |      | V             |
| $Z_{RDY}$                   | Pull High Input Impedance                                      | $T_J = 25^\circ\text{C}$   |      | 100   |      | k $\Omega$    |
| $V_{RDY-High}$              | HIGH Voltage of RDY  |  | 4.8  | 5.0   |      | V             |
| $V_{RDY-Low}$               | LOW Voltage of RDY   | Pull High Current = 1 mA   |      |       | 0.5  | V             |
| <b>PFC Output Driver1~2</b> |  |  |      |       |      |               |
| $V_{GATE-CLAMP}$            | Gate Output Clamping Voltage                                   | $V_{DD} = 22\text{ V}$   | 13   | 15    | 17   | V             |
| $V_{GATE-L}$                | Gate Low Voltage   | $V_{DD} = 15\text{ V}$ , $I_O = 100\text{ mA}$   |      |       | 1.5  | V             |
| $V_{GATE-H}$                | Gate High Voltage  | $V_{DD} = 13\text{ V}$ , $I_O = 100\text{ mA}$   | 8    |       |      | V             |
| $t_r$                       | Gate Rising Time   | $V_{DD} = 15\text{ V}$ , $C_L = 4.7\text{ nF}$ ,<br>O/P = 2 V to 9 V   |      | 70    |      | ns            |
| $t_f$                       | Gate Falling Time  | $V_{DD} = 15\text{ V}$ , $C_L = 4.7\text{ nF}$ ,<br>O/P = 9 V to 2 V   |      | 60    |      | ns            |
| <b>LPT Section</b>          |  |  |      |       |      |               |
| $R_{LS}$                    | Range of Inductance Setting                                    |  | 12   |       | 87   | k $\Omega$    |
| $V_{LS-MIN}$                | Voltage Difference between $V_{FBPFC}$ and $V_{ACD}$ on LS Pin | $V_{FBPFC} - V_{ACD} \geq 0\text{ V}$  |      | 50    |      | mV            |
| <b>Gain Modulator</b>       |  |  |      |       |      |               |
| $I_{AC}$                    | Input for AC Current <sup>(3,6)</sup>                          | Multiplier Linear Range  | 0    |       | 65   | $\mu\text{A}$ |
| BW                          | Bandwidth <sup>(3,6)</sup>                                     | $I_{AC} = 40\text{ }\mu\text{A}$   |      | 2     |      | kHz           |
| $V_{RM}$                    | Voltage of $R_M$ (Output Current of Gain Modulator * $R_M$ )   | $V_{IAC} = 106.07\text{ V}$ , $R_{IAC} = 6\text{ M}\Omega$ ,<br>$V_{FBPFC} = 2.25\text{ V}$ , $V_{BIBO} = 2\text{ V}$ ,<br>$V_{CM2} > 4.5\text{ V}$ ( $V_{AC} = 75\text{ V}$ ),<br>$T_J = 25^\circ\text{C}$                              |      | 0.490 |      | V             |
|                             |  | $V_{IAC} = 120.21\text{ V}$ , $R_{IAC} = 6\text{ M}\Omega$ ,<br>$V_{FBPFC} = 2.25\text{ V}$ , $V_{BIBO} = 2\text{ V}$ ,<br>$V_{CM2} > 4.5\text{ V}$ ( $V_{AC} = 85\text{ V}$ ),<br>$T_J = 25^\circ\text{C}$                              |      | 0.430 |      |               |
|                             |  | $V_{IAC} = 155.56\text{ V}$ , $R_{IAC} = 6\text{ M}\Omega$ ,<br>$V_{FBPFC} = 2.25\text{ V}$ , $V_{BIBO} = 2\text{ V}$ ,<br>$V_{CM2} > 4.5\text{ V}$ ( $V_{AC} = 110\text{ V}$ ),<br>$T_J = 25^\circ\text{C}$                             |      | 0.327 |      |               |
|                             |  | $V_{IAC} = 311.13\text{ V}$ , $R_{IAC} = 12\text{ M}\Omega$ ,<br>$V_{FBPFC} = 2.25\text{ V}$ , $V_{BIBO} = 2\text{ V}$ ,<br>$V_{CM2} > 4.5\text{ V}$ , $V_{VIR} > 3.5\text{ V}$<br>( $V_{AC} = 220\text{ V}$ ), $T_J = 25^\circ\text{C}$ |      | 0.320 |      |               |
|                             |  | $V_{IAC} = 373.35\text{ V}$ , $R_{IAC} = 12\text{ M}\Omega$ ,<br>$V_{FBPFC} = 2.25\text{ V}$ , $V_{BIBO} = 2\text{ V}$ ,<br>$V_{CM2} > 4.5\text{ V}$ , $V_{VIR} > 3.5\text{ V}$<br>( $V_{AC} = 264\text{ V}$ ), $T_J = 25^\circ\text{C}$ |      | 0.260 |      |               |
| $R_M$                       | Resistor of Gain Modulator Output                              | $R_M = V_{RM}/I_{MO}$  |      | 7.5   |      | k $\Omega$    |

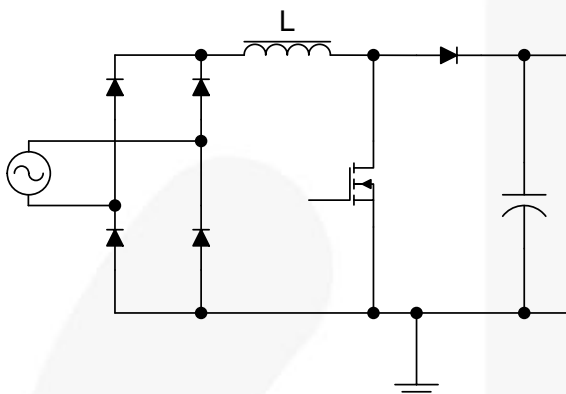
### Notes:

- This parameter, although guaranteed by design, is not 100% production tested.
- The setting range of resistance at the RI pin is between 53.3 k $\Omega$  and 10.7 k $\Omega$ .
- The  $R_{LS}$  and  $R_{GC}$  setting suggestion follows the calculation result from Fairchild documents: AN-4164, AN-4165, FEBFAN9673\_B01H1500A, FEBFAN9673\_B01H2500A, and design tools.
- Frequency of AC input should be <75 Hz.
- LPK specification is guaranteed at state of PFC working.
- Pull the CM pin LOW to ground to enable an individual channel for voltage on the CM pin of less than 0.2 V.

## Theory of Operation

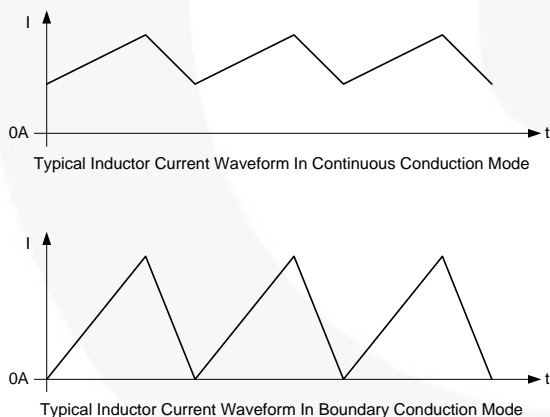
### 1. Continuous Conduction Mode (CCM)

The boost converter, shown in Figure 4, is the most popular topology for power factor correction (PFC) in AC-DC power supplies. This can be attributed to the continuous input current waveform provided by the boost inductor and the boost converter's input voltage range including 0 V. These fundamental properties make close-to-unity power factor easier to achieve.



**Figure 4. Basic PFC Boost Converter**

The boost converter can operate in Continuous Conduction Mode (CCM) or in Boundary Conduction Mode (BCM). These two descriptive names refer to the current flowing in the energy storage inductor of the boost power stage.

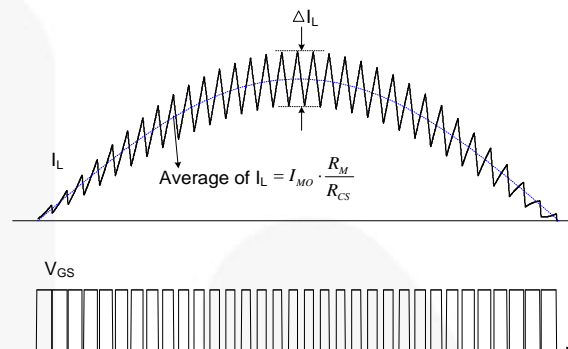


**Figure 5. CCM vs. BCM Control**

As the names indicate, the current in Continuous Conduction Mode (CCM) is continuous in the inductor. In Boundary Conduction Mode (BCM), the new switching period is initiated when the inductor current returns to zero. There are many fundamental differences in CCM and BCM operation and the respective designs of the boost converter. The FAN9672 is designed for CCM control, as Figure 5 shows. This method reduces inductor current ripple because the start current of each cycle is typically not 0 A. The ripple is controlled by the operation frequency and inductance design. This characteristic can decrease the maximum peak current of the power semiconductor.

### 2. Gain Modulator (IAC, LPK, VEA)

The FAN9672 employs two control loops for power factor correction: a current control loop and a voltage control loop. The current control loop shapes inductor current, as shown in Figure 6, through a current command,  $I_{MO}$ , from the gain modulator.



**Figure 6. CCM PFC Operation Waveforms**

The gain modulator is the block that provides the reference to control PFC output power. The current of the gain modulator,  $I_{MO}$ , is a function of  $V_{VEA}$ ,  $I_{IAC}$ , and LPK; as shown in the Figure 7.

There are three inputs to the gain modulator:

- $I_{IAC}$  A current representing the instantaneous input voltage (amplitude and wave shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is fed into the gain modulator on  $I_{IAC}$ . Sampling current  $I_{IAC}$  minimizes ground noise; important in high-power, switching-power conversion environment. The gain modulator responds linearly to this current.
- $V_{LPK}$  Voltage proportional to the peak voltage of the bridge rectifier when the PFC is working. The signal is the output of peak-detect circuit and its input is from the IAC pin. This factor of the gain modulator is input-voltage feed-forward control. This voltage information is not valid when the PFC is not working.
- $V_{VEA}$  The output of the voltage error amplifier,  $V_{VEA}$ . The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal,  $I_{MO}$ , calculated by Equation (1):

$$I_{MO} = K \times \frac{I_{IAC} \times V_{VEA}}{V_{LPK}^2} \quad (1)$$

The current signal,  $I_{MO}$ , is in the form of a full-wave rectified sinusoid at twice the line frequency. The gain modulator forms the reference for the current error loop and ultimately controls the instantaneous current drawn from the power line.

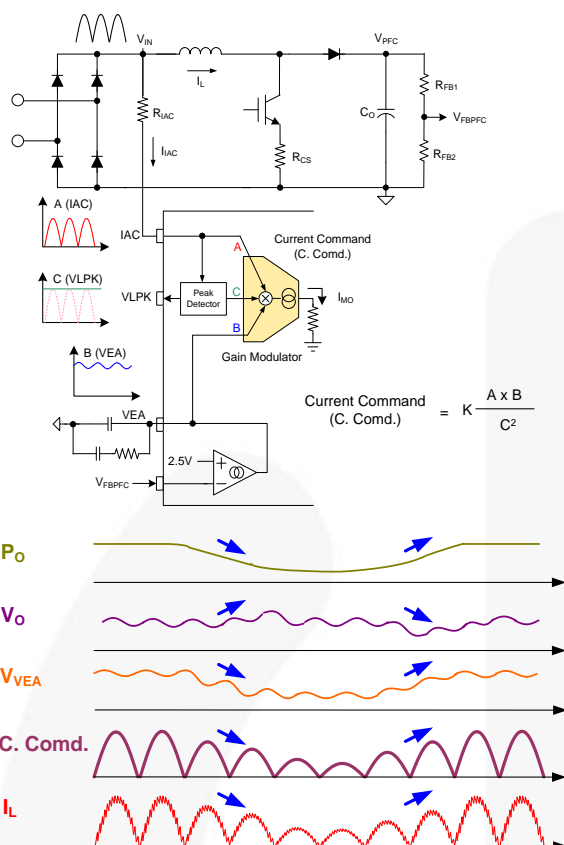


Figure 7. Input of Gain Modulation

### 3. Current Balance

Current matching of the different channels is important for interleaved control. There are several main points that need to careful consideration on this topic.

The current control of each channel is based on the sense signal,  $V_{CS}$ , to track the current command of the multiplier, as shown in Figure 8.

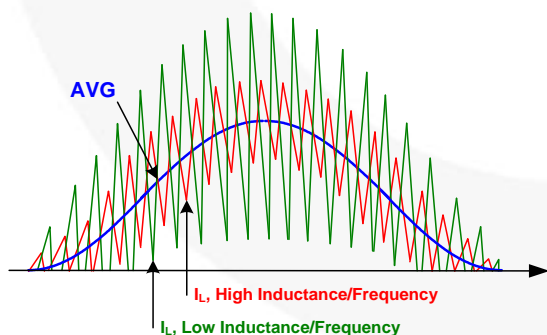


Figure 8. Average Current Mode Control

The main factors to system balance are layout and device tolerance. The tolerance of the shunt resistor for the current sense is especially important. If the feedback signal,  $V_{CS}$ , has a large deviation due to the tolerance of the sense resistor; the current of the channels is unbalanced. A high precision resistor is necessary.

High-power applications require the system current be large, so the distance of the layout trace between the current sense resistors and the controller or power ground (negative of output capacitor) to IC ground is important, as Figure 9 shows. The longer trace and larger current make the offset voltage and ground bounce differ significantly for different channels. Decreasing the deviation can balance the different channels. Follow the layout guidance of application notes AN-4164 and AN-4165.

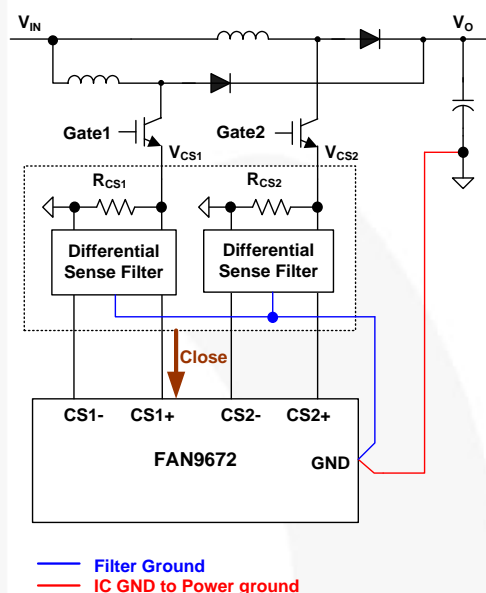


Figure 9. Current Balance Factors

### 4. Interleaving

The FAN9672 controller is used to control two channel boost converters connected in parallel. The controller operates in average-current mode and Continuous Conduction Mode (CCM). Each channel affords one-third the power when the system operates close to full load or when channel management is disabled.

Parallel power processing increases the number of power components, but the current rating of independent channels is reduced, so power semiconductors with lower current ratings can be applied. Another advantage of interleaved control is that the net output current ripple is the average of all interleaved channels' current ripple values. This results in a much lower net current ripple at the output capacitor, which extends the life cycle of the capacitor.

The switches of the two boost converters can be operated at two-channel / 180° out of phase. The interleaving controller can reduce the total ripple current of input. The FAN9672 offers two types of channel management method selectable by the user.

## 5. Channel Management / CM Control

The CM pin is used for channel management. The relationship of CM and the gain of the slave channel is shown in Figure 10. The level of CM determines the power level ( $V_{VEA}$ ) for reducing the output power for the slave PFC. The FAN9672 starts to reduce the current command ( $I_{MO} \cdot R_M$ ) for channel 2 by gain 2 when the  $V_{VEA}$  level is lower than its CM level, as Figure 11 and Figure 12 show. The output power of the slave channel is reduced in response to the reduction of current. Typical  $G_{ain2}$  is 1~0. Example: when CM2 is set in 3 V and  $V_{VEA}$  is less than the CM2 voltage, the CM block reduces the command for channel 2 as:

$$V_{gmi2+} = I_{MO} \cdot R_M \cdot G_{ain2} \quad (2)$$

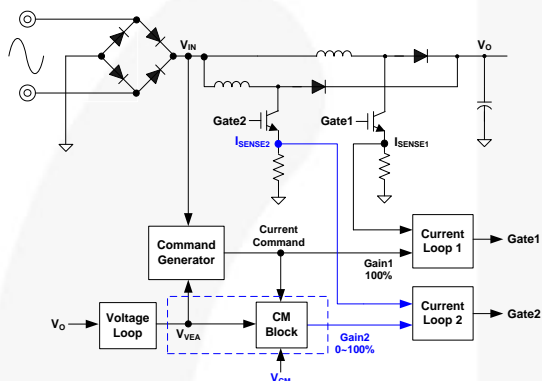


Figure 10. Channel Management / Gain Slave Channel Relationship

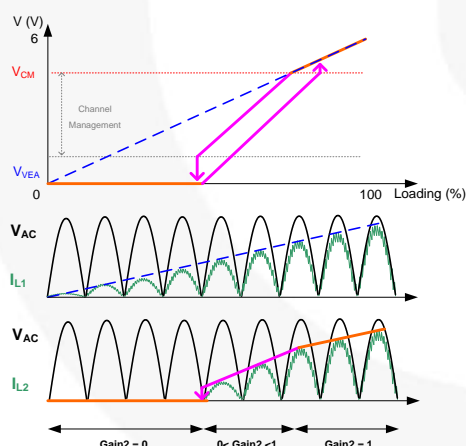


Figure 11.  $V_{VEA}$  and Gain2 Relationship

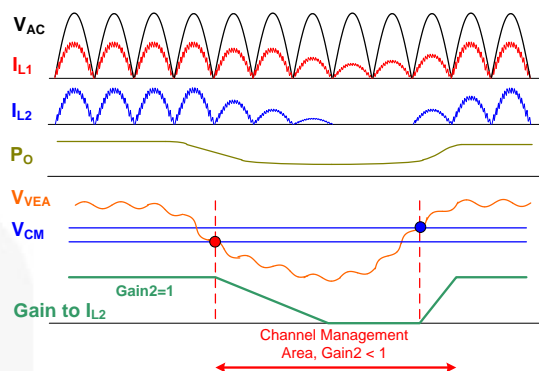


Figure 12.  $V_{VEA}$  and  $V_{CM}$  Relationship in Channel Management Operation

Table 1 describes the phase and gain change of each channel when the PFC operates at various loads. The loading decreases the gain to the slave until it is disabled. The phase CM Mode doesn't change when channel 2 is disabled as shown in Figure 13.

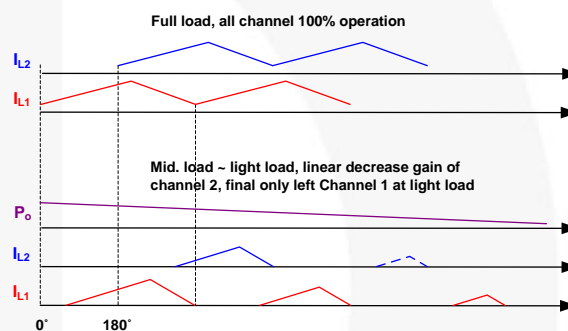


Figure 13. Phase and Gain Change of CM Control

Table 1. Phase and Gain Change of CM Control

| CM (Channel Management)             | Phase        |                   |
|-------------------------------------|--------------|-------------------|
|                                     | Channel 1    | Channel 2         |
| Heavy Load (Two Channel 100% Works) | 0° (Gain1=1) | 180° (Gain2=1)    |
| Mid. Load                           | 0° (Gain1=1) | 180° (0<Gain2<1)  |
| Light Load (Only Channel1 Left )    | 0° (Gain1=1) | Disable (Gain2=0) |

## 6. Channel Management 2: External Control

To disable the Channel Management (CM) function and control the channels with an external signal from the MCU, the configuration is shown in Figure 14. If  $V_{CM} > 4\text{ V}$ , the channel is disabled. To enable the channel,  $V_{CM}$  must be 0 V, as Figure 15 shows.

The CM pin of the slave should be connected with a switch  $S_2$  to ground. When  $V_{VEA} < V_{P2-OFF-L}$ , the slave PFC turns off. If  $V_{VEA} > V_{P2-OFF-H}$ , the slave PFC turns on. One pin of MCU must read the  $V_{VEA}$  signal to determine when to turn on / off the slave. ( $V_{P2-OFF-L}$  and  $V_{P2-OFF-H}$  are hysteresis levels required in MCU software.) When  $S_2$  turns on, CM disables and the slave works normally, as shown in Figure 16.

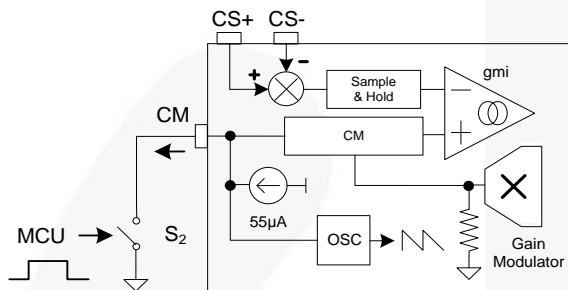


Figure 14. Channel Management by MCU

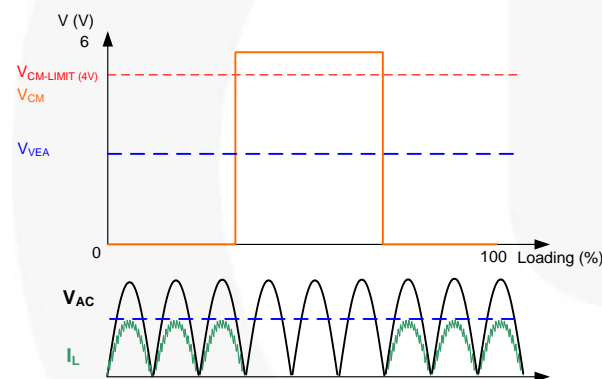


Figure 15. Channel Management by MCU

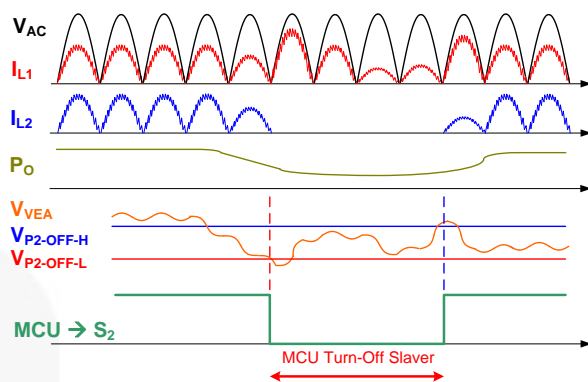


Figure 16. Channel Management by External Signal from MCU

The phase of each channel controlled by external signal changes when the loading changes, as illustrated in Table 2 and Figure 17. When the MCU disables channel 2 at mid-load ~ light load, the PFC only operation by channel 1.

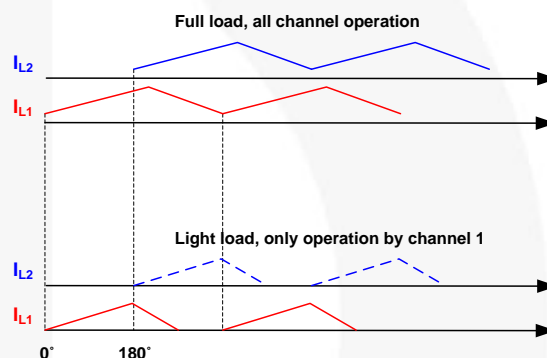


Figure 17. Phase Change under External Signal Control

Table 2. Phase Change of External Signal Control

| External Signal Control           | Phase<br>(Disable Channel: $V_{CM} > 4\text{ V}$ , Enable Channel: $V_{CM} = 0\text{ V}$ ) |                                    |
|-----------------------------------|--|------------------------------------|
|                                   | Channel 1  | Channel 2                          |
| Heavy Load (All Channels Enabled) | 0°   | 180°                               |
| Light Load (Channel2)             | 0°   | Disable ( $V_{CM2} > 4\text{ V}$ ) |
| Disable All System                | $V_{CM1} > 4\text{ V}$ , All Channels Disabled   |                                    |



## Functional Description

### Internal Oscillator (RI)

The internal oscillator frequency is determined by external resistor,  $R_{RI}$ , on the RI pin. The frequency of the oscillator is given by:

$$f_{OSC} = \frac{8 \times 10^8}{R_{RI}} \quad (3)$$

### Current-Control Loop of Boost Stage

As shown in Figure 18, there are two control loops for PFC: a current-control loop and a voltage-control loop. Based on the reference signal obtained at the IAC pin, the relationship of current loop as:

$$I_L \cdot R_{CS} = I_{MO} \cdot R_M \cdot G_{LU} = I_{IAC} \cdot G \cdot G_{LU} \cdot R_M \quad (4)$$

The current sense  $I_L \cdot R_{CS}$  is controlled by the current command from the multiplier;  $I_{MO} \cdot R_M$ . The  $I_{MO}$  is the relationship of three input factors:  $I_{AC}$ ,  $V_{EA}$ , and  $LPK$ .  $G_{ain2}$  is a gain between 0~1 from the channel management block for the slave channel.

### Voltage-Control Loop of Boost Stage

The voltage-control loop regulates PFC output voltage by using the internal error amplifier,  $G_{mv}$ , such that the FBPF voltage is the same as the internal reference voltage of 2.5 V. This stabilizes PFC output voltage and decreases the 120 Hz ripple of the PFC output voltage. PFC Over-Voltage Protection (OVP) protects the power circuit from damage from an excessive voltage in a sudden load change. When the voltage on FBPF exceeds 2.75 V, the PFC output driver shuts down.

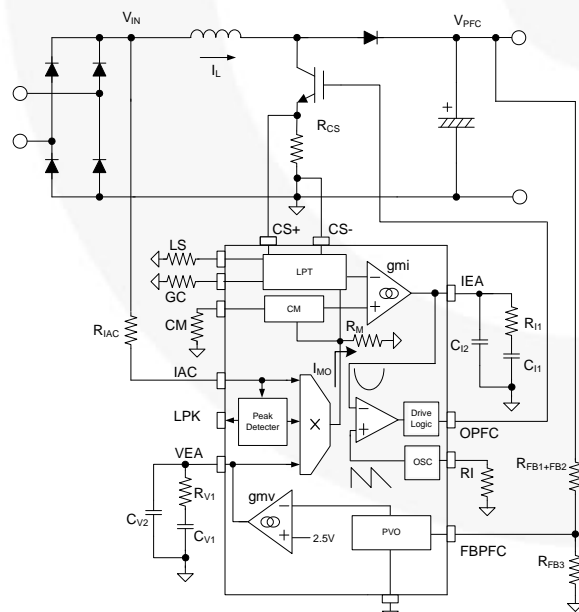


Figure 18. Gain Modulation Block

### TriFault Detect™

To improve power supply reliability, reduce system component count, and simplify compliance to UL 1950 safety standards; the FAN9672 includes Fairchild's TriFault Detect™ technology. This feature monitors FBPF for certain PFC fault conditions.

In the event of a feedback path failure, the output of the PFC can exceed operating limits. Should FBPF go to low, too high, or open; TriFault Detect senses the error and terminates the PFC output drive.

TriFault Detect is an entirely internal circuit. It requires no external components to perform its function.

### PFC Over-Voltage Protection (OVP)

FAN9672 has an auto-restart OVP function. When the feedback level,  $V_{FBPF}$ , of the PFC reaches 2.75 V (reference level is 2.5 V); the PFC gate signal stops until the output voltage decreases and  $V_{FBPF}$  returns to 2.5 V, when the PFC restarts regulation.

### Linear Predict Function (GC & LC)

The linear predict function is used to emulate the behavior of inductor current when the MOSFET is off. The resistors on the GC and LS pins ( $R_{GC}$  and  $R_{LS}$ ) are used to adjust the DC gain and compensation, respectively. The resistors are determined by:

$$R_{LS} = \frac{L_{PFC}}{1.5 \times 10^{-9} \times R_{CS} \times \left( \frac{R_{FB1} + R_{FB2} + R_{FB3}}{R_{FB3}} \right)} \quad (5)$$

$$R_{GC} = \frac{6 \times 10^6}{\left( \frac{R_{FB1} + R_{FB2} + R_{FB3}}{R_{FB3}} \right)} \quad (6)$$

### PFC Brown-In /Out (BIBO)

An internal AC Under-Voltage Protection (UVP) comparator monitors the AC input information from  $V_{IN}$ , as the waveform in Figure 19 shows. The FAN9672 disables OPFC when the  $V_{BIBO}$  is less than 1.05 V for 410 ms. If  $V_{BIBO}$  is over 1.9 V / 1.75 V, the PFC stage is enabled. The  $V_{IR}$  pin is used to set the AC input range according to Table 3.

Table 3. BIBO Setting of Various AC Input

| Input Range | AC (V)  | $R_{VIR}$ Setting (kΩ) | $R_{IAC}$ Setting (MΩ) | BIBO Level (V) |
|-------------|---------|------------------------|------------------------|----------------|
| Full-Range  | 85~ 264 | 10                     | 6                      | 85 / 75        |
| HV-Single   | 180~264 | 470                    | 12                     | 170 / 160      |

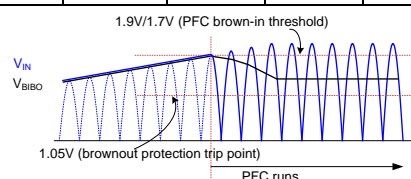


Figure 19.  $V_{BIBO}$  According to the PFC Operation

## Differential Current Sensing (CS+, CS-)

The FAN9672 has two groups of differential current sensing pins. The CS+ and CS- are the inputs of internal differential amplifier. Switching noise problems in interleaved PFC control is more critical than on a single channel, especially for current sensing. The FAN9672 uses a differential amplifier to eliminate switching noise from other channels. This makes the PFC more stable in higher power applications and eliminates switching noise from other channels. As Figure 20 shows, ground bounce can be decreased by a differential sense function.

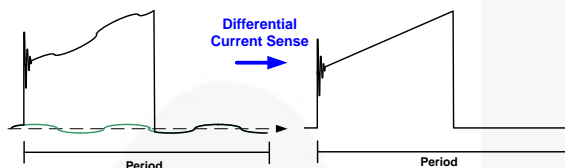


Figure 20. Differential Current Sense

## PFC Gate Driver

For high-power applications, the switch device of the system requires high driver current. The totem-pole circuit shown in Figure 21 is recommended.

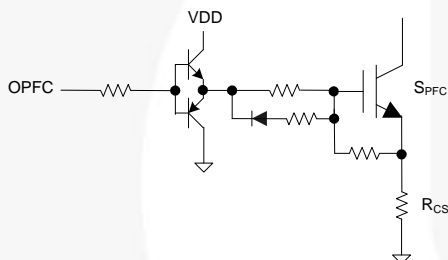


Figure 21. Gate Drive Circuit

## Current-Limit Protection

The FAN9672 includes three “cases” of current-limit protection to protect against OCP and inductor saturation:  $V_{VEA}$ ,  $I_{LIMIT}$ , and  $I_{LIMIT2}$ . The current limit thresholds,  $V_{LIMIT1}$  and  $V_{LIMIT2}$ , are controlled by the selection of the resistor for the application.

**Case 1, power (normal state):** In the normal case, current / power should be controlled by command  $V_M$  from the gain modulator. When  $V_{VEA}$  rises to 6 V, the output power and current of the system are at their peak. The power and current can't increase further.

**Case 2, current limit 1 (abnormal state):** The current command from the gain modulator is  $k \cdot I_{AC} \cdot V_{VEA} / V_{LPK}^2$ . When in abnormal state (e.g. AC cycle miss and return in a short period), the  $V_{LPK}$  has a delay before returning to the original level. This delay significantly increases the current command. If the command is greater than the clamp limit level,  $V_{LIMIT}$ , it limits as shown in Figure 22 and Figure 23. The peak current of this state can be used as the maximum current designed for each channel such that inductor current is not saturated.

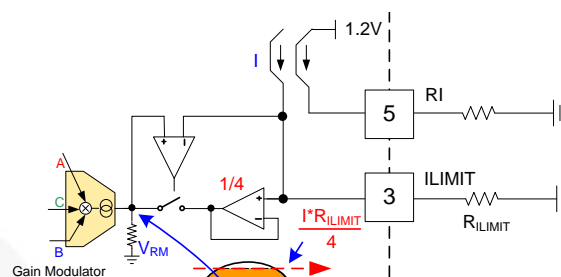


Figure 22. Current Command Limit by ILIMIT

**Case 3, current limit 2 (saturation state):** In case 3, use the level 80%~90% of maximum current of the switch device serve as the saturation protection. This current protection is a cycle-by-cycle limit.

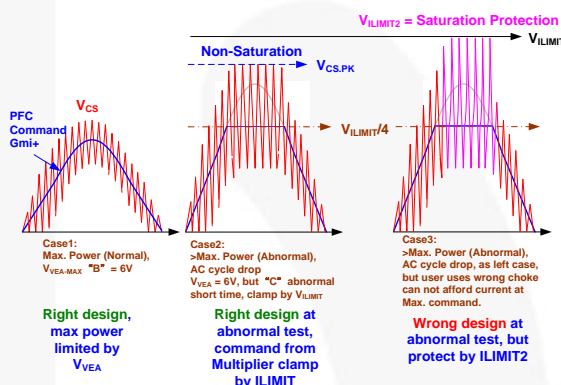


Figure 23. ILIMIT and ILIMIT2 Setting

## Programmable PFC Output Voltage (PVO)

Decreasing the PFC output voltage can improve the efficiency of the PFC stage. The PVO pin is used to modulate output voltage, as shown in Figure 24. This function is controlled by an external voltage signal on PVO pin from MCU or other source.

$V_{PVO}$  should be over 0.5 V and the relationship for  $V_{PVO}$  and  $V_{FBPFC}$  is given by:

$$V_{FBPFC} = 2.5V - \left[ \frac{V_{PVO}}{4} \right] \quad (7)$$

Example: If PVO input is 1 V;  $R_{FB1} + R_{FB2} = 3.7 \text{ M}\Omega$ ,  $R_{FB3} = 23.7 \text{ k}\Omega$ ,  $V_{FBPFC} = 2.25 \text{ V}$ , and PFC  $V_O = 354 \text{ V}$ .

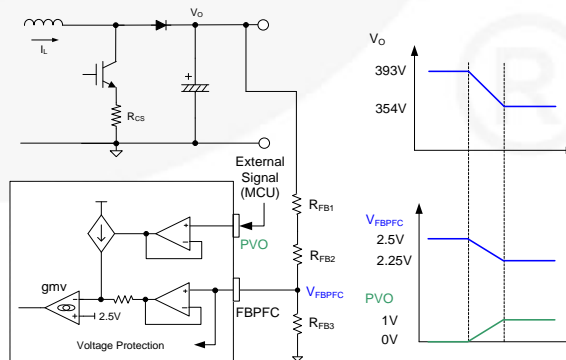


Figure 24. Programmable PFC Output Voltage

## RDYF and AC Line Off / AC “Sag”

The RDY function is used to signal MCU that the controller is ready and the power stage can start to operate. When the feedback voltage of FBPFC rises to 2.4 V, the  $V_{RDY}$  signal pulls HIGH to indicate to the MCU that the next power stage can start, as shown in Figure 25. If the AC line is OFF (or AC signal drops for a long time), the FAN9672 enters brownout and  $V_{RDY}$  pulls LOW to indicate to the MCU that the power stage should stop, as shown in Figure 26. When the AC signal drops for only a short time and the IC does not brown out, the FAN9672 recovers the  $V_{PFC}$  (same as  $V_{FBPFC}$ ) when the AC signal is restored to normal, as shown in Figure 27.

AC “sag” means the AC drops to a low level, such as 110 V / 220 V  $\rightarrow$  40 V. AC “missing” means the AC drops to 0 V. If AC drops, the PFC attempts to transfer energy to  $V_O$  before  $V_O$  drops to the 50% level. If AC is 0 V, the PFC can't transfer energy. If the level reaches 50%; the PFC stops, resets, and waits for AC to return.

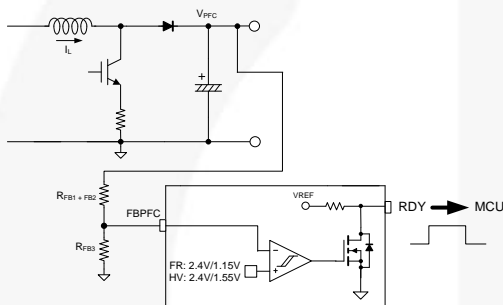


Figure 25. RDY Function to MCU

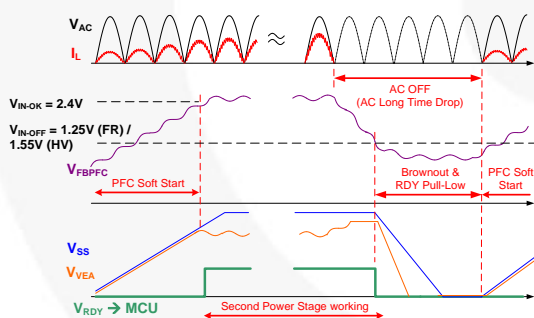


Figure 26. When AC Drops for a Long Time

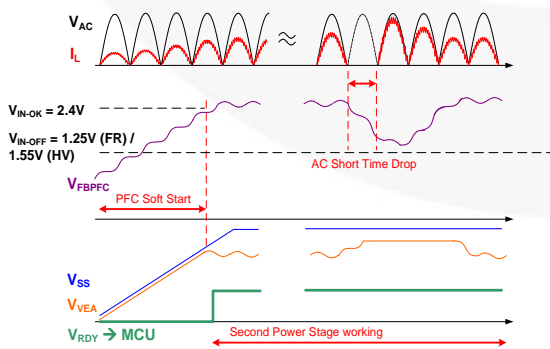


Figure 27. When AC Drops Only Briefly

## Soft-Start

Soft-start is combined with RDY pin operation, as Figure 25 through Figure 27 show. During startup, the RDY pin remains LOW until the PFC output voltage reaches 96% of its nominal value. When the supply voltage of the downstream converter is controlled by the RDY pin, the PFC stage starts with no load since the downstream converter does not operate until the PFC output voltage reaches a required level.

Usually, the error amplifier output,  $V_{EA}$ , is saturated to HIGH during startup because the actual output voltage is less than the target value.  $V_{EA}$  remains saturated to HIGH until the PFC output voltage reaches its target value. Once the PFC output reaches its target value, the error amplifier comes out of saturation. However, it takes several line cycles for  $V_{EA}$  to drop to its proper value for output regulation, which delivers more power to the load than required, causing output voltage overshoot. To prevent output voltage overshoot during startup caused by the saturation of error amplifier, the FAN9672 clamps the error amplifier output voltage ( $V_{EA}$ ) by the  $V_{SS}$  value until PFC output reaches 96% of its nominal value.

## Input Voltage Peak Detection

The input AC peak voltage is sensed at the IAC pin. The input voltage is used for feed-forward control in the gain modulator circuit and output to the LPK pin for MCU use. All the functions require the RMS value of the input voltage waveform. Since the RMS value of the AC input voltage is directly proportional to its peak, it is sufficient to find the peak instead of the more-complicated and slower method of integrating the input voltage over a half line cycle. The internal circuit of the IAC pin works with peak detection of the input AC waveform, as Figure 28 shows.

One of the important benefits of this approach is that the peak indicates the correct RMS value even at no load, when the HF filter capacitor at the input side of the boost converter is not discharged around the zero-crossing of the line waveform. Another notable benefit is that, during line transients when the peak exceeds the previously measured value, the input-voltage feed-forward circuit can react immediately, without waiting for a valid integral value at the end of the half line period. Furthermore, lack of zero-crossing detection lead to false integrator detection, while the peak detector works properly during light-load operation.

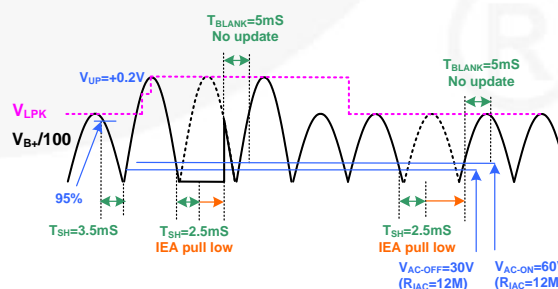


Figure 28. Waveform of LPK Function

The relationship of  $V_{IN.PK}$  to  $V_{LPK}$  is shown in Figure 29. The peak detection circuits detect the  $V_{IN}$  information from  $I_{AC}$ .  $R_{LPK}$  sets the ratio of  $V_{IN}$  to  $V_{LPK}$  via a resistor  $R_{RLPK}$ , as described in Equation (8). The target value of  $V_{LPK}$  is one percent (1%) of  $V_{INpk}$ . The maximum  $V_{LPK}$  cannot be over 3.8 V when system operation is at maximum AC input.

As in the below design example, assume the maximum  $V_{IN.PK}$  at 373 V (264 V<sub>AC</sub>), the relationship of  $V_{IN.PK} / V_{LPK}$  is 100, and  $V_{LPK} = 3.73 \text{ V} < 3.8 \text{ V}$ .

$$V_{LPK} = \frac{V_{IN.PK}}{100} \times \frac{R_{RLPK}}{12.4k} \quad (8)$$

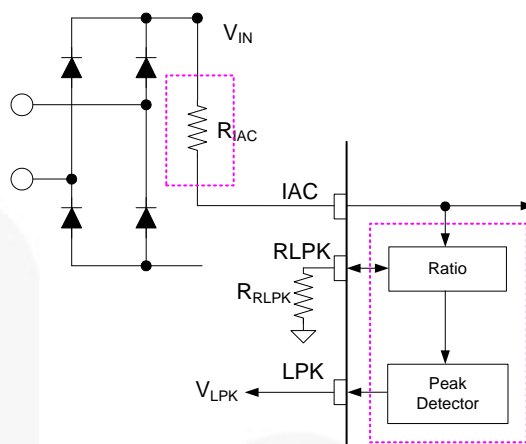


Figure 29. Relationship of  $V_{IN.PK}$  to  $V_{LPK}$

## Typical Performance Characteristics

Typical characteristics are provided at  $V_{DD} = 15\text{ V}$  unless otherwise noted.

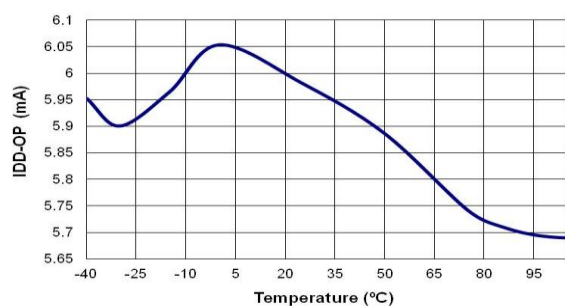


Figure 30.  $I_{DD-OP}$  vs. Temperature

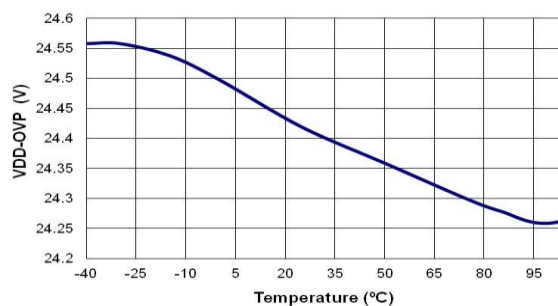


Figure 31.  $V_{DD-OPP}$  vs. Temperature

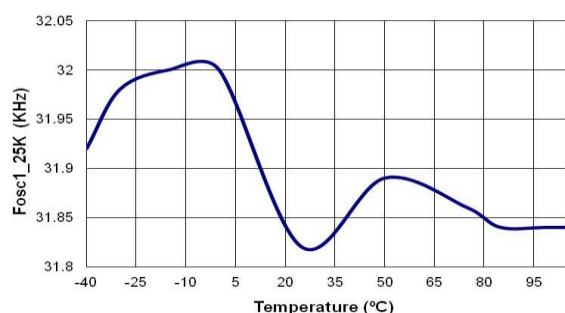


Figure 32.  $f_{osc}$  vs. Temperature

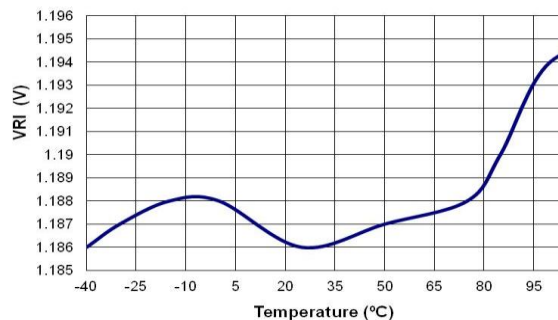


Figure 33.  $V_{RI}$  vs. Temperature

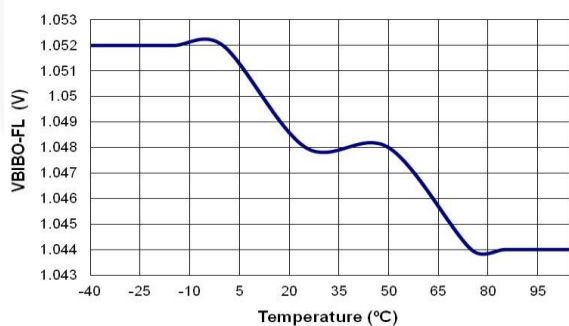


Figure 34.  $V_{BIBO-FL}$  vs. Temperature

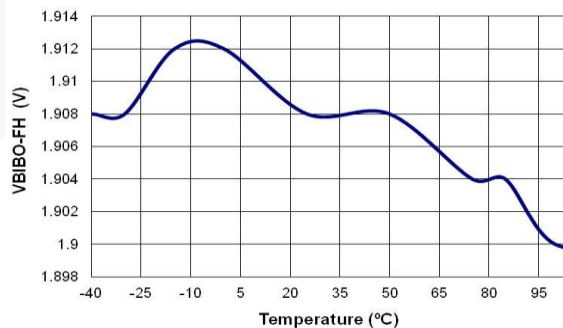


Figure 35.  $V_{BIBO-FH}$  vs. Temperature

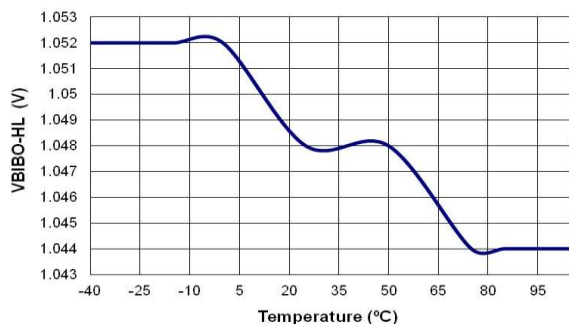


Figure 36.  $V_{BIBO-HL}$  vs. Temperature

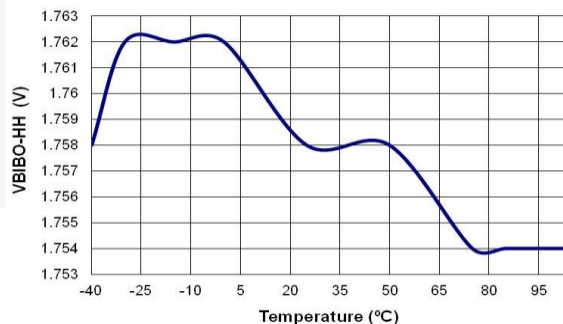


Figure 37.  $V_{BIBO-HH}$  vs. Temperature



## Typical Performance Characteristics

Typical characteristics are provided at  $V_{DD} = 15\text{ V}$  unless otherwise noted.

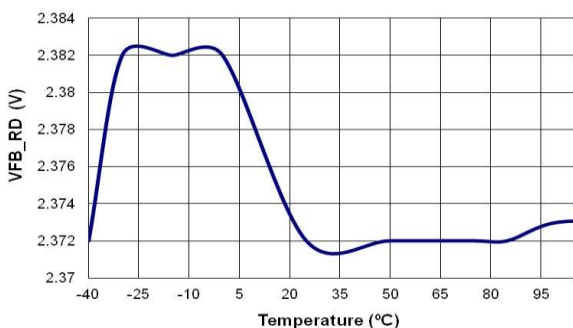


Figure 38.  $V_{FBPFC-RD}$  vs. Temperature

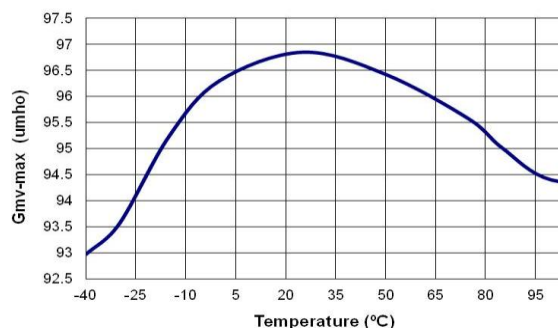


Figure 39.  $G_{mV-MAX}$  vs. Temperature

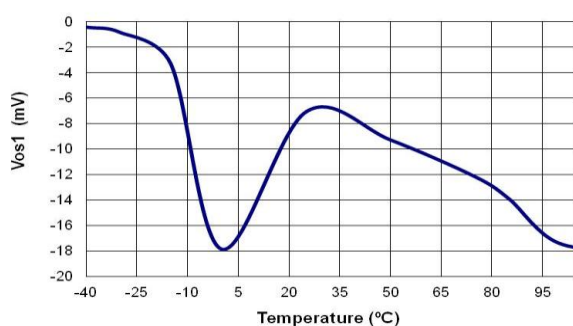


Figure 40.  $V_{OFFSET}$  vs. Temperature

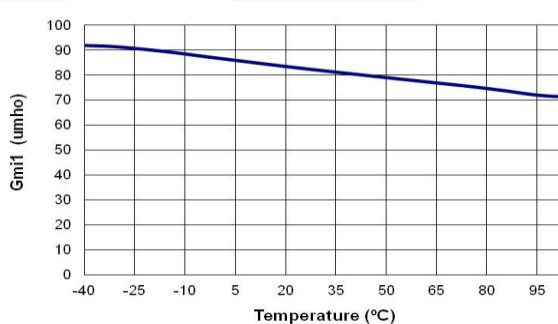


Figure 41.  $G_{mI}$  vs. Temperature

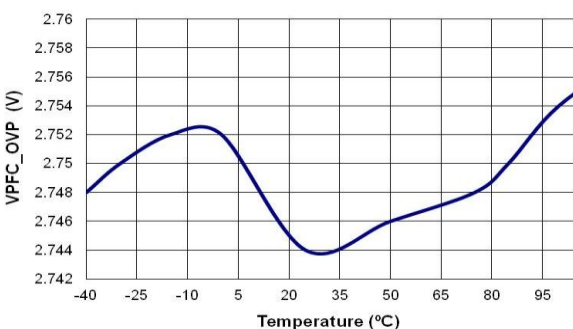


Figure 42.  $V_{PFC-OVP}$  vs. Temperature

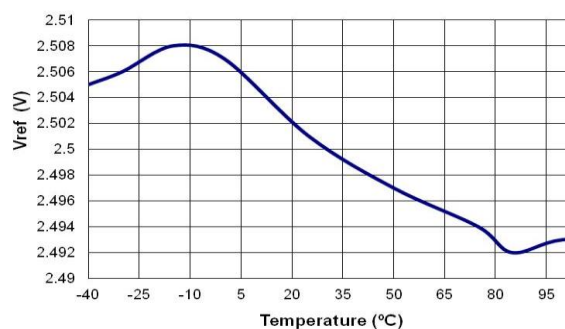


Figure 43.  $V_{REF}$  vs. Temperature

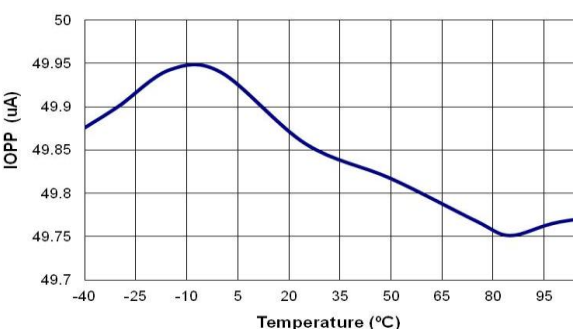


Figure 44.  $I_{LIMIT}$  vs. Temperature

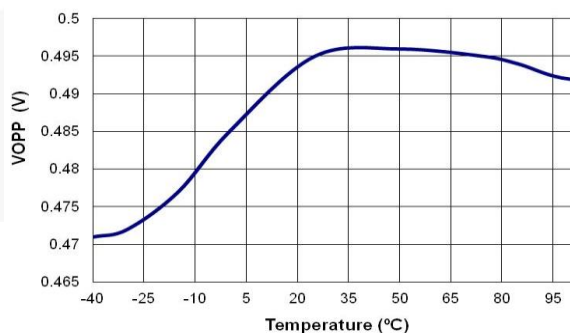


Figure 45.  $V_{LIMIT}$  vs. Temperature

## Typical Performance Characteristics

Typical characteristics are provided at  $V_{DD} = 15\text{ V}$  unless otherwise noted.

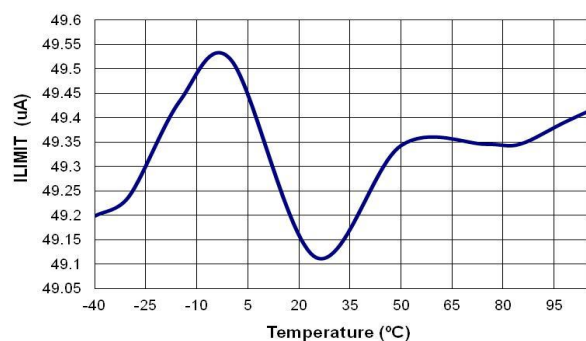


Figure 46.  $I_{LIMIT2}$  vs. Temperature

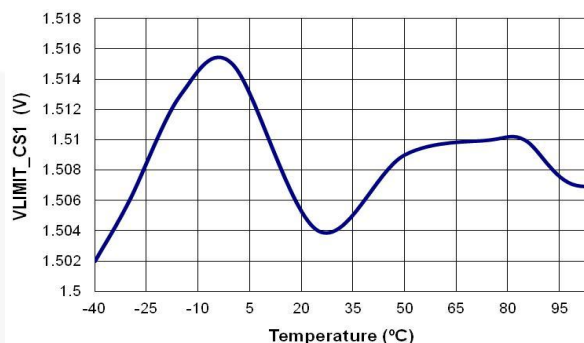


Figure 47.  $V_{LIMIT2-CS1}$  vs. Temperature

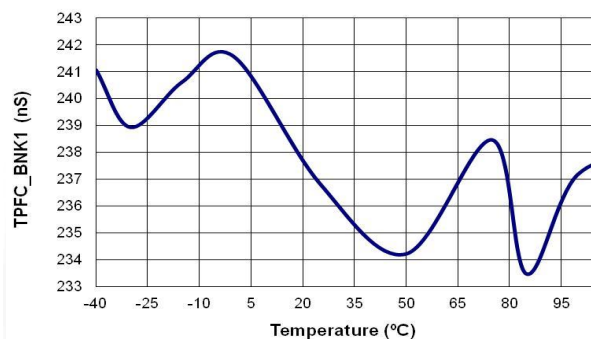


Figure 48.  $t_{PFC-BNK}$  vs. Temperature

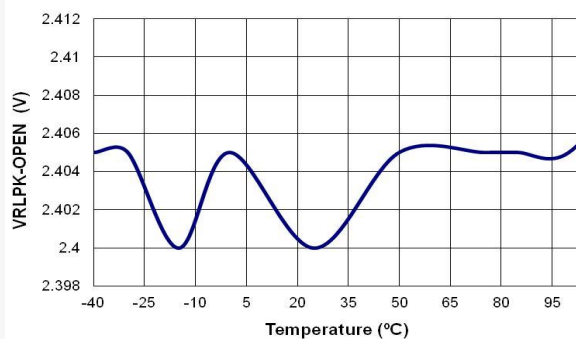


Figure 49.  $V_{RLPK-OPEN}$  vs. Temperature

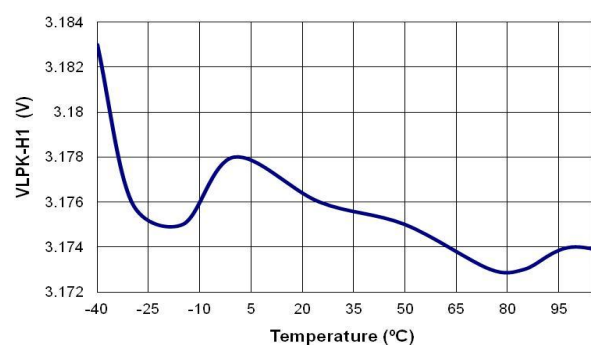


Figure 50.  $V_{LPK-H1}$  vs. Temperature

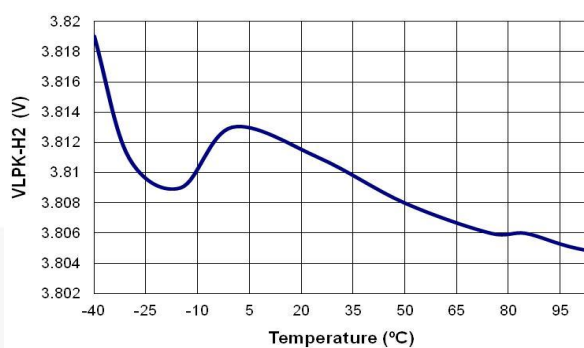


Figure 51.  $V_{LPK-H2}$  vs. Temperature

## Typical Application Circuit

| Application                   | Output Power | Input Voltage           | Output Voltage / Output Current |
|-------------------------------|--------------|-------------------------|---------------------------------|
| Single-Stage, Two-Channel PFC | 3400 W       | 180~264 V <sub>AC</sub> | 393 V / 8.48 A                  |

## Features

- 180 V<sub>AC</sub> ~264 V, Two-Channel PFC Using FAN9672
- Switch-Charge Technique of Gain Modulator for Better PF and Lower THD
- 40 kHz Low Switching Frequency Operation with IGBT
- Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Protection ( $I_{LIMIT}$ ), Inductor Saturation Protection ( $I_{LIMIT2}$ )

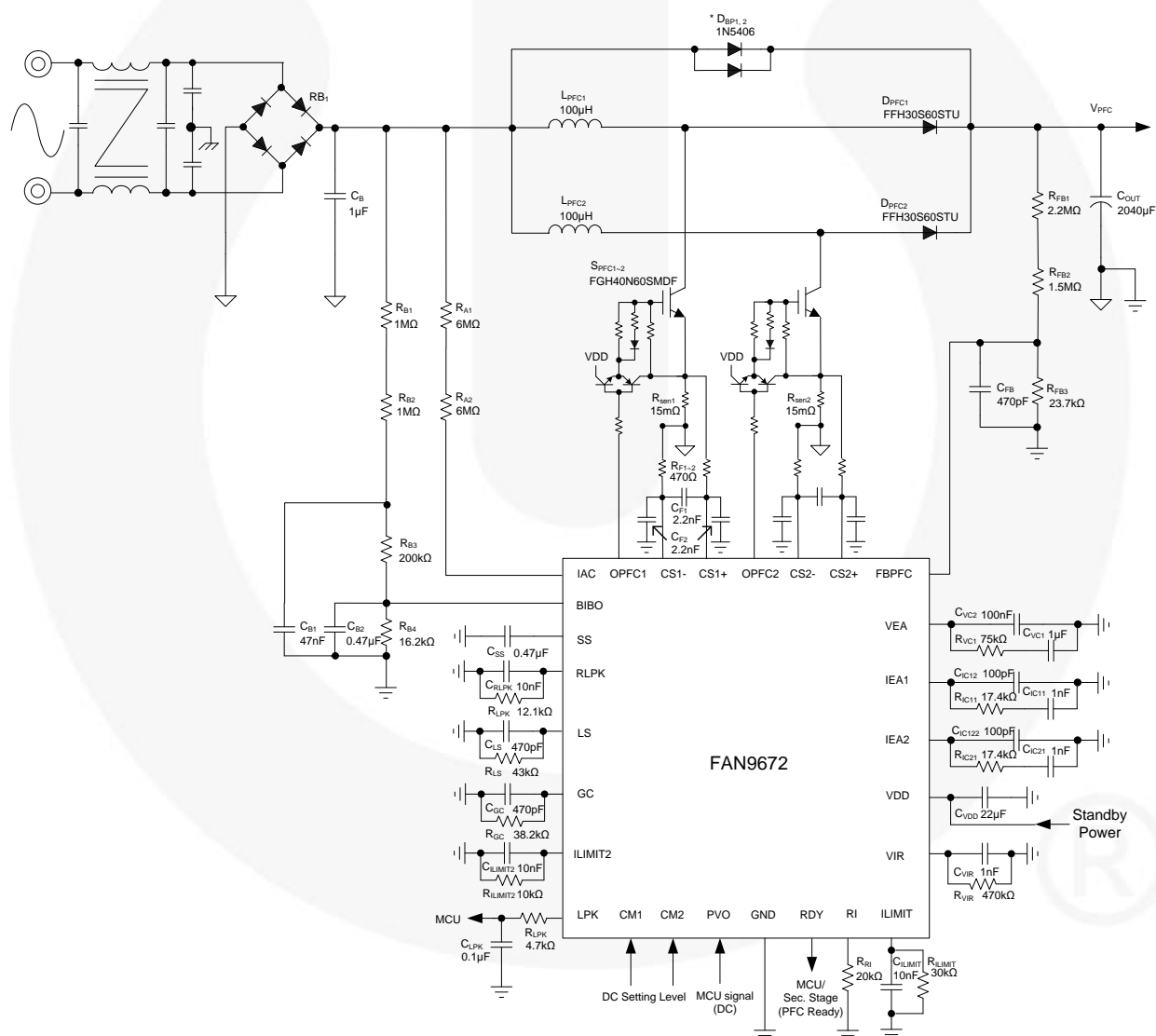


Figure 52. Schematic of Design Example



## Specifications

- $V_{DD}$  Maximum Rating: 20 V
- $V_{DD}$  OVP: 24 V
- $V_{CC}$  UVLO: 10.3 V / 12.8 V
- PVO: 0 V~1 V
- PFC Soft-Start:  $C_{SS} = 0.47 \mu F$
- Brown-In / Out: 170 V / 160 V
- Switching Frequency: 40 kHz
- Gate Clamp: 2.4 V / 1.55 V (96% / 62%)
- $R_{IAC}$ : 12 M $\Omega$

## Inductor Schematic Diagram

- Core: QP3925H (3C94)
- Bobbin: 7 Pins

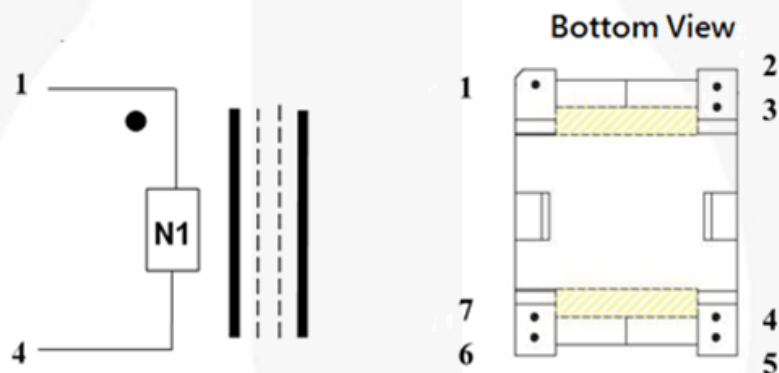


Figure 53. Inductor Schematic Diagram

Table 4. Winding Specification

| No. | Winding  | Pin (S $\rightarrow$ F) | Wire              | Turns | Winding Method   |
|-----|--|-------------------------|-------------------|-------|------------------|
| 1   | N1   | 1 $\rightarrow$ 6, 7    | 0.2 $\phi$ ×35 *1 | 25    | Solenoid Winding |
| 2   | Insulation: Polyester Tape $t = 0.025$ mm, 2 Layer |                         |                   |       |                  |
| 3   | Copper-Foil 1.2T to PIN4, 5                        |                         |                   |       |                  |

Table 5. MOSFET and Diode Reference Specification

| IGBTs          |              |
|----------------|--------------|
| Voltage Rating |              |
| 600 V (IGBT)   | FGH40N60SMDF |
| Boost Diodes   |              |
| 600 V          | FFH30S60STU  |

## Typical Performance

**Table 6. Efficiency**

|                      | 25% Load | 50% Load | 75% Load | 100% Load |
|----------------------|----------|----------|----------|-----------|
| <b>180 V / 50 Hz</b> | 96.31    | 96.63    | 96.60    | 96.41     |
| <b>220 V / 50 Hz</b> | 97.01    | 97.34    | 97.33    | 97.17     |
| <b>264 V / 50 Hz</b> | 97.76    | 97.92    | 97.92    | 97.77     |

**Table 7. Power Factor**

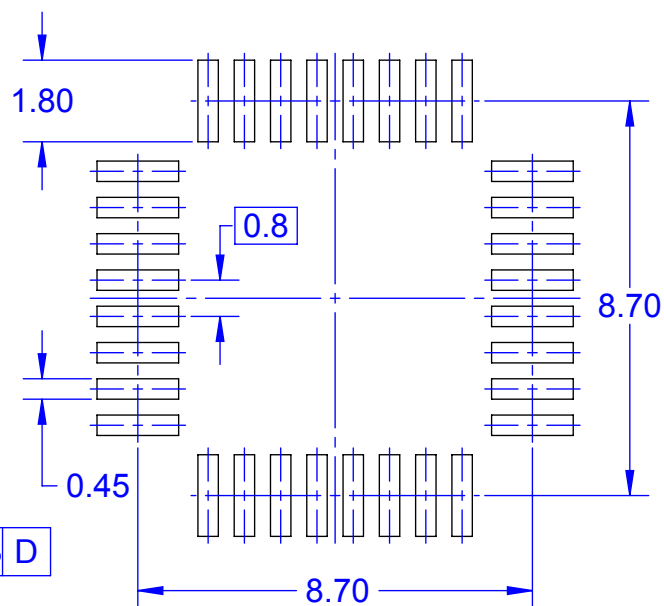
|                      | 25% Load | 50% Load | 75% Load | 100% Load |
|----------------------|----------|----------|----------|-----------|
| <b>180 V / 50 Hz</b> | 0.9546   | 0.9857   | 0.9917   | 0.9955    |
| <b>220 V / 50 Hz</b> | 0.9397   | 0.9694   | 0.9780   | 0.9879    |
| <b>264 V / 50 Hz</b> | 0.8402   | 0.9158   | 0.9337   | 0.9500    |

**Table 8. Total Harmonic Distortion**

|                      | 25% Load | 50% Load | 75% Load | 100% Load |
|----------------------|----------|----------|----------|-----------|
| <b>180 V / 50 Hz</b> | 14.51    | 10.98    | 8.87     | 6.96      |
| <b>220 V / 50 Hz</b> | 20.12    | 17.24    | 15.30    | 11.87     |
| <b>264 V / 50 Hz</b> | 50.52    | 36.86    | 33.11    | 29.26     |

## System Design Precautions

- Pay attention to the inrush current when AC input is first connected to the boost PFC convertor. It is recommended to use NTC and a parallel connected relay circuit to reduce inrush current.
- Add bypass diode to provide a path for inrush current when PFC start up.
- The PFC stage is normally used to provide power to a downstream DC-DC or inverter. It's recommend that downstream power stage is enabled to operate at full load once the PFC output voltage has reaches a level close to the specified steady-state value.
- The PVO function is used to change the output voltage of PFC,  $V_{PFC}$ . The  $V_{PFC}$  should be kept at least 25 V higher than  $V_{IN}$ .



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910

**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local  
Sales Representative

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[FAN9672Q](#)

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)

Email: [org@lifeelectronics.ru](mailto:org@lifeelectronics.ru)

[www.lifeelectronics.ru](http://www.lifeelectronics.ru)