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Kind regards,

Team Nexperia



# PNTC123JMB

NPN resistor-equipped transistor; R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

Rev. 1 — 16 May 2012

Product data sheet

## 1. Product profile

### 1.1 General description

NPN Resistor-Equipped Transistor (RET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA123JMB.

### 1.2 Features and benefits

- 100 mA output current capability
- Reduces component count
- Built-in bias resistors
- Reduces pick and place costs
- Simplifies circuit design
- AEC-Q101 qualified
- Leadless ultra small SMD plastic package
- Low package height of 0.37 mm

### 1.3 Applications

- Low-current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications
- Mobile applications

### 1.4 Quick reference data

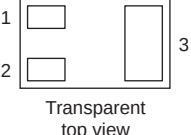
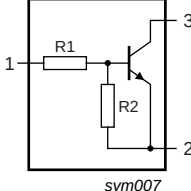
Table 1. Quick reference data

| Symbol           | Parameter                 | Conditions               | Min  | Typ | Max  | Unit       |
|------------------|---------------------------|--------------------------|------|-----|------|------------|
| V <sub>CEO</sub> | collector-emitter voltage | open base                | -    | -   | 50   | V          |
| I <sub>O</sub>   | output current            |                          | -    | -   | 100  | mA         |
| R1               | bias resistor 1 (input)   | T <sub>amb</sub> = 25 °C | 1.54 | 2.2 | 2.86 | k $\Omega$ |
| R2/R1            | bias resistor ratio       |                          | 17   | 21  | 26   |            |



2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description        | Simplified outline                                                                                            | Graphic symbol                                                                      |
|-----|--------|--------------------|---------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 1   | I      | input (base)       |  <p>SOT883B (DFN1006B-3)</p> |  |
| 2   | G      | GND (emitter)      |                                                                                                               |                                                                                     |
| 3   | O      | output (collector) |                                                                                                               |                                                                                     |

3. Ordering information

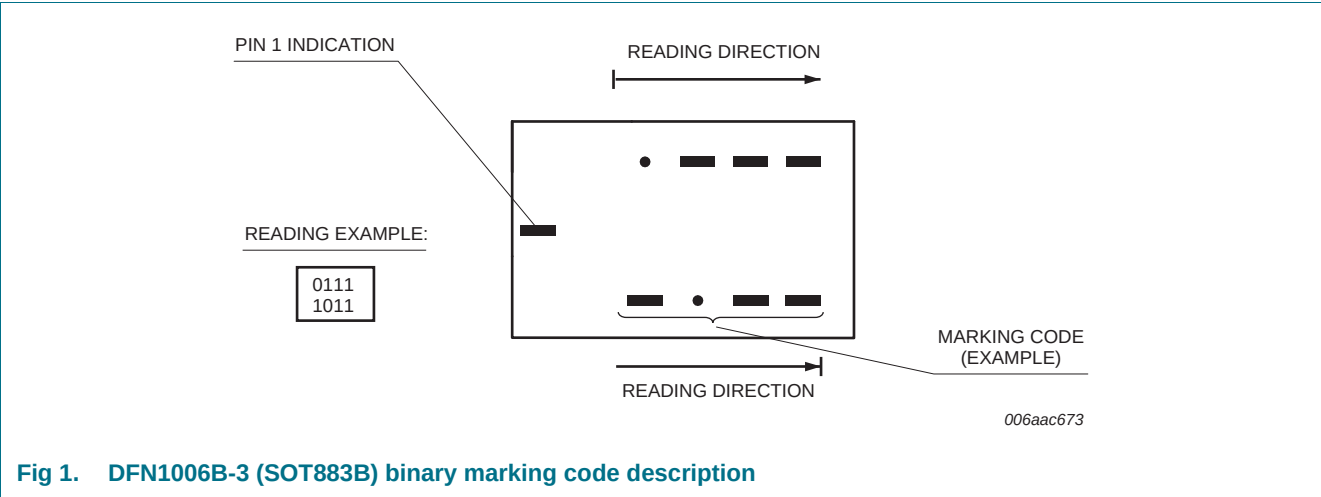
Table 3. Ordering information

| Type number | Package    |                                                                                |         |
|-------------|------------|--------------------------------------------------------------------------------|---------|
|             | Name       | Description                                                                    | Version |
| PDTC123JMB  | DFN1006B-3 | Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm | SOT883B |

4. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PDTC123JMB  | 0001 0111    |



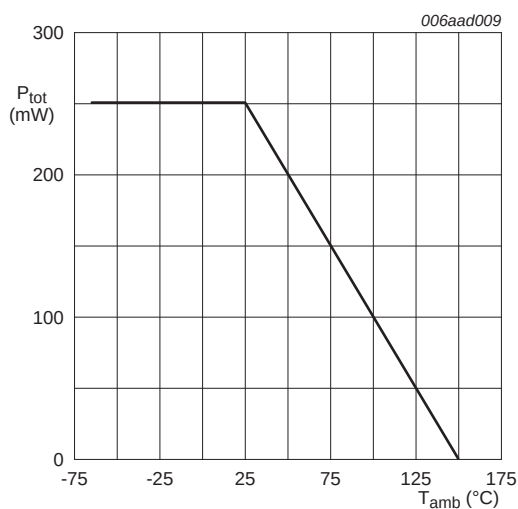
## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol    | Parameter                 | Conditions                               | Min | Max | Unit |
|-----------|---------------------------|------------------------------------------|-----|-----|------|
| $V_{CBO}$ | collector-base voltage    | open emitter                             | -   | 50  | V    |
| $V_{CEO}$ | collector-emitter voltage | open base                                | -   | 50  | V    |
| $V_{EBO}$ | emitter-base voltage      | open collector                           | -   | 10  | V    |
| $V_I$     | input voltage             | positive                                 | -   | 12  | V    |
|           |                           | negative                                 | -   | -5  | V    |
| $I_O$     | output current            |                                          | -   | 100 | mA   |
| $I_{CM}$  | peak collector current    | pulsed; $t_p \leq 1$ ms                  | -   | 100 | mA   |
| $P_{tot}$ | total power dissipation   | $T_{amb} \leq 25$ °C <a href="#">[1]</a> | -   | 250 | mW   |
| $T_j$     | junction temperature      |                                          | -   | 150 | °C   |
| $T_{amb}$ | ambient temperature       |                                          | -65 | 150 | °C   |
| $T_{stg}$ | storage temperature       |                                          | -65 | 150 | °C   |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

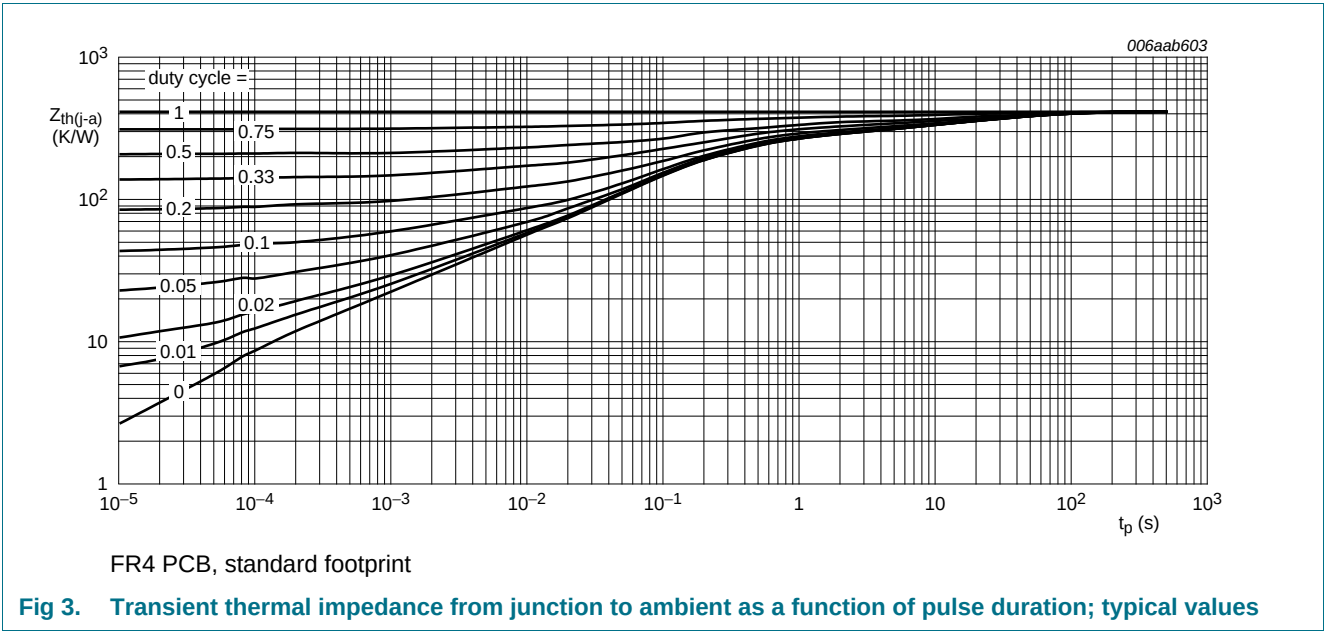
**Fig 2. Power derating curve for DFN1006B-3 (SOT883B)**

6. Thermal characteristics

Table 6. Thermal characteristics

| Symbol        | Parameter                                   | Conditions  | Min | Typ | Max | Unit |
|---------------|---------------------------------------------|-------------|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | -   | -   | 500 | K/W  |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

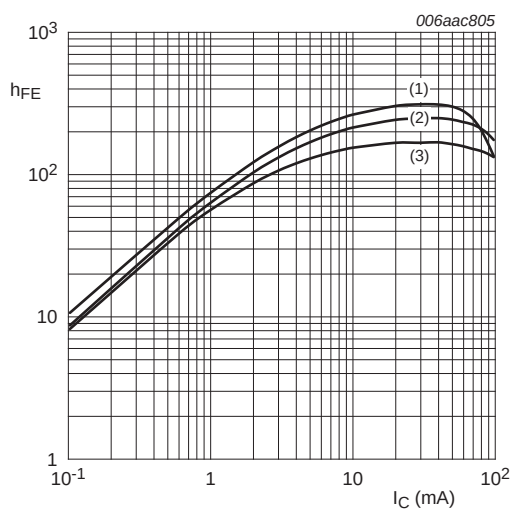


## 7. Characteristics

**Table 7. Characteristics**

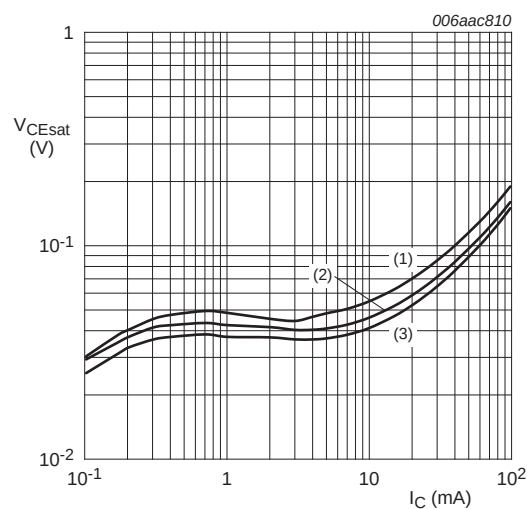
| Symbol       | Parameter                            | Conditions                                                                                                                             | Min  | Typ  | Max  | Unit          |
|--------------|--------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{CBO}$    | collector-base cut-off current       | $V_{CB} = 50 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $T_{amb} = 25 \text{ }^{\circ}\text{C}$                                                | -    | -    | 100  | nA            |
| $I_{CEO}$    | collector-emitter cut-off current    | $V_{CE} = 30 \text{ V}$ ; $I_B = 0 \text{ A}$ ; $T_{amb} = 25 \text{ }^{\circ}\text{C}$                                                | -    | -    | 1    | $\mu\text{A}$ |
|              |                                      | $V_{CE} = 30 \text{ V}$ ; $I_B = 0 \text{ A}$ ; $T_j = 150 \text{ }^{\circ}\text{C}$                                                   | -    | -    | 5    | $\mu\text{A}$ |
| $I_{EBO}$    | emitter-base cut-off current         | $V_{EB} = 5 \text{ V}$ ; $I_C = 0 \text{ A}$ ; $T_{amb} = 25 \text{ }^{\circ}\text{C}$                                                 | -    | -    | 180  | $\mu\text{A}$ |
| $h_{FE}$     | DC current gain                      | $V_{CE} = 5 \text{ V}$ ; $I_C = 10 \text{ mA}$ ; $T_{amb} = 25 \text{ }^{\circ}\text{C}$                                               | 100  | -    | -    |               |
| $V_{CEsat}$  | collector-emitter saturation voltage | $I_C = 5 \text{ mA}$ ; $I_B = 0.25 \text{ mA}$ ; $T_{amb} = 25 \text{ }^{\circ}\text{C}$                                               | -    | -    | 100  | mV            |
| $V_{I(off)}$ | off-state input voltage              | $V_{CE} = 5 \text{ V}$ ; $I_C = 100 \text{ } \mu\text{A}$ ; $T_{amb} = 25 \text{ }^{\circ}\text{C}$                                    | -    | 0.6  | 0.5  | V             |
| $V_{I(on)}$  | on-state input voltage               | $V_{CE} = 0.3 \text{ V}$ ; $I_C = 5 \text{ mA}$ ; $T_{amb} = 25 \text{ }^{\circ}\text{C}$                                              | 1.1  | 0.75 | -    | V             |
| R1           | bias resistor 1 (input)              | $T_{amb} = 25 \text{ }^{\circ}\text{C}$                                                                                                | 1.54 | 2.2  | 2.86 | kΩ            |
| R2/R1        | bias resistor ratio                  |                                                                                                                                        | 17   | 21   | 26   |               |
| $C_C$        | collector capacitance                | $V_{CB} = 10 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $i_e = 0 \text{ A}$ ;<br>$f = 1 \text{ MHz}$ ; $T_{amb} = 25 \text{ }^{\circ}\text{C}$ | -    | -    | 2.5  | pF            |
| $f_T$        | transition frequency                 | $V_{CE} = 5 \text{ V}$ ; $I_C = 10 \text{ mA}$ ; $f = 100 \text{ MHz}$ ;<br>$T_{amb} = 25 \text{ }^{\circ}\text{C}$                    | [1]  | 230  | -    | MHz           |

[1] Characteristics of built-in transistor.



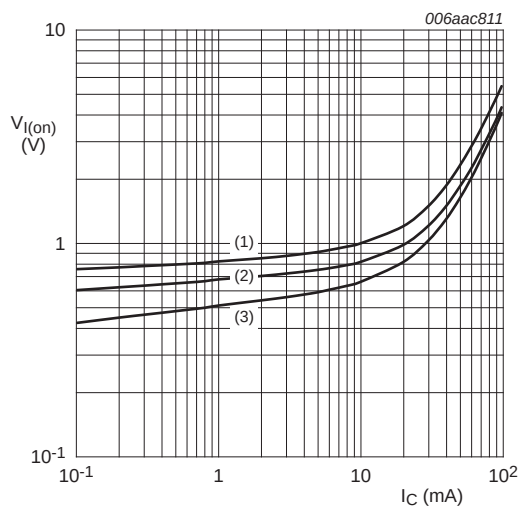
$V_{CE} = 5 \text{ V}$   
 (1)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$

**Fig 4. DC current gain as a function of collector current; typical values**



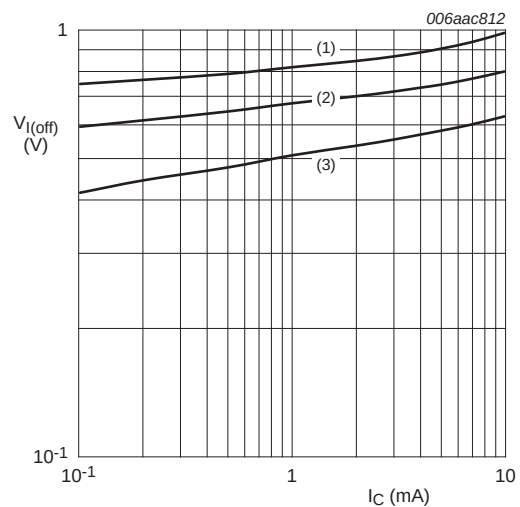
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$

**Fig 5. Collector-emitter saturation voltage as a function of collector current; typical values**



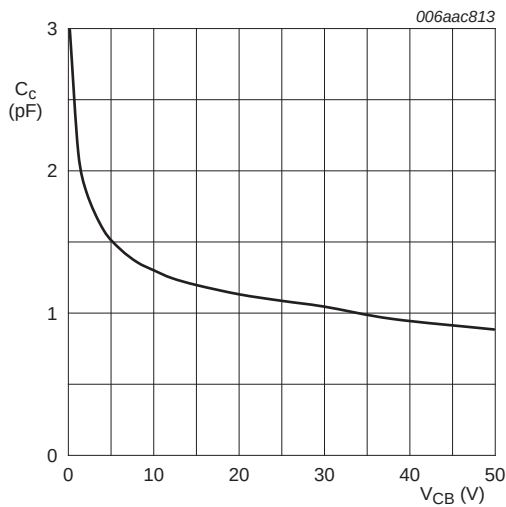
$V_{CE} = 0.3\text{ V}$   
(1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$   
(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
(3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 6. On-state input voltage as a function of collector current; typical values



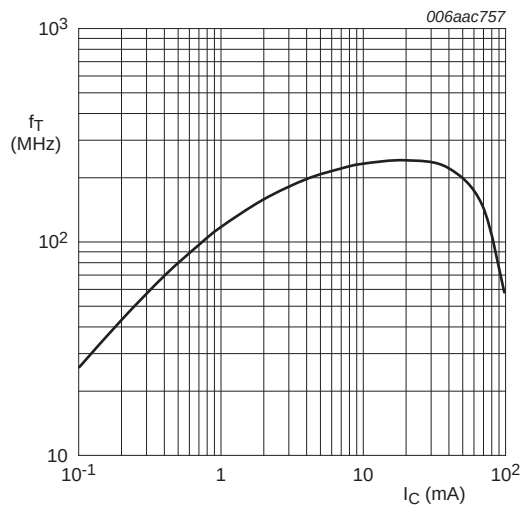
$V_{CE} = 5\text{ V}$   
(1)  $T_{amb} = -40\text{ }^{\circ}\text{C}$   
(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
(3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 7. Off-state input voltage as a function of collector current; typical values



$f = 1\text{ MHz}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 8. Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 9. Transition frequency as a function of collector current; typical values of built-in transistor

## 8. Test information

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

9. Package outline

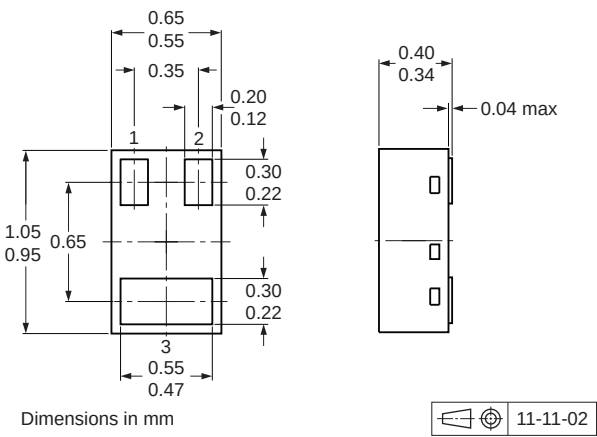


Fig 10. Package outline SOT883B (DFN1006B-3)

10. Soldering

Footprint information for reflow soldering

SOT883B

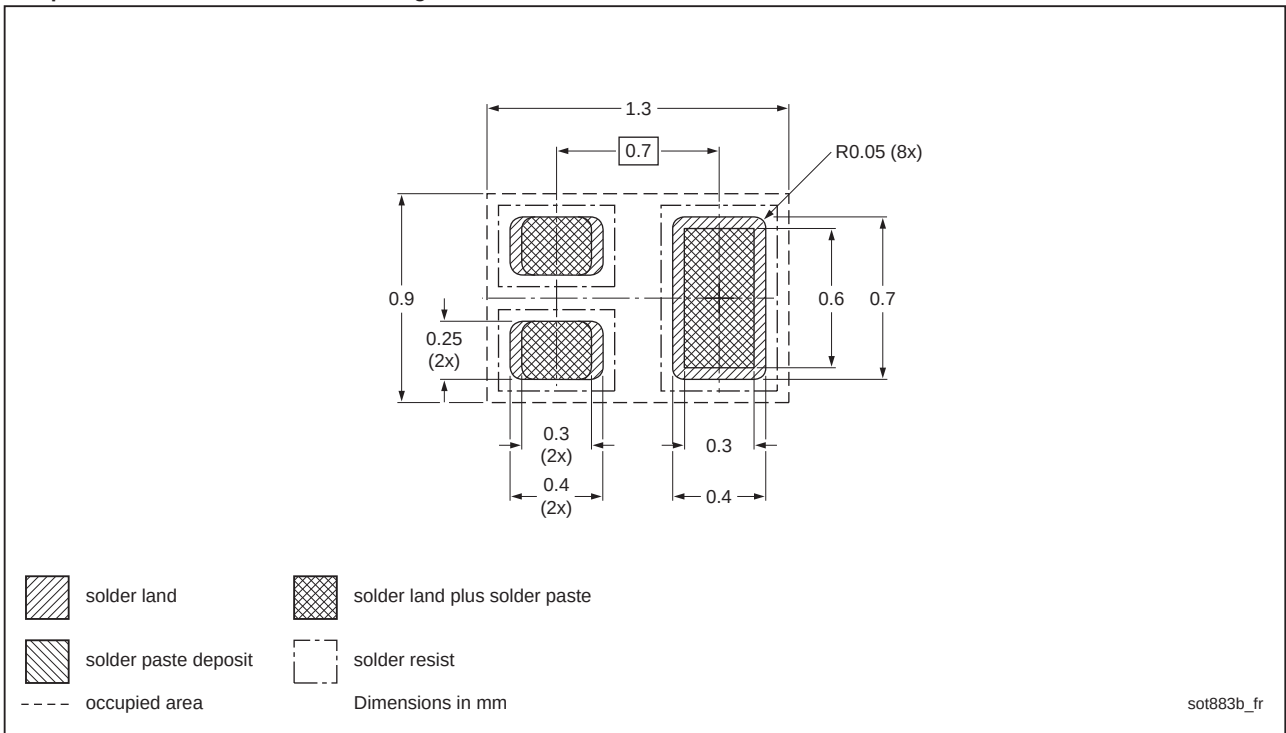


Fig 11. Reflow soldering footprint for SOT883B (DFN1006B-3)



## 11. Revision history

Table 8. Revision history

| Document ID    | Release date | Data sheet status  | Change notice | Supersedes |
|----------------|--------------|--------------------|---------------|------------|
| PDTC123JMB v.1 | 20120516     | Product data sheet | -             | -          |

## 12. Legal information

### 12.1 Data sheet status

| Document status <sup>[1] [2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|------------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet       | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet     | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet         | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

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Document identifier: PDTC123JMB

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