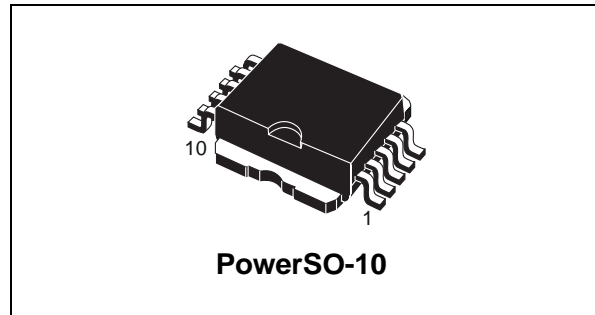


Single channel high-side driver

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN610SP-E	10m Ω	45 A	36V

- ECOPACK[®]: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Output current: 45 A
- CMOS compatible inputs
- Proportional load current sense
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Very low standby power consumption
- Protection against loss of ground and loss of V_{CC}
- Reverse battery protected
- In compliance with the 2002/95/EC european directive



Description

The VN610SP-E is a monolithic device made using STMicroelectronics[™] VIPower[™] M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio).

Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSO-10 [™]	VN610SP-E	VN610SPTR-E

Contents

- 1 Block diagram and pin description 5**

- 2 Electrical specifications 6**
 - 2.1 Absolute maximum ratings 6
 - 2.2 Thermal data 7
 - 2.3 Electrical characteristics 8
 - 2.4 Electrical characteristics curves 15

- 3 Application information 17**
 - 3.1 GND protection network against reverse battery 17
 - 3.1.1 Solution 1: a resistor in the ground line (R_{GND} only) 17
 - 3.1.2 Solution 2: a diode (D_{GND}) in the ground line 18
 - 3.2 Load dump protection 18
 - 3.3 MCU I/O protection 18
 - 3.4 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$) 19

- 4 Package and PCB thermal data 20**
 - 4.1 PowerSO-10 thermal data 20

- 5 Package and packing information 23**
 - 5.1 ECOPACK[®] packages 23
 - 5.2 PowerSO-10 mechanical data 23
 - 5.3 PowerSO-10 packing information 25

- 6 Revision history 26**

List of tables

Table 1.	Device summary	1
Table 2.	Suggested connections for unused and not connected pins	5
Table 3.	Absolute maximum ratings	6
Table 4.	Thermal data.	7
Table 5.	Power	8
Table 6.	Protections	8
Table 7.	V _{CC} - output diode	9
Table 8.	Current sense ($9\text{ V} \leq V_{CC} \leq 16\text{ V}$).	9
Table 9.	Switching ($V_{CC} = 13\text{ V}$).	10
Table 10.	Logic inputs.	10
Table 11.	Truth table.	11
Table 12.	Electrical transient requirements on V _{CC} pin (part 1/3).	13
Table 13.	Electrical transient requirements on V _{CC} pin (part 2/3).	13
Table 14.	Electrical transient requirements on V _{CC} pin (part 3/3).	13
Table 15.	Thermal parameters	22
Table 16.	PowerSO-10 mechanical data	24
Table 17.	Document revision history	26

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	5
Figure 3.	Current and voltage conventions	6
Figure 4.	I_{OUT}/I_{SENSE} versus I_{OUT}	11
Figure 5.	Switching characteristics	12
Figure 6.	Waveforms	14
Figure 7.	Off-state output current	15
Figure 8.	High level input current	15
Figure 9.	Input low level	15
Figure 10.	Input high level	15
Figure 11.	Input clamp voltage	15
Figure 12.	Input hysteresis voltage	15
Figure 13.	Overshoot shutdown	16
Figure 14.	I_{LIM} vs T_{case}	16
Figure 15.	Turn-on voltage slope	16
Figure 16.	Turn-off voltage slope	16
Figure 17.	On-state resistance vs T_{case}	16
Figure 18.	On-state resistance vs V_{CC}	16
Figure 19.	Application schematic	17
Figure 20.	Maximum turn-off current versus load inductance ⁽¹⁾	19
Figure 21.	PowerSO-10 PC board ⁽¹⁾	20
Figure 22.	$R_{thj-amb}$ vs PCB copper area in open box free air condition	20
Figure 23.	Thermal impedance junction ambient single pulse	21
Figure 24.	Thermal fitting model of a single channel in PowerSO-10	21
Figure 25.	PowerSO-10 package dimensions	23
Figure 26.	PowerSO-10 suggested pad layout and tube shipment (no suffix)	25
Figure 27.	PowerSO-10 tape and reel shipment (suffix "TR")	25

1 Block diagram and pin description

Figure 1. Block diagram

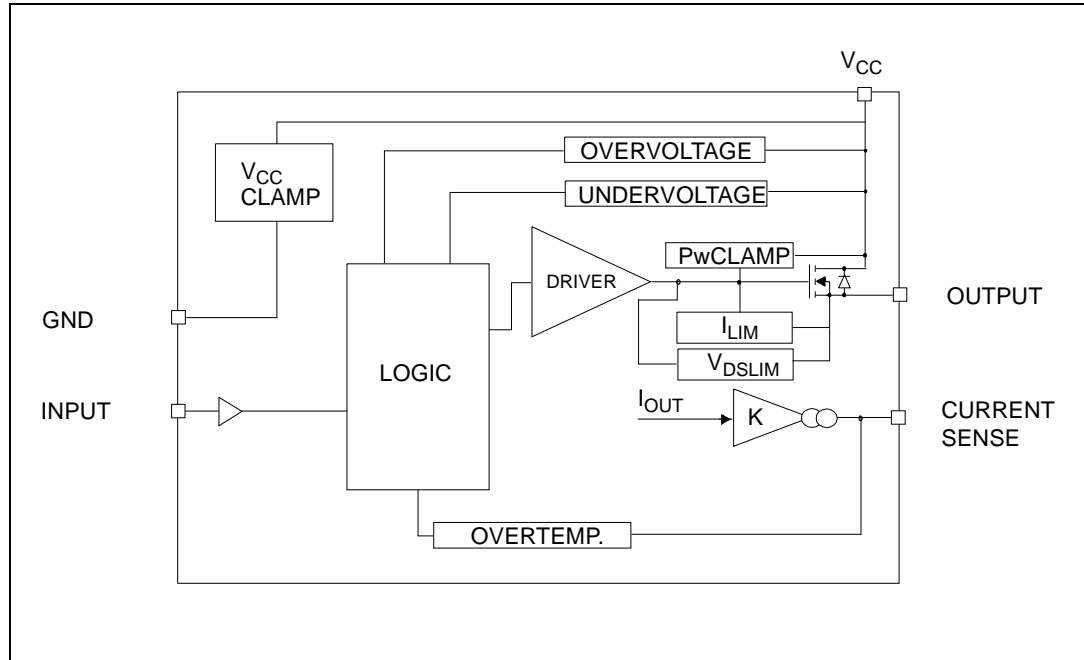


Figure 2. Configuration diagram (top view)

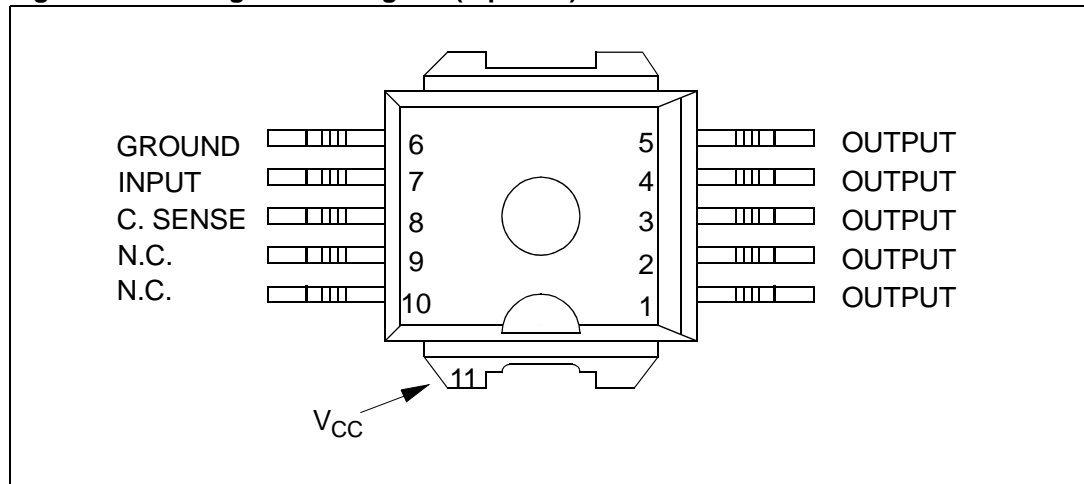
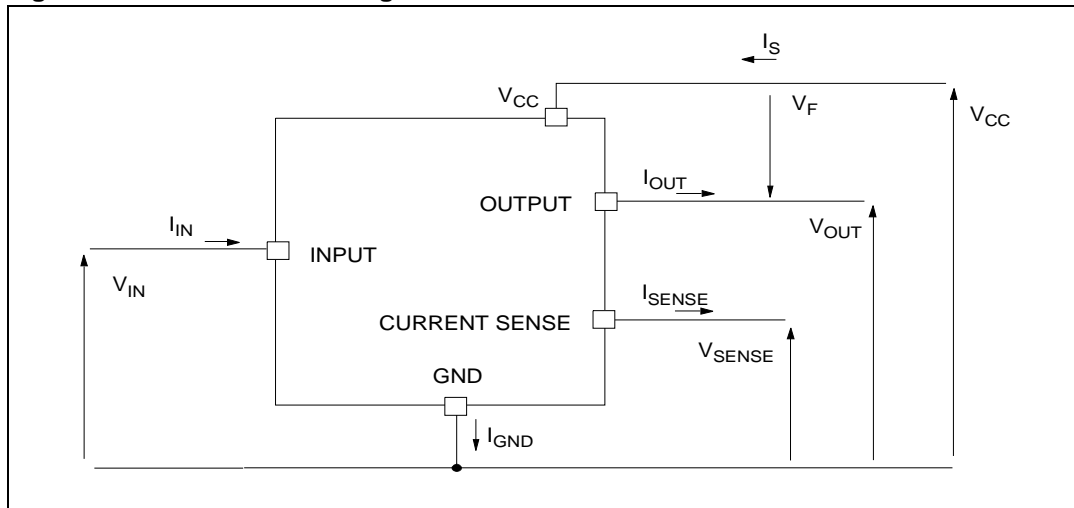


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1 KΩ resistor	X		Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	- 0.3	V
$-I_{GND}$	DC reverse ground pin current	- 200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	- 50	A
I_{IN}	DC input current	+/- 10	mA
V_{CSense}	Current sense maximum voltage	- 3 + 15	V V
V_{ESD}	Electrostatic discharge (human body model: $R = 1.5K\Omega$; $C = 100pF$)		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- OUTPUT	5000	V
	- V_{CC}	5000	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy ($L = 0.05\text{mH}$; $R_L = 0\Omega$; $V_{bat} = 13.5\text{V}$; $T_{jstart} = 150^\circ\text{C}$; $I_L = 75\text{A}$)	193	mJ
P_{tot}	Power dissipation at $T_c \leq 25^\circ\text{C}$	139	W
T_j	Junction operating temperature	Internally limited	$^\circ\text{C}$
T_c	Case operating temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage temperature	-55 to 150	$^\circ\text{C}$

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
$R_{thj-case}$	Thermal resistance junction-case (max)	0.9		$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (max)	50.9 ⁽¹⁾	36 ⁽²⁾	$^\circ\text{C}/\text{W}$

1. When mounted on a standard single-sided FR-4 board with 0.5 cm² of Cu (at least 35 μm thick).

2. When mounted on a standard single-sided FR-4 board with 6 cm² of Cu (at least 35 μm thick).

2.3 Electrical characteristics

Values specified in this section are for $8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise stated. Per each channel.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown	See ⁽¹⁾	36			V
R_{ON}	On-state resistance	$I_{OUT} = 15A$; $T_j = 25^{\circ}C$ $I_{OUT} = 15A$; $T_j = 150^{\circ}C$ $I_{OUT} = 9A$; $V_{CC} = 6V$			10 20 35	m Ω m Ω m Ω
V_{clamp}	Clamp voltage	$I_{CC} = 20mA^{(1)}$	41	48	55	V
I_S	Supply current	Off-state; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$ Off-state; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$; $T_j=25^{\circ}C$ On-state; $V_{IN} = 5V$; $V_{CC} = 13V$; $I_{OUT} = 0A$; $R_{SENSE} = 3.9k\Omega$		10 10	25 20 5	μA μA mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$	0		50	μA
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0V$; $V_{OUT} = 3.5V$	-75		0	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT}=0V$; $V_{CC}=13V$; $T_j=125^{\circ}C$			5	μA
$I_{L(off4)}$	Off-state output current	$V_{IN}=V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}C$			3	μA

1. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Protections⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	DC short circuit current	$V_{CC} = 13V$; $5.5V < V_{CC} < 36V$	45	75	120 120	A A
T_{TSD}	Thermal shutdown temperature		150	175	200	$^{\circ}C$
T_R	Thermal reset temperature		135			$^{\circ}C$
T_{HYST}	Thermal hysteresis		7	15		$^{\circ}C$

Table 6. Protections⁽¹⁾ (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{demag}	Turn-off output voltage clamp	$I_{\text{OUT}} = 2\text{A}; V_{\text{IN}} = 0\text{V}; L = 6\text{mH}$	$V_{\text{CC}}-41$	$V_{\text{CC}}-48$	$V_{\text{CC}}-55$	V
V_{ON}	Output voltage drop limitation	$I_{\text{OUT}} = 1.5\text{A}$ $T_{\text{j}} = -40^{\circ}\text{C}\dots+150^{\circ}\text{C}$		50		mV

1. To ensure long term reliability under heavy over-load or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 7. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{F}	Forward on voltage	$-I_{\text{OUT}} = 8\text{A}; T_{\text{j}} = 150^{\circ}\text{C}$	-	-	0.6	V

Table 8. Current sense ($9\text{V} \leq V_{\text{CC}} \leq 16\text{V}$)⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 1.5\text{A}; V_{\text{SENSE}} = 0.5\text{V};$ $T_{\text{j}} = -40^{\circ}\text{C}\dots150^{\circ}\text{C}$	3300	4400	6000	
dK_1/K_1	Current sense ratio drift	$I_{\text{OUT}} = 1.5\text{A}; V_{\text{SENSE}} = 0.5\text{V};$ $T_{\text{j}} = -40^{\circ}\text{C}\dots150^{\circ}\text{C}$	-10		+10	%
K_2	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 15\text{A}; V_{\text{SENSE}} = 4\text{V};$ $T_{\text{j}} = -40^{\circ}\text{C}$ $T_{\text{j}} = 25^{\circ}\text{C}\dots150^{\circ}\text{C}$	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current sense ratio drift	$I_{\text{OUT}} = 15\text{A}; V_{\text{SENSE}} = 4\text{V};$ $T_{\text{j}} = 25^{\circ}\text{C}\dots150^{\circ}\text{C}$	-6		+6	%
K_3	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 45\text{A}; V_{\text{SENSE}} = 4\text{V};$ $T_{\text{j}} = -40^{\circ}\text{C}$ $T_{\text{j}} = 25^{\circ}\text{C}\dots150^{\circ}\text{C}$	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current sense ratio drift	$I_{\text{OUT}} = 45\text{A}; V_{\text{SENSE}} = 4\text{V};$ $T_{\text{j}} = 25^{\circ}\text{C}\dots150^{\circ}\text{C}$	-6		+6	%
I_{SENSE0}	Analog sense current	$V_{\text{CC}} = 6\dots16\text{V}; I_{\text{OUT}} = 0\text{A};$ $V_{\text{SENSE}} = 0\text{V};$ $T_{\text{j}} = -40^{\circ}\text{C}\dots150^{\circ}\text{C}$ Off-state; $V_{\text{IN}} = 0\text{V}$ On-state; $V_{\text{IN}} = 5\text{V}$	0 0		5 10	μA μA
V_{SENSE}	Max analog sense output voltage	$V_{\text{CC}} = 5.5\text{V}; I_{\text{OUT}} = 7.5\text{A};$ $R_{\text{SENSE}} = 10\text{k}\Omega$ $V_{\text{CC}} > 8\text{V}, I_{\text{OUT}} = 15\text{A};$ $R_{\text{SENSE}} = 10\text{k}\Omega$	3.5 5			V V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	$V_{\text{CC}} = 13\text{V}; R_{\text{SENSE}} = 3.9\text{k}\Omega$		5.5		V

Table 8. Current sense (9 V ≤ V_{CC} ≤ 16 V)⁽¹⁾ (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R _{VSENSEH}	Analog sense output impedance in overtemperature condition	V _{CC} = 13V; T _j > T _{TSD} ; Output open		400		Ω
t _{DSENSE}	Current sense delay response	To 90% I _{SENSE} ⁽²⁾			500	μs

1. See [Figure 4](#).

2. Current sense signal delay after positive input slope.

Table 9. Switching (V_{CC} = 13 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	R _L = 0.87Ω	-	50	-	μs
t _{d(off)}	Turn-on delay time	R _L = 0.87Ω	-	50	-	μs
(dV _{OUT} /dt) _{on}	Turn-on voltage slope	R _L = 0.87Ω	-	See Figure 15	-	V/μs
(dV _{OUT} /dt) _{off}	Turn-off voltage slope	R _L = 0.87Ω	-	See Figure 16	-	V/μs

Table 10. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{IL}	Input low level voltage				1.25	V
I _{IL}	Low level input current	V _{IN} = 1.25V	1			μA
V _{IH}	Input high level voltage		3.25			V
I _{IH}	High level input current	V _{IN} = 3.25V			10	μA
V _{I(hyst)}	Input hysteresis voltage		0.5			V
V _{ICL}	Input clamp voltage	I _{IN} = 1mA I _{IN} = - 1mA	6	6.8 - 0.7	8	V V

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}

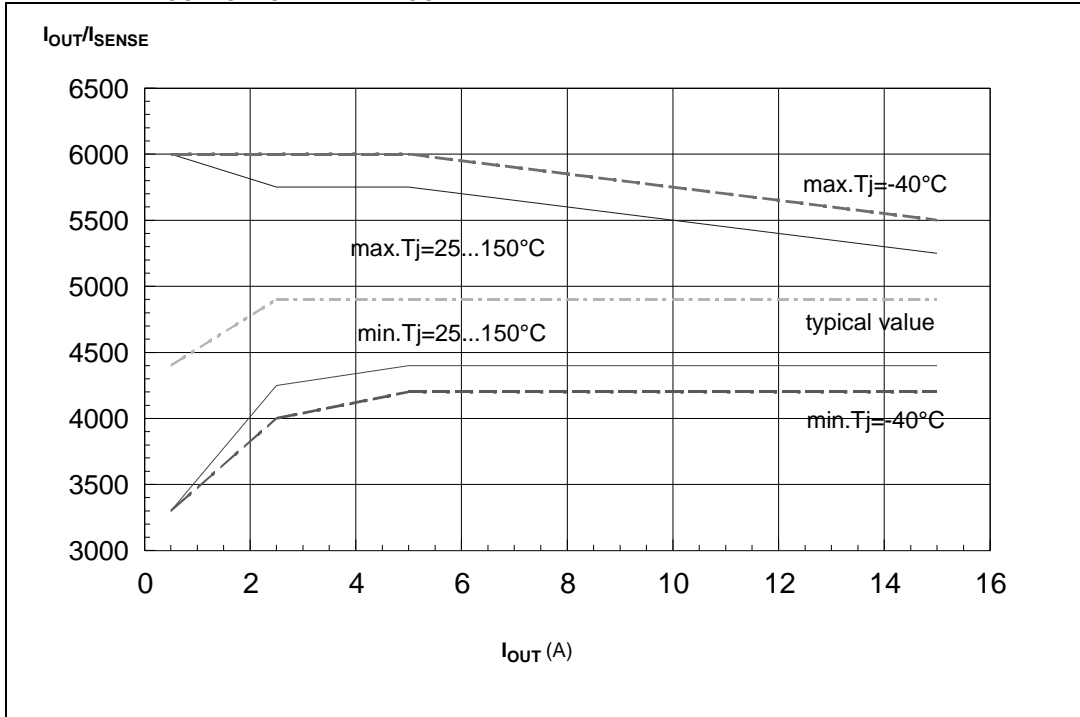


Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Under-voltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	$(T_j < T_{TSD})$ 0
	H	L	$(T_j > T_{TSD}) V_{SENSEH}$
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

Figure 5. Switching characteristics

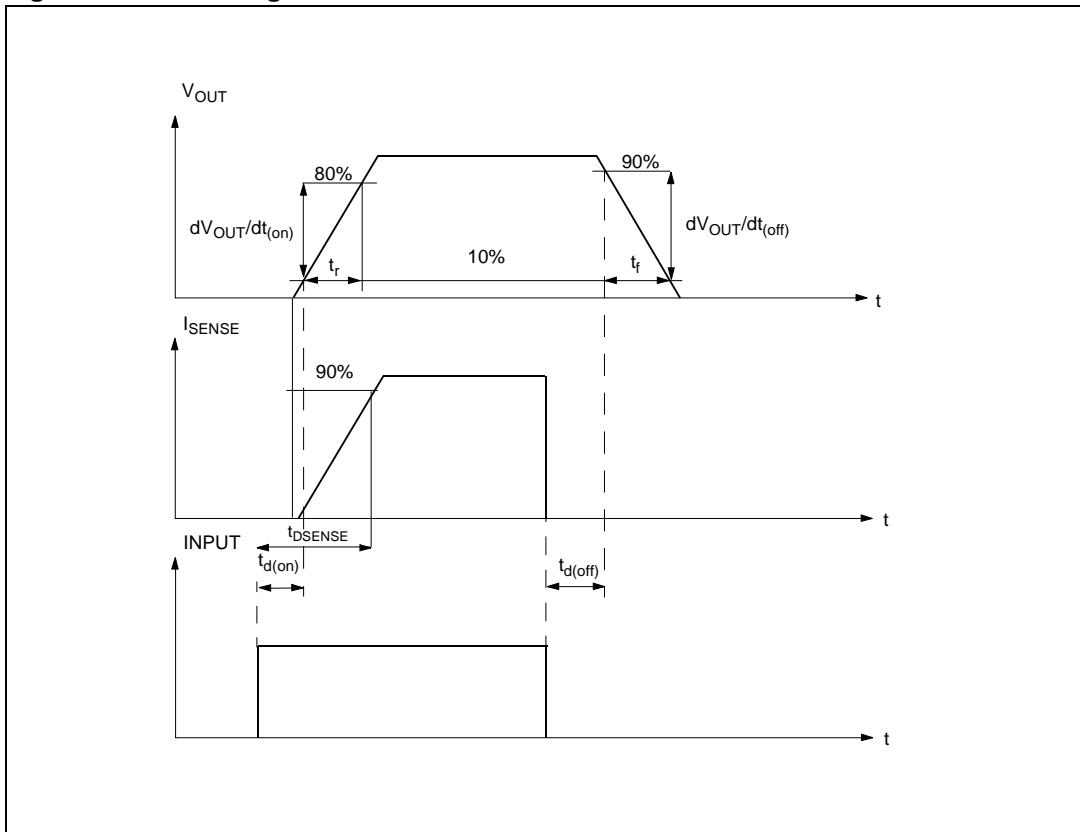


Table 12. Electrical transient requirements on V_{CC} pin (part 1/3)

ISO T/R 7637/1 test pulse	Test levels				Delays and impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

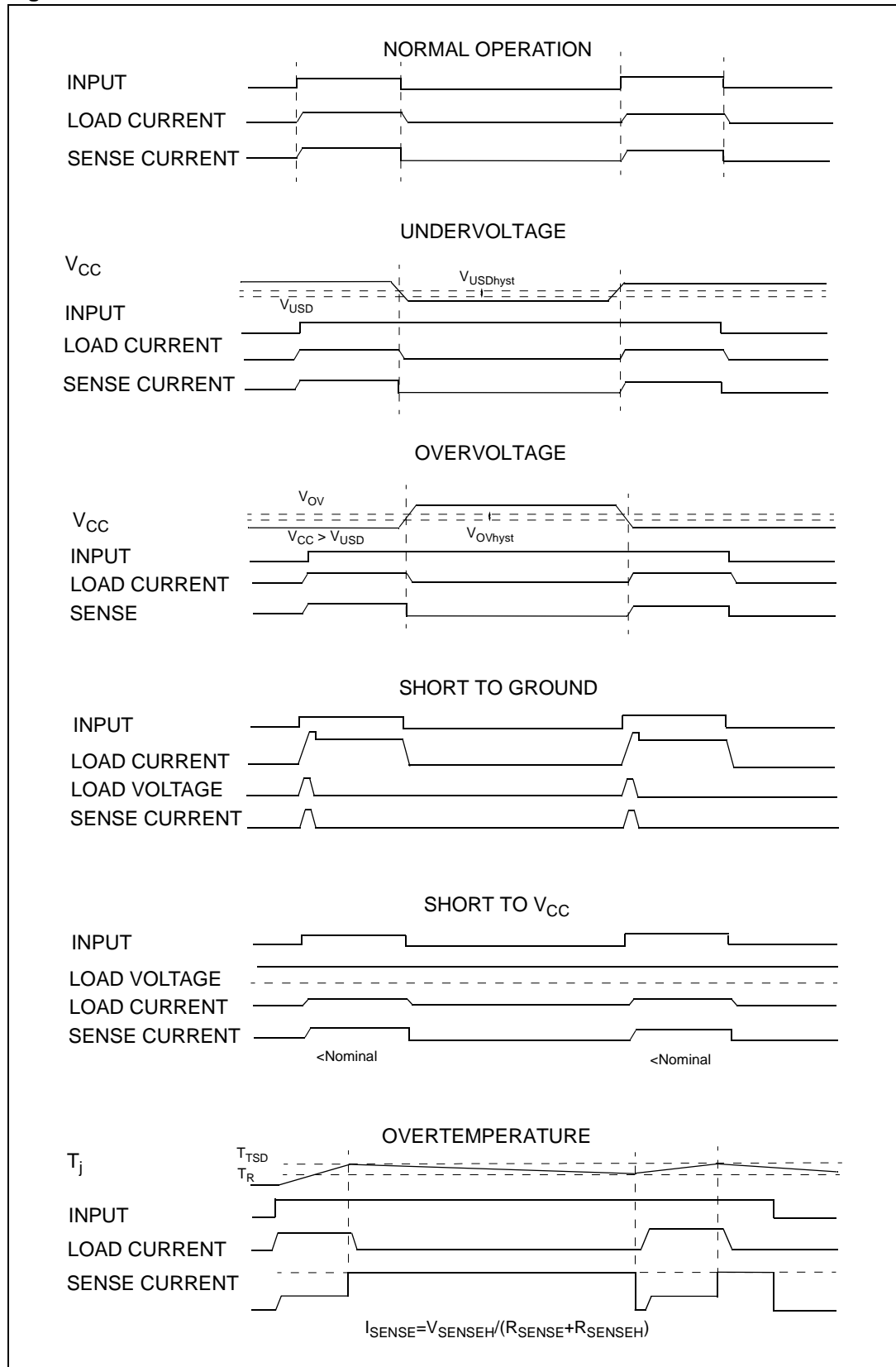
Table 13. Electrical transient requirements on V_{CC} pin (part 2/3)

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 14. Electrical transient requirements on V_{CC} pin (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

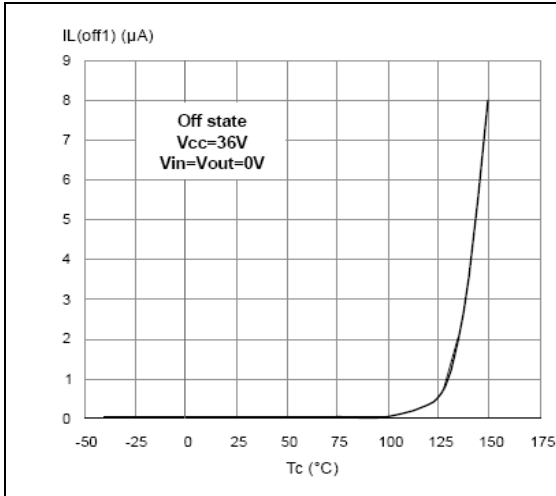


Figure 8. High level input current

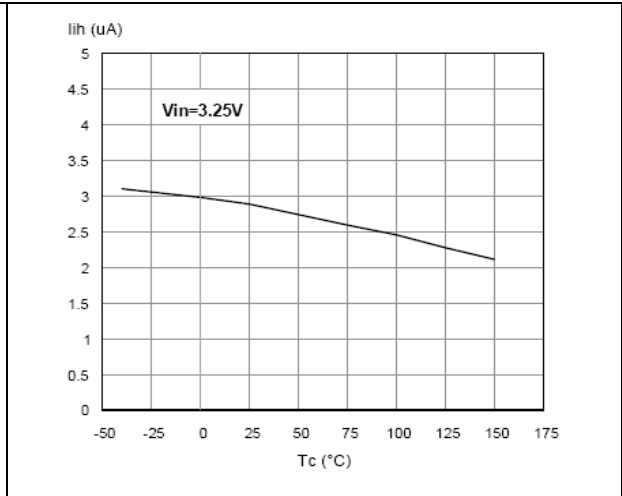


Figure 9. Input low level

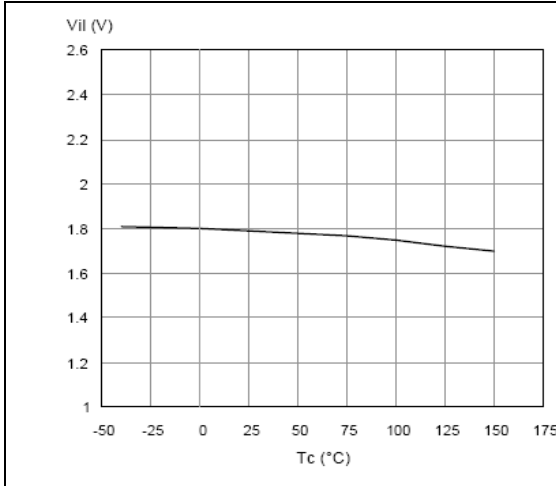


Figure 10. Input high level

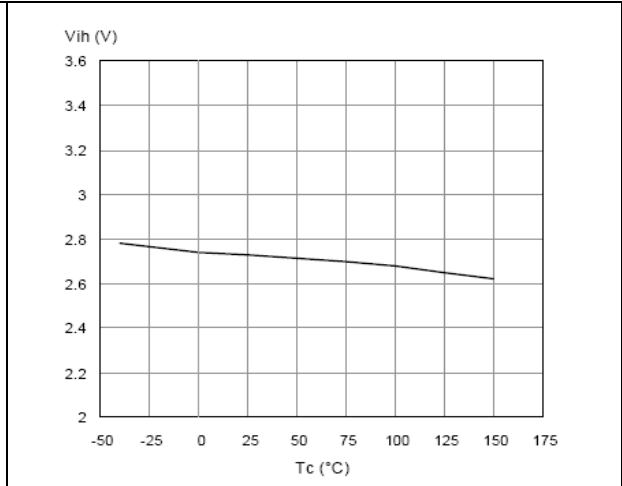


Figure 11. Input clamp voltage

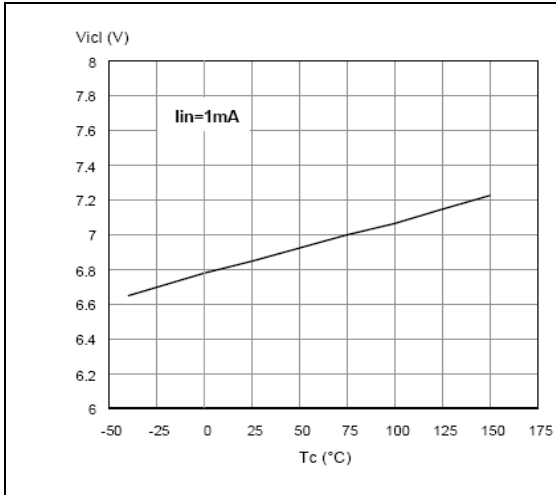


Figure 12. Input hysteresis voltage

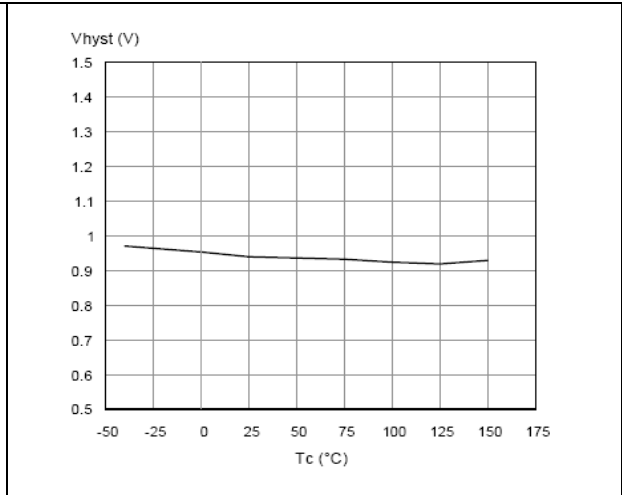


Figure 13. Overvoltage shutdown

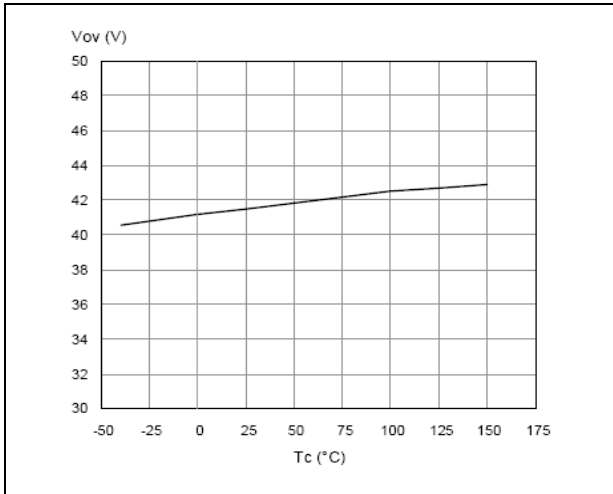


Figure 14. I_{LIM} vs T_{case}

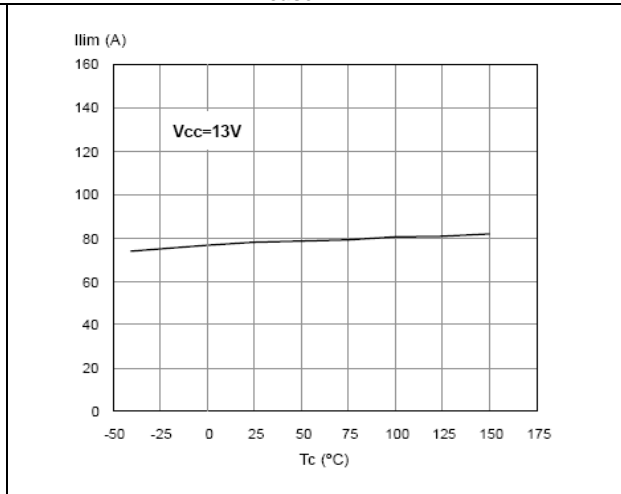


Figure 15. Turn-on voltage slope

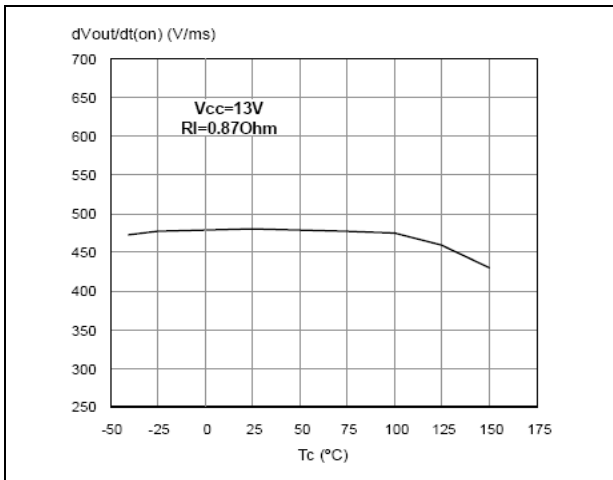


Figure 16. Turn-off voltage slope

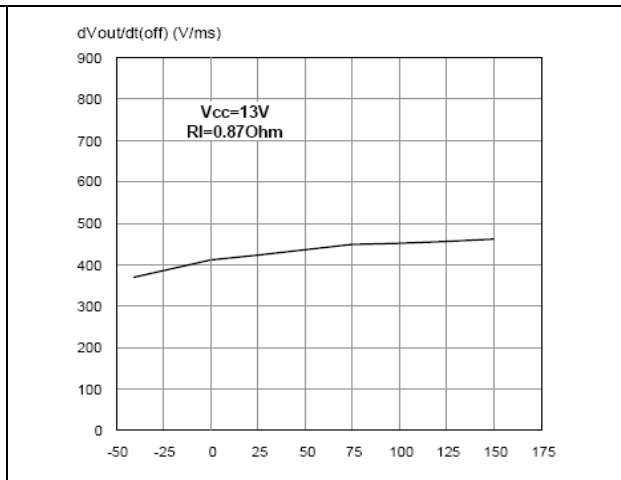


Figure 17. On-state resistance vs T_{case}

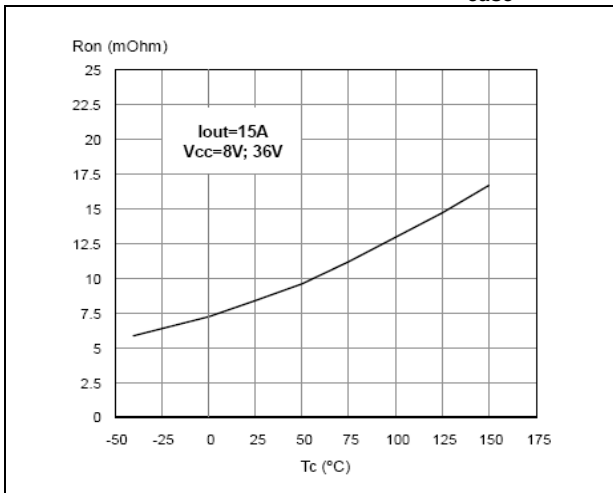
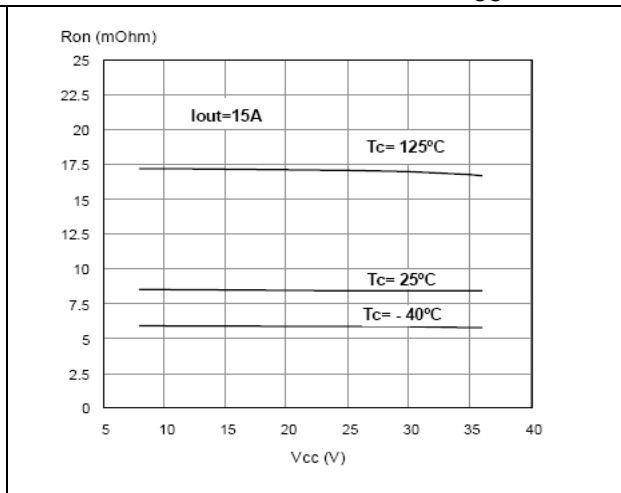
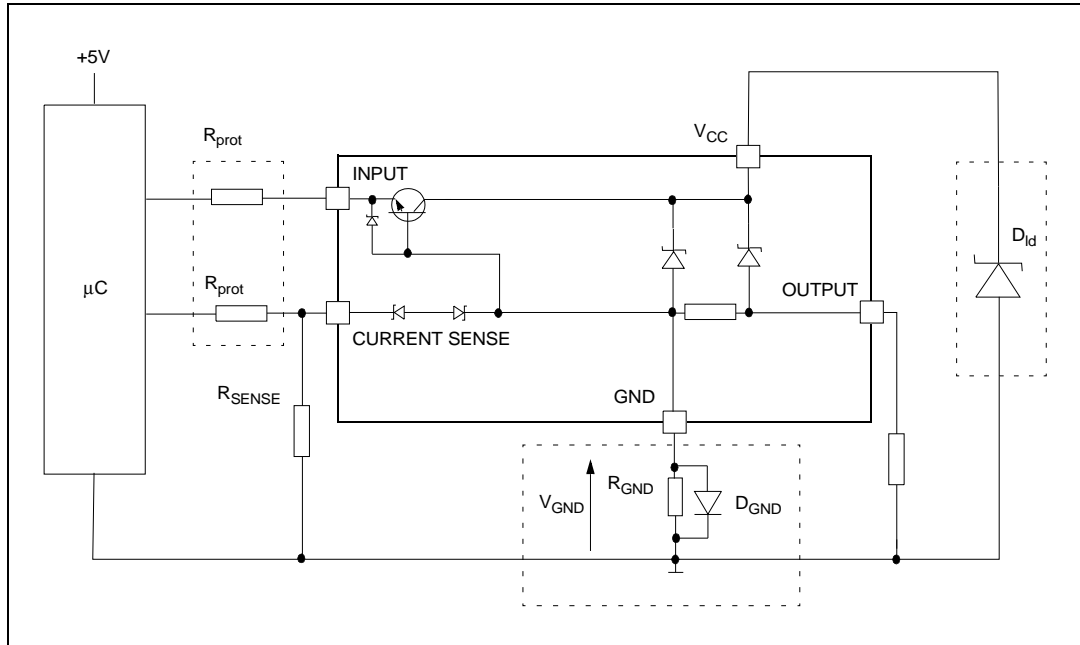


Figure 18. On-state resistance vs V_{CC}



3 Application information

Figure 19. Application schematic



3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600\text{mV} / (I_{S(ON)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(ON)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} produces a shift ($I_{S(ON)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND} .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1k\Omega$) should be inserted in parallel to D_{GND} if the device is driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network produces a shift ($\approx 600mV$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift not varies if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT pin is to leave them unconnected, while unused SENSE pin has to be connected to ground pin.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in the ISO T/R 7637/1 table.

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins is pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

$$V_{CCpeak} = -100V$$

$$I_{latchup} \geq 20mA$$

$$V_{OH\mu C} \geq 4.5V$$

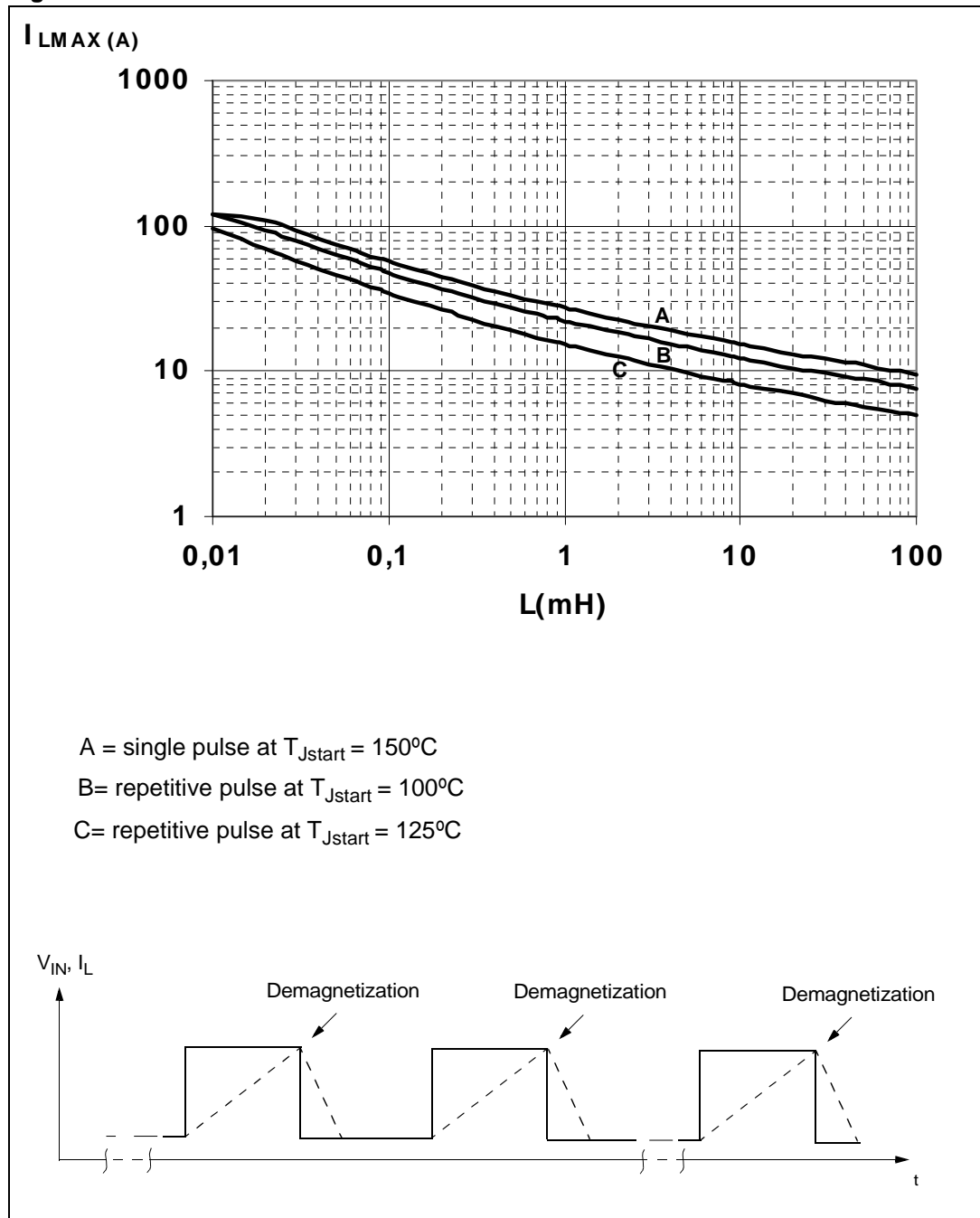
$$5k\Omega \leq R_{prot} \leq 65k\Omega.$$

Recommended values are:

$$R_{prot} = 10k\Omega$$

3.4 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 20. Maximum turn-off current versus load inductance⁽¹⁾

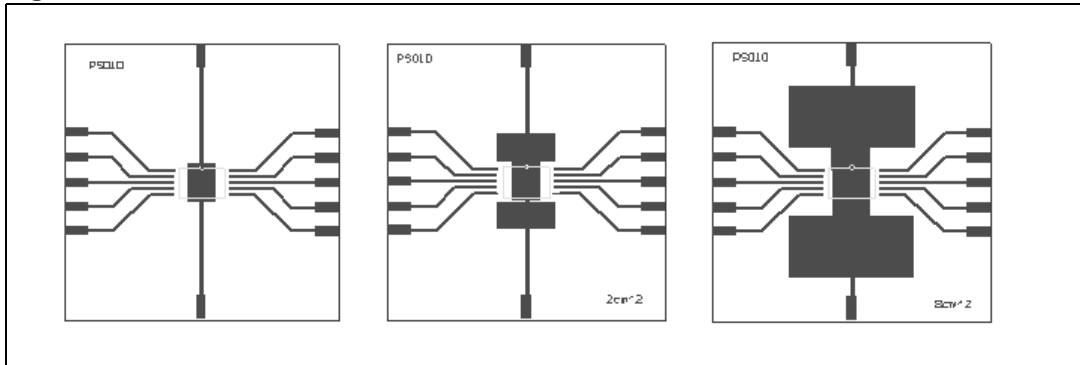


1. Values are generated with $R_L = 0\Omega$.
 In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 PowerSO-10 thermal data

Figure 21. PowerSO-10 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35 μ m, Copper areas: from minimum pad-lay-out to 8cm²).

Figure 22. $R_{thj-amb}$ vs PCB copper area in open box free air condition

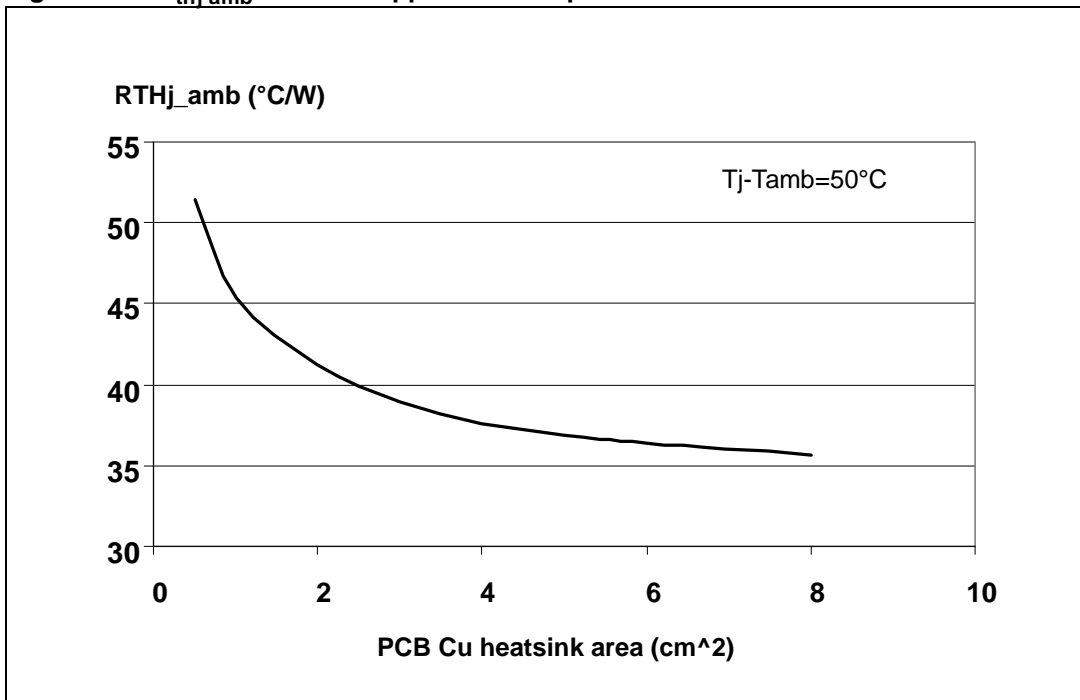
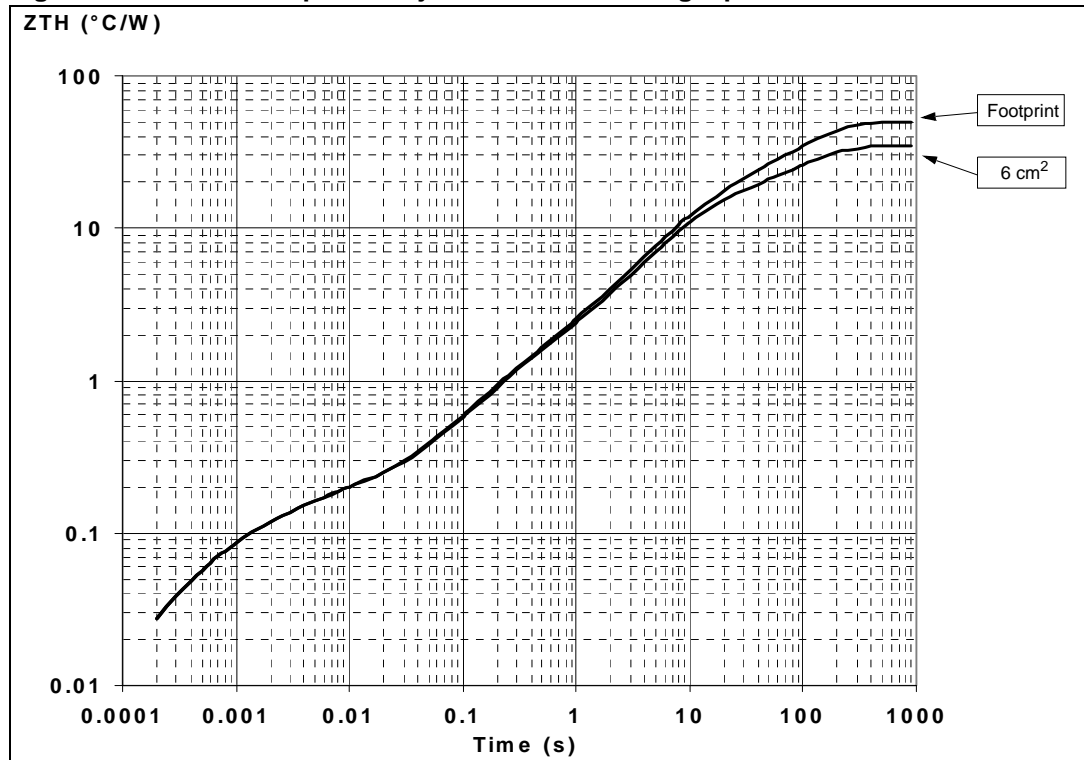


Figure 23. Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 24. Thermal fitting model of a single channel in PowerSO-10

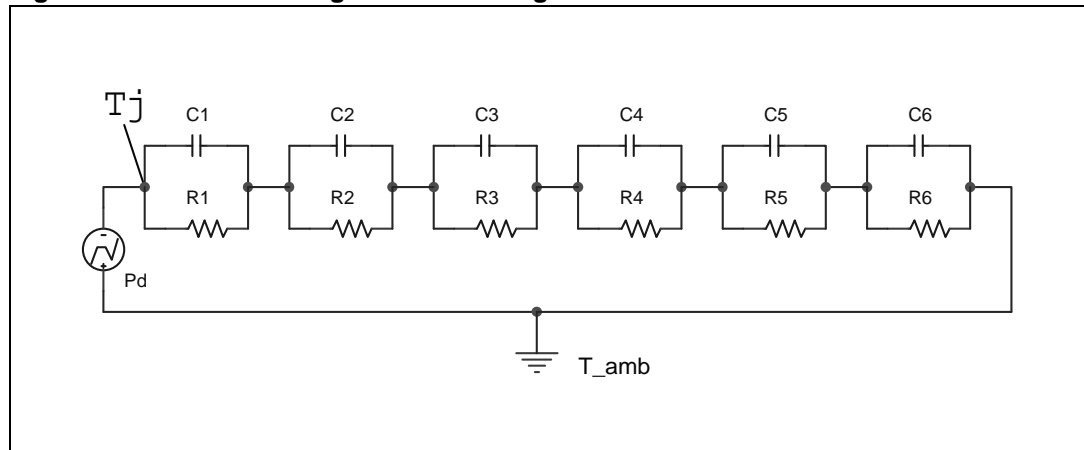


Table 15. Thermal parameters

Area / island (cm ²)	Footprint	6
R1 (°C/W)	0.016	
R2 (°C/W)	0.06	
R3 (°C/W)	0.08	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.002	
C2 (W.s/°C)	1E-02	
C3 (W.s/°C)	0.04	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

5 Package and packing information

5.1 ECOPACK[®] packages

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5.2 PowerSO-10 mechanical data

Figure 25. PowerSO-10 package dimensions

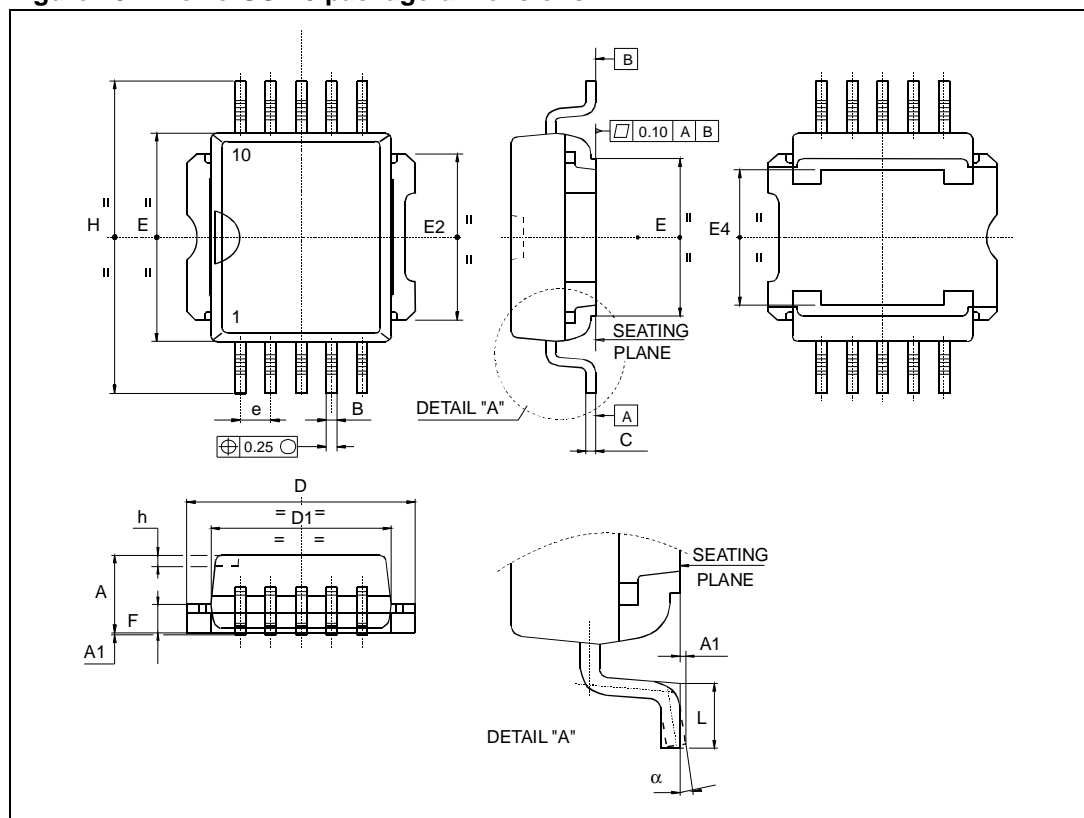


Table 16. PowerSO-10 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	3.35		3.65
A ⁽¹⁾	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B ⁽¹⁾	0.37		0.53
C	0.35		0.55
C ⁽¹⁾	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 ⁽¹⁾	7.30		7.50
E4	5.90		6.10
E4 ⁽¹⁾	5.90		6.30
e		1.27	
F	1.25		1.35
F ⁽¹⁾	1.20		1.40
H	13.80		14.40
H ⁽¹⁾	13.85		14.35
h		0.50	
L	1.20		1.80
L ⁽¹⁾	0.80		1.10
a	0°		8°
α ⁽¹⁾	2°		8°

1. Muar only POA P013P.

5.3 PowerSO-10 packing information

Figure 26. PowerSO-10 suggested pad layout and tube shipment (no suffix)

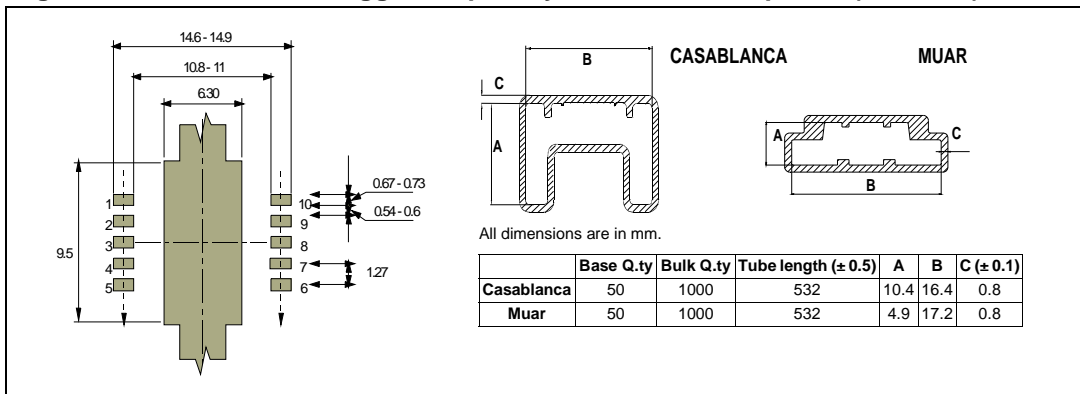
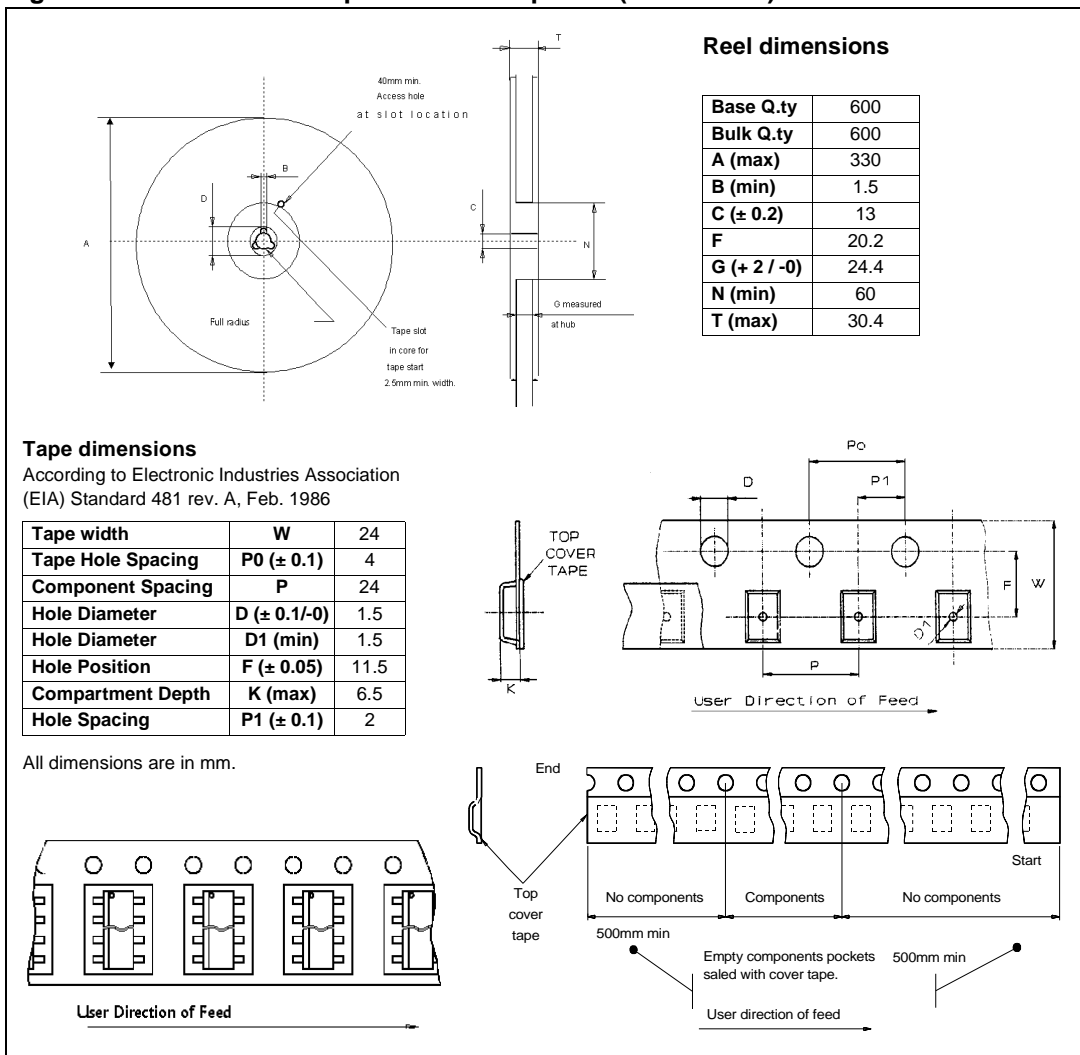


Figure 27. PowerSO-10 tape and reel shipment (suffix "TR")



6 Revision history

Table 17. Document revision history

Date	Revision	Changes
01-Oct-2004	1	Initial release.
23-Jun-2008	2	Changed template. Not changed document content.
11-Dec-2009	3	Formatted entire document. Updated features list.
29-Jun-2010	4	Updated following tables: <ul style="list-style-type: none">– <i>Table 9: Switching ($V_{CC} = 13 V$)</i>– <i>Table 15: Thermal parameters</i>– Updated <i>Figure 24: Thermal fitting model of a single channel in PowerSO-10</i>
19-Sep-2013	5	Updated Disclaimer.

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