




Thyristor/Thyristor, 570 A (SUPER MAGN-A-PAK Power Modules)



SUPER MAGN-A-PAK

FEATURES

- High current capability
- High surge capability
- Industrial standard package
- 3000 V_{RMS} isolating voltage with non-toxic substrate
- Designed and qualified for industrial level
- UL approved file E78996 
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

TYPICAL APPLICATIONS

- Motor starters
- DC motor controls - AC motor controls
- Uninterruptible power supplies

PRODUCT SUMMARY	
I _{T(AV)}	570 A
Type	Modules - Thyristor, Standard
Package	SMAP
Circuit	Two SCRs Doubler Circuit

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
I _{T(AV)}	T _C = 74 °C	570	A
I _{T(RMS)}	T _C = 74 °C	895	
I _{TSM}	50 Hz	17 800	
	60 Hz	18 700	
I ² t	50 Hz	1591	kA ² s
	60 Hz	1452	
I ² √t		15 910	kA ² √s
V _{RRM}	Range	1800	V
T _{Stg}	Range	-40 to +135	°C
T _J	Range	-40 to +135	

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V _{RRM} /V _{DRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I _{RRM} /I _{DRM} MAXIMUM AT T _J = T _J MAXIMUM mA
VS-VSKT570-18PbF	18	1800	1900	120



ON-STATE CONDUCTION					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave		570	A
				74	°C
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction, half sine wave at $T_C = 74\text{ °C}$		895	A
Maximum peak, one-cycle, non-repetitive on-state surge current	I_{TSM}, I_{FSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	kA
		t = 8.3 ms			
		t = 10 ms	100 % V_{RRM} reapplied		
		t = 8.3 ms			
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied	kA ² s	
		t = 8.3 ms			
		t = 10 ms	100 % V_{RRM} reapplied		
		t = 8.3 ms			
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied		15 910	kA ² √s
Low level value or threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$, $T_J = T_J$ maximum)		0.864	V
High level value of threshold voltage	$V_{T(TO)2}$	(I $> \pi \times I_{T(AV)}$, $T_J = T_J$ maximum)		0.97	
Low level value on-state slope resistance	r_{t1}	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$, $T_J = T_J$ maximum)		0.411	mΩ
High level value on-state slope resistance	r_{t2}	(I $> \pi \times I_{T(AV)}$, $T_J = T_J$ maximum)		0.362	
Maximum on-state voltage drop	V_{TM}	$I_{pk} = 1500\text{ A}$, $T_J = 25\text{ °C}$, $t_p = 10\text{ ms}$ sine pulse		1.50	V
Maximum holding current	I_H	$T_J = 25\text{ °C}$, anode supply 12 V resistive load		500	mA
Maximum latching current	I_L			1000	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum rate of rise of turned-on current	di/dt	$T_J = T_J$ maximum, $I_{TM} = 400\text{ A}$, V_{DRM} applied		1000	A/μs
Typical delay time	t_d	Gate current 1 A, $di_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\% V_{DRM}$, $T_J = 25\text{ °C}$		2.0	μs
Typical turn-off time	t_q	$I_{TM} = 750\text{ A}$; $T_J = T_J$ maximum, $di/dt = -60\text{ A}/\mu\text{s}$, $V_R = 50\text{ V}$, $dV/dt = 20\text{ V}/\mu\text{s}$, gate 0 V 100 Ω		200	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to $V_D = 80\% V_{DRM}$		1000	V/μs
RMS insulation voltage	V_{INS}	t = 1 s		3000	V
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied		120	mA



TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	W
Maximum peak average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d \% = 50$	2.0	
Maximum peak positive gate current	$+I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0	A
Maximum peak positive gate voltage	$+V_{GM}$		20	
Maximum peak negative gate voltage	$-V_{GM}$		5.0	V
Maximum DC gate current required to trigger	I_{GT}	$T_J = 25$ °C, $V_{ak} 12$ V	200	mA
DC gate voltage required to trigger	V_{GT}		3.0	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	10	mA
DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		-40 to +135	°C
Maximum storage temperature range	T_{Stg}		-40 to +135	
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.065	K/W
Maximum thermal resistance, case to heatsink per module	R_{thC-hs}	Mounting surface smooth, flat and greased	0.02	
Mounting torque ± 10 %	SMAP to heatsink	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.	6-8	Nm
	busbar to SMAP		12-15	
Approximate weight			1500	g
Case style		See dimensions (link at the end of datasheet)	SUPER MAGN-A-PAK	

ΔR_{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.009	0.006	$T_J = T_J$ maximum	K/W
120°	0.011	0.011		
90°	0.014	0.015		
60°	0.021	0.022		
30°	0.037	0.038		

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

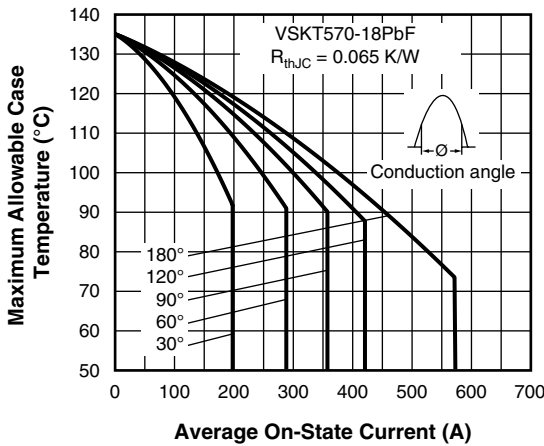


Fig. 1 - Current Ratings Characteristics

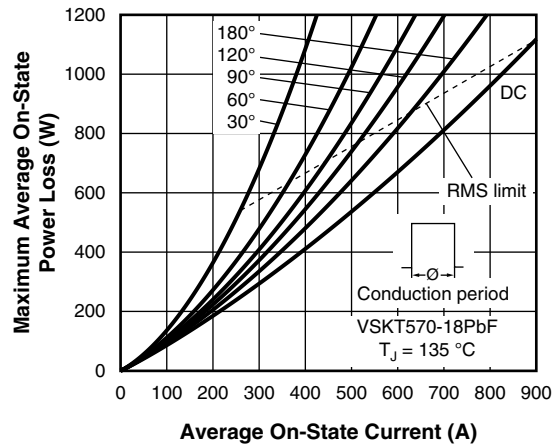


Fig. 4 - On-State Power Loss Characteristics

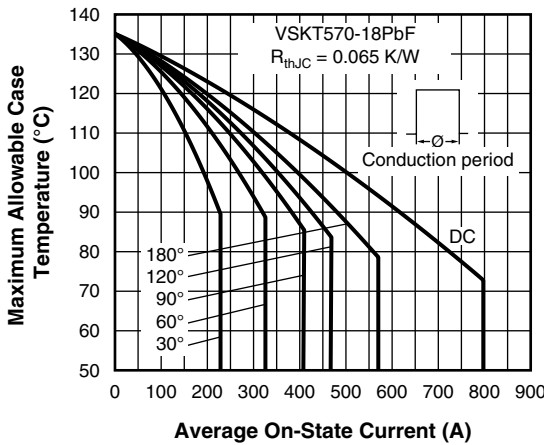


Fig. 2 - Current Ratings Characteristics

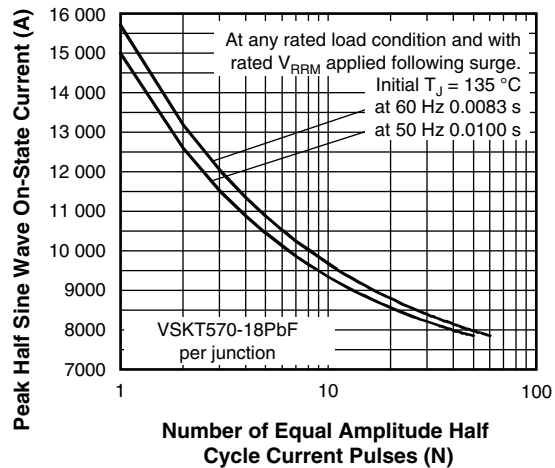


Fig. 5 - Maximum Non-Repetitive Surge Current

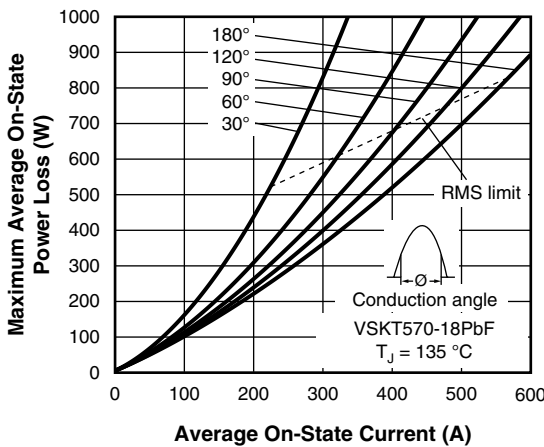


Fig. 3 - On-State Power Loss Characteristics

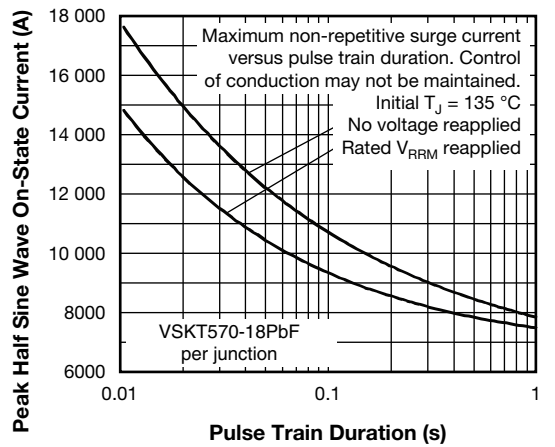


Fig. 6 - Maximum Non-Repetitive Surge Current

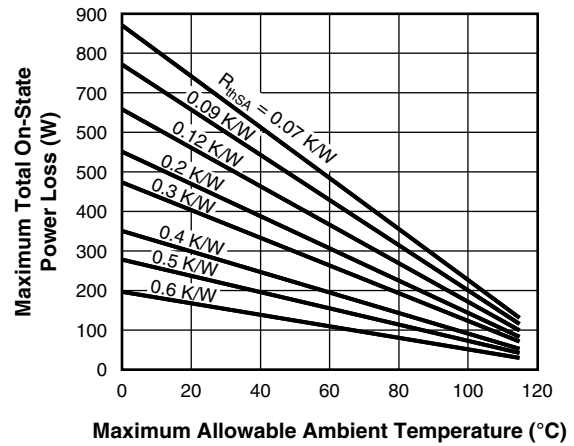
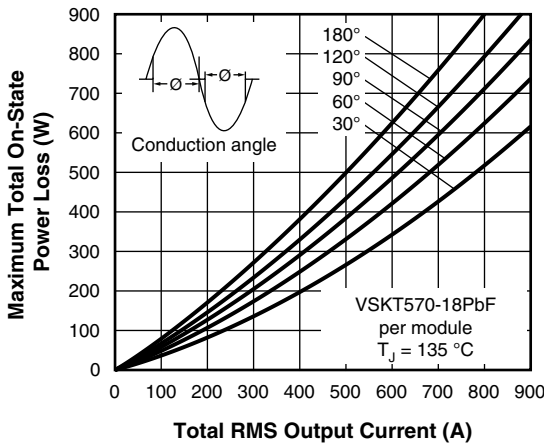


Fig. 7 - On-State Power Loss Characteristics

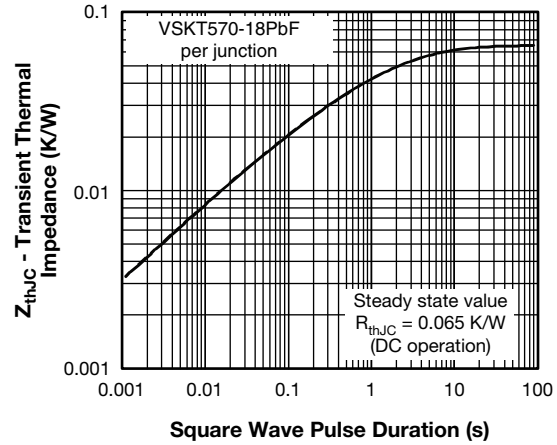
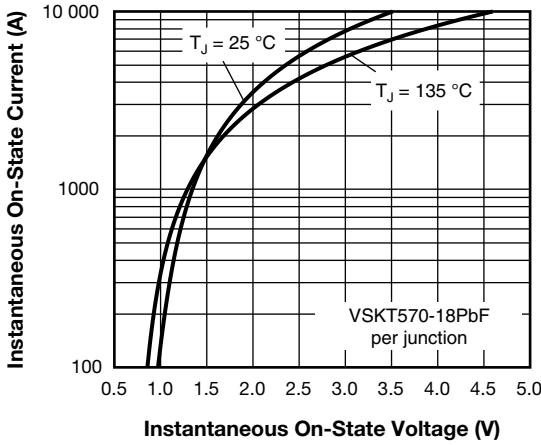


Fig. 8 - On-State Voltage Drop Characteristics

Fig. 9 - Thermal Impedance Z_{thJC} Characteristics

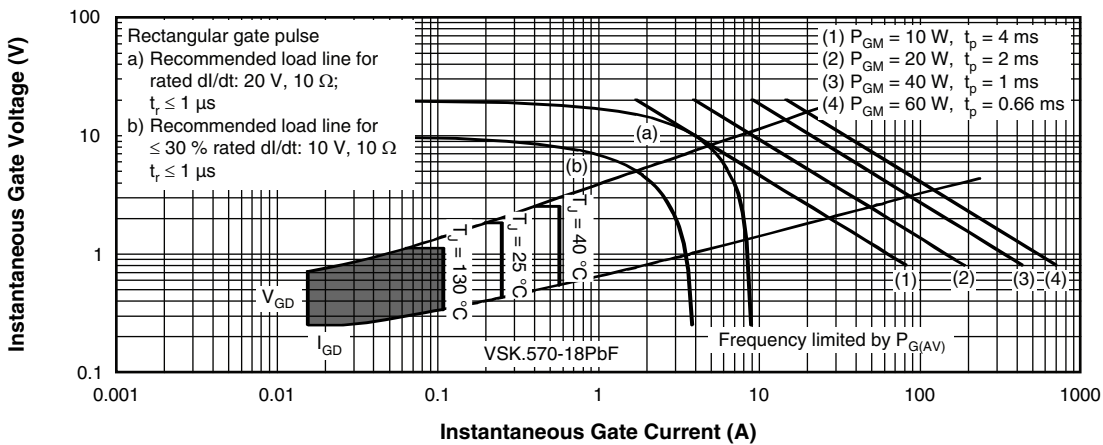


Fig. 10 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code	VS-	VSK	T	570	-	18	PbF
	①	②	③	④		⑤	⑥

- 1** - Vishay Semiconductors product
- 2** - Module type
- 3** - Circuit configuration (see below)
- 4** - Current rating
- 5** - Voltage code x 100 = V_{RRM}
- 6** - Lead (Pb)-free

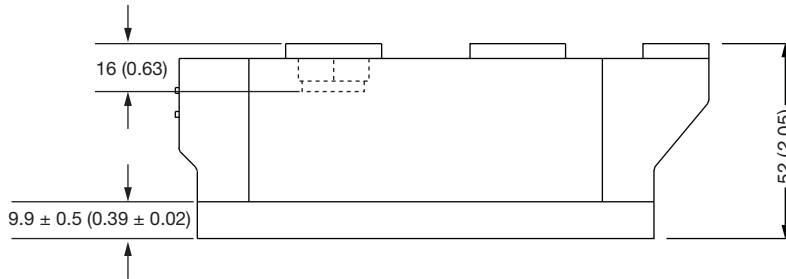
CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs doubler circuit	T	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95283

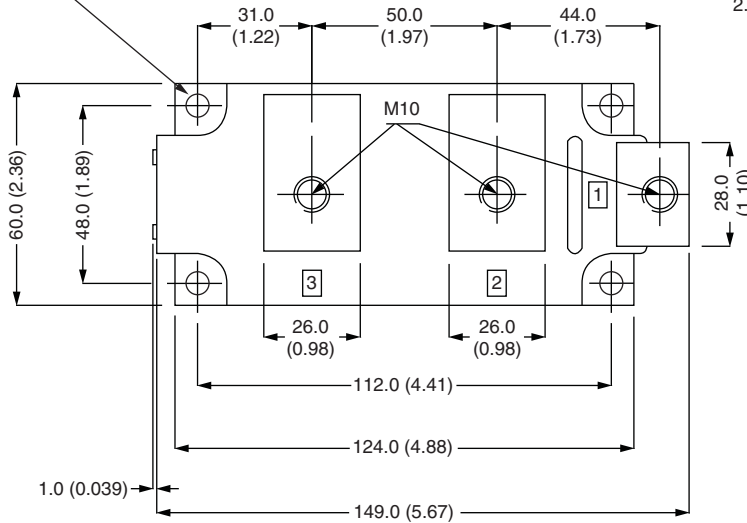


Super MAGN-A-PAK Thyristor/Diode

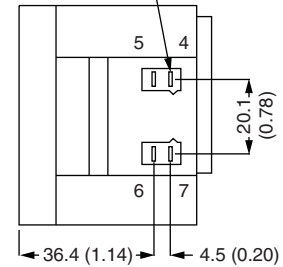
DIMENSIONS in millimeters (inches)



Ø 6.5 mm ± 0.3 mm x 4 Holes (Typ.)



Fast-on tabs
2.8 x 0.8 (0.11 x 0.03)



5, 6 = Gate
4, 7 = Cathode



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