

## N-channel 650 V, 0.85 $\Omega$ typ., 4.5 A MDmesh M2 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data

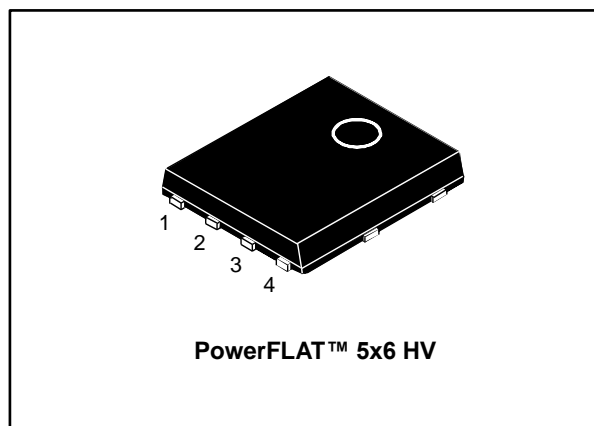


Figure 1: Internal schematic diagram

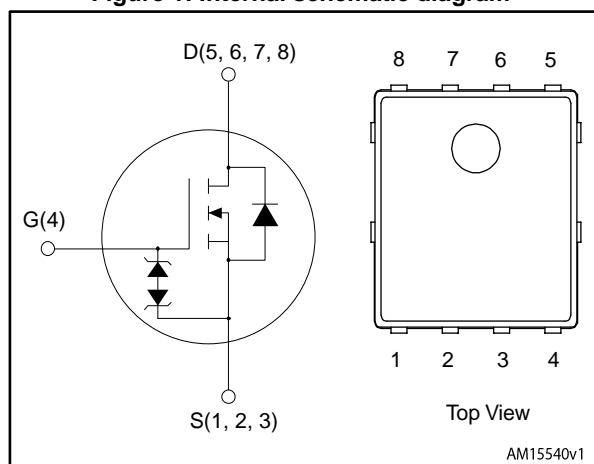


Table 1: Device summary

| Order code | Marking | Package           | Packing       |
|------------|---------|-------------------|---------------|
| STL10N65M2 | 10N65M2 | PowerFLAT™ 5x6 HV | Tape and reel |

### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STL10N65M2 | 650 V           | 1.00 $\Omega$            | 4.5 A          |

- Extremely low gate charge
- Lower R<sub>DS(on)</sub> x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

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## Contents

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol         | Parameter  | Value      | Unit             |
|----------------|--|------------|------------------|
| $V_{GS}$       | Gate-source voltage  | $\pm 25$   | V                |
| $I_D^{(1)}$    | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$   | 4.5        | A                |
|                | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$  | 2.8        | A                |
| $I_{DM}^{(2)}$ | Drain current pulsed   | 18         | A                |
| $P_{TOT}$      | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$  | 48         | W                |
| $I_{AR}$       | Avalanche current, repetitive or non-repetitive (pulse width limited by $T_j$ max)                                   | 0.9        | A                |
| $E_{AS}$       | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 95         | mJ               |
| $dv/dt^{(3)}$  | Peak diode recovery voltage slope  | 15         | V/ns             |
| $dv/dt^{(4)}$  | MOSFET $dv/dt$ ruggedness  | 50         |                  |
| $T_j$          | Operating junction temperature range   | -55 to 150 | $^\circ\text{C}$ |
| $T_{stg}$      | Storage temperature range  |            |                  |

**Notes:**

(1)The value is limited by package.

(2)Pulse width is limited by safe operating area.

(3) $I_{SD} \leq 4.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(\text{peak})} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

(4) $V_{DS} \leq 520\text{ V}$

**Table 3: Thermal data**

| Symbol                     | Parameter                        | Value | Unit                      |
|----------------------------|----------------------------------|-------|---------------------------|
| $R_{thj\text{-case}}$      | Thermal resistance junction-case | 2.6   | $^\circ\text{C}/\text{W}$ |
| $R_{thj\text{-pcb}}^{(1)}$ | Thermal resistance junction-pcb  | 50    | $^\circ\text{C}/\text{W}$ |

**Notes:**

(1)When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz Cu

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4: On/off-state**

| Symbol        | Parameter                         | Test conditions  | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|--|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                    | 650  |      |          | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$                                |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$<br>$T_C = 125\text{ °C}^{(1)}$ |      |      | 100      | $\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                             |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                             | 2    | 3    | 4        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 2.5\text{ A}$                                  |      | 0.85 | 1.00     | $\Omega$      |

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 5: Dynamic**

| Symbol                     | Parameter                             | Test conditions   | Min. | Typ. | Max. | Unit     |
|----------------------------|---------------------------------------|---|------|------|------|----------|
| $C_{iss}$                  | Input capacitance                     | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0\text{ V}$   | -    | 315  | -    | pF       |
| $C_{oss}$                  | Output capacitance                    |   | -    | 18   | -    | pF       |
| $C_{rss}$                  | Reverse transfer capacitance          |   | -    | 0.86 | -    | pF       |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent capacitance energy related | $V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$   | -    | 109  | -    | pF       |
| $R_g$                      | Intrinsic gate resistance             | $f = 1\text{ MHz}$ open drain   | -    | 6.6  | -    | $\Omega$ |
| $Q_g$                      | Total gate charge                     | $V_{DD} = 520\text{ V}$ , $I_D = 5\text{ A}$<br>$V_{GS} = 0\text{ to }10\text{ V}$<br>(see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> ) | -    | 10.3 | -    | nC       |
| $Q_{gs}$                   | Gate-source charge                    |   | -    | 2.4  | -    | nC       |
| $Q_{gd}$                   | Gate-drain charge                     |   | -    | 4.8  | -    | nC       |

**Notes:**

<sup>(1)</sup> $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$ .

Table 6: Switching times

| Symbol       | Parameter           | Test conditions   | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 325 \text{ V}$ , $I_D = 2.5 \text{ A}$ ,<br>$R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$<br>(see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a><br>and <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 7.5  | -    | ns   |
| $t_r$        | Rise time           |   | -    | 6.6  | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |   | -    | 22.5 | -    | ns   |
| $t_f$        | Fall time           |   | -    | 18   | -    | ns   |

Table 7: Source-drain diode

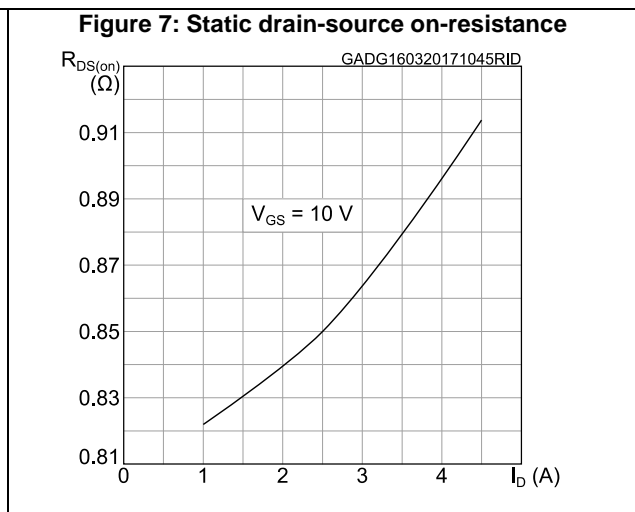
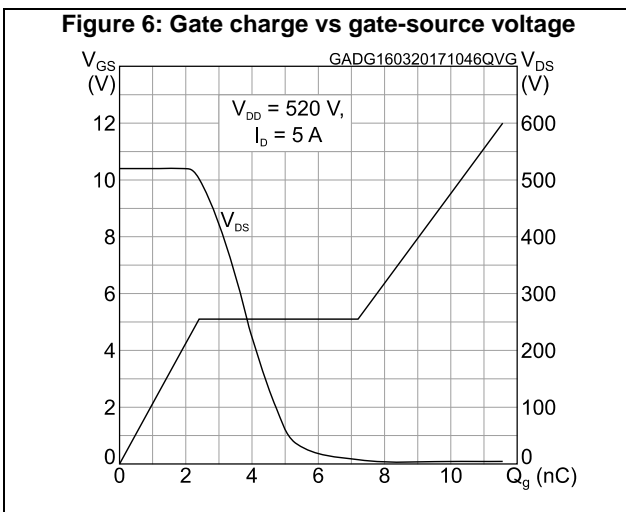
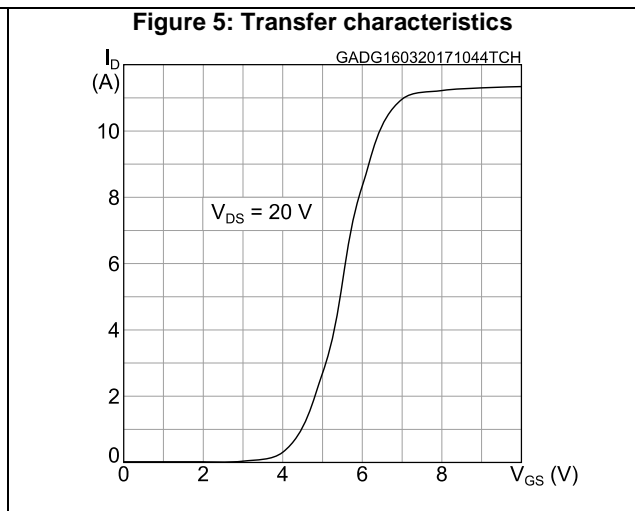
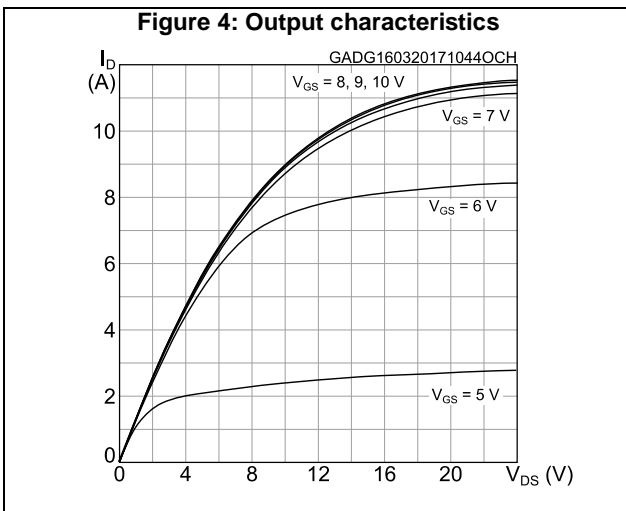
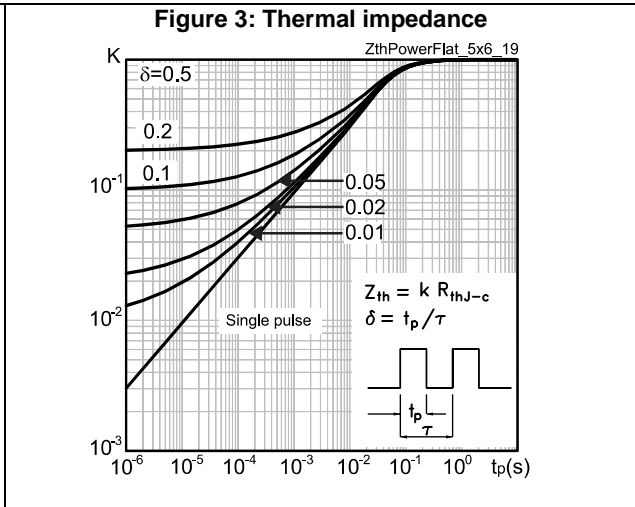
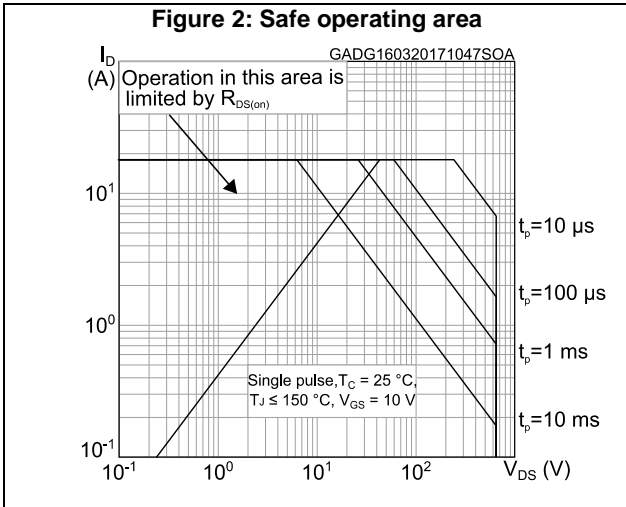
| Symbol          | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|--|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |  | -    |      | 4.5  | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |  | -    |      | 18   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 4.5 \text{ A}$ , $V_{GS} = 0 \text{ V}$  | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60 \text{ V}$<br>(see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )                                      | -    | 276  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 1.7  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 12.5 |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$<br>(see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 312  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 1.9  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 12.4 |      | A             |

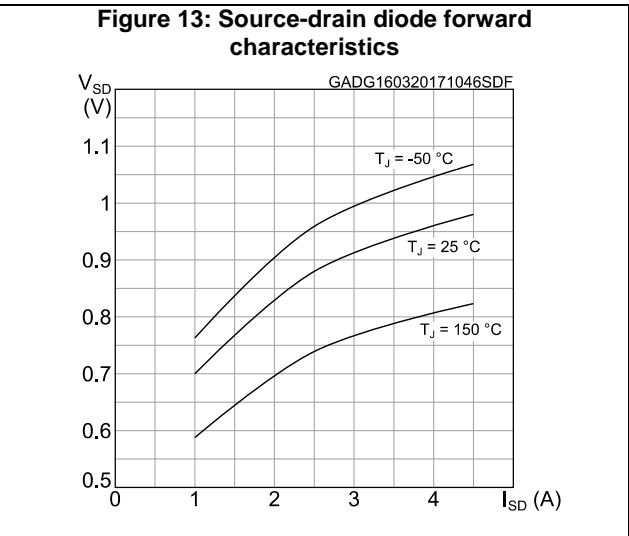
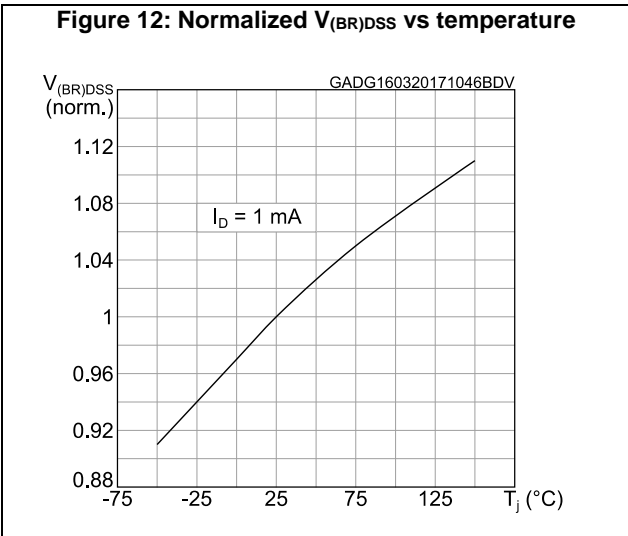
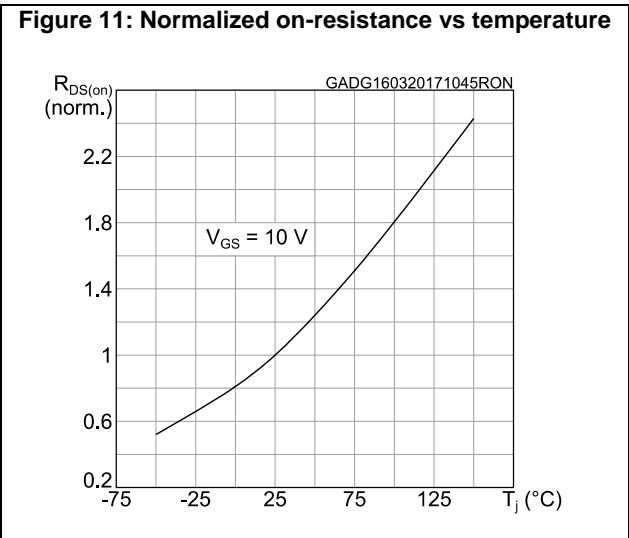
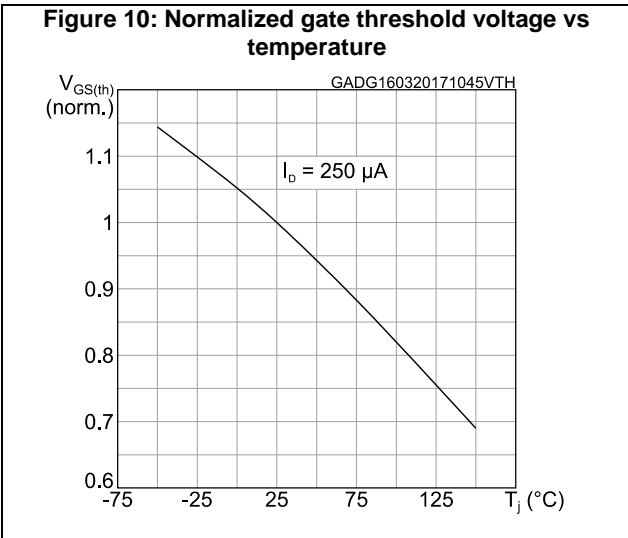
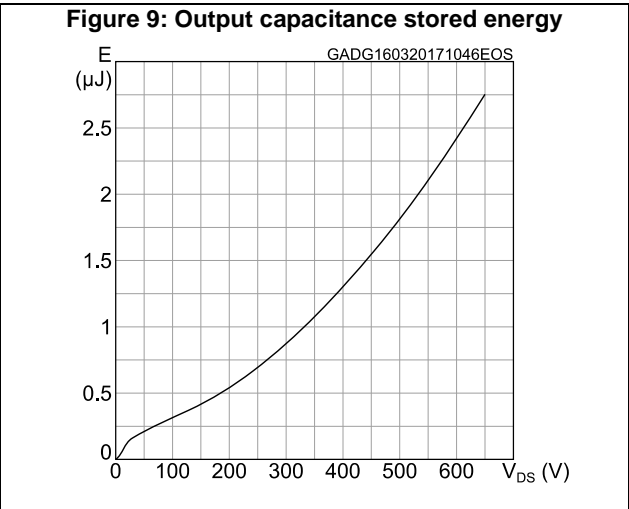
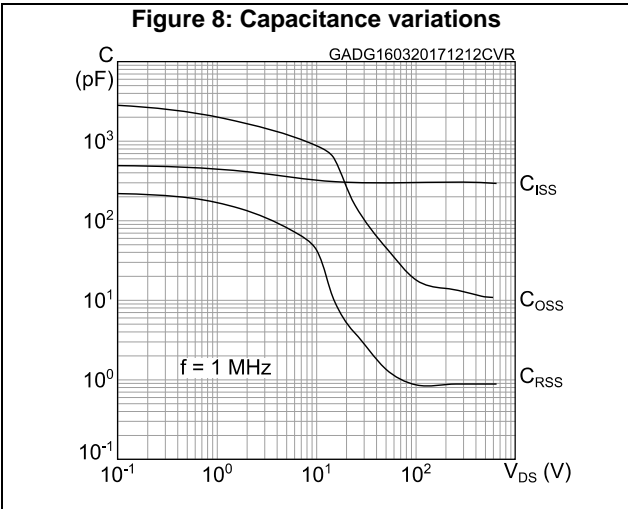
**Notes:**

(1)Pulse width is limited by safe operating area.

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

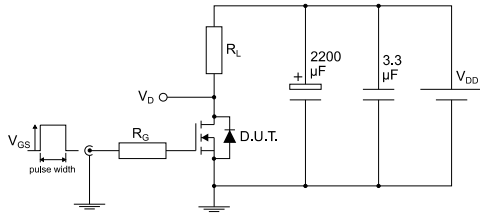
## 2.1 Electrical characteristics (curves)





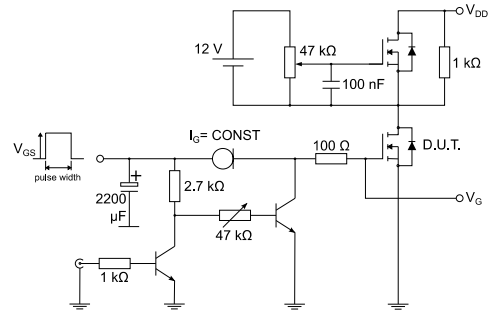
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



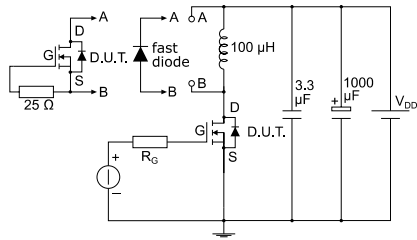
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**Figure 15: Test circuit for gate charge behavior**



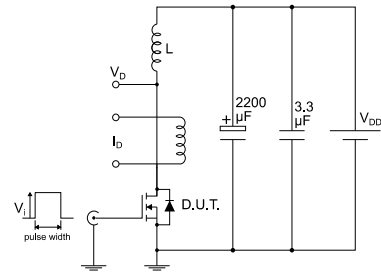
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**Figure 16: Test circuit for inductive load switching and diode recovery times**



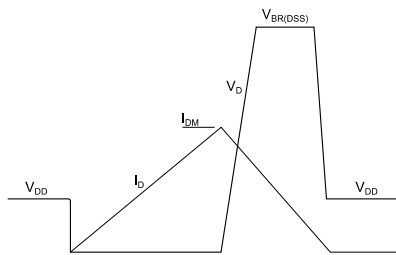
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**Figure 17: Unclamped inductive load test circuit**



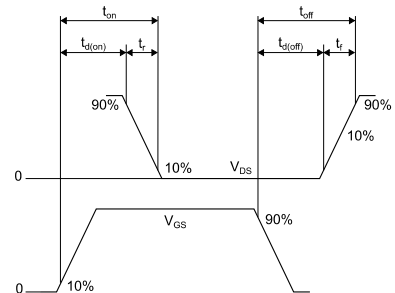
AM01471v1

**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

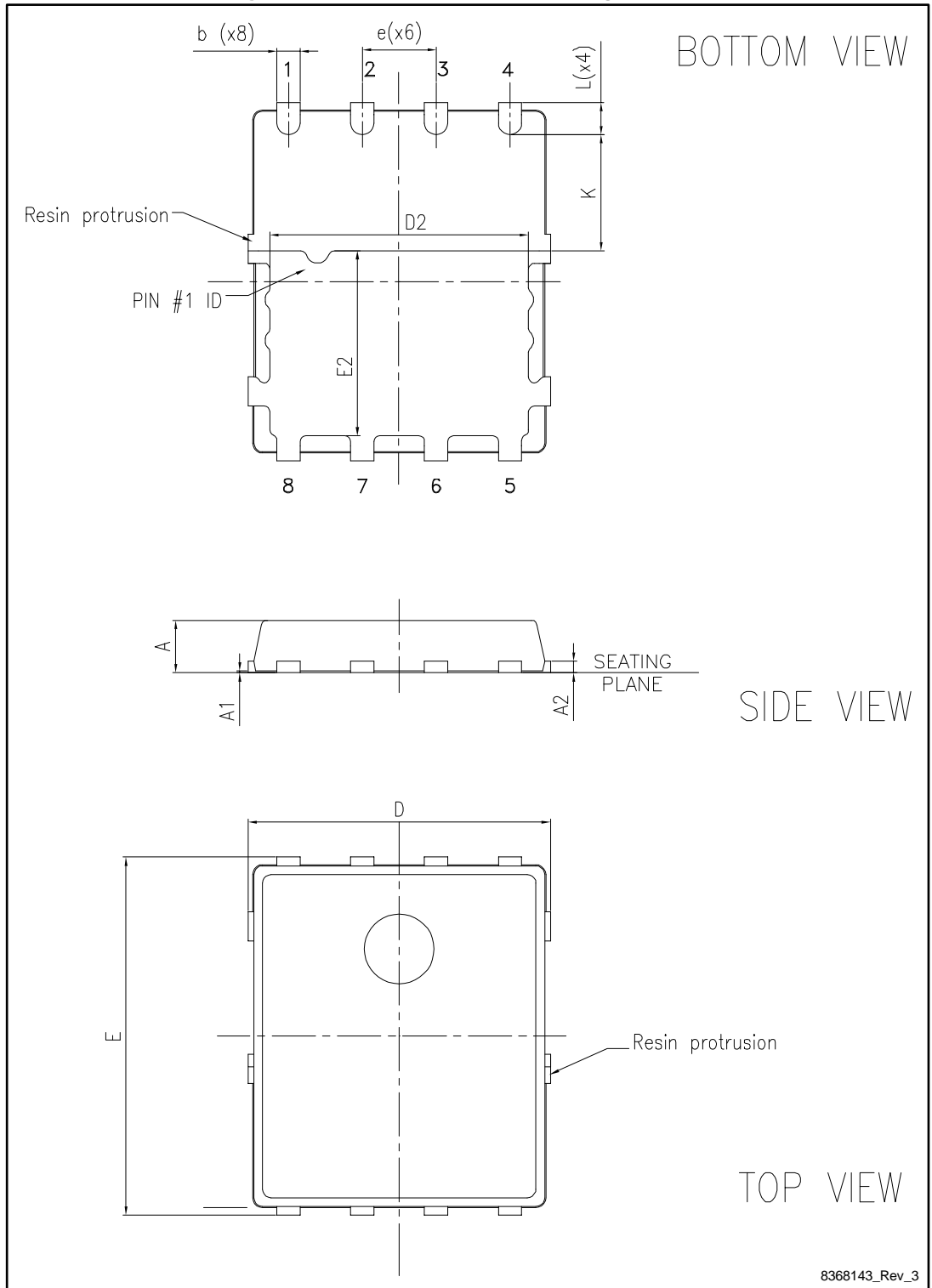
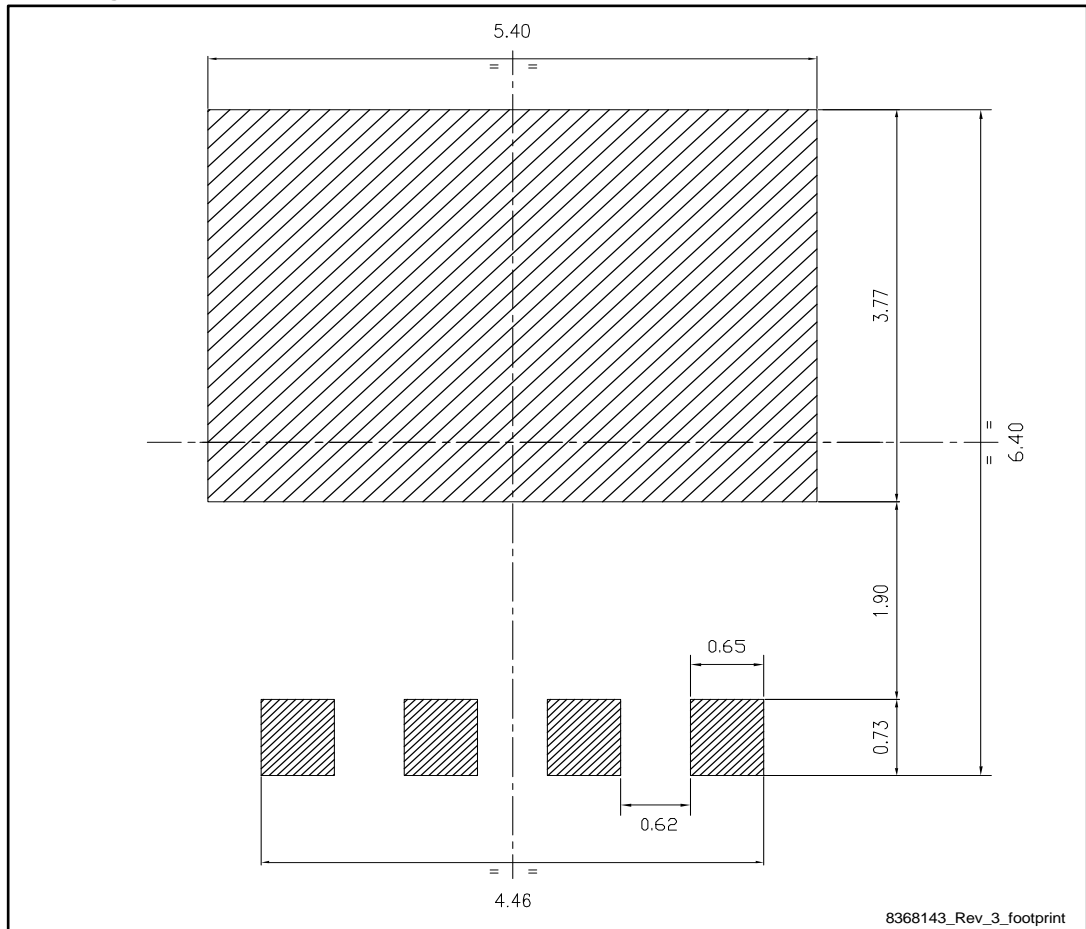


Table 8: PowerFLAT™ 5x6 HV mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 0.80 |      | 1.00 |
| A1   | 0.02 |      | 0.05 |
| A2   |      | 0.25 |      |
| b    | 0.30 |      | 0.50 |
| D    | 5.10 | 5.20 | 5.30 |
| E    | 6.05 | 6.15 | 6.25 |
| E2   | 3.10 | 3.20 | 3.30 |
| D2   | 4.30 | 4.40 | 4.50 |
| e    |      | 1.27 |      |
| L    | 0.50 | 0.55 | 0.60 |
| K    | 1.90 | 2.00 | 2.10 |

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

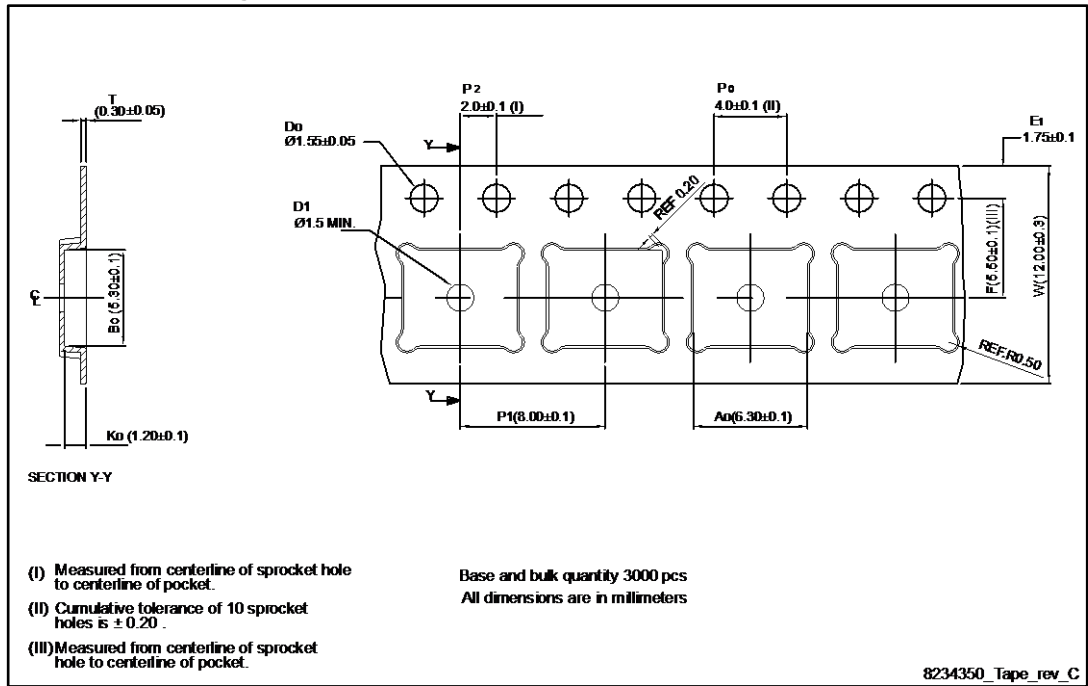


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

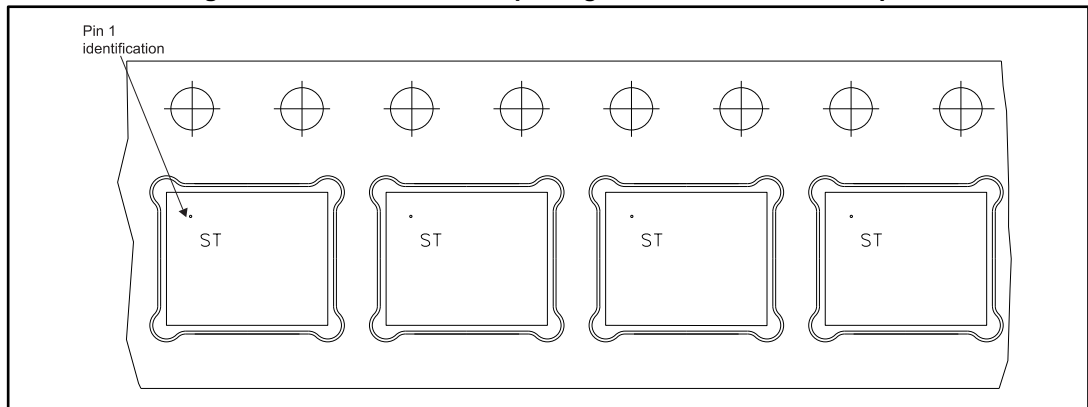
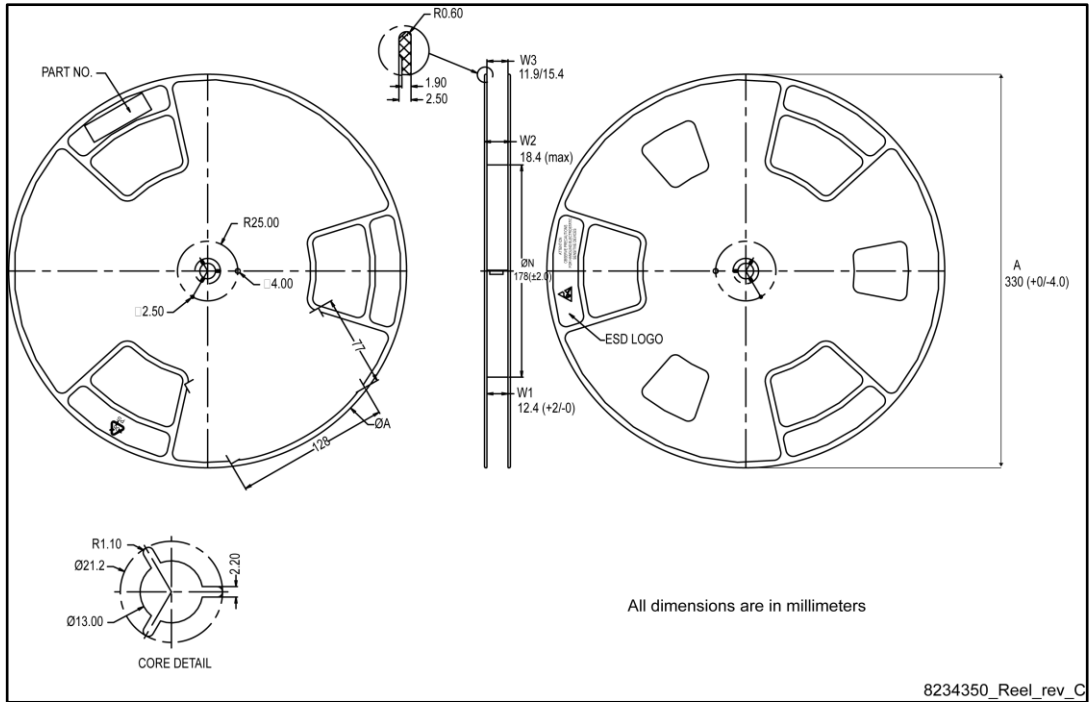


Figure 24: PowerFLAT™ 5x6 reel



## 5 Revision history

Table 9: Document revision history

| Date        | Revision | Changes       |
|-------------|----------|---------------|
| 16-Mar-2017 | 1        | First release |

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