Intel® Itanium® Processor 9300 Series and 9500 Series

Intel® Itanium® Processor Quad-Core 1.86-1.73 GHz with 24 MB L3 Cache 9350
Intel® Itanium® Processor Quad-Core 1.73-1.60 GHz with 20 MB L3 Cache 9340
Intel® Itanium® Processor Quad-Core 1.60-1.46 GHz with 20 MB L3 Cache 9330
Intel® Itanium® Processor Quad-Core 1.46-1.33 GHz with 16 MB L3 Cache 9320
Intel® Itanium® Processor Dual-Core 1.60 GHz Fixed Frequency with 10 MB L3 Cache 9310

Intel® Itanium® Processor Eight-Core 2.53 GHz with 32 MB LLC Cache 9560
Intel® Itanium® Processor Four-Core 2.40 GHz with 32 MB LLC Cache 9550
Intel® Itanium® Processor Eight-Core 2.13 GHz with 24 MB LLC Cache 9540
Intel® Itanium® Processor Four-Core 1.73 GHz with 20 MB LLC Cache 9520

Datasheet

November 2012

Reference Number: 322821-002

Contents

Figures

Tables

Revision History

Document Number	Revision Number	Description	Date
322821	-002	• Initial release of the 9300/9500 document.	November 2012
322821	-001	• Initial release of the document.	February 2010

§

1 Introduction

1.1 Overview

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series employ Explicitly Parallel Instruction Computing (EPIC) design concepts for a tighter coupling between hardware and software. In this design style, the interface between hardware and software is designed to enable the software to exploit all available compile-time information, and efficiently deliver this information to the hardware. It addresses several fundamental performance bottlenecks in modern computers, such as memory latency, memory address disambiguation, and control flow dependencies. The EPIC constructs provide powerful architectural semantics, and enable the software to make global optimizations across a large scheduling scope, thereby exposing available Instruction Level Parallelism (ILP) to the hardware. The hardware takes advantage of this enhanced ILP, and provides abundant execution resources. Additionally, it focuses on dynamic run-time optimizations to enable the compiled code schedule to flow at high throughput. This strategy increases the synergy between hardware and software, and leads to greater overall performance.

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series system interface, with its 4 full width and 2 half width Intel® QuickPath Interconnects, enables each processor to directly connect to other system components, thus can be used as an effective building block for very large systems. The balanced core and memory subsystem provide high performance for a wide range of applications ranging from commercial workloads to high performance technical computing.

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series are pin compatible and support a range of computing needs and configurations from a 2-way to large SMP servers (although OEM field upgrade methodologies vary). This document provides the electrical, mechanical and thermal specifications that must be met when using the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series in your systems.

Intel® Itanium® Processor 9300 Series

Intel® Itanium® Processor Quad-Core 1.86-1.73 GHz with 24 MB L3 Cache 9350
Intel® Itanium® Processor Quad-Core 1.73-1.60 GHz with 20 MB L3 Cache 9340
Intel® Itanium® Processor Quad-Core 1.60-1.46 GHz with 20 MB L3 Cache 9330
Intel® Itanium® Processor Quad-Core 1.46-1.33 GHz with 16 MB L3 Cache 9320
Intel® Itanium® Processor Dual-Core 1.60 GHz Fixed Frequency with 10 MB L3 Cache 9310

Product Features

- Quad Core
  - Four complete 64-bit processing cores on one processor.
  - Includes Dynamic Domain Partitioning.
- Advanced EPIC (Explicitly Parallel Instruction Computing) Architecture for current and future requirements of high-end enterprise and technical workloads.
  - Provide a variety of advanced implementations of parallelism, predication, and speculation, resulting in superior Instruction-Level Parallelism (ILP).
- Intel® Hyper-Threading Technology
  - Two times the number of OS threads per core.
- Wide, parallel hardware based on Intel® Itanium® architecture for high performance:
  - Integrated on-die L3 cache of up to 24 MB; cache hints for L1, L2, and L3 caches for reduced memory latency.
  - 128 general and 128 floating-point registers supporting register rotation.
  - Register stack engine for effective management of processor resources.
  - Support for predication and speculation.
- Extensive RAS features for business-critical applications, for example:
  - Machine check architecture with extensive ECC and parity protection.
  - On-chip thermal management.
  - Built-in processor information ROM (PIROM).
  - Built-in programmable EEPROM.
  - Hot-Plug Socket
  - Hot-add and hot removal.
  - Double Device Data Correction (DDDC) for x4 DRAMs, plus correction of a single bit error.
  - Single Device Data Correction (SDDC) for x8 DRAMs, plus correction of a single bit error.
  - Intel® QuickPath Interconnect Dynamic Link Width Reduction.
  - Intel® QuickPath Interconnect Clock Fail-Safe Feature.
  - Intel QuickPath Interconnect (Intel® QPI) Hot-Add and Removal.
  - DIMM Sparing, Memory Scrubbing, Memory Mirroring, and Memory Migration.
  - Architected firmware stack, including PAL and SAL support.
  - Directory-based and source-based coherency protocol.
  - Intel QPI poisoning, viral containment and cleanup.
- On-die Memory Controller
  - Each memory controller supports two Intel® Scalable Memory Interconnects.
  - Support for one Scalable Memory Buffer per Intel Scalable Memory Interconnect; four Scalable Memory Buffers per processor.
  - High memory bandwidth, thus improved performance.
  - 4.8 GT/s for the Intel® 7500 Scalable Memory Buffer.
- Intel® Virtualization Technology for virtualization for data-intensive applications.
  - Reduce virtualization complexity.
  - Improve virtualization performance.
  - Increase operating system compatibility.
- Intel® Cache Safe Technology ensures mainframe-caliber availability.
  - Minimize L3 cache errors.
  - Disable cache entries that have become hard errors.
  - Improve availability.
- High bandwidth Intel® QuickPath Interconnect for multiprocessor scalability:
  - 4 full and 2 half width Intel QPI Links
  - 4.8GT/s transfer rate.
  - Systems are easily scaled without sacrificing performance.
- Features to support flexible platform environments:
  - IA-32 Execution Layer supports IA-32 application binaries.
  - Bi-endian support.
  - Processor abstraction layer eliminates processor dependencies.

The Intel® Itanium® Processor 9300 Series delivers new levels of flexibility, reliability, performance, and cost-effective scalability for your most data-intensive business and technical applications. It provides 24 megabytes L3 cache accessed at core speed, Hyper-Threading Technology for increased performance, Intel® Virtualization Technology for improved virtualization, Intel® Cache Safe Technology for increased availability.

The Intel® Itanium® Processor 9300 Series consists of up to 4 core processors and a system interface unit. Each processor core provides a 6-wide, 8-stage deep execution pipeline. The resources consist of six integer units, six multimedia units, two load and two store units, three branch units and two floating-point units each capable of extended, double and single precision arithmetic. The hardware employs dynamic prefetch, branch prediction, a register scoreboard, and non-blocking caches to optimize for compile-time non-determinism. Each core provides duplication of all architectural state to support hardware multithreading, thus enabling greater throughput. Three levels of on-die cache minimize overall memory latency. It interfaces with the Ararat "1" Voltage Regulator Module, which used exclusively with the Intel® Itanium® Processor 9300 Series.

Intel® Itanium® Processor 9500 Series

Intel® Itanium® Processor Eight-Core 2.53 GHz with 32 MB LLC Cache 9560
Intel® Itanium® Processor Four-Core 2.40 GHz with 32 MB LLC Cache 9550
Intel® Itanium® Processor Eight-Core 2.13 GHz with 24 MB LLC Cache 9540
Intel® Itanium® Processor Four-Core 1.73 GHz with 20 MB LLC Cache 9520

Product Features

- Eight Core
  - Eight complete 64-bit processing cores on one processor, with two threads per core.
  - Each core provides in-order issue and execution of up to twelve instructions per cycle.
  - Includes dynamic domain partitioning and static hard partitioning.
- Advanced EPIC (Explicitly Parallel Instruction Computing) Architecture for current and future requirements of high-end enterprise and technical workloads.
  - Provide a variety of advanced implementations of parallelism, predication, and speculation, resulting in superior Instruction-Level Parallelism (ILP).
- Intel® Hyper-Threading Technology
  - Dual Domain Multithreading with independent front end and back end thread domains providing hardware support for 2 threads per core.
  - Support for Intel® Itanium® Processor New-Instructions.
- Wide, parallel hardware based on Intel® Itanium® architecture for high performance:
  - Integrated on-die LLC cache of up to 32MB; cache hints for FLC, MLC, and LLC caches for reduced memory latency.
  - 160 general and 128 floating-point registers supporting register rotation.
  - Register stack engine for effective management of processor resources.
  - Support for predication and speculation.
- Extensive RAS features for business-critical applications, for example:
  - Machine check architecture with extensive ECC and parity protection with firmware first error handling.
  - End-to-end error detection.
  - On-chip thermal management and power management.
  - Built-in processor information ROM (PIROM).
  - Built-in programmable EEPROM.
  - Hot Plug Socket.
  - Hot-add and hot removal support.
  - Double Device Data Correction (DDDC) for x4 DRAMs, plus correction support of a single bit error.
  - Single Device Data Correction (SDDC) for x8 and x4 DRAMs, plus correction of a single bit error.
  - Intel® QuickPath Interconnect Dynamic Link Width Reduction.
  - Intel® QuickPath Interconnect Clock Fail-Safe Feature.
  - Intel® QuickPath Interconnect Hot-Add and Removal.
  - Memory DIMM and Rank Sparing, Memory Scrubbing, Memory Mirroring, and Memory Migration.
  - Intel® Turbo Boost Technology, featuring sustained boost.
  - Architected firmware stack, including PAL and SAL support.
  - Directory-based and source-based coherency protocol.
  - Intel QPI poisoning, viral containment and cleanup.
- Two On-die Memory Controllers
  - Each memory controller supports two Intel® Scalable Memory Interconnects that operate in lockstep.
  - Support for one Scalable Memory Buffer per Intel Scalable Memory Interconnect; four Scalable Memory Buffers per processor.
  - High memory bandwidth, thus improved performance.
  - 4.8 GT/s for the Intel® 7500 Scalable Memory Buffer.
  - 6.4 GT/s for the Intel® 7510 Scalable Memory Buffer.
- Intel® Instruction Replay Technology to replay core pipeline for pipeline management and core RAS.
- Intel® Virtualization Technology (Intel® VT) for Intel® 64 or Itanium ®architecture (Intel ® Vt-i) 3 - Virtualization Support Extensions for Intel® Virtualization Technology.
  - Reduce virtualization complexity.
  - Improve virtualization performance via hardware optimization.
  - Increase operating system compatibility.
- Intel® Cache Safe Technology ensure mainframe-caliber availability.
  - Minimize LLC cache errors.
  - Disable cache entries that have become hard errors.
  - Directory Cache covers 33% more cache lines.
  - Improve availability.
- High bandwidth Intel® QuickPath Interconnect for multiprocessor scalability:
  - 4 full and 2 half width Intel QPI Links
  - 6.4GT/s transfer rate with aggregate data bandwidth of 28.8 GB/s.
  - Systems are easily scaled without sacrificing performance.
- Features to support flexible platform environments:
  - Fully compatible with binaries for the Intel Itanium processor family with Instruction level advancements.
  - LGA1248 Socket Level compatible with the Intel® Itanium® Processor 9300 Series.
  - Bi-endian support.
  - Processor abstraction layer eliminates processor dependencies.

The Intel® Itanium® Processor 9500 Series delivers increased levels of flexibility, reliability, performance, and cost-effective scalability for your most data-intensive business and technical applications.

The Intel® Itanium® Processor 9500 Series processor provides up to 32 megabytes LLC cache, Hyper-Threading Technology for increased performance, Intel® Virtualization Technology for improved virtualization, Intel® Cache Safe Technology for increased availability. Intel® Turbo Boost Technology, featuring sustained boost. The Intel® Itanium® Processor 9500 Series employs advanced power monitoring and control to deliver a higher processor frequency at all times, for maximum performance on all workloads. The result is a higher thermal envelope utilization for more overall performance. The Intel® Itanium® Processor 9500 Series offers large cache arrays covered by ECC including the large LLC utilizing double correct/triple detect (DECTED) and protecting the MLI/MLD with in-line single correct/double detect (SECDED). In addition, the processor provides extensive parity protection and parity interleaving on nearly all RFs, end-to-end parity protection with recovery-support on all critical internal buses and data paths including the ring. Residue protection on Floating Point unit, along with the adoption of radiation-hardened (RAD) sequential latching elements for vulnerable architectural and state. The Intel® Itanium® Processor 9500 Series processor interfaces exclusively with the Ararat II Voltage Regulator Module.

The Intel® Itanium® Processor 9500 Series consists of up to 8 core processors and a system interface unit. Each processor core provides a 12-wide, 11-stage deep execution pipeline. The resources consist of six integer units, one integer multiply unit, four multimedia units, two load/store units, three branch units and two floating-point units each capable of extended, double and single precision arithmetic. The hardware employs dynamic prefetch, branch prediction, a register scoreboard, and non-blocking caches to optimize for compile-time non-determinism. 32 additional stacked general registers are provided over the Intel® Itanium® Processor 9300 Series, and hardware support is provided for denormal, unnormal, and pseudo-normal operands for floating point software assist offloading.

New instructions on the Intel® Itanium® Processor 9500 Series simplify common tasks. They include: clz (count leading zeros), mpy4 and mpyshl4(unsigned integer multiply/ shift and multiply), mov-to-DAHR/mv-from-DAHR (for improved MLD/FLD prefetcher hinting and performance), and hint@priority (used by the processor to temporarily allocate more resources to a thread). Advanced Explicitly Parallel Instruction Computing (EPIC) is enhanced on the Intel® Itanium® Processor 9500 Series by increasing the capacity of retiring instructions per cycle from 6 to a maximum of 12 instructions per cycle per core.

Intel® Hyper-threading Technology is enhanced in the Intel® Itanium® Processor 9500 Series with dual domain multithreading, which enables independent front-end and back-end pipeline execution to improve multi-thread efficiency and performance for both new and legacy applications. It provides hardware support for two threads per core, with a threaded 96 entry per thread Instruction Buffer and threaded MLDTLB and FLDTLB, and a dedicated load return path from the MLD to the integer register file. Three levels of on-die cache minimize overall memory latency, with 16 KB instruction cache FLI/16 KB write-through data cache FLD that comprise the FLC and 512 KB MLI/ 256 KB writeback data cache MLD that comprise the MLC.

The Intel® Itanium® Processor 9500 Series offers a new RAS feature: Intel® Instruction Replay Technology. Pipeline replay resolves stall conditions that occur when the microprocessor pipeline encounters a resource hazard that prevents immediate execution. In a replay, the instruction that encountered the resource hazard is removed from the pipeline, along with all the instructions that come after it. The instruction is then read again out of the instruction buffer for replay and re-executed. To ensure a replay can be initiated for any instruction in the pipeline that encounters a resource hazard, a copy of each instruction is maintained in the instruction buffer until the instruction has successfully traversed the pipeline and is no longer needed. If necessary, an instruction can replay multiple times. As a result, Intel® Instruction Replay Technology automatically detects and many corrects soft errors in the instruction pipeline. With this technology, soft errors can be identified and corrected in as few as seven clock cycles, which is fast enough to be invisible to the software running on the platform.

1.2 Architectural Overview

The sections below give an overview of the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series.

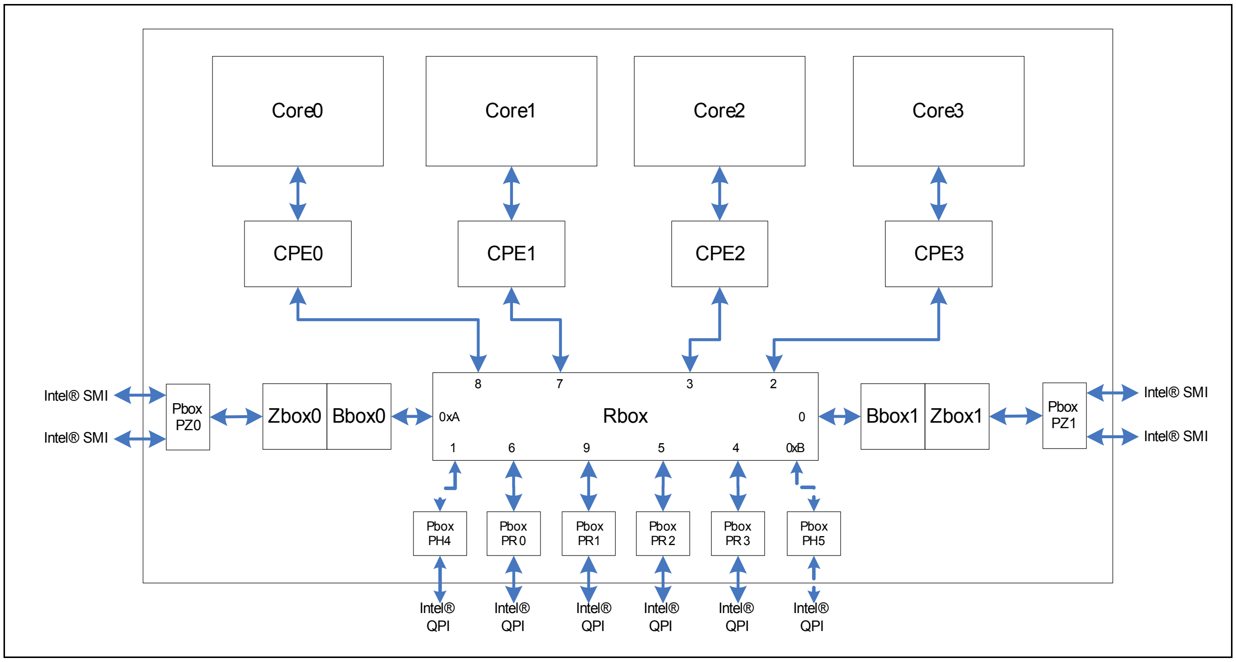
1.2.1 Intel® Itanium® Processor 9300 Series Overview

The Intel® Itanium® Processor 9300 Series processor is a quad-core architecture. It supports up to four processor cores, each with its own L3, L2, and L1 level cache. Also supported are the following page sizes for purges or inserts: 4K, 8K, 16K, 64K, 256K, 1M, 4M, 16M, 64M, 256M, 1G, 4G.

The architecture interfacing the cores to the system is referred to as the System Interface. Each processor core has it own Caching Agent (CPE). The CPE interfaces between the processor core and the Intel QuickPath Interconnect. The Intel® Itanium® Processor 9300 Series processor has two Home Agents (Bbox). The Bbox interfaces between the memory controller and the Intel® QuickPath Interconnect and supports a directory cache. Each Bbox interfaces with a memory controllers (Zbox). Each memory controller supports two Intel SMI in lockstep. The Intel SMI are the interconnects to Intel® 7500 Scalable Memory Buffer. The processor supports six Intel QuickPath Interconnects at the socket, four full width and two half width. The Caching Agent, Home Agent, and Intel QuickPath Interconnects are connected via a 12-port Crossbar Router, each port supporting the Intel QuickPath Interconnect protocol. Figure 1-1 shows the Intel® Itanium® Processor 9300 Series block diagram.

The Intel QPI viral and poison fields are used to flag corrupted system state and bad data accordingly. Once it has “gone viral”, an Intel QPI agent will set the viral field within all packet headers. Viral mode is entered in three ways: receiving a viral packet, upon a detecting fatal/panic error, or when a global viral signal (from Cboxes) is asserted. Viral is cleared on Reset. Poisoning is used to indicate bad data on a per-flit basis. Poison does not indicate corrupted system coherency, but rather that a particular block of data is not reliable.

Figure 1-1. Intel® Itanium® Processor 9300 Series Processor Block Diagram

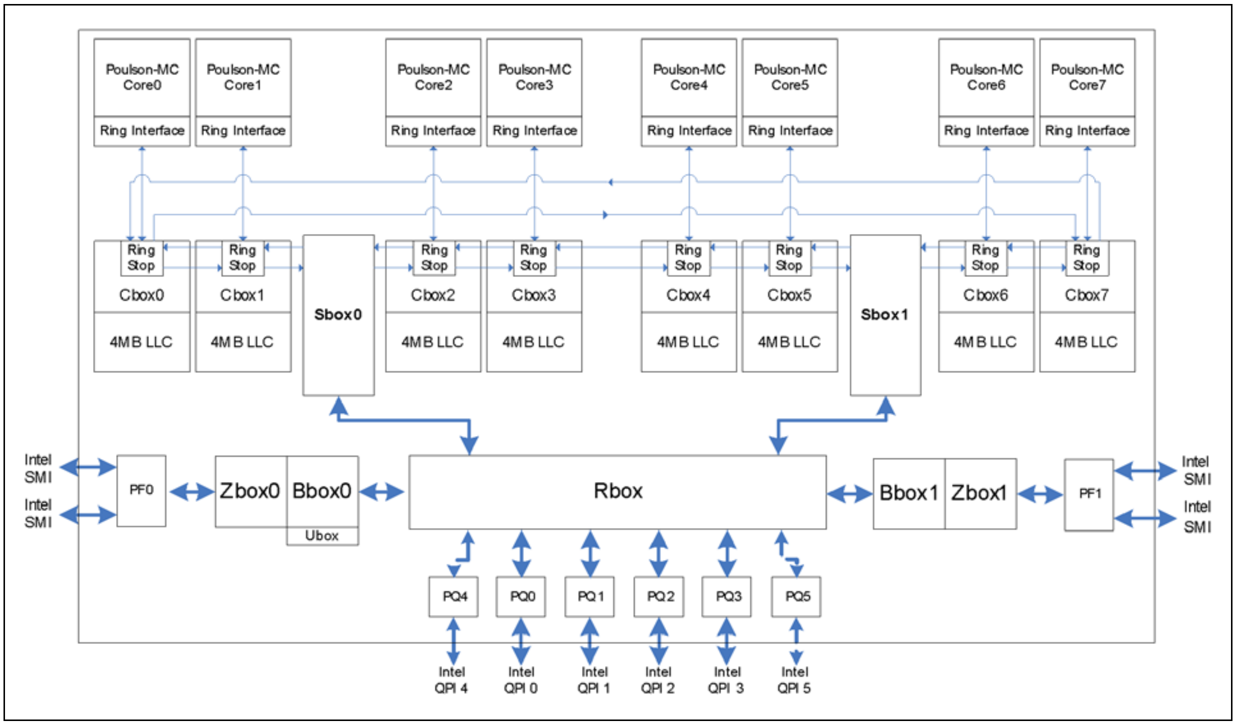


1.2.2 Intel® Itanium® Processor 9500 Series Overview

The Intel® Itanium® Processor 9500 Series is an eight core architecture. It supports up to eight cores, each with its own First Level Cache (FLC) and Mid Level Cache (MLC), both of which are split into instruction and data caches (FLI/FLD and MLI/MLD, respectively). The Last Level Cache (LLC) is shared among the cores and supports up to 32 MB. Also supported are the following page sizes for purges or inserts: 4K, 8K, 16K, 64K, 256K, 1M, 4M, 16M, 64M, 256M, 1G, 4G.

The architecture interfacing the cores to the system is referred to as the uncore. Each Intel® Itanium® Processor 9500 Series core interfaces to the Ring. The Ring provides connectivity to the Last Level Cache via the Cache Controllers (Cboxes). The Ring also provides connectivity to Intel QPI via Ring/Sbox. The Sbox and Cbox provide the supports for the two Intel QPI Caching Agents. The processor has two Home Agents (Bbox). The Bbox interfaces between the memory controller and the Intel® QuickPath Interconnect and supports a directory cache. Each memory controller supports two Intel® Scalable Memory Interconnects (Intel® SMI) in lockstep. The Intel SMI are the interconnects to Scalable Memory Buffer. The Intel® Itanium® Processor 9500 Series processor supports six Intel® QuickPath Interconnects at the socket, four full width and two half width. The Caching Agent, Home Agent, and Intel® QuickPath Interconnects are connected via a 10-port Crossbar Router, each port supporting the Intel® QuickPath Interconnect protocol. Figure 1-2 shows the processor block diagram.

Figure 1-2. Intel® Itanium® Processor 9500 Series Processor Block Diagram



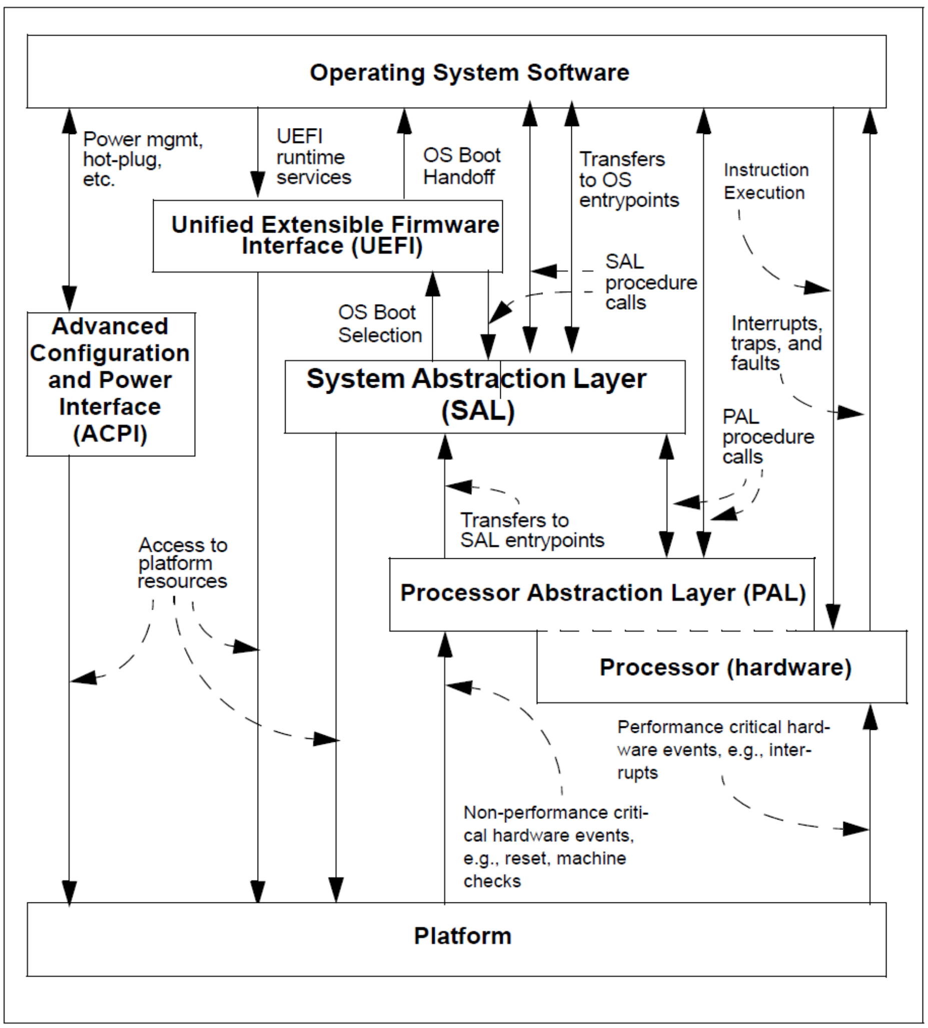
The Intel QPI viral and poison fields are used to flag corrupted system state and bad data accordingly. Once it has “gone viral”, an Intel QPI agent will set the viral field within all packet headers. Viral mode is entered in three ways: receiving a viral packet, upon a detecting fatal/panic error, or when a global viral signal (from Cboxes) is asserted. Viral is cleared on Reset. Poisoning is used to indicate bad data on a per-flit basis. Poison does not indicate corrupted system coherency, but rather that a particular block of data is not reliable.

Intel® Itanium® Processor 9500 Series PAL's Demand Based Switching (DBS) support includes implementations of Power/Performance states (P-states) and Halt states (C-states). For the PAL Halt state interface and architected specifications of the PAL P-state interface, see the *Intel® Itanium® Architecture Software Developer's Manual*, Volume 2, Section 11.6. PAL controls the Intel® Itanium® Processor 9500 Series processor power through a special built-in microcontroller that manipulates voltage and frequency. PAL communicates requested P-states to this controller through internal registers.

As shown in Figure 1-3, Itanium architecture-based firmware consists of several major components: Processor Abstraction Layer (PAL), System Abstraction Layer (SAL), Unified Extensible Firmware Interface (UEFI) and Advanced Configuration and Power Interface (ACPI). PAL, SAL, UEFI and ACPI together provide processor and system initialization for an operating system boot. PAL and SAL provide machine check abort handling. PAL, SAL, UEFI and ACPI provide various run-time services for system functions which may vary across implementations. The interactions of the various services that PAL, SAL, UEFI and ACPI provide are illustrated in Figure 1-3. In the context of this model and throughout the rest of this chapter, the System Abstraction Layer (SAL) is a firmware layer which isolates operating system and other higher level software from implementation differences in the platform, while PAL is the firmware layer that abstracts the processor implementation.

Protection Keys provide a method to restrict permission by tagging each virtual page with a unique protection domain identifier. The Protection Key Registers (PKR) represent a register cache of all protection keys required by a process. The operating system is responsible for management and replacement polices of the protection key cache. Before a memory access (including IA-32) is permitted, the processor compares a translation's key value against all keys contained in the PKRs. If a matching key is not found, the processor raises a Key Miss fault. If a matching Key is found, access to the page is qualified by additional read, write and execute protection checks specified by the matching protection key register. If these checks fail, a Key Permission fault is raised. Upon receipt of a Key Miss or Key Permission fault, software can implement the desired security policy for the protection domain. Some processor models may implement additional protection key registers and protection key bits. Unimplemented bits and registers are reserved. Please see the processor-specific documentation for further information on the number of protection key registers and protection key bits implemented on the processor.

Figure 1-3. Intel® Itanium® Processor 9500 Series Firmware Diagram



1.3 Processor Feature Comparison

The Intel® Itanium® Processor 9300 Series processor and Intel® Itanium® Processor 9500 Series processor features are compared below in Table 1-1.

Table 1-1. Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series Feature Comparison

Description	Intel® Itanium® Processor 9300 Series	Intel® Itanium® Processor 9500 Series
Socket	LG1248	LG1248
Transistors	2 billion	3.1 billion
Cores/Threads	up to 4/8	up to 8/16
Clock speeds	up to 1.86 GHz via Intel® Turbo Boost with sustained boost	1.73 - 2.53 GHz
Integrated on-die cache	L1 (L1I 16K/L1D 16K), L2 (L2I 512K, L2D 256K), inclusive L3 (6 MB per core, up to 24 MB)	FLC (FLI 16K/FLD 16K), MLC (MLI 512K, MLD 256K), LLC (shared, up to 32 MB)
Ararat Voltage Regulator Module Support	Ararat "I"	Ararat II
Supported speeds	DDR3-800	DDR3-800 and DDR3-1067
Intel QPI links	6 (4 full/2 half width at up to 4.8 GT/s)	6 (4 full/2 half width at up to 6.4 GT/s)
Intel QPI Hot-plug	Supported	Supported
Intel QPI Link self-healing	Supported	Supported
Intel QPI Clock fail-safe	Supported	Supported
Intel QPI Data scrambling	Supported	Required
Intel QPI Periodic retraining	Not Supported	Required[1]
Integrated memory controllers	2	2
Intel® SMI Interface	Intel® 7500 Scalable Memory Buffer (4.8 GT/s)	Intel® 7500 Scalable Memory Buffer (4.8 GT/s) Intel® 7510 Scalable Memory Buffer (6.4 GT/s)
Intel® SMI Hot-plug	Supported	Supported
Physical address space/virtual address space	50 physical/64 virtual	50 physical/64 virtual
Caching agent architecture	four caching agents per socket where each agent is responsible for all of the address space and dedicated to a core	two caching agents per socket are responsible for half the address space and shared among the cores
Home agents per socket	2	2
Directory Cache	Supported	Supported
Intel® Virtualization Technology (Intel® VT)	Intel® Vt-i 2	Intel® Vt-i 3
Hot add/hot removal at Intel QPI link and DIMM memory interface	Supported	Supported
Hot add CPU	Supported[2,3]	Supported[2,3]
Hot add memory	Supported[2,3]	Supported[2,3]
Hot remove/hot replace memory	Supported[2,3]	Supported[2,3]
Memory sparing technique	DIMM	DIMM and Rank
Memory scrubbing	Supported	Supported
Memory mirroring	Supported	Supported

Description	Intel® Itanium® Processor 9300 Series	Intel® Itanium® Processor 9500 Series
Memory patrolling	Supported	Supported
Memory migration	Supported	Supported
Support for mixing of x4 and x8 on the same DDR channel	Not Supported	Supported
Online/Offline CPU (OS assisted)	Supported	Supported
Online/Offline Memory (OS assisted)	Supported	Supported
Online/Offline I/O Hub	Supported	Supported
Thermal Design Power (TDP) SKUs	130W, 155W, 185W	130W and 170W

Notes:

1. OEM responsible for specifying platform-specific retraining interval.
2. Electrical isolation only, no physical add/remove supported.
3. Assume spare is installed.

1.4 Processor Abstraction Layer

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series require implementation-specific Processor Abstraction Layer (PAL) firmware. PAL firmware supports processor initialization, error recovery, and other functionality. It provides a consistent interface to system firmware and operating systems across processor hardware implementations. The *Intel® Itanium® Architecture Software Developer's Manual,* Volume 2: System Architecture, describes PAL. Platforms must provide access to the firmware address space and PAL at reset to allow the processors to initialize.

The System Abstraction Layer (SAL) firmware contains platform-specific firmware to initialize the platform, boot to an operating system, and provide runtime functionality. Further information about SAL is available in the *Intel® Itanium® Processor Family System Abstraction Layer Specification*.

1.5 Mixing Processors of Different Frequencies and Cache Sizes

All Intel® Itanium® Processor 9300 Series processors and Intel® Itanium® Processor 9500 Series in the same system partition are required to have the same last level cache size and identical core frequency. Mixing processors of different core frequencies, cache sizes, and mixing Intel® Itanium® Processor 9300 Series with Intel® Itanium® Processor 9500 Series is not supported and has not been validated by Intel. Operating system support for multiprocessing with mixed components should also be considered.

1.6 Terminology

In this document, "the processor" refers to the Intel® Itanium® Processor 9300 Series and/or Intel® Itanium® Processor 9500 Series, unless otherwise indicated.

An '_N' notation after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when RESET_N is low, a processor reset has been requested. When NMI is high, a non-maskable interrupt has occurred. In the case of lines where the name does not imply an active state but describes part of a binary sequence (such as address or data), the '_N' notation implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a Hex 'A', and D [3:0] _N = 'LHLH' also refers to a Hex 'A' (H = High logic level, L = Low logic level).

A signal name has all capitalized letters, for example, VCTERM.

A symbol referring to a voltage level, current level, or a time value carries a plain subscript, for example, Vccio, or a capitalized abbreviated subscript, for example, TCO.

1.7 State of Data

The data contained in this document is subject to change. It is the best information that Intel is able to provide at the publication date of this document.

1.8 Reference Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents:

Document Name
Intel® Itanium® Processor 9300 Series and 9500 Series Specification Update
Intel® Itanium® Architecture Software Developer's Manual, Volume 1: Application Architecture
Intel® Itanium® Architecture Software Developer's Manual, Volume 2: System Architecture
Intel® Itanium® Architecture Software Developer's Manual, Volume 3: Instruction Set Reference
Intel® Itanium® Architecture Software Developer's Manual, Volume 4: IA-32 Instruction Set Reference
Intel® Itanium® 9300 Series Processor Reference Manual for Software Development and Optimization
Intel® Itanium® 9500 Series Processor Reference Manual for Software Development and Optimization
Intel® Itanium® Processor Family System Abstraction Layer Specification
Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series Platform Design Guide
System Management Bus (SMBus) Specification

Note: Contact your Intel representative or check http://developer.intel.com for the latest revision of the reference documents.

§

2 Electrical Specifications

This chapter describes the electrical specifications of the Intel® Itanium® Processor 9300 Series and 9500 Series processors.

2.1 Intel® QuickPath Interconnect and Intel® Scalable Memory Interconnect Differential Signaling

The links for Intel® QuickPath Interconnect (Intel® QPI) and Intel® Scalable Memory Interconnect (Intel® SMI) signals use differential signaling. The Intel® SMI bus pins are referred to as FB-DIMM pins on the package. The termination voltage level for the processor for uni-directional serial differential links, each link consisting of a pair of opposite-polarity (D+, D-) signals, is V_{SS}.

Termination resistors are provided on the processor silicon and are terminated to V_{SS}, thus eliminating the need to terminate the links on the system board for the Intel® QuickPath Interconnect and FB-DIMM signals.

When designing a system, Intel strongly recommends that design teams perform analog simulations of the Intel® QuickPath Interconnect and FB-DIMM pins. Please refer to the latest available revision of the *Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series Platform Design Guide.*

Figure 2-1 illustrates the active on-die termination (ODT) of these differential signals. All the differential signals listed in Table 2-1 have ODT resistors. Also included in the table are the debug signals.

Figure 2-1. Active ODT for a Differential Link Example

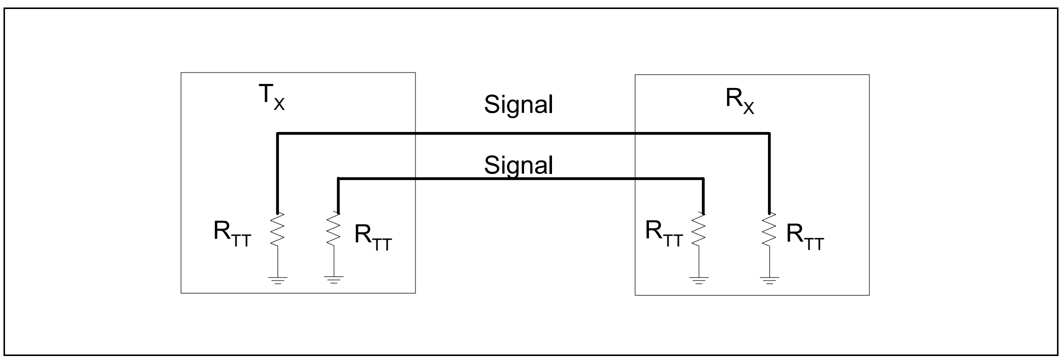


Table 2-1. Signals with R_{TT}

Signal	Termination
CSI[3:0]R[P/N]Dat[19:0] CSI[5:4]R[P/N]Dat[9:0] CSI[3:0]T[P/N]Dat[19:0] CSI[5:4]T[P/N]Dat[9:0] CSI[5:0]R[P/N]Clk CSI[5:0]T[P/N]Clk	VSS
FBD0NBICLK[A/B][P/N]0 FBD1NBICLK[C/D][P/N]0 FBD0SBOCLK[A/B][P/N]0 FBD1SBOCLK[C/D][P/N]0 FBD0NBI[A/B][P/N][13:0] FBD1NBI[C/D][P/N][13:0] FBD0SBO[A/B][P/N][10:0] FBD1SBO[C/D][P/N][10:0]	VSS
XDPOCPD_N[7:0] TRIGGER_N[1:0] XDPOCPFRAME_N XDPOCP_STRB_IN_N PRBMODE_REQST_N XDPOCP_STRB_OUT_N PRBMODE_RDY_N	VCCIO

2.2 Signal Groups

The signals are grouped by buffer type and similar characteristics as listed in Table 2-2. The buffer type indicates which signaling technology and specifications apply to the signals.

Table 2-2. Signal Groups (Sheet 1 of 3)

Signal Group	Buffer Type	Signals 1, 2, 3
Differential System Reference Clock		
Differential	CMOS In Differential Pair	SYSCLK, SYSCLK_N; SYSUTST_REFCLK_N, SYSUTST_REFCLK
Intel® QuickPath Interconnect Signal Groups		
Differential	Input	CSI[3:0]R[P/N]Dat[19:0], CSI[5:4]R[P/N][9:0] CSI[5:0]R[P/N]CLK
Differential	Output	CSI[3:0]T[P/N]Dat[19:0], CSI[5:4]T[P/N][9:0], CSI[5:0]T[P/N]CLK
FB-DIMM Signals		
Differential	Input	FBD0NBICLK[A/B][P/N]0 FBD1NBICLK[C/D][P/N]0
Differential	Output	FBD0SBOCLK[A/B][P/N]0 FBD1SBOCLK[C/D][P/N]0
Differential	Input	FBD0NBI[A/B][P/N][13:0] FBD1NBI[C/D][P/N][13:0]
Differential	Output	FBD0SBO[A/B][P/N][10:0] FBD1SBO[C/D][P/N][10:0]
TAP		

Table 2-2. Signal Groups (Sheet 2 of 3)

Signal Group	Buffer Type	Signals 1, 2, 3
Single-ended	CMOS Inputs	TCK, TDI, TMS, TRST_N
	GTL Open Drain Output	TDO
SMBus		
Single-ended	GTL I/O	SMBCLK, SMBDAT
SPD Bus		
Single-ended	GTL I/O	SPDCLK SPDDAT
Setup		
Single-ended	GTL Input	BOOTMODE[1:0], SKTID[2:0]
System Management		
Single-ended	CMOS Input	LRGSCLSYS
Flash ROM Port		
Single-ended	GTL-open Drain Input	FLASHROM_CFG[2:0], FLASHROM_DATI
	GTL-open Drain Output	FLASHROM_CS[3:0]_N, FLASHROM_CLK, FLASHROM_DATO, FLASHROM_WP_N
ERROR Bus		
Single-ended	GTL Open Drain Output GTL Input	ERROR[0]_N, ERROR[1]_N MEM_THROTTLE_L
Power-up		
Single-ended	GTL Input	PWRGOOD, RESET_N
Thermal		
Single-ended	GTL-Open Drain Output GTL Input	PROCHOT_N, THERMTRIP_N, THERMALERT_N FORCEPR_N
VID Port[4] (Intel® Itanium® Processor 9300 Series)		
Single-ended	CMOS Output	VID_VCCCORE[6:0], VID_VCCCACHE[5:0], VID_VCCUNCORE[6:0]
SVID Port[4] (Intel® Itanium® Processor 9500 Series)		
Single-ended	GTL Output	SVID_CLK
	GTL I/O	SVD_DATIO
	GTL Input	SVID_ALERT_N
Voltage Regulator [4]		
Single-ended	Open Collector/Drain Output	VR_THERMTRIP_N, VRPWRGD (Intel® Itanium® Processor 9300 Series processor), VR_READY (Intel® Itanium® Processor 9500 Series processor), VR_FAN_N
Voltage Regulator Control [4]		
Single-ended	CMOS Input GTL Input Open Collector/Drain Output	VROUTPUT_ENABLE0 VR_THERMALERT_N VR_THERMTRIP_N, VRPWRGD, VR_FAN_N

Table 2-2. Signal Groups (Sheet 3 of 3)

Signal Group	Buffer Type	Signals 1, 2, 3
Debug		
Single-ended	GTL I/O	XDPOCPD_N[7:0],TRIGGER_N[1:0] XDPOCPFRAME_N
	GTL Input	XDPOCP_STRB_IN_N, PRBMODE_REQST_N
	GTL Output	XDPOCP_STRB_OUT_N, PRBMODE_RDY_N
Power Supplies		
	Core	V_{CCCORE}[4]
	Uncore	$V_{CCUNCORE}$[4]
	Cache (Intel® Itanium® Processor 9300 Series)	$V_{CCCACHE}$[4]
	Analog	V_{CCA}
	I/O	V_{CCIO}
	Stand-by	V_{CC33_SM}
V_{CC33_SM} Pins		
PIROM	Input	PIR_SCL
	I/O	PIR_SDA
	Input	PIR_A0
	Input	PIR_A1
	Input	SM_WP

Notes:

1. CMOS signals have a reference voltage (Vref) equal to VCCIO/2.
2. GTL signals have a reference voltage (Vref) equal to VCCIO*(2/3).
3. All single-ended buffer types, including inputs, outputs and input/outputs, include an on-die pull up resistor between 4 kOhms and 8.7 kOhms. Recommended values for external pull-downs on the inputs and input/output signals must meet the V_{il} specification for that buffer.

2.3 Reference Clocking Specifications

The processor has one input reference clock, SYSCLK/SYSCLK_N for the Intel® QPI interface. The processor timing specified in this section is defined at the processor pins unless otherwise noted.

Table 2-3. Intel® QuickPath Interconnect/Intel® Scalable Memory Interconnect Reference Clock Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Notes
fsysclk (ssc-off)	System clock frequency	133.31	133.33	133.34	MHz	
Fsyclk (scc-on)	System clock frequency	132.62	132.99	133.37	MHz	
$ER_{sysclk\text{-}diff\text{-}Rise}$, $ER_{sysclk\text{-}diff\text{-}Fall}$	Differential Rising and Falling Edge Rates	1.0		4.0	V/ns	3,4
$T_{sysclk\_dutycycle}$	Duty cycle of Reference clock	40		60	% period	3
$C_{i\text{-}CK}$	Clock Input Capacitance	0.5		2.0	pf	
VH	Differential High Input Voltage	0.15			V	3
VL	Differential Low Input Voltage			-0.15	V	3
V_{Cross}	Absolute crossing point	0.25	0.35	0.55	V	1, 5, 6
V_{Cross_delta}	Peak-peak variation			140	mv	1, 5, 7
$V_{RB\text{-}Diff}$	Differential Ringback voltage threshold	-100		100	mV	3, 10

Table 2-3. Intel® QuickPath Interconnect/Intel® Scalable Memory Interconnect Reference Clock Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Notes
T_{Stable}	Allowed time before ringback	500			ps	3, 10
$T_{REFCLK\text{-}JITTER\text{-}RMS\text{-}ONEPLL}$	Accumulated rms jitter over n UI of a given PLL model output in response to the jittery reference clock input. The PLL output is generated by convolving the measured reference clock phase jitter with a given PLL transfer function. Here n=12.			0.5	ps	2

Note:
1. Measurement taken from single-ended waveform.
2. The given PLL parameters are: Underdamping (z) = 0.8 and natural frequency = fn = 7.86E6 Hz; wn = 2 *fn. N_minUI = 12 for Intel® QuickPath Interconnect 4.8 Gt/s channel.
3. Measurement taken from differential waveform.
4. Measured from -150 mV to +150 mV on the differential waveform (derived from SYSCLK minus SYSCLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 2-4.
5. Measured at crossing point where the instantaneous voltage value of the rising edge SYSCLK equals the falling edge SYSCLK_N. See Figure 2-2.
6. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 2-3.
7. Defined as the total variation of all crossing voltages of Rising SYSCLK and falling SYSCLK_N. This is the maximum allowed variance in Vcross for any particular system. See Figure 2-2.
8. Defined as the maximum instantaneous voltage including overshoot. See Figure 2-2.
9. Defined as the minimum instantaneous voltage including undershoot. See Figure 2-2.
10. T_{Stable} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100 mV range. See Figure 2-5.

Figure 2-2. Single-ended Maximum and Minimum Levels and V_{cross} Levels

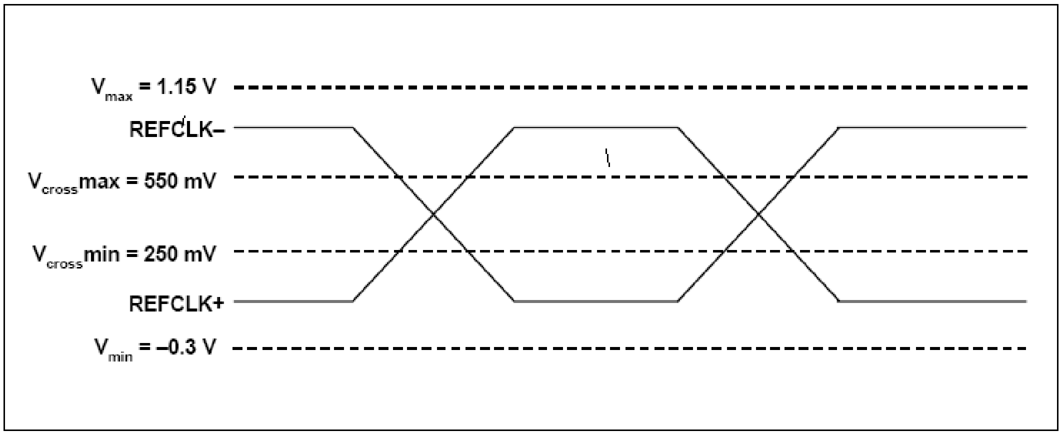


Figure 2-3. $V_{cross\text{-}delta}$ Definition

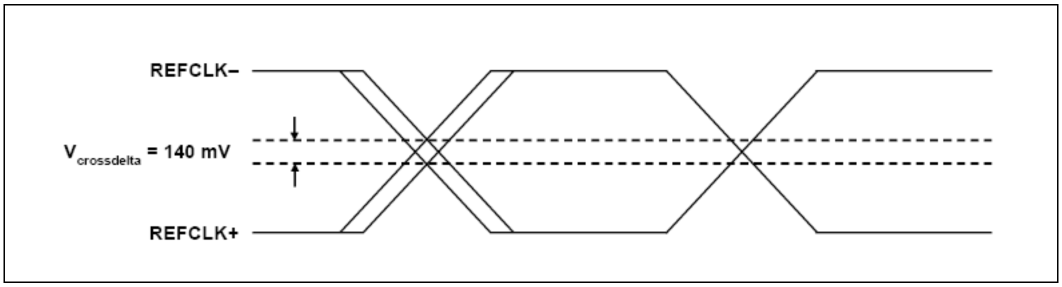


Figure 2-4. Differential Edge Rate Definition

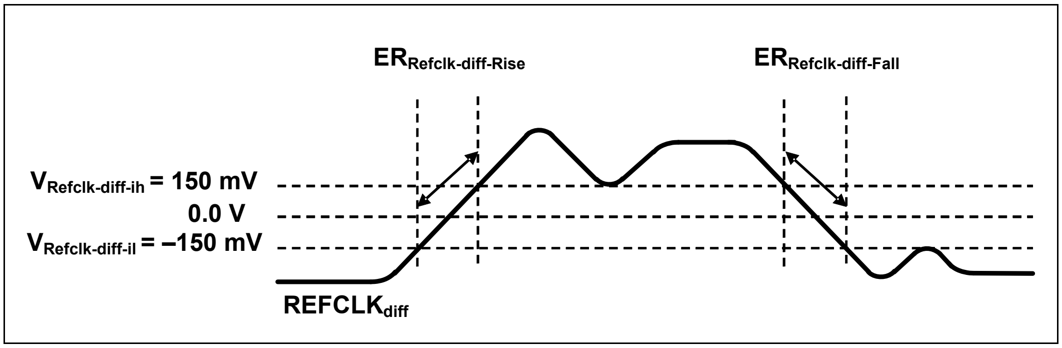
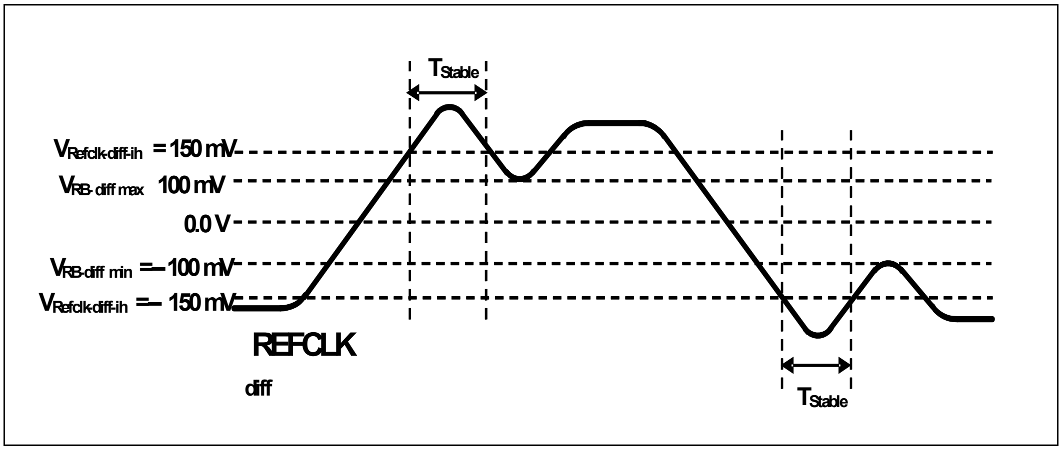


Figure 2-5. V_{RB} and T_{Stable} Definitions



2.4 Intel® QuickPath Interconnect and Intel® SMI Signaling Specifications

2.4.1 Intel® Itanium® Processor 9300 Series Intel® QuickPath Interconnect and Intel® SMI Specifications for 4.8 GT/s

The applicability of this section applies to Intel® QPI for the Intel® Itanium® Processor 9300 Series. This section contains information for Intel® QPI slow boot up speed (1/4 frequency of the reference clock) and processor's normal operating frequency, 4.8 GT/s, for Intel® QPI and Intel® SMI.

For Intel® QPI slow boot up speed, the signaling rate is defined as 1/4 the rate of the system reference clock. For example, a 133 MHz system reference clock would have a forwarded clock frequency of 33.33 MHz and the signaling rate would be 66.67 MT/s.

The transfer rates available for the processor are shown in Table 2-4. Transmitter and receiver parameters for Intel® QPI slow mode, Intel® QPI and Intel® SMI are shown in Table 2-5 and Table 2-6 respectively.

Table 2-4. Intel® Itanium® Processor 9300 Series Clock Frequency Table

Intel® QuickPath Interconnect Forwarded Clock Frequency	Intel® QuickPath Interconnect Data Transfer Rate
33.33 MHz	66.66 MT/s (see note 1)
2.40 GHz	4.8 GT/s

Notes:

1. This speed is the 1/4 SysClk Frequency.

Table 2-5. Intel® Itanium® Processor 9300 Series Transmitter Parameter Values for Intel® QuickPath Interconnect and Intel SMI Channels @ 4.8 GT/s (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Notes
UI_{avg}	Average UI size at 4.8 GT/s		208.33		ps	
$N_{MIN\text{-}UI\text{-}Validation}$	# of UI over which the eye mask voltage and timing spec needs to be validated	1E6				
$T_{slew\text{-}rise\text{-}fall\text{-}pin}$	Defined as the slope of the rising or falling waveform as measured between ±100 mV of the differential transmitter output, data or clock	6		12	V/ns	
$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	Transmitter differential swing	900		1300	mV	
R_{TX}	Transmitter termination resistance	37.4		47.6	Ω	4
$Z_{TX\_LINK\_DETECT}$	Link Detection Resistor	500		2000	Ω	
$V_{TX\_LINK\_DETECT}$	Link Detection Resistor Pull-up Voltage			max VCCIO	V	
$T_{DATA\_TERM\_SKEW}$ Intel® QPI	Skew between first to last data termination meeting $Z_{RX\_LOW\_CM\_DC}$	600			UI	2
$T_{DATA\_TERM\_SKEW}$ Intel® SMI	Skew between first to last data termination meeting $Z_{RX\_LOW\_CM\_DC}$	780			UI	2
$T_{INBAND\_RESET\_SENSE}$	Time taken by inband reset detector to sense Inband Reset	8k		256k	UI	
T_{CLK_DET}	Time taken by clock detector to observe clock stability	8k		256k	UI	
$T_{SYSCLK\text{-}Tx\text{-}VARIABILITY}$	Phase variability between reference Clk (at Tx input) and Tx output.			500	ps	
$TX_{EQ\text{-}BOOST}$	Voltage ratio between the cursor and the post-cursor when transmitting successive ones	0		25	dB	3
$V_{Tx\text{-}CM\text{-}PIN}$	Transmitter data or clock common mode level	23		27	%	
$V_{Tx\text{-}CM\text{-}RIPPLE\text{-}PIN}$	Transmitter data or clock common mode ripple	0		14	%	8,9

Table 2-5. Intel® Itanium® Processor 9300 Series Transmitter Parameter Values for Intel® QuickPath Interconnect and Intel SMI Channels @ 4.8 GT/s (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Notes
$TX_{DUTY\text{-}CYCLE\text{-}PIN}$	Transmitter clock or data duty cycle at the pin. Transmit duty cycle at the pin, defined as UI to UI jitter as specified by the Intel® QPI Electrical Specification, Rev 1.0.	-0.076		0.076	UI-UI	6
$T_{TX\text{-}DATA\text{-}CLK\text{-}SKEW\text{-}PIN}$	Delay of any data lane relative to clock lane, as measured at Tx output	-0.5		0.5	UI	1,2
$TX_{ACC\text{-}JIT\text{-}N\_UI\text{-}1E\text{-}9}$	Peak-to-peak accumulated jitter out of any TX data or clock over 0<= n <= N UI where N=12, measured with 1E-9 probability.	0		0.18	UI	5
$TX_{JITUI\text{-}UI\text{-}1E\text{-}9PIN}$	Transmitter clock or data UI-UI jitter at 1E-9 probability.	0		0.17	UI	5
$RL_{TX\text{-}DIFF}$	Transmitter Differential return loss from 50MHz to 2GHz	-10		dB		7
$RL_{TX\text{-}DIFF}$	Transmitter Differential return loss from 2GHz to 4GHz	-6		dB		7

Notes:
1. Parameter value at full Intel® QPI Refclk.
2. Stagger offset = 0xF.
3. See Figure 2-6.
4. The termination small signal resistance; tolerance over the entire signalling voltage range shall not exceed ±5 ohms.
5. Requires Matlab script.
6. Refer to Intel® QuickPath Interconnect (Intel® QPI) - Electrical Specifications for calculation of this value. Note that UI to UI. definition is used herein, where the value of UI-UI DCD = 2*UI DCD.
7. See Figure 2-7.
8. Applies to Vtx-diff-pp-pin.
9. Peak-to-peak value of the ripple.

Table 2-6. Intel® Itanium® Processor 9300 Series Receiver Parameter Values for Intel® QuickPath Interconnect and Intel® SMI Channels @ 4.8 GT (Sheet 1 of 2)

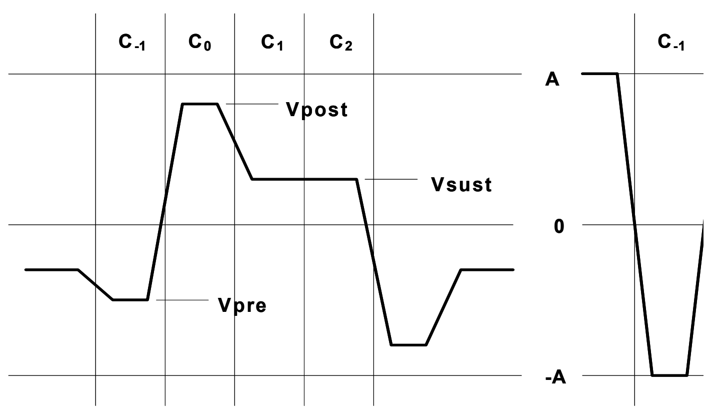
Symbol	Parameter	Min	Nom	Max	Units	Notes
R_{RX}	RX termination resistance	37.4		47.6	Ω	3
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	-0.5		3.5	UI	2
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	0.48		0.52	UI	1
$RL_{RX\text{-}DIFF}$	Receiver differential return loss from 50 MHz to 2 GHz	-10		dB		6
$RL_{RX\text{-}DIFF}$	Receiver differential return loss from 2GHz to 4GHz	-6		dB		6
$V_{Rx\text{-}data\text{-}cm\text{-}pin}$	Receiver data common mode level	125		350	mV	2
$V_{Rx\text{-}data\text{-}cm\text{-}ripple\text{-}pin}$	Receiver data common mode ripple	0		100	$mV_{p\text{-}p}$	
$V_{Rx\text{-}clk\text{-}cm\text{-}pin}$	Receiver clock common mode level	175		350	mV	
$V_{Rx\text{-}clk\text{-}cm\text{-}ripple\text{-}pin}$	Receiver clock common mode ripple	0		100	$mV_{p\text{-}p}$	
$V_{RX\text{-}eye\text{-}data\text{-}pin}$	Minimum eye height at pin for data	200			mV	4
$V_{RX\text{-}eye\text{-}clk\text{-}pin}$	Minimum eye height at pin for clk	225			mV	5

Table 2-6. Intel® Itanium® Processor 9300 Series Receiver Parameter Values for Intel® QuickPath Interconnect and Intel® SMI Channels @ 4.8 GT (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Notes
$T_{RX\text{-}eye\text{-}pin}$	Minimum eye width at pin for clk and data	0.6			UI	4
QPI BER_{Lane}	Bit Error Rate per lane valid for 4.8 and 6.4 GT/s			1.0E-14	Events	
SMI BER_{Lane}	Bit Error Rate per lane valid for 4.8 and 6.4 GT/s			1.0E-12	Events	

Notes:
1. Parameter value at 1/4 Intel® QPI Refclk.
2. Parameter value at full Intel® QPI Refclk.
3. The termination small signal resistance; tolerance over the entire signalling voltage range shall not exceed ±5 ohms with regard to the average of the values measured in the high output voltage state and the low output voltage state for that pin.
4. HVM guaranteed error free value for stressed PRBS signaling across PVT. Link BER is the dominant spec of which eye dimensions are only one factor, and improving another factor could compensate for eye height or width.
5. HVM guaranteed error free value for stressed ‘1010 signaling across PVT. Link BER is the dominant spec of which eye dimensions are only one factor, and improving another factor could compensate for eye height or width.
6. See Figure 2-8.

Figure 2-6. TX Equalization Diagram



Vpre = $A(C_{-1} - C_0 - C_1 - C_2)$

Vpost = $A(C_{-1} + C_0 - C_1 - C_2)$

Vsust = $A(C_{-1} + C_0 + C_1 + C_2)$

C_0 = 1 – sum of abs value of other coeficents

Vpost - Vpre – Vsust = $|C_{-1}| + |C_0| + |C_1| + |C_2| = 1$

%Peaking = Vpost/Vsust

Example: A=500mV, C_{-1}= -0.035, C_0= 0.685, C_1= -0.28, C_2= 0

Vpre = 0.500(-0.035 – 0.685 + 0.28) = 0.5(-0.44) = -220mV

Vpost = 0.500(-0.035 + 0.685 + 0.28) = 0.5(0.93) = 465mV

Vsust = 0.500(-0.035 + 0.685 – 0.28) = 0.5(0.37) = 185mV

TXEQ-BOOST = 20log(Vpost/Vsust) = 20log(465/185) = 8dB

Peaking = 465/185 = 251%

Figure 2-7. TX Return Loss

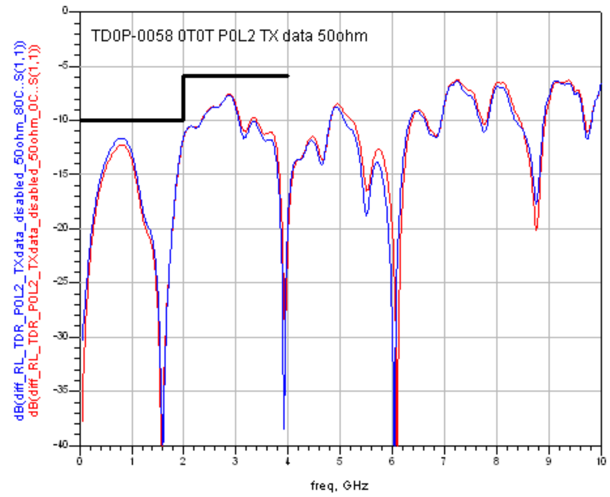
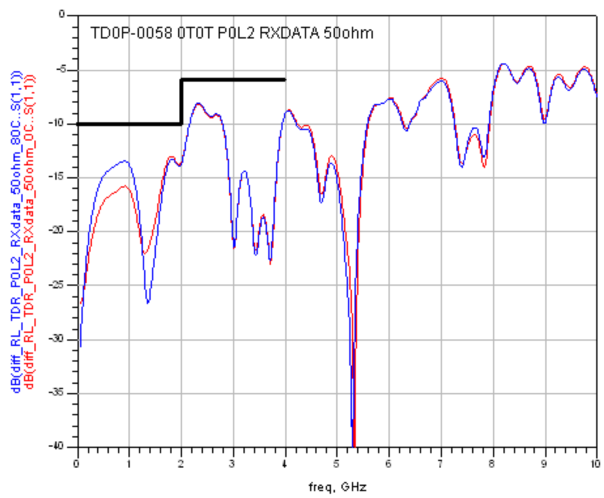


Figure 2-8. RX Return Loss



2.4.2 Intel® Itanium® Processor 9500 Series Requirements for Intel® QuickPath Interconnect for 4.8 and 6.4 GT/s

The applicability of this section applies to Intel® Itanium® Processor 9500 Series. This section contains information for slow boot up speed (1/4 frequency of the reference clock), 4.8 GT/s, and 6.4 GT/s, for Intel® QPI and Intel® SMI.

For Intel® QPI slow boot up speed, the signaling rate is defined as 1/4 the rate of the system reference clock. For example, a 133 MHz system reference clock would have a forwarded clock frequency of 33.33 MHz and the signaling rate would be 66.67 MT/s.

The transfer rates available for the processor are shown in Table 2-7. Transmitter and receiver parameters for Intel® QPI slow mode, Intel® QPI and Intel® SMI are shown in Table 2-8 and Table 2-9 respectively.

Table 2-7. Intel® Itanium® Processor 9500 Series Clock Frequency Table

Intel® QuickPath Interconnect Forwarded Clock Frequency	Intel® QuickPath Interconnect Data Transfer Rate
33.33 MHz	66.66 MT/s (see note 1)
2.40 GHz	4.8 GT/s
3.2 GHz	6.4 GT/s

Notes:
1. This speed is the 1/4 SysClk Frequency.

The applicability of this section applies to Intel® QPI for the Intel® Itanium® Processor 9500 Series. This section contains information for slow boot up speed (1/4 frequency of the reference clock), 4.8 GT/s, and 6.4 GT/s.

Specifications for link speed independent specifications are called out in Table 2-8.

Electrical specifications for Transmit and Receive for 4.8 GT/s are captured in Table 2-9 and for 6.4 GT/s are captured in Table 2-10.

Table 2-8. Intel® Itanium® Processor 9500 Series Link Speed Independent Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
UIavg	Average UI size at “G” GT/s (Where G = 4.8, 6.4, and so on)	0.999 * nominal	1000/G	1.001 * nominal	psec	
$T_{slew-rise-fall-pin}$	Defined as the slope of the rising or falling waveform as measured between ±100mV of the differential transmitter output, for any data or clock	9		20	V/nsec	
$\Delta Z_{TX\_LOW\_CM\_DC}$	Defined as: $(max(Z_{TX\_LOW\_CM\_DC}) - min(Z_{TX\_LOW\_CM\_DC})) / Z_{TX\_LOW\_CM\_DC}$ expressed in %, over full range of Tx single ended voltage	-6		6	% of $Z_{TX\_LOW\_CM\_DC}$	
$\Delta Z_{RX\_LOW\_CM\_DC}$	Defined as: $(max(Z_{TX\_LOW\_CM\_DC}) - min(Z_{TX\_LOW\_CM\_DC})) / Z_{TX\_LOW\_CM\_DC}$ expressed in %, over full range of Tx single ended voltage	-6	0	6	% of $Z_{TX\_LOW\_CM\_DC}$	
$N_{MIN-UI-Validation}$	# of UI over which the eye mask voltage and timing spec needs to be validated	1,000,000				
$Z_{TX\_HIGH\_CM\_DC}$	Single ended DC impedance to GND for either D+ or D- of any data bit at Tx	4k			Ω	
$Z_{RX\_HIGH\_CM\_DC}$	Single ended DC impedance to GND for either D+ or D- of any data bit at Rx	4k			Ω	1

Table 2-8. Intel® Itanium® Processor 9500 Series Link Speed Independent Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$Z_{TX\_LINK\_DETECT}$	Link Detection Resistor	500		2000	Ω	
$V_{TX\_LINK\_DETECT}$	Link Detection Resistor Pull-up Voltage			max VCCIO	V	
$T_{DATA\_TERM\_SKEW}$	Skew between first to last data termination meeting $Z_{RX\_LOW\_CM\_DC}$			128	UI	
$T_{INBAND\_RESET\_SENSE}$	Time taken by inband reset detector to sense Inband Reset			1.5	µs	
$Tclk_{\_DET}$	Time taken by clock detector to observe clock stability			20K	UI	
$T_{CLK\_FREQ\_DET}$	Time taken by clock frequency detector to decide slow vs. operational clock after stable clock			32	Reference Clock Cycles	
$T_{Refclk-Tx-Variability}$	Phase variability between reference Clk (at Tx input) and Tx output.			500	psec	
$T_{Refclk-Rx-Variability}$	Phase variability between reference Clk (at Rx input) and Rx output.	1000			psec	
$L_{D+/D-RX-Skew}$	Phase skew between D+ and D- lines for any data bit at Rx			0.03	UI	
BER_{Lane}	Bit Error Rate per lane valid for 4.8 and 6.4 GT/s			1.0E-14	Events	

Notes:

1. Used during initialization. It is the state of “OFF” condition for the receiver when only the minimum termination is connected.

Table 2-9. Intel® Itanium® Processor 9500 Series Transmitter and Receiver Parameter Values for Intel® QPI Channel at 4.8 GT/s (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$V_{Tx-diff-pp-pin}$	Transmitter differential swing	900		1400	mV	1
$Z_{TX\_LOW\_CM\_DC}$	DC resistance of Tx terminations at half the single ended swing (which is usually 0.25*$V_{Tx-diff-pp-pin}$) bias point	37.4		50	Ω	
$Z_{RX\_LOW\_CM\_DC}$	DC resistance of Rx terminations at half the single ended swing (which is usually 0.25*$V_{Tx-diff-pp-pin}$) bias point	37.4		50	Ω	
$V_{Tx-cm-dc-pin}$	Transmitter output DC common mode, defined as average of V_{D+} and V_{D-}	0.23		0.27	Fraction of $V_{Tx-diff-pp-pin}$	
$V_{Tx-cm-ac-pin}$	Transmitter output AC common mode, defined as ((V_{D+} + V_{D-})/2 - $V_{Tx-cm-dc-pin}$)	-0.0375		0.0375	Fraction of $V_{Tx-diff-pp-pin}$	2
$TX_{duty-pin}$	Average of UI-UI jitter	-0.055		0.055	UI	
$TX_{jitUI-UI-1E-7-pin}$	UI-UI jitter measured at Tx output pins with 1E-7 probability	-0.075		0.075	UI	
$TX_{jitUI-UI-1E-9-pin}$	UI-UI jitter measured at Tx output pins with 1E-9 probability.	-0.085		0.085	UI	

Table 2-9. Intel® Itanium® Processor 9500 Series Transmitter and Receiver Parameter Values for Intel® QPI Channel at 4.8 GT/s (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$TX_{clk-acc-jit-N\_UI-1E-7}$	p-p accumulated jitter out of transmitter over 0 <= n <= N UI where N=12, measured with 1E-7 probability.	0		0.15	UI	
$TX_{clk-acc-jit-N\_UI-1E-9}$	p-p accumulated jitter out of transmitter over 0 <= n <= N UI where N=12, measured with 1E-9 probability.	0		0.17	UI	
$T_{Tx-data-clk-skew-pin}$	Delay of any data lane relative to clock lane, as measured at Tx output	-0.5		0.5	UI	
$V_{Rx-diff-pp-pin}$	Voltage eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI).	225		1200	mV	
$T_{Rx-diff-pp-pin}$	Timing eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI)	0.63		1	UI	
$T_{Rx-data-clk-skew-pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	-1		3	UI	
V_{Rx-CLK}	Forward CLK Rx input voltage sensitivity (differential pp)			180	mV	
$V_{Rx-cm-dc-pin}$	DC common mode ranges at the Rx input for any data or clock channel	125		350	mV	
$V_{Rx-cm-ac-pin}$	AC common mode ranges at the Rx input for any data or clock channel, defined as: $((V_{D+} + V_{D-}/2 - V_{RX-cm-dc-pin})$	-50		50	mV	2

Notes:
1. 1300 mVpp swing is recommended when CPU to CPU or CPU to IOH length is within 2" of PDG max trace length. Note that default value is 1100 mVpp.
2. Measure AC CM noise at the TX and decimate to its spectral components. For all spectral components above 3.2 GHz, apply the attenuation of the channel at the appropriate frequency. If the resultant AC CM at the receiver is met after taking out the appropriate spectral components meets the RX AC CM spec then we can allow the transmitter AC CM noise to pass.

Table 2-10. Intel® Itanium® Processor 9500 Series Transmitter and Receiver Parameter Values for Intel® QPI at 6.4 GT/s (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$V_{Tx-diff-pp-pin}$	Transmitter differential swing	900		1400	mV	1
$Z_{TX\_LOW\_CM\_DC}$	DC resistance of Tx terminations at half the single ended swing (which is usually $0.25*V_{Tx-diff-pp-pin}$) bias point	37.4		50	Ω	
$Z_{RX\_LOW\_CM\_DC}$	DC resistance of Rx terminations at half the single ended swing (which is usually $0.25*V_{Tx-diff-pp-pin}$) bias point	37.4		50	Ω	
$V_{Tx-cm-dc-pin}$	Transmitter output DC common mode, defined as average of V_{D+} and V_{D-}	0.23		0.27	Fraction of $V_{Tx-diff-pp-pin}$	4

Table 2-10. Intel® Itanium® Processor 9500 Series Transmitter and Receiver Parameter Values for Intel® QPI at 6.4 GT/s (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$V_{Tx\text{-}cm\text{-}ac\text{-}pin}$	Transmitter output AC common mode, defined as $((V_{D+} + V_{D-})/2 - V_{Tx\text{-}cm\text{-}dc\text{-}pin})$	-0.0375		0.0375	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	2
$TX_{duty\text{-}pin}$	Average of absolute UI-UI jitter	-0.06		0.06	UI	
$TX_{jitUI\text{-}UI\text{-}1E\text{-}7\text{-}pin}$	UI-UI jitter measured at Tx output pins with 1E-7 probability.	-0.085		0.085	UI	3
$TX_{jitUI\text{-}UI\text{-}1E\text{-}9\text{-}pin}$	UI-UI jitter measured at Tx output pins with 1E-9 probability.	-0.09		0.09	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}7}$	p-p accumulated jitter out of transmitter over 0 <= n <= N UI where N=12, measured with 1E-7 probability.	0		0.15	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}9}$	p-p accumulated jitter out of transmitter over 0 <= n <= N UI where N=12, measured with 1E-9 probability.	0		0.17	UI	
$T_{Tx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to clock lane, as measured at Tx output	-0.5		0.5	UI	
$V_{Rx\text{-}diff\text{-}pp\text{-}pin}$	Voltage eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI).	155		1400	mV	2, 5
$T_{Rx\text{-}diff\text{-}pp\text{-}pin}$	Timing eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI)	0.61		1	UI	
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	-1		4	UI	
$V_{Rx\text{-}CLK}$	Forward CLK Rx input voltage sensitivity (differential pp)			150	mV	
$V_{Rx\text{-}cm\text{-}dc\text{-}pin}$	DC common mode ranges at the Rx input for any data or clock channel	90		350	mV	
$V_{Rx\text{-}cm\text{-}ac\text{-}pin}$	AC common mode ranges at the Rx input for any data or clock channel, defined as: $((V_{D+} + V_{D-}/2 - V_{RX\text{-}cm\text{-}dc\text{-}pin})$	-50		50	mV	

Notes:
1. 1300 mVpp swing is recommended when CPU to CPU or CPU to IOH length is within 2” of PDG max trace length. Note that default value is 1200 mVpp.
2. Measure AC CM noise at the TX and decimate to its spectral components. For all spectral components above 3.2 GHz, apply the attenuation of the channel at the appropriate frequency. If the resultant AC CM at the receiver is met after taking out the appropriate spectral components meets the RX AC CM spec then we can allow the transmitter AC CM noise to pass.
3. Measured with neighboring lines being quiet and the remaining lines toggling PRBS patterns.
4. DC CM can be relaxed to 0.20 and 0.30 Vdiffp-p swing if RX has wide DC common mode range.
5. Based on transmitting a PRBS pattern.

2.4.3 Intel® Itanium® Processor 9500 Series Processor Requirements for Intel® SMI Specifications for 6.4 GT/s

This section defines the high-speed differential point-to-point signaling link for Intel® SMI for the Intel® Itanium® Processor 9500 Series. The link consists of a transmitter and a receiver and the interconnect between them. The specifications described in this section covers 6.4 Gb/s operation. The parameters for Intel® SMI at 6.4 GT/s and lower are captured in Table 2-11 and the PLL specification for transmit and receive are captured in Table 2-12.

Table 2-11. Intel® Itanium® Processor 9500 Series Transmitter and Receiver Parameter Values for Intel® SMI at 6.4 GT/s and lower (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	Transmitter differential swing	800		1200	mV	
$Z_{TX\_LOW\_CM\_DC}$	DC resistance of Tx terminations at half the single ended swing (which is usually 0.25*$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	37.4		50	Ω	
$Z_{RX\_LOW\_CM\_DC}$	DC resistance of Rx terminations at half the single ended swing (which is usually 0.25*$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	37.4		50	Ω	
$V_{Tx\text{-}diff\text{-}pp\text{-}CLK\text{-}pin}$	Transmitter differential swing using a CLK like pattern	0.9*min(VTx-diff-pp-pin)		max(VTxdiff -pp-pin)	mV	1
$V_{Tx\text{-}cm\text{-}dc\text{-}pin}$	Transmitter output DC common mode, defined as average of V_{D+} and V_{D-}	0.23		0.27	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	3
$V_{Tx\text{-}cm\text{-}ac\text{-}pin}$	Transmitter output AC common mode, defined as ((V_{D+} + V_{D-})/2 - $V_{Tx\text{-}cm\text{-}dc\text{-}pin}$)	-0.0375		0.0375	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	
$TX_{duty\text{-}UI\text{-}pin}$	This is computed as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.	0		0.018	UI	
TX1UI-Rj-NoXtalk-pin	Rj value of 1-UI jitter. With X-talk off, but on-die system like noise present. This extraction is to be done after software correction of DCD	0		0.008	UI	2
TX1UI-Dj-NoXtalk--pin	pp Dj value of 1-UI jitter. With X-talk off, but on-die system like noise present.	-0.01		0.01	UI	2
TXN-UI-Rj-NoXtalkpin	Rj value of N-UI jitter. With X-talk off, but on-die system like noise present. Here 1 < N < 9.This extraction is to be done after software correction of DCD	0		0.012	UI	2
TXN-UI-Dj-NoXtalkpin	pp Dj value of N-UI jitter. With X-talk off, but on-die system like noise present. Here 1 < N < 9.Dj here indicated Djdd of dual-dirac fitting, after software correction of DCD	-0.04	0.04	0.2	UI	2
$T_{Tx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to clock lane, as measured at Tx output	-0.5		0.5	UI	
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	-1		3.5	UI	
$V_{Rx\text{-}CLK}$	Forward CLK Rx input voltage sensitivity (differential pp)			150	mV	

Table 2-11. Intel® Itanium® Processor 9500 Series Transmitter and Receiver Parameter Values for Intel® SMI at 6.4 GT/s and lower (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
VRx-Vmargin	Any data lane Rx input voltage (differential pp) measured at BER=1E-9			100	mV	
TRx-Tmargin	Timing width for any data lane using repetitive patterns and clean forwarded CLK, measured at BER=1E-9	0.8			UI	
$V_{Rx\text{-}cm\text{-}dc\text{-}pin}$	DC common mode ranges at the Rx input for any data or clock channel, defined as average of VD+ and VD-.	125		350	mV	
$V_{Rx\text{-}cm\text{-}ac\text{-}pin}$	AC common mode ranges at the Rx input for any data or clock channel, defined as: $((V_{D+} + V_{D-}/2 - V_{RX\text{-}cm\text{-}dc\text{-}pin})$	-50		50	mV	

Notes:

1. This is the swing specification for the forwarded CLK output. Note that this specification will also have to be suitably de-embedded for package/PCB loss to translate the value to the pad, since there is a significant variation between traces in a setup.
2. While the X-talk is off, on-die noise similar to that occurring with all the transmitter and receiver lanes toggling will still need to be present. When a socket is not present in the transmitter measurement setup, in many cases the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. Therefore for all Tx measurements, use of a socket should be avoided. The contribution of cross-talk may be significant and should be done using the same setup at Tx and compared against the expectations of full link signaling. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be ran to determine link feasibility.
3. DC CM can be relaxed to 0.20 and 0.30 Vdiffp-p swing if RX has wide DC common mode range.

Table 2-12. PLL Specification for TX and RX

Symbol	Parameter	Min	Max	Units	Notes
$F_{PLL\text{-}BW\_TX\text{-}RX}$	-3dB bandwidth	4	16	MHz	
$JitPk_{TX\text{-}RX}$	Jitter Peaking		3	dB	

2.5 Processor Absolute Maximum Ratings

Table 2-13 specifies absolute maximum and minimum ratings for the Intel® Itanium® Processor 9300 Series. Within operational maximum and minimum limits, the processor functionality and long-term reliability can be expected. The processor maximum ratings listed in Table 2-13 are applicable for the 130 W, 155 W, and 185 W parts.

Table 2-14 specifies absolute maximum and minimum ratings for the Intel® Itanium® Processor 9500 Series. Within operational maximum and minimum limits, the processor functionality and long-term reliability can be expected. The processor maximum ratings listed in Table 2-14 are applicable for the 130 W and 170 W parts.

At conditions outside operational maximum ratings, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within operational maximum and minimum ratings after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

2.5.1 Intel® Itanium® Processor 9300 Series Absolute Maximum Ratings

Table 2-13. Intel® Itanium® Processor 9300 Series Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{CCCORE}	Processor core supply voltage with respect to VSS	–0.3	1.55	V	1,2
$V_{CCUNCORE}$	Processor uncore supply voltage with respect to VSS	–0.3	1.55	V	1,2
V_{CCA}	Processor Analog Supply Voltage with respect to VSS	–0.3	1.89	V	1,2
V_{CCIO}	Processor I/O Supply Voltage with respect to VSS	–0.3	1.55	V	1,2
V_{CC33_SM}	Processor 3.3 V Supply Voltage with respect to VSS	-0.3	3.465	V	1,2

Notes:
1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Section 2.6.3. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.

2.5.2 Intel® Itanium® Processor 9500 Series Absolute Maximum Ratings

Table 2-14. Intel® Itanium® Processor 9500 Series Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{CCCORE}	Processor core supply voltage with respect to VSS	-0.3	1.42	V	1,2
$V_{CCUNCORE}$	Processor uncore supply voltage with respect to VSS	-0.3	1.42	V	1,2
V_{CCA}	Processor Analog Supply Voltage with respect to VSS	-0.3	1.89	V	1,2
V_{CCIO}	Processor I/O Supply Voltage with respect to VSS	-0.3	1.55	V	1,2
V_{CC33_SM}	Processor 3.3 V Supply Voltage with respect to VSS	-0.3	3.465	V	1,2

Notes:
1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Section 2.6.4. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.

2.6 Processor DC Specifications

Table 2-15 through Table 2-35 list the DC specifications for the Intel® Itanium® Processor 9300 Series and 9500 Series and are valid only while meeting specifications for case temperature, clock frequency, and input voltages.

The following notes apply:

- Unless otherwise noted, all specifications in the tables apply to all frequencies
- For the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series, these specifications are based on characterized data from silicon measurements.

2.6.1 Flexible Motherboard Guidelines for the Intel® Itanium® Processor 9300 Series

The Flexible Motherboard (FMB) guidelines are estimates of the maximum ratings that the processor will have over certain time periods. The ratings are only estimates as actual specifications for future processors may differ. The processor may or may not have specifications equal to the FMB value in the foreseeable future.

Table 2-15 defines the FMB voltage specification values applied to the 130W, and 155W/185W Intel® Itanium® Processor 9300 Series stock-keeping units (SKUs). Current specifications are identified for each processor SKU separately in Table 2-16 through Table 2-17.

Table 2-18 defines the FMB voltage specification values applied to the 130 W and 170 W SKUs for the Intel® Itanium® Processor 9500 Series. Current specifications are identified for each processor SKU separately in Table 2-19.

Table 2-15. FMB Voltage Specifications for the Intel® Itanium® Processor 9300 Series

Symbol	Parameter	Min	Typ	Max	Units	Notes
VID_{Range}	VCCCORE VID Range	0.8	1.1	1.35	V	
$UVID_{Range}$	VCCUNCORE VID Range	0.8	1.1	1.35	V	
VCCUNCORE	Processor uncore supply voltage	See Table 2-20 and Figure 2-10			V	2,1
VCCCORE	Processor core supply voltage	See Table 2-21 and Figure 2-11			V	2,3,4
VCCCACHE	Processor cache supply voltage	See Table 2-22 and Figure 2-12			V	5
VID Transition	VID step size during transition		± 12.5		mV	
VID_DCshift	Total allowable DC load line shift from VID steps.			-450	mV	6
VCCIO	Processor I/O supply voltage at die including all AC and DC	1.08	1.15	1.22	V	7
VCCIO	Processor I/O supply voltage (high frequency AC p-p noise at die)	0		50	mV	
VCCIO	Processor I/O supply voltage at package pin including all AC and DC	1.147	1.175	1.203	V	8
VCCA	Processor analog supply voltage (DC spec)	1.764	1.8	1.836	V	
VCCA	Processor analog supply voltage (AC tolerance for noise at scope full bandwidth)		1.8	±25	mV	9, 10
VCCA	Processor analog supply voltage (AC tolerance for noise > 1MHz)		1.8	±15	mV	9, 11
VCCA	Processor analog supply voltage (Total = DC spec + AC tolerance)	1.739	1.8	1.861	V	
VCC33_SM	3.3 V supply voltage	3.135	3.3	3.465	V	

Notes:

1. The voltage specification requirements are measured across the VCCUNCORESENSE and VSSUNCORESENSE pins using an oscilloscope set to a 100 MHz bandwidth and probes that are 1.5 pF maximum capacitance and 1 mOhms minimum impedance at the processor socket. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the scope probe.

2. These voltages are target only. A variable voltage source should exist on systems in the event that a different voltage is required. See Ararat Voltage Regulator Module Design Guide for more information.
3. Uncore, Core, and Cache voltage and Current Rating are at the Package Pad.
4. The voltage specification requirements are measured across the VCCCORESENSE and VSSCORESENSE pins using an oscilloscope set to a 100 MHz bandwidth and probes that are 1.5 pF maximum capacitance and 1 MOhm minimum impedance at the processor socket. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the scope probe.
5. The voltage specification requirements are measured across the VCCCACHESENSE and VSSCACHESENSE pins using an oscilloscope set to a 100 MHz bandwidth and probes that are 1.5 pF maximum capacitance and 1 mOhms minimum impedance at the processor socket. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the scope probe.
6. Warm boot reset, only in downward direction.
7. Min and Max range is spec at the die for both VCCIO. This range includes 50 mV p-p AC noise. It also includes any DC and AC tolerances at package pin.
8. The FMB remote sense tolerance is ±2.5% for DC to 20 MHz at the package, where ±1.5% is allotted for a DC to 1 MHz range and an additional ±1% for 1 MHz to 20 MHz. Similarly, ±6.4% is allotted for DC to 20 MHz at the die. It is expected that VCCIO regulators meet ±1.5% at the remote sense location based on the general remote sense termination point location as described in Figure 2-16, VR Sense Point (Representation). For future processor compatibility, it is strongly recommended that the platform query the PIROM to assure VCCIO is set to the appropriate level prior to powering up the VCCIO supply.
9. All voltage regulation measurements taken at remote sense termination points.
10. For peak-to-peak Ripple and Noise (R&N) measured with full bandwidth (BW) of the scope (Min 1 GHz BW scope is required): set scope diff probe and the scope at full BW (capture waveform A, channel 1).
11. For peak-to-peak Ripple and Noise (R&N) measured above 1 MHz:
 Step 1 = set both: scope diff probe and/or the scope at 1 MHz BW limit (capture waveform B, channel 2).
 Step 2 = calculate A-B (use scope Math function: subtract channel 1 - channel 2).

Table 2-16. FMB 130W Current Specifications for the Intel® Itanium® Processor 9300 Series

Symbol	Parameter	Max	Units	Notes
I_{CC_CORE}	I_{CC} for core	151	A	
$I_{CC\_CORE\_TDC}$	Thermal Design Current for Core	100	A	1
$I_{CC\_CORE\_STEP}$	Max Load step for core	95	A	2
$d_{ICC\_CORE/dt}$	Slew rate for core at Ararat output	154	A/us	
I_{CC_UNCORE}	ICC for uncore	50	A	
$I_{CC\_UNCORE\_TDC}$	Thermal Design Current for Uncore	43	A	3
$I_{CC\_UNCORE\_STEP}$	Max Load step for uncore	22	A	4
$dI_{CC\_UNCORE/dt}$	Slew rate for uncore at Ararat output	75	A/us	
I_{CC_IO}	ICC for processor I/O	22	A	5
I_{CC_Analog}	ICC for processor Analog	4	A	
I_{CC33_SM}	ICC33 for main supply	200	mA	

Notes:

1. ICC_CORE_TDC is the sustained (DC equivalent) current that the processor core is capable of drawing indefinitely and should be used for the Ararat voltage regulator temperature assessment. The Ararat voltage regulator is responsible for monitoring its temperature and asserting the VR_FAN_N, VR_THERMALERT_N, VR_THERMTRIP_N signals sequentially to inform the processor and platform of a thermal excursion. Of the three signals, only VR_THERMALTERT_N is monitored by the processor. Please see the Ararat Voltage Regulator Module Design Guide for further details. The processor is capable of drawing ICC_CORE_TDC indefinitely. Refer to Figure 2-9 for further details on the average processor current draw over various time durations. This parameter is based on design characterization and is not tested.
2. During system power on, the pulse inrush (ICC_CORE_STEP) can be as high as 130A peak-to-peak.
3. ICC_UNCORE_TDC is the sustained (DC equivalent) current that the processor uncore is capable of drawing indefinitely and should be used for the Ararat voltage regulator temperature assessment. The Ararat voltage regulator is responsible for monitoring its temperature and asserting the VR_FAN_N, VR_THERMALERT_N, VR_THERMTRIP_N signals sequentially to inform the processor and platform of a thermal excursion. Of the three signals, only VR_THERMALTERT_N is monitored by the processor. Please see the Ararat Voltage Regulator Module Design Guide for further details. The processor is capable of drawing ICC_UNCORE_TDC indefinitely. This parameter is based on design characterization and is not tested.
4. During system power on, the pulse inrush (ICC_UNCORE_STEP) can be as high as 40A peak-to-peak.
5. The ICC_IO current specification applies to the total current from VCCIO pins.

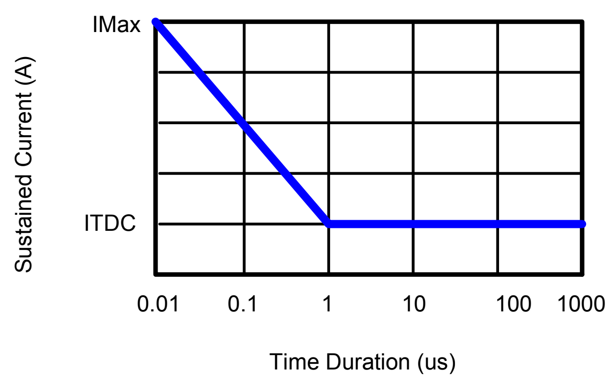
Table 2-17. FMB 155W/185W Current Specifications for the Intel® Itanium® Processor 9300 Series

Symbol	Parameter	Max	Units	Notes
I_{CC_CORE}	I_{CC} for core	180	A	
$I_{CC\_CORE\_TDC}$	Thermal Design Current for Core	131	A	1
$I_{CC\_CORE\_STEP}$	Max Load step for core	95	A	2
$d_{ICC\_CORE/dt}$	Slew rate for core at Ararat output	154	A/us	
I_{CC_UNCORE}	I_{CC} for uncore	50	A	
$I_{CC\_UNCORE\_TDC}$	Thermal Design Current for Uncore	43	A	3
$I_{CC\_UNCORE\_STEP}$	Max Load step for uncore	22	A	4
$dI_{CC\_UNCORE/dt}$	Slew rate for uncore at Ararat output	75	A/us	
I_{CC_IO}	I_{CC} for processor I/O	22	A	5
I_{CC_Analog}	I_{CC} for processor Analog	4	A	
I_{CC33_SM}	I_{CC33} for main supply	200	mA	

Notes:

1. ICC_CORE_TDC is the sustained (DC equivalent) current that the processor core is capable of drawing indefinitely and should be used for the Ararat voltage regulator temperature assessment. The Ararat voltage regulator is responsible for monitoring its temperature and asserting the VR_FAN_N, VR_THERMALERT_N, VR_THERMTRIP_N signals sequentially to inform the processor and platform of a thermal excursion. Of the three signals, only VR_THERMALTERT_N is monitored by the processor. Please see the Ararat Voltage Regulator Module Design Guide for further details. The processor is capable of drawing ICC_CORE_TDC indefinitely. Refer to Figure 2-9 for further details on the average processor current draw over various time durations. This parameter is based on design characterization and is not tested.
2. During system power on, the pulse inrush (ICC_CORE_STEP) can be as high as 130A peak-to-peak.
3. ICC_UNCORE_TDC is the sustained (DC equivalent) current that the processor uncore is capable of drawing indefinitely and should be used for the Ararat voltage regulator temperature assessment. The Ararat voltage regulator is responsible for monitoring its temperature and asserting the VR_FAN_N, VR_THERMALERT_N, VR_THERMTRIP_N signals sequentially to inform the processor and platform of a thermal excursion. Of the three signals, only VR_THERMALTERT_N is monitored by the processor. Please see the Ararat Voltage Regulator Module Design Guide for further details. The processor is capable of drawing ICC_UNCORE_TDC indefinitely. This parameter is based on design characterization and is not tested.
4. During system power on, the pulse inrush (ICC_UNCORE_STEP) can be as high as 40A peak-to-peak.
5. The ICC_IO current specification applies to the total current from VCCIO pins.

Figure 2-9. Processor I_{CC_CORE} Load Current versus Time



2.6.2 Flexible Motherboard Guidelines for the Intel® Itanium® Processor 9500 Series

The Flexible Motherboard (FMB) guidelines are estimates of the maximum ratings that the processor will have over certain time periods. The ratings are only estimates as actual specifications for future processors may differ. The processor may or may not have specifications equal to the FMB value in the foreseeable future.

Table 2-18 defines the FMB voltage specification values applied to the 130 W and 170 W SKUs for the Intel® Itanium® Processor 9500 Series. Current specifications are identified for each processor SKU separately in Table 2-19.

Table 2-18. FMB Voltage Specifications for the Intel® Itanium® Processor 9500 Series

Symbol	Parameter	Min	Typ	Max	Units	Notes
$CVID_{Range}$	VCCCORE VID Range	0.800	1.105	1.22	V	1
$CVID_{Boot}$	VCCCORE VID default value		0		V	1
$UVID_{Range}$	VCCUNCORE VID Range	0.800	0.975	1.19	V	1
$UVID_{Boot}$	VCCUNCORE VID default value		1.0		V	1
VCCUNCORE	Processor uncore supply voltage	See Table 2-23 and Figure 2-15			V	2, 1
VCCCORE	Processor core supply voltage	See Table 2-24 and Figure 2-14			V	2, 3, 4
VID Transition	VID step size during transition		± 5		mV	
VID_DCshift	Total allowable DC load line shift from VID steps.			-420	mV	5
VCCIO	Processor I/O supply voltage at die including all AC and DC	1.011	1.050	1.094	V	6
VCCIO	Processor I/O supply voltage (high frequency AC p-p noise at die)			35	mV	
VCCIO	Processor I/O supply voltage at package pin including all AC and DC	1.026	1.075	1.088	V	7
VCCA	Processor analog supply voltage (DC spec)	1.764	1.8	1.836	V	8
VCCA	Processor analog supply voltage (AC tolerance for noise at scope full bandwidth)		1.8	±25	mV	8, 9
VCCA	Processor analog supply voltage (AC tolerance for noise > 1MHz)		1.8	±15	mV	9, 10
VCCA	Processor analog supply voltage (Total = DC spec + AC tolerance)	1.739	1.8	1.861	V	
VCCA Ramp	Min time allowed to ramp VCCA from 10% to 90% typical value	1		10	ms	
VCC33_SM	3.3 V supply voltage	3.135	3.3	3.465	V	

Notes:
1. The voltage specification requirements are measured across the VCCUNCORESENSE and VSSUNCORESENSE pins using an oscilloscope set to a 100 MHz bandwidth and probes that are 1.5 pF maximum capacitance and 1 mOhms minimum impedance at the processor socket. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the scope probe.
2. These voltages are target only. A variable voltage source should exist on systems in th e event that a different voltage is required. See the Ararat II Voltage Regulator Module Design Guide for more information.
3. Uncore and Core voltage and Current Rating are at the Package Pad.
4. The voltage specification requirements are measured across the VCCCORESENSE and VSSCORESENSE pins using an oscilloscope set to a 100 MHz bandwidth and probes that are 1.5 pF maximum capacitance and 1 mOhms minimum impedance at the processor socket. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the scope probe.
5. Warm boot reset, only in downward direction.
6. Min and Max range is spec at the die for VCCIO. This range includes 35 mV p-p AC noise. It also includes any DC and AC tolerances at package pin.

7. The FMB remote sense tolerance is ±2.5% for DC to 20 MHz at the package, where ±1.5% is allotted for a DC to 1 MHz range and an additional ±1.0% for 1 MHz to 20 MHz. Similarly, ±6.4% is allotted for DC to 20 MHz at the die. It is expected that VCCIO regulators meet ±1.5% at the remote sense location based on the general remote sense termination point location as described in Figure 2-16 VR Sense Point (Representation). For future processor compatibility, it is strongly recommended that the platform query the PIROM to assure VCCIO is set to the appropriate level prior to powering up the VCCIO supply.
8. All voltage regulation measurements taken at remote sense termination points.
9. For peak-to-peak Ripple and Noise (R&N) measured with full bandwidth (BW) of the scope (Min 1 GHz BW scope is required): set scope diff probe and the scope at full BW (capture waveform A, channel 1).
10. For peak-to-peak Ripple and Noise (R&N) measured above 1 MHz:
 Step 1 = set both: scope diff probe and/or the scope at 1 MHz BW limit (capture waveform B, channel 2)
 Step 2 = calculate A-B (use scope Math function: subtract channel 1 - channel 2).

Table 2-19. FMB 170W and 130W Current Specifications for the Intel® Itanium® Processor 9500 Series

Symbol	Parameter	Max	Min	Units	Notes
I_{CC_CORE}	I_{CC} for core	35.0		A	1
$I_{CC\_CORE\_TDC}$	Thermal Design Current for Core	30.0		A	1, 2
$I_{CC\_CORE\_STEP}$	Max Load step for core	14.62		A	1, 3
$d_{ICC\_CORE/dt}$	Slew rate for core at Ararat output	34.4		A/us	1
I_{CC_UNCORE}	I_{CC} for uncore	80.0		A	
$I_{CC\_UNCORE\_TDC}$	Thermal Design Current for Uncore	75.0		A	4
$I_{CC\_UNCORE\_STEP}$	Max Load step for uncore	30.4		A	5
$dI_{CC\_UNCORE/dt}$	Slew rate for uncore at Ararat output	168.0		A/us	
I_{CC_IO}	I_{CC} for processor I/O	17.2		A	6
$d_{ICC\_IO/dt}$	Slew rate for IO at the package pin	54.0		A/us	
$I_{CC\_IO\_STEP}$	Max Load step for max slew rate	5.1		A	7
$T_{CC\_IO\_STEP}$	Time between steps		4.7	us	7
I_{CC_Analog}	I_{CC} for processor Analog	4		A	
I_{CC33_SM}	I_{CC33} for main supply	200		mA	

Notes:
1. Values per core pair.
2. ICC_CORE_TDC is the sustained (DC equivalent) current that the processor core is capable of drawing indefinitely and should be used for the Ararat voltage regulator temperature assessment. The Ararat voltage regulator is responsible for monitoring its temperature and asserting the VR_FAN_N, VR_THERMALERT_N, VR_THERMTRIP_N signals sequentially to inform the processor and platform of a thermal excursion. Of the three signals, only VR_THERMALTERT_N is monitored by the processor. Please see the Ararat II Voltage Regulator Module Design Guide for further details. The processor is capable of drawing ICC_CORE_TDC indefinitely.
3. During system power on, the pulse inrush (ICC_CORE_STEP) can be as high as 35A peak-to-peak.
4. ICC_UNCORE_TDC is the sustained (DC equivalent) current that the processor uncore is capable of drawing indefinitely and should be used for the Ararat voltage regulator temperature assessment. The Ararat voltage regulator is responsible for monitoring its temperature and asserting the VR_FAN_N, VR_THERMALERT_N, VR_THERMTRIP_N signals sequentially to inform the processor and platform of a thermal excursion. Of the three signals, only VR_THERMALTERT_N is monitored by the processor. Please see the Ararat II Voltage Regulator Module Design Guide for further details. The processor is capable of drawing ICC_UNCORE_TDC indefinitely. This parameter is based on design characterization and is not tested.
5. During system power on, the pulse inrush (ICC_UNCORE_STEP) can be as high as 40A peak-to-peak.
6. The ICC_IO current specification applies to the total current from VCCIO pins.
7. The max load step represents the maximum current required during Intel® QPI and Intel® SMI port initialization. The min time between steps represents the time between Intel® QPI and Intel® SMI initialization.

2.6.3 Intel® Itanium® Processor 9300 Series Uncore, Core, and Cache Tolerances

2.6.3.1 Uncore Static and Transient Tolerances

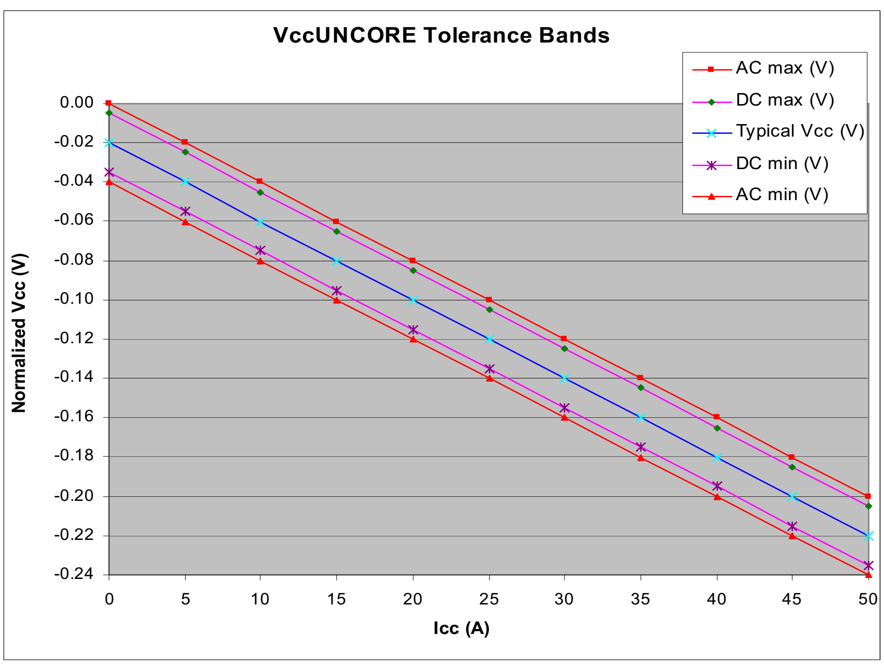
Table 2-20 and Figure 2-10 specify static and transient tolerances for the uncore outputs.

Table 2-20. $V_{CCUNCORE}$ Static and Transient Tolerance for Intel® Itanium® Processor 9300 Series

Uncore Current (A)	Voltage Deviation from VID Setting (V)1,2,3,4		
I_{CC_UNCORE}	V_{CC_Max}	V_{CC_Typ}	V_{CC_Min}
0	VID - 0	VID - 0.02	VID - 0.04
5	VID - 0.02	VID - 0.04	VID - 0.06
10	VID - 0.04	VID - 0.06	VID - 0.08
15	VID - 0.06	VID - 0.08	VID - 0.1
20	VID - 0.08	VID - 0.1	VID - 0.12
25	VID - 0.1	VID - 0.12	VID - 0.14
30	VID - 0.12	VID - 0.14	VID - 0.16
35	VID - 0.14	VID - 0.16	VID - 0.18
40	VID - 0.16	VID - 0.18	VID - 0.2
45	VID - 0.18	VID - 0.2	VID - 0.22
50	VID - 0.2	VID - 0.22	VID - 0.24

Notes:
1. The V_{CC_MIN} and V_{CC_MAX} load lines represent static and transient limits.
2. This table is intended to aid in reading discrete points on Figure 2-10.
3. The load lines specify voltage limits at the die measured at the $V_{CCUNCORESENSE}$ and $V_{SSUNCORESENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins. Refer to the Ararat Voltage Regulator Module Design Guide for socket load line guidelines and VR implementation.
4. V_{DC}(max)=VID-R_{ll}*I_{CC}-5 mV; V_{DC}(min)=VID-R_{ll}*I_{CC}-35mV; R_{ll}=4 mW.

Figure 2-10. $V_{CCUNCORE}$ Static and Transient Tolerance for Intel® Itanium® Processor 9300 Series



2.6.3.2 Core Static and Transient Tolerances

Table 2-21 and Figure 2-11 specify static and transient tolerances for the core outputs.

Table 2-21. V_{CCCORE} Static and Transient Tolerance for Intel® Itanium® Processor 9300 Series (Sheet 1 of 2)

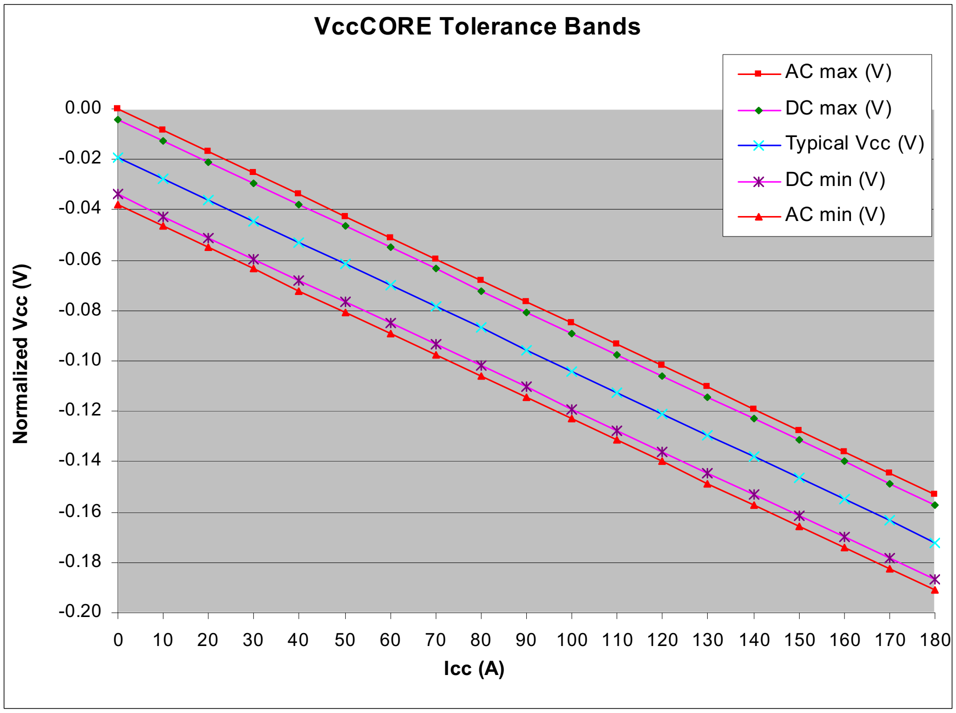
Core Current (A)	Voltage Deviation from VID Setting (V)1,2,3,4		
I_{CC_CORE}	V_{CC_Max}	V_{CC_Typ}	V_{CC_Min}
0	VID - 0	VID - 0.02	VID - 0.04
5	VID - 0.004	VID - 0.024	VID - 0.044
10	VID - 0.009	VID - 0.029	VID - 0.049
15	VID - 0.013	VID - 0.033	VID - 0.053
20	VID - 0.017	VID - 0.037	VID - 0.057
25	VID - 0.021	VID - 0.041	VID - 0.061
30	VID - 0.026	VID - 0.046	VID - 0.066
35	VID - 0.03	VID - 0.05	VID - 0.07
40	VID - 0.034	VID - 0.054	VID - 0.074
45	VID - 0.038	VID - 0.058	VID - 0.078
50	VID - 0.043	VID - 0.063	VID - 0.083
55	VID - 0.047	VID - 0.067	VID - 0.087
60	VID - 0.051	VID - 0.071	VID - 0.091
65	VID - 0.055	VID - 0.075	VID - 0.095
70	VID - 0.06	VID - 0.08	VID - 0.1
75	VID - 0.064	VID - 0.084	VID - 0.104
80	VID - 0.068	VID - 0.088	VID - 0.108
85	VID - 0.072	VID - 0.092	VID - 0.112
90	VID - 0.077	VID - 0.097	VID - 0.117
95	VID - 0.081	VID - 0.101	VID - 0.121
100	VID - 0.085	VID - 0.105	VID - 0.125
105	VID - 0.089	VID - 0.109	VID - 0.129
110	VID - 0.094	VID - 0.114	VID - 0.134
115	VID - 0.098	VID - 0.118	VID - 0.138
120	VID - 0.102	VID - 0.122	VID - 0.142
125	VID - 0.106	VID - 0.126	VID - 0.146
130	VID - 0.111	VID - 0.131	VID - 0.151
135	VID - 0.115	VID - 0.135	VID - 0.155
140	VID - 0.119	VID - 0.139	VID - 0.159
145	VID - 0.123	VID - 0.143	VID - 0.163
150	VID - 0.128	VID - 0.148	VID - 0.168
155	VID - 0.132	VID - 0.152	VID - 0.172
160	VID - 0.136	VID - 0.156	VID - 0.176
165	VID - 0.14	VID - 0.16	VID - 0.18

Table 2-21. V_{CCCORE} Static and Transient Tolerance for Intel® Itanium® Processor 9300 Series (Sheet 2 of 2)

Core Current (A)	Voltage Deviation from VID Setting (V)1,2,3,4		
I_{CC_CORE}	V_{CC_Max}	V_{CC_Typ}	V_{CC_Min}
170	VID - 0.145	VID - 0.165	VID - 0.185
175	VID - 0.149	VID - 0.169	VID - 0.189
180			

Notes:
1. The V_{CC_MIN} and V_{CC_MAX} load lines represent static and transient limits.
2. This table is intended to aid in reading discrete points on Figure 2-11.
3. The load lines specify voltage limits at the die measured at the $V_{CCCORESENSE}$ and $V_{SSCORESENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins. Refer to the Ararat Voltage Regulator Module Design Guide for socket load line guidelines and VR implementation.
4. $V_{DC}(max)=VID-R_{ll}*I_{CC}-4$ mV; $V_{DC}(nom)=VID-R_{ll}*I_{CC}-19$ mV; $V_{DC}(min)=VID-R_{ll}*I_{CC}-34$mV; $R_{ll}=0.85$ mΩ.

Figure 2-11. V_{CCCORE} Static and Transient Tolerance for Intel® Itanium® Processor 9300 Series



2.6.3.3 Cache Static and Transient Tolerances

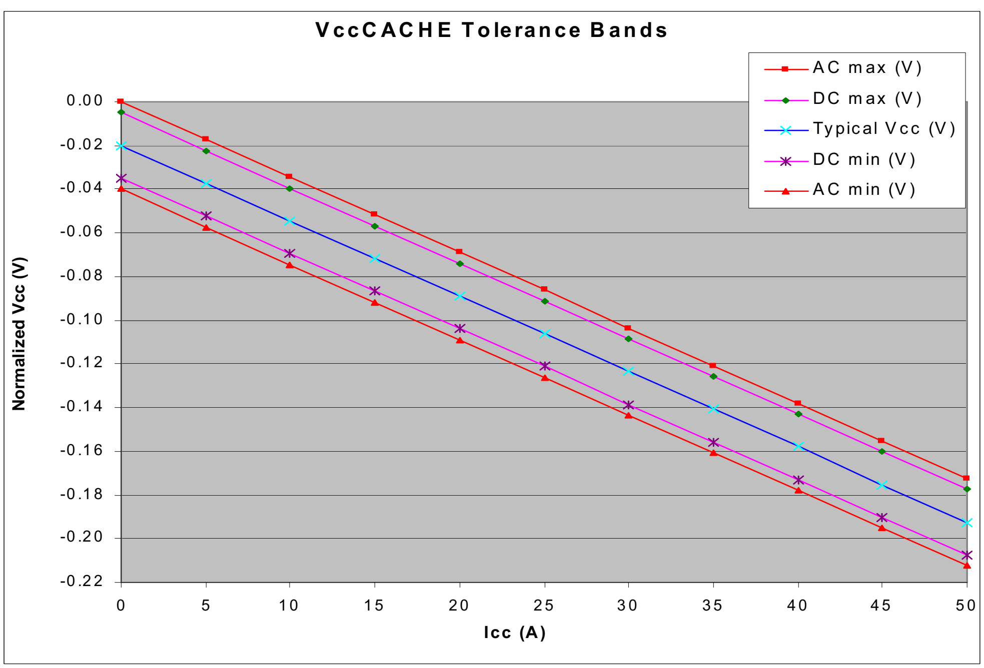
Table 2-22 and Figure 2-12 specify static and transient tolerances for the cache outputs.

Table 2-22. $V_{CCCACHE}$ Static and Transient Tolerance for Intel® Itanium® Processor 9300 Series

Cache Current (A)	Voltage Deviation from VID Setting (V)1,2,3,4		
I_{CC_CACHE}	V_{CC_Max}	V_{CC_Typ}	V_{CC_Min}
0	VID - 0	VID - 0.02	VID - 0.04
5	VID - 0.017	VID - 0.037	VID - 0.057
10	VID - 0.035	VID - 0.055	VID - 0.075
15	VID - 0.052	VID - 0.072	VID - 0.092
20	VID - 0.069	VID - 0.089	VID - 0.109
25	VID - 0l.086	VID - 0.106	VID - 0.126
30	VID - 0.104	VID - 0.124	VID - 0.144
35	VID - 0.121	VID - 0.141	VID - 0.161
40	VID - 0.138	VID - 0.158	VID - 0.178
45	VID - 0.155	VID - 0.175	VID - 0.195
50	VID - 0.173	VID - 0.193	VID - 0.213
55	VID - 0.19	VID - 0.21	VID - 0.23

Notes:
1. The V_{CC_MIN} and V_{CC_MAX} load lines represent static and transient limits.
2. This table is intended to aid in reading discrete points on Figure 2-12.
3. The load lines specify voltage limits at the die measured at the $V_{CCCACHESENSE}$ and $V_{SSCACHESENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins. Refer to the Ararat Voltage Regulator Module Design Guide for socket load line guidelines and VR implementation.
4. $V_{DC}(max)$=VID-R_{ll}*I_{CC}-5 mV; $V_{DC}(min)$=VID-R_{ll}*I_{CC}-35 mV; R_{ll}=3.45 mW.

Figure 2-12. $V_{CCCACHE}$ Static and Transient Tolerance for Intel® Itanium® Processor 9300 Series



2.6.4 Intel® Itanium® Processor 9500 Series Uncore and Core Tolerances

2.6.4.1 Uncore Static and Transient Tolerances

Table 2-23 and Figure 2-13 specify static and transient tolerances for the uncore outputs.

Table 2-23. $V_{CCUNCORE}$ Static and Transient Tolerance for the Intel® Itanium® Processor 9500 Series

Uncore Current (A)	Voltage Deviation from VID Setting (V)1,2,3,4		
I_{CC_UNCORE}	V_{CC_Max}	V_{CC_Typ}	V_{CC_Min}
0	VID + 0.015	VID	VID - 0.015
5	VID + 0.00875	VID - 0.00625	VID - 0.02125
10	VID + 0.0025	VID - 0.0125	VID - 0.0275
15	VID - 0.00375	VID - 0.01875	VID - 0.03375
20	VID - 0.01	VID - 0.025	VID - 0.04
25	VID - 0.01625	VID - 0.03125	VID - 0.04625
30	VID - 0.0225	VID - 0.0375	VID - 0.0525
35	VID - 0.02875	VID - 0.04375	VID - 0.05875
40	VID - 0.035	VID - 0.05	VID - 0.065
45	VID - 0.04125	VID - 0.05625	VID - 0.07125
50	VID - 0.0475	VID - 0.0625	VID - 0.0775
55	VID - 0.05375	VID - 0.06875	VID - 0.08375
60	VID - 0.06	VID - 0.075	VID - 0.09
65	VID - 0.06625	VID - 0.08125	VID - 0.09625
70	VID - 0.0725	VID - 0.0875	VID - 0.1025

Notes:
1. The V_{CC_MIN} and V_{CC_MAX} load lines represent static and transient limits.
2. This table is intended to aid in reading discrete points on Figure 2-14.
3. The load lines specify voltage limits at the die measured at the VCCUNCORESENSE and VSSUNCORESENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS pins. Refer to the Ararat II Voltage Regulator Module Design Guide for socket load line guidelines and VR implementation.
4. $V_{DC}(max)$=VID-R_{ll}*I_{CC}+15 mV; $V_{DC}(min)$=VID-R_{ll}*I_{CC}-15 mV; R_{ll}=1.25 mOhm.

Figure 2-13. $V_{CCUNCORE}$ Static and Transient Tolerance for the Intel® Itanium® Processor 9500 Series

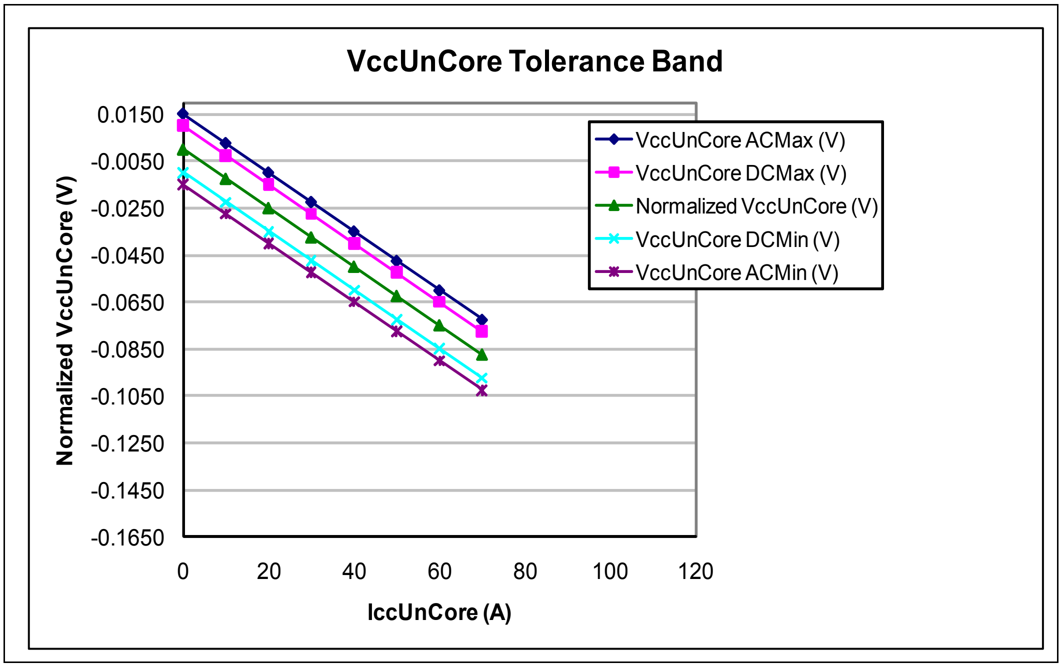
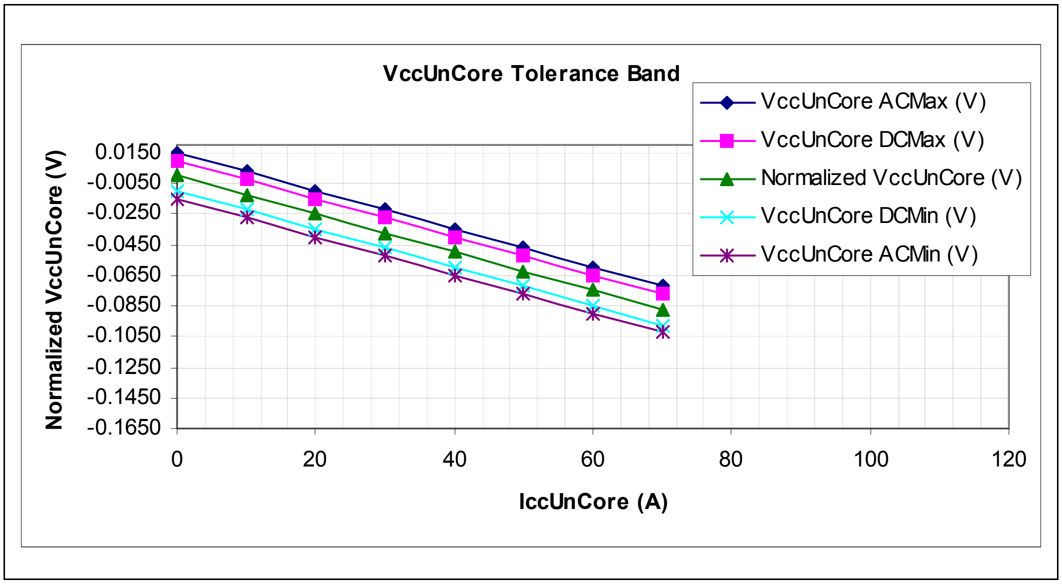


Figure 2-14. $V_{CCUNCORE}$ Load Line for the Intel® Itanium® Processor 9500 Series



2.6.4.2 Core Static and Transient Tolerances

Table 2-24 and Figure 2-15 specify static and transient tolerances for the core outputs.

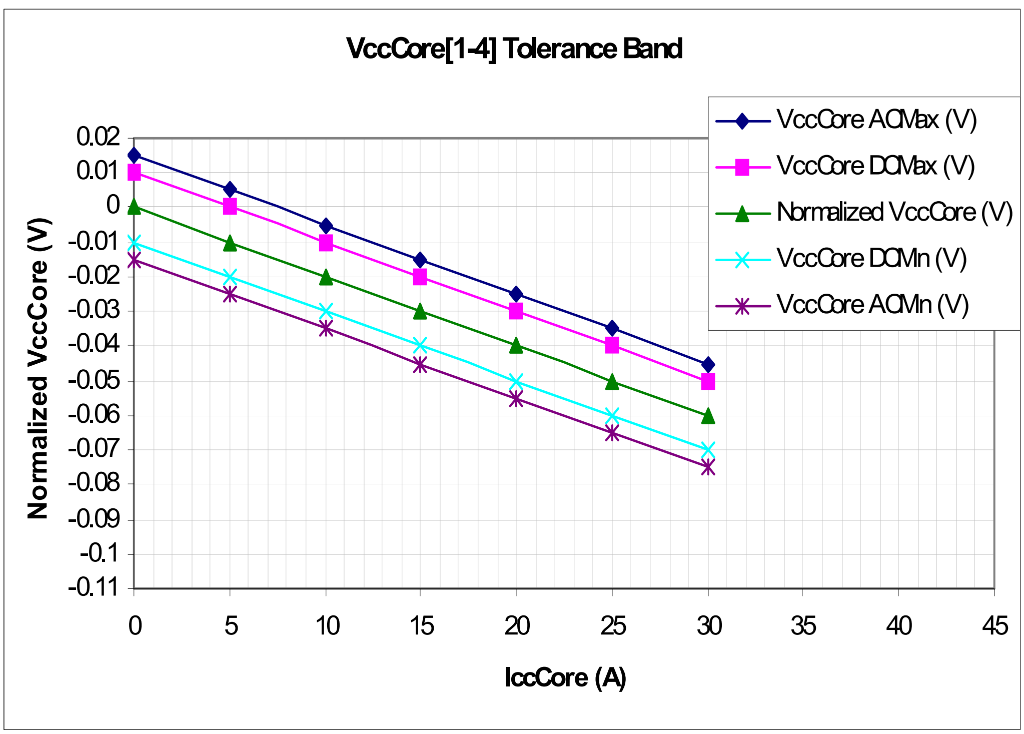
Table 2-24. V_{CCCORE} Static and Transient Tolerance for the Intel® Itanium® Processor 9500 Series

Core Current (A)	Voltage Deviation from VID Setting (V)1,2,3,4		
I_{CC_CORE}	V_{CC_Max}	V_{CC_Typ}	V_{CC_Min}
0	VID + 0.015	VID	VID - 0.015
5	VID + 0.005	VID - 0.010	VID - 0.025
10	VID - 0.005	VID - 0.020	VID - 0.035
15	VID - 0.015	VID - 0.030	VID - 0.045
20	VID - 0.025	VID - 0.040	VID - 0.055
25	VID - 0.035	VID - 0.050	VID - 0.065
30	VID - 0.045	VID - 0.060	VID - 0.075

Notes:

1. The V_{CC_MIN} and V_{CC_MAX} load lines represent static and transient limits.
2. This table is intended to aid in reading discrete points on Figure 2-15.
3. The load lines specify voltage limits at the die measured at the VCCCORESENSE and VSSCORESENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS pins. Refer to the Ararat II Voltage Regulator Module Design Guide for socket load line guidelines and VR implementation.
4. V_{DC}(max)=VID-R_{ll}*I_{CC}+15 mV; V_{DC}(nom)=VID-R_{ll}*I_{CC}; V_{DC}(min)=VID-R_{ll}*I_{CC}-15 mV; R_{ll}= 2 mOhms.

Figure 2-15. V_{CCCORE} Load Line for the Intel® Itanium® Processor 9500 Series



2.6.5 Overshoot and Undershoot Guidelines

Overshoot (or undershoot) is the value of the maximum voltage above or below VSS. The overshoot and undershoot specifications limit transitions beyond VCCIO or VSS due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (that is, if the overshoot or undershoot is great enough). Determining the impact of an overshoot or undershoot condition requires knowledge of the magnitude, the pulse duration, and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot or undershoot.

2.6.5.1 Overshoot/Undershoot Magnitude, Pulse Duration and Activity Factor

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series, both are referenced to VSS. It is important to note that overshoot and undershoot conditions are separate and their impact must be determined independently.

Pulse duration describes the total amount of time that an overshoot or undershoot event exceeds the overshoot or undershoot reference voltage. Activity factor (AF) describes the frequency of overshoot or undershoot occurrence relative to a clock. Since the highest frequency of assertion of a single-ended signal is every other clock, an AF = 1 indicates that the specific overshoot or undershoot waveform occurs every other clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot or undershoot waveform occurs one time in every 200 clock cycles. The highest frequency of assertion of any differential signal is every active edge of its associated clock (not the reference clock). So, an AF = 1 indicates that the specific overshoot or undershoot waveform occurs every cycle.

2.6.5.2 Overshoot/Undershoot Specifications

The overshoot and undershoot specifications listed in the following table specify the allowable overshoot or undershoot for a single overshoot or undershoot event. Table 2-25 specifies the maximum overshoot and undershoot for the Intel® Itanium® Processor 9300 Series, while Table 2-26 specifies the maximum overshoot and under-shoot for the Intel® Itanium® Processor 9500 Series, respectively, identifying both the single ended and the differential signalling pins. The overshoot and undershoot values assume an activity factor of 100% and a pulse width of 25% over the signal pulse width. The tables also include the absolute maximum and minimum values beyond which the processor is not guaranteed to operate properly. These values assume a pulse width of 1% and an activity factor of 100%.

2.6.5.2.1 Overshoot and Undershoot Specifications for the Intel® Itanium® Processor 9300 Series

Table 2-25. Overshoot and Undershoot Specifications For Differential Intel® QuickPath Interconnect and Intel® SMI and Single-Ended Signals for the Intel® Itanium® Processor 9300 Series (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit
$V_{MAX\text{-}OS\text{-}SE}$	Overshoot for single-ended signals		1.45	V
$V_{MIN\text{-}US\text{-}SE}$	Undershoot for single-ended signals	-0.247		V
$V_{ABSMAX\text{-}OS\text{-}SE}$	Absolute Max for single-ended signals		1.6	V
$V_{ABSMIN\text{-}US\text{-}SE}$	Absolute Min for single-ended signals	-0.425		V

Table 2-25. Overshoot and Undershoot Specifications For Differential Intel® QuickPath Interconnect and Intel® SMI and Single-Ended Signals for the Intel® Itanium® Processor 9300 Series (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit
$V_{MAX\text{-}OS\text{-}DIFF}$	Overshoot for Intel® QPI and Intel® SMI signals		1.54	V
$V_{MAX\text{-}US\text{-}DIFF}$	Undershoot for Intel® QPI and Intel® SMI signals	-0.337		V
$V_{ABSMAX\text{-}OS\text{-}DIFF}$	Absolute Max for Intel® QPI and Intel® SMI signals		1.7	V
$V_{ABSMAX\text{-}US\text{-}DIFF}$	Absolute Min for Intel® QPI and Intel® SMI signals	-0.525		V
$V_{MAX\_OS\_SYSCLK}$	Sysclk single-ended maximum voltage		1.54	V
$V_{MIN\_US\_SYSCLK}$	Sysclk single-ended minimum voltage	-0.337		V

2.6.5.2.2 Overshoot and Undershoot Specifications for the Intel® Itanium® Processor 9500 Series

Table 2-26. Overshoot and Undershoot Specifications For Differential Intel® QuickPath Interconnect and Intel® SMI and Single-Ended Signals for the Intel® Itanium® Processor 9500 Series

Symbol	Parameter	Min	Max	Unit
$V_{MAX\text{-}OS\text{-}SE}$	Overshoot for single-ended signals		1.36	V
$V_{MIN\text{-}US\text{-}SE}$	Undershoot for single-ended signals	-0.22		V
$V_{ABSMAX\text{-}OS\text{-}SE}$	Absolute Max for single-ended signals		1.46	V
$V_{ABSMIN\text{-}US\text{-}SE}$	Absolute Min for single-ended signals	-0.32		V
$V_{MAX\text{-}OS\text{-}DIFF}$	Overshoot for Intel® QPI and Intel® SMI signals		1.3	V
$V_{MAX\text{-}US\text{-}DIFF}$	Undershoot for Intel® QPI and Intel® SMI signals	-0.3		V
$V_{ABSMAX\text{-}OS\text{-}DIFF}$	Absolute Max for Intel® QPI and Intel® SMI signals		1.4	V
$V_{ABSMAX\text{-}US\text{-}DIFF}$	Absolute Min for Intel® QPI and Intel® SMI signals	-0.4		V
$V_{MAX\_OS\_SYSCLK}$	Sysclk single-ended maximum voltage		1.3	V
$V_{MIN\_US\_SYSCLK}$	Sysclk single-ended minimum voltage	-0.3		V

2.6.6 Signal DC Specifications

Table 2-27 through Table 2-35 state the DC specifications for the single-ended signal groups defined in Table 2-2.

Table 2-27. Voltage Regulator Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0	0.4	V	
V_{IH}	Input High Voltage	0.8	3.6	V	
V_{OH}	Output High Voltage	0.8	3.6	V	1, 2, 3, 4, 5
V_{OL}	Output Low Voltage	0	0.4	V	1, 2, 3, 4, 5

Notes:
1. Open collector and drain outputs need pull-up resistors on the motherboard.

2. These outputs can be pulled up to VCCIO or VCC_STBY on the platform.
3. Pull-up resistance should limit current to 2 mA.
4. Actual V_{OH} and V_{OL} levels are determined by pull-up resistance and supply voltage values.
5. These values are based on 2.2 KΩ pull-up to 3.3 V supply.

Table 2-28. Voltage Regulator Control Group DC Specification

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0	(VCCIO*0.67) - 0.2	V	
V_{IH}	Input High Voltage	(VCCIO*0.67) + 0.2	VCCIO	V	
V_{OH}	Output High Voltage			V	1, 2, 3, 4
V_{OL}	Output Low Voltage			V	1, 2, 3, 4

Notes:

1. Open collector and drain outputs need pull-up resistors on the motherboard.
2. Actual V_{OH} and V_{OL} levels determined by pull-up resistance and supply voltage value. Refer to the Ararat Voltage Regulator Module Design Guide or the Ararat II Voltage Regulator Module Design Guide for I_{OL} max.
3. See *Intel® Itanium® 9300 Series and Intel® Itanium® 9500 Series Platform Design Guide* for recommended resistor values.
4. VR_THERMALERT_N is an input to the top of the package and an output from the bottom of the package. V_{IH} and V_{IL} levels are for the input at the top of the package, sensed by the processor; V_{OH} and V_{OL} are for the output levels on the package pins at the bottom of the package.

Table 2-29. TAP and System Management Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0	(VCCIO*0.5) - 0.2	V	
V_{IH}	Input High Voltage	(VCCIO*0.5) + 0.2	VCCIO	V	
V_{OH}	Output High Voltage	VCCIO-0.2	VCCIO	V	
V_{OL}	Output Low Voltage	0	0.25	V	1
I_{OL}	Output Low Current	16	23	mA	1
I_{ILeak}	Input Leakage Current	–200	200	µA	2, 3, 4
I_{OLeak}	Output Leakage Current	–1000	200	µA	

Notes:

1. With 50 W termination to VCCIO at the far end.
2. With V at the pin at 1.1 V and 0 V. System designers are advised to check the tolerance of their voltage regulator solutions to ensure V at the pin is 1.1 V.
3. Internal weak pull-up included for TCLK.
4. Internal weak pull-up included for TRST_N, TMS and TDI.

Table 2-30. Error, FLASHROM, Power-Up, Setup, and Thermal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0	(VCCIO*0.67) - 0.2	V	
V_{IH}	Input High Voltage	(VCCIO*0.67) + 0.2	VCCIO	V	
V_{OH}	Output High Voltage	VCCIO-0.2	VCCIO	V	
V_{OL}	Output Low Voltage	0	0.25	V	1
I_{OL}	Output Low Current	16	23	mA	1
I_{ILeak}	Input Leakage Current	–1000	200	µA	2
I_{OLeak}	Output Leakage Current	–1000	200	µA	

Notes:

1. With 50W termination to VCCIO at the far end.

2. With input leakage current measured at the pin with 0V and with 1.1 V supplied to the pin. System designers are advised to check the tolerance of their voltage regulator solutions to ensure a voltage of 1.1 V at the pin.

2.6.6.1 VID_VCCCORE, VID_VCCUNCORE, and VID_VCCCACHE DC Specifications for the Intel® Itanium® Processor 9300 Series

The Intel® Itanium® Processor 9300 Series processor supplies top side VID signal pins to the Arafat Voltage Regulator Module, as shown in Table 2-31.

Table 2-31. VID_VCCCORE[6:0], VID_VCCUNCORE[6:0] and VID_VCCCACHE[5:0] DC Specifications for the Intel® Itanium® Processor 9300 Series

Symbol	Parameter	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	VCCIO-0.1	VCCIO	V	1
V_{OL}	Output Low Voltage	0	0.1	V	1
I_{OLeak}	Output Leakage Current	–200	200	µA	1, 2

Notes:
1. These parameters are not tested and are based on design simulations.
2. Leakage to VSS with pin held at 1.1 V and leakage to 1.1 V with pin held at VSS.

2.6.6.2 SVID Group DC Specifications for the Intel® Itanium® Processor 9500 Series

The Intel® Itanium® Processor 9500 Series implements a Serial VID BUS that is used to transfer power management information between the microprocessor and the five output voltages. Voltage levels are compliant to the VR12.0 1V TTL signaling requirements and are shown in Table 2-32.

Table 2-32. SVID Group DC Specifications for the Intel® Itanium® Processor 9500 Series

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0	(VCCIO*0.5) - 0.2	V	
V_{IH}	Input High Voltage	(VCCIO*0.5) + 0.2	VCCIO	V	
V_{OH}	Output High Voltage	VCCIO-0.2	VCCIO	V	
V_{OL}	Output Low Voltage	0	0.25	V	1
I_{OL}	Output Low Current	16	23	mA	1
I_{ILeak}	Input Leakage Current	–200	200	µA	2
I_{OLeak}	Output Leakage Current	–200	200	µA	

Notes:
1. With 50W termination to VCCIO at the far end.
2. With input leakage current measured at the pin with 0V and with 1.075V supplied to the pin. System designers are advised to check the tolerance of their voltage regulator solutions to ensure Vpin of 1.1 V.

Table 2-33. SMBus and Serial Presence Detect (SPD) Bus Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0	(VCCIO*0.67) -0.2	V	1
V_{IH}	Input High Voltage	(VCCIO*0.67) + 0.2	VCCIO	V	1
V_{OL}	Output Low Voltage	0	0.25	V	1
I_{OL}	Output Low Current	16	23	mA	1,2
I_{LEAK}	Input Leakage Current	–1000	200	µA	1
I_{LO}	Output Leakage Current	–1000	200	µA	1

Notes:
1. These parameters are based on design characterization and are not tested.
2. With 50Ω termination to VCCIO at the far end.

Table 2-34. Debug Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0	(VCCIO*0.67) - 0.2	V	
V_{IH}	Input High Voltage	(VCCIO*0.67) + 0.2	VCCIO	V	
V_{OH}	Output High Voltage	VCCIO-0.2	VCCIO	V	
V_{OL}	Output Low Voltage	0	0.35	V	1
I_{OL}	Output Low Current	13	23	mA	1
I_{ILeak}	Input Leakage Current	–1000	200	µA	2
I_{OLeak}	Output Leakage Current	–1000	200	µA	

Notes:
1. With 2 parallel 50Ω termination to VCCIO at the far end.
2. With input leakage current measured at the pin with 0V and with 1.1V supplied to the pin. System designers are advised to check the tolerance of their voltage regulator solutions to ensure Vpin of 1.1 V.

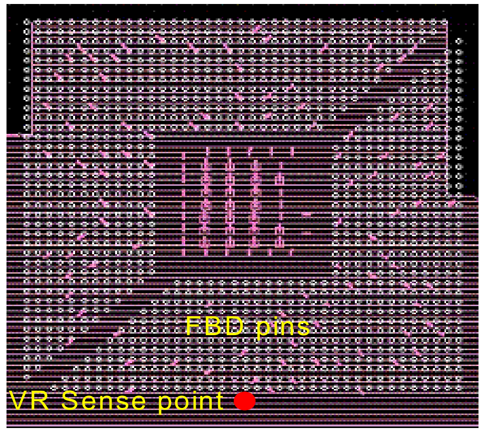
Table 2-35. PIROM Signal Group DC Specifications

Symbol	Parameter	Min	TYP	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.6		Vcc*0.3		2,1
V_{IH}	Input High Voltage	Vcc*0.7		Vcc +0.5		2,1
V_{OL2}	Output Low Voltage (I_{OL} = 2.1 mA)			0.4		2
V_{OL1}	Output Low Voltage (I_{OL} = 0.15 mA)			0.2		2
I_{ILeak}	Input Leakage Current		0.1	3.0		2
I_{OLeak}	Output Leakage Current		0.05	3.0		2

Notes:
1. V_{IL}(min) and V_{IH}(max) are reference only and are not tested.
2. Applicable over recommended operating range T = -40 °C to +88 °C; Vcc = +1.7 V to +3.6 V.

2.6.7 Motherboard-Socket Specification for VR Sense Point

Figure 2-16. VR Sense Point (Representation)



Note: ±1.5% DC (DC to 1 MHz) and ±1% AC (1 MHz to 20 MHz) specified at MB/socket.

2.7 Core and Uncore Voltage Identification

The VID_VCCCORE[6:0] and VID_VCCUNCORE[6:0] lands supply the encoding that determine the voltage to be supplied by the VCCCORE and VCCUNCORE voltage regulators. The VID_VCCCORE and VID_VCCUNCORE specifications for the Intel® Itanium® Processor 9300 Series and 9500 Series are defined in the *Ararat 170 Watt Voltage Regulator Module Design Guide* and *Ararat II Voltage Regulator Module Design Guide*, respectively. The voltage set by the VID_VCCCORE and VID_VCCUNCORE lands are the maximum VCCCORE and VCCUNCORE voltage allowed by the processor.

Individual processor VID_VCCCORE and VID_VCCUNCORE values may be calibrated during manufacturing such that two devices at the same core speed may have different default VID_VCCCORE and VID_VCCUNCORE settings. Furthermore, any Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series can drive different VID_VCCCORE and VID_VCCUNCORE settings during normal operation. Table 2-36 and Table 2-37 specify the voltage levels corresponding to the state of VID_VCCCORE and VID_VCCUNCORE for the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series respectively. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level.

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series provide the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (VCCCORE). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in many VID transitions as necessary to reach the target core voltage. Transitions above the specified VID are not permitted.

The Ararat voltage regulator must be capable of regulating its output to the value defined by the new VID. Please refer to the *Ararat 170 Watt Voltage Regulator Module Design Guide* for the Intel® Itanium® Processor 9300 Series processor or the *Ararat II Voltage Regulator Module Design Guide* for the Intel® Itanium® Processor 9500 Series.

2.7.1 Core and Uncore Voltage Identification for the Intel® Itanium® Processor 9300 Series

Table 2-36. Intel® Itanium® Processor 9300 Series VCCCORE (VID_VCCCORE) and VCCUNCORE and (VID_VCCUNCORE) Voltage Identification Definition for Ararat (Sheet 1 of 2)

Hex	VID6	VID 5	VID 4	VID3	VID 2	VID 1	VID 0	VID (V)		Hex	VID6	VID5	VID4	VID3	VID2	VID1	VI D0	VID (V)
00	0	0	0	0	0	0	0	OFF		2E	0	1	0	1	1	1	0	1.0375
01	0	0	0	0	0	0	1	1.6000		2F	0	1	0	1	1	1	1	1.0250
02	0	0	0	0	0	1	0	1.5875		30	0	1	1	0	0	0	0	1.0125
03	0	0	0	0	0	1	1	1.5750		31	0	1	1	0	0	0	1	1.000
04	0	0	0	0	1	0	0	1.5625		32	0	1	1	0	0	1	0	0.9875
05	0	0	0	0	1	0	1	1.5500		33	0	1	1	0	0	1	1	0.9750
06	0	0	0	0	1	1	0	1.5375		34	0	1	1	0	1	0	0	0.9625
07	0	0	0	0	1	1	1	1.5250		35	0	1	1	0	1	0	1	0.9500
08	0	0	0	1	0	0	0	1.5125		36	0	1	1	0	1	1	0	0.9375
09	0	0	0	1	0	0	1	1.5000		37	0	1	1	0	1	1	1	0.9250
0A	0	0	0	1	0	1	0	1.4875		38	0	1	1	1	0	0	0	0.9125
0B	0	0	0	1	0	1	1	1.4750		39	0	1	1	1	0	0	1	0.9000
0C	0	0	0	1	1	0	0	1.4625		3A	0	1	1	1	0	1	0	0.8875
0D	0	0	0	1	1	0	1	1.4500		3B	0	1	1	1	0	1	1	0.8750
0E	0	0	0	1	1	1	0	1.4375		3C	0	1	1	1	1	0	0	0.8625
0F	0	0	0	1	1	1	1	1.4250		3D	0	1	1	1	1	0	1	0.8500
10	0	0	1	0	0	0	0	1.4125		3E	0	1	1	1	1	1	0	0.8375
11	0	0	1	0	0	0	1	1.4000		3F	0	1	1	1	1	1	1	0.8250
12	0	0	1	0	0	1	0	1.3875		40	1	1	1	0	0	0	0	0.8125
13	0	0	1	0	0	1	1	1.3750		41	1	1	1	0	0	0	1	0.8000
14	0	0	1	0	1	0	0	1.3625		42	1	1	1	0	0	1	0	0.7875
15	0	0	1	0	1	0	1	1.3500		43	1	0	1	0	0	1	1	0.7750
16	0	0	1	0	1	1	0	1.3375		44	1	0	0	0	1	0	0	0.7625
17	0	0	1	0	1	1	1	1.3250		45	1	0	0	0	1	0	1	0.7500
18	0	0	1	1	0	0	0	1.3125		46	1	0	0	0	1	1	0	0.7375
19	0	0	1	1	0	0	1	1.3000		47	1	0	0	0	1	1	1	0.7250
1A	0	0	1	1	0	1	0	1.2870		48	1	0	0	1	0	0	0	0.7125
1B	0	0	1	1	0	1	1	1.2750		49	1	0	0	1	0	0	1	0.7000
1C	0	0	1	1	1	0	0	1.2625		4A	1	0	0	1	0	1	0	0.6875
1D	0	0	1	1	1	0	1	1.2500		4B	1	0	0	1	0	1	1	0.6750
1E	0	0	1	1	1	1	0	1.2375		4C	1	0	0	1	1	0	0	0.6625
1F	0	0	1	1	1	1	1	1.2250		4D	1	0	0	1	1	0	1	0.6500
20	0	1	0	0	0	0	0	1.2125		4E	1	0	0	1	1	1	0	0.6375
21	0	1	0	0	0	0	1	1.2000		4F	1	0	0	1	1	1	1	0.6250
22	0	1	0	0	0	1	0	1.1875		50	1	0	0	0	0	0	0	0.6125
23	0	1	0	0	0	1	1	1.1750		51	1	0	0	0	0	0	1	0.6000
24	0	1	0	0	1	0	0	1.1625		52	1	0	0	0	0	1	0	0.5875

Table 2-36. Intel® Itanium® Processor 9300 Series VCCCORE (VID_VCCCORE) and VCCUNCORE and (VID_VCCUNCORE) Voltage Identification Definition for Ararat (Sheet 2 of 2)

Hex	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VID (V)		Hex	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VID (V)
25	0	1	0	0	1	0	1	1.1500		53	1	0	0	0	0	1	1	0.5750
26	0	1	0	0	1	1	0	1.1375		54	1	0	1	0	1	0	0	0.5625
27	0	1	0	0	1	1	1	1.1250		55	1	0	1	0	1	0	1	0.5500
28	0	1	0	1	0	0	0	1.1125		56	1	0	1	0	1	1	0	0.5375
29	0	1	0	1	0	0	1	1.1000		57	1	0	1	0	1	1	1	0.5250
2A	0	1	0	1	0	1	0	1.0875		58	1	0	1	1	0	0	0	0.5125
2B	0	1	0	1	0	1	1	1.0750		59	1	0	1	1	0	0	1	0.5000
2C	0	1	0	1	1	0	0	1.0625		7F	1	1	1	1	1	1	1	OFF
2D	0	1	0	1	1	0	1	1.0500										

2.7.2 Core and Uncore Voltage Identification for the Intel® Itanium® Processor 9500 Series

Table 2-37. Intel® Itanium® Processor 9500 Series VCCCORE (VID_VCCCORE) and VCCUNCORE and (VID_VCCUNCORE) Voltage Identification Definition for Ararat II (Sheet 1 of 4)

Hex	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VID (V)		Hex	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VID (V)
00	0	0	0	0	0	0	0	0	OFF		27	0	0	1	0	0	1	1	1	0.440
01	0	0	0	0	0	0	0	1	0.250		28	0	0	1	0	1	0	0	0	0.445
02	0	0	0	0	0	0	1	0	0.255		29	0	0	1	0	1	0	0	1	0.450
03	0	0	0	0	0	0	1	1	0.260		2A	0	0	1	0	1	0	1	0	0.455
04	0	0	0	0	0	1	0	0	0.265		2B	0	0	1	0	1	0	1	1	0.460
05	0	0	0	0	0	1	0	1	0.270		2C	0	0	1	0	1	1	0	0	0.465
06	0	0	0	0	0	1	1	0	0.275		2D	0	0	1	0	1	1	0	1	0.470
07	0	0	0	0	0	1	1	1	0.280		2E	0	0	1	0	1	1	1	0	0.475
08	0	0	0	0	1	0	0	0	0.285		2F	0	0	1	0	1	1	1	1	0.480
09	0	0	0	0	1	0	0	1	0.290		30	0	0	1	1	0	0	0	0	0.485
0A	0	0	0	0	1	0	1	0	0.295		31	0	0	1	1	0	0	0	1	0.490
0B	0	0	0	0	1	0	1	1	0.300		32	0	0	1	1	0	0	1	0	0.495
0C	0	0	0	0	1	1	0	0	0.305		33	0	0	1	1	0	0	1	1	0.500
0D	0	0	0	0	1	1	0	1	0.310		34	0	0	1	1	0	1	0	0	0.505
0E	0	0	0	0	1	1	1	0	0.315		35	0	0	1	1	0	1	0	1	0.510
0F	0	0	0	0	1	1	1	1	0.320		36	0	0	1	1	0	1	1	0	0.515
10	0	0	0	1	0	0	0	0	0.325		37	0	0	1	1	0	1	1	1	0.520
11	0	0	0	1	0	0	0	1	0.330		38	0	0	1	1	1	0	0	0	0.525
12	0	0	0	1	0	0	1	0	0.335		39	0	0	1	1	1	0	0	1	0.530
13	0	0	0	1	0	0	1	1	0.340		3A	0	0	1	1	1	0	1	0	0.535
14	0	0	0	1	0	1	0	0	0.345		3B	0	0	1	1	1	0	1	1	0.540
15	0	0	0	1	0	1	0	1	0.350		3C	0	0	1	1	1	1	0	0	0.545

Table 2-37. Intel® Itanium® Processor 9500 Series VCCCORE (VID_VCCCORE) and VCCUNCORE and (VID_VCCUNCORE) Voltage Identification Definition for Ararat II (Sheet 2 of 4)

Hex	VID 7	VID6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	VID (V)		Hex	VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VI D0	VID (V)
16	0	0	0	1	0	1	1	0	0.355		3D	0	0	1	1	1	1	0	1	0.550
17	0	0	0	1	0	1	1	1	0.360		3E	0	0	1	1	1	1	1	0	0.555
18	0	0	0	1	1	0	0	0	0.365		3F	0	0	1	1	1	1	1	1	0.560
19	0	0	0	1	1	0	0	1	0.370		40	0	1	1	1	0	0	0	0	0.565
1A	0	0	0	1	1	0	1	0	0.375		41	0	1	1	1	0	0	0	1	0.570
1B	0	0	0	1	1	0	1	1	0.380		42	0	1	1	1	0	0	1	0	0.575
1C	0	0	0	1	1	1	0	0	0.385		43	0	1	0	1	0	0	1	1	0.580
1D	0	0	0	1	1	1	0	1	0.390		44	0	1	0	0	0	1	0	0	0.585
1E	0	0	0	1	1	1	1	0	0.395		45	0	1	0	0	0	1	0	1	0.590
1F	0	0	0	1	1	1	1	1	0.400		46	0	1	0	0	0	1	1	0	0.595
20	0	0	1	0	0	0	0	0	0.405		47	0	1	0	0	0	1	1	1	0.600
21	0	0	1	0	0	0	0	1	0.410		48	0	1	0	0	1	0	0	0	0.605
22	0	0	1	0	0	0	1	0	0.415		49	0	1	0	0	1	0	0	1	0.610
23	0	0	1	0	0	0	1	1	0.420		4A	0	1	0	0	1	0	1	0	0.615
24	0	0	1	0	0	1	0	0	0.425		4B	0	1	0	0	1	0	1	1	0.620
25	0	0	1	0	0	1	0	1	0.430		4C	0	1	0	0	1	1	0	0	0.625
26	0	0	1	0	0	1	1	0	0.435		4D	0	1	0	0	1	1	0	1	0.630
4E	0	1	0	0	1	1	1	0	0.635		76	0	1	1	1	0	1	1	0	0.835
4F	0	1	0	0	1	1	1	1	0.640		77	0	1	1	1	0	1	1	1	0.840
50	0	1	0	0	0	0	0	0	0.645		78	0	1	1	1	1	0	0	0	0.845
51	0	1	0	0	0	0	0	1	0.650		79	0	1	1	1	1	0	0	1	0.850
52	0	1	0	0	0	0	1	0	0.655		7A	0	1	1	1	1	0	1	0	0.855
53	0	1	0	0	0	0	1	1	0.660		7B	0	1	1	1	1	0	1	1	0.860
54	0	1	0	1	0	1	0	0	0.665		7C	0	1	1	1	1	1	0	0	0.865
55	0	1	0	1	0	1	0	1	0.670		7D	0	1	1	1	1	1	0	1	0.870
56	0	1	0	1	0	1	1	0	0.675		7E	0	1	1	1	1	1	1	0	0.875
57	0	1	0	1	0	1	1	1	0.680		7F	0	1	1	1	1	1	1	1	0.880
58	0	1	0	1	1	0	0	0	0.685		80	1	0	0	0	0	0	0	0	0.885
59	0	1	0	1	1	0	0	1	0.690		81	1	0	0	0	0	0	0	1	0.890
5A	0	1	0	1	1	0	1	0	0.695		82	1	0	0	0	0	0	1	0	0.895
5B	0	1	0	1	1	0	1	1	0.700		83	1	0	0	0	0	0	1	1	0.900
5C	0	1	0	1	1	1	0	0	0.705		84	1	0	0	0	0	1	0	0	0.905
5D	0	1	0	1	1	1	0	1	0.710		85	1	0	0	0	0	1	0	1	0.910
5E	0	1	0	1	1	1	1	0	0.715		86	1	0	0	0	0	1	1	0	0.915
5F	0	1	0	1	1	1	1	1	0.720		87	1	0	0	0	0	1	1	1	0.920
60	0	1	1	0	0	0	0	0	0.725		88	1	0	0	0	1	0	0	0	0.925
61	0	1	1	0	0	0	0	1	0.730		89	1	0	0	0	1	0	0	1	0.930
62	0	1	1	0	0	0	1	0	0.735		8A	1	0	0	0	1	0	1	0	0.935
63	0	1	1	0	0	0	1	1	0.740		8B	1	0	0	0	1	0	1	1	0.940
64	0	1	1	0	0	1	0	0	0.745		8C	1	0	0	0	1	1	0	0	0.945

Table 2-37. Intel® Itanium® Processor 9500 Series VCCCORE (VID_VCCCORE) and VCCUNCORE and (VID_VCCUNCORE) Voltage Identification Definition for Ararat II (Sheet 3 of 4)

Hex	VID 7	VID6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	VID (V)	Hex	VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID0	VID (V)
65	0	1	1	0	0	1	0	1	0.750	8D	1	0	0	0	1	1	0	1	0.950
66	0	1	1	0	0	1	1	0	0.755	8E	1	0	0	0	1	1	1	0	0.955
67	0	1	1	0	0	1	1	1	0.760	8F	1	0	0	0	1	1	1	1	0.960
68	0	1	1	0	1	0	0	0	0.765	90	1	0	0	1	0	0	0	0	0.965
69	0	1	1	0	1	0	0	1	0.770	91	1	0	0	1	0	0	0	1	0.970
6A	0	1	1	0	1	0	1	0	0.775	92	1	0	0	1	0	0	1	0	0.975
6B	0	1	1	0	1	0	1	1	0.780	93	1	0	0	1	0	0	1	1	0.980
6C	0	1	1	0	1	1	0	0	0.785	94	1	0	0	1	0	1	0	0	0.985
6D	0	1	1	0	1	1	0	1	0.790	95	1	0	0	1	0	1	0	1	0.990
6E	0	1	1	0	1	1	1	0	0.795	96	1	0	0	1	0	1	1	0	0.995
6F	0	1	1	0	1	1	1	1	0.800	97	1	0	0	1	0	1	1	1	1.000
70	0	1	1	1	0	0	0	0	0.805	98	1	0	0	1	1	0	0	0	1.005
71	0	1	1	1	0	0	0	1	0.810	99	1	0	0	1	1	0	0	1	1.010
72	0	1	1	1	0	0	1	0	0.815	9A	1	0	0	1	1	0	1	0	1.015
73	0	1	1	1	0	0	1	1	0.820	9B	1	0	0	1	1	0	1	1	1.020
74	0	1	1	1	0	1	0	0	0.825	9C	1	0	0	1	1	1	0	0	1.025
75	0	1	1	1	0	1	0	1	0.830	9D	1	0	0	1	1	1	0	1	1.030
9E	1	0	0	1	1	1	1	0	1.035	C6	1	1	0	0	0	1	1	0	1.235
9F	1	0	0	1	1	1	1	1	1.040	C7	1	1	0	0	0	1	1	1	1.240
A0	1	0	1	0	0	0	0	0	1.045	C8	1	1	0	0	1	0	0	0	1.245
A1	1	0	1	0	0	0	0	1	1.050	C9	1	1	0	0	1	0	0	1	1.250
A2	1	0	1	0	0	0	1	0	1.055	CA	1	1	0	0	1	0	1	0	1.255
A3	1	0	1	0	0	0	1	1	1.060	CB	1	1	0	0	1	0	1	1	1.260
A4	1	0	1	0	0	1	0	0	1.065	CC	1	1	0	0	1	1	0	0	1.265
A5	1	0	1	0	0	1	0	1	1.070	CD	1	1	0	0	1	1	0	1	1.270
A6	1	0	1	0	0	1	1	0	1.075	CE	1	1	0	0	1	1	1	0	1.275
A7	1	0	1	0	0	1	1	1	1.080	CF	1	1	0	0	1	1	1	1	1.280
A8	1	0	1	0	1	0	0	0	1.085	D0	1	1	0	1	0	0	0	0	1.285
A9	1	0	1	0	1	0	0	1	1.090	D1	1	1	0	1	0	0	0	1	1.290
AA	1	0	1	0	1	0	1	0	1.095	D2	1	1	0	1	0	0	1	0	1.295
AB	1	0	1	0	1	0	1	1	1.100	D3	1	1	0	1	0	0	1	1	1.300
AC	1	0	1	0	1	1	0	0	1.105	D4	1	1	0	1	0	1	0	0	1.305
AD	1	0	1	0	1	1	0	1	1.110	D5	1	1	0	1	0	1	0	1	1.310
AE	1	0	1	0	1	1	1	0	1.115	D6	1	1	0	1	0	1	1	0	1.315
AF	1	0	1	0	1	1	1	1	1.120	D7	1	1	0	1	0	1	1	1	1.320
B0	1	0	1	1	0	0	0	0	1.125	D8	1	1	0	1	1	0	0	0	1.325
B1	1	0	1	1	0	0	0	1	1.130	D9	1	1	0	1	1	0	0	1	1.330
B2	1	0	1	1	0	0	1	0	1.135	DA	1	1	0	1	1	0	1	0	1.335
B3	1	0	1	1	0	0	1	1	1.140	DB	1	1	0	1	1	0	1	1	1.340
B4	1	0	1	1	0	1	0	0	1.145	DC	1	1	0	1	1	1	0	0	1.345

Table 2-37. Intel® Itanium® Processor 9500 Series VCCCORE (VID_VCCCORE) and VCCUNCORE and (VID_VCCUNCORE) Voltage Identification Definition for Ararat II (Sheet 4 of 4)

Hex	VID 7	VID6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	VID (V)		Hex	VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VI D0	VID (V)
B5	1	0	1	1	0	1	0	1	1.150		DD	1	1	0	1	1	1	0	1	1.350
B6	1	0	1	1	0	1	1	0	1.155		DE	1	1	0	1	1	1	1	0	1.355
B7	1	0	1	1	0	1	1	1	1.160		DF	1	1	0	1	1	1	1	1	1.360
B8	1	0	1	1	1	0	0	0	1.165		E0	1	1	1	0	0	0	0	0	1.365
B9	1	0	1	1	1	0	0	1	1.170		E1	1	1	1	0	0	0	0	1	1.370
BA	1	0	1	1	1	0	1	0	1.175		E2	1	1	1	0	0	0	1	0	1.375
BB	1	0	1	1	1	0	1	1	1.180		E3	1	1	1	0	0	0	1	1	1.380
BC	1	0	1	1	1	1	0	0	1.185		E4	1	1	1	0	0	1	0	0	1.385
BD	1	0	1	1	1	1	0	1	1.190		E5	1	1	1	0	0	1	0	1	1.390
BE	1	0	1	1	1	1	1	0	1.195		E6	1	1	1	0	0	1	1	0	1.395
BF	1	0	1	1	1	1	1	1	1.200		E7	1	1	1	0	0	1	1	1	1.400
C0	1	1	0	0	0	0	0	0	1.205		E8	1	1	1	0	1	0	0	0	1.405
C1	1	1	0	0	0	0	0	1	1.210		E9	1	1	1	0	1	0	0	1	1.410
C2	1	1	0	0	0	0	1	0	1.215		EA	1	1	1	0	1	0	1	0	1.415
C3	1	1	0	0	0	0	1	1	1.220		EB	1	1	1	0	1	0	1	1	1.420
C4	1	1	0	0	0	1	0	0	1.225		EC	1	1	1	0	1	1	0	0	1.425
C5	1	1	0	0	0	1	0	1	1.230		ED	1	1	1	0	1	1	0	1	1.430
EE	1	1	1	0	1	1	1	0	1.435		F7	1	1	1	1	0	1	1	1	1.480
EF	1	1	1	0	1	1	1	1	1.440		F8	1	1	1	1	1	0	0	0	1.485
F0	1	1	1	1	0	0	0	0	1.445		F9	1	1	1	1	1	0	0	1	1.490
F1	1	1	1	1	0	0	0	1	1.450		FA	1	1	1	1	1	0	1	0	1.495
F2	1	1	1	1	0	0	1	0	1.455		FB	1	1	1	1	1	0	1	1	1.500
F3	1	1	1	1	0	0	1	1	1.460		FC	1	1	1	1	1	1	0	0	1.505
F4	1	1	1	1	0	1	0	0	1.465		FD	1	1	1	1	1	1	0	1	1.510
F5	1	1	1	1	0	1	0	1	1.470		FE	1	1	1	1	1	1	1	0	1.515
F6	1	1	1	1	0	1	1	0	1.475		FF	1	1	1	1	1	1	1	1	1.520

2.8 Cache Voltage Identification (Intel® Itanium® Processor 9300 Series only)

The Cache Voltage Identification (CVID) value supplies the voltage for VCCCACHE, the L3 cache voltage for the Intel® Itanium® Processor 9300 Series. The VID_VCCCACHE specification for the processor is supported by the *Ararat I Regulator Module Design Guide*. The voltage set by the VID_VCCCACHE value is the maximum VCCCACHE voltage allowed by the processor.

Individual processor CVID values may be calibrated during manufacturing such that two devices at the same core speed may have different default VID_VCCCACHE settings.

The processor uses the VID_VCCCACHE value to support automatic selection of the power supply voltages. Table 2-38 specifies the voltage level corresponding to the state of VID_VCCCACHE. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to a low voltage level. See the *Ararat I Regulator Module Design Guide* for more details.

Table 2-38. Cache (VID_VCCCACHE) Voltage Identification Definition for Ararat

Hex	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	VID (V)		Hex	VID5	VID4	VID3	VID2	VID1	VID0	VID (V)
00	0	0	0	0	0	0	OFF		20	1	0	0	0	0	0	1.2125
01	0	0	0	0	0	1	1.6000		21	1	0	0	0	0	1	1.2000
02	0	0	0	0	1	0	1.5875		22	1	0	0	0	1	0	1.1875
03	0	0	0	0	1	1	1.5750		23	1	0	0	0	1	1	1.1750
04	0	0	0	1	0	0	1.5625		24	1	0	0	1	0	0	1.1625
05	0	0	0	1	0	1	1.5500		25	1	0	0	1	0	1	1.1500
06	0	0	0	1	1	0	1.5375		26	1	0	0	1	1	0	1.1375
07	0	0	0	1	1	1	1.5250		27	1	0	0	1	1	1	1.1250
08	0	0	1	0	0	0	1.5125		28	1	0	1	0	0	0	1.1125
09	0	0	1	0	0	1	1.5000		29	1	0	1	0	0	1	1.1000
0A	0	0	1	0	1	0	1.4875		2A	1	0	1	0	1	0	1.0875
0B	0	0	1	0	1	1	1.4750		2B	1	0	1	0	1	1	1.0750
0C	0	0	1	1	0	0	1.4625		2C	1	0	1	1	0	0	1.0625
0D	0	0	1	1	0	1	1.4500		2D	1	0	1	1	0	1	1.0500
0E	0	0	1	1	1	0	1.4375		2E	1	0	1	1	1	0	1.0375
0F	0	0	1	1	1	1	1.4250		2F	1	0	1	1	1	1	1.0250
10	0	1	0	0	0	0	1.4125		30	1	1	0	0	0	0	1.0125
11	0	1	0	0	0	1	1.4000		31	1	1	0	0	0	1	1.000
12	0	1	0	0	1	0	1.3875		32	1	1	0	0	1	0	0.9875
13	0	1	0	0	1	1	1.3750		33	1	1	0	0	1	1	0.9750
14	0	1	0	1	0	0	1.3625		34	1	1	0	1	0	0	0.9625
15	0	1	0	1	0	1	1.3500		35	1	1	0	1	0	1	0.9500
16	0	1	0	1	1	0	1.3375		36	1	1	0	1	1	0	0.9375
17	0	1	0	1	1	1	1.3250		37	1	1	0	1	1	1	0.9250
18	0	1	1	0	0	0	1.3125		38	1	1	1	0	0	0	0.9125
19	0	1	1	0	0	1	1.3000		39	1	1	1	0	0	1	0.9000
1A	0	1	1	0	1	0	1.2870		3A	1	1	1	0	1	0	0.8875
1B	0	1	1	0	1	1	1.2750		3B	1	1	1	0	1	1	0.8750
1C	0	1	1	1	0	0	1.2625		3C	1	1	1	1	0	0	0.8625
1D	0	1	1	1	0	1	1.2500		3D	1	1	1	1	0	1	0.8500
1E	0	1	1	1	1	0	1.2375		3E	1	1	1	1	1	0	0.8375
1F	0	1	1	1	1	1	1.2250		3F	1	1	1	1	1	1	0.8250

2.9 RSVD, Unused, and DEBUG Pins

All RSVD (RESERVED) pins must be left unconnected. Connection of these pins to power, VSS, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors.

For reliable operation, always terminate unused inputs or bi-directional signals to their respective deasserted states. A resistor must be used when tying bi-directional signals to power or ground, also allowing for system testability. Unused pins of Intel® QuickPath Interconnect and FB-DIMM ports may be left as no-connects since termination is provided on the processor silicon.

Unused outputs may be terminated on the system board or left connected. Note that leaving unused outputs unterminated may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in latest revisions of *Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series Platform Design Guide*.

Debug pins have ODT and can be left as no-connects. Their routing guidelines are provided in the *Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series Platform Design Guide*.

2.10 Mixing Processors

Intel will support mixing CPUs in the same system or hard partition as defined below. A hard partition is a smaller system capable of booting an OS, consisting of one or more processors, memory and I/O controller hubs that are formed by domain partitioning.

1. CPUs from adjacent steppings. For example if one cpu is from stepping N, and another cpu is from the next stepping, N+1, then CPU_N and CPU_{N+1} are compatible. Similarly CPU_N is not compatible with CPU_{N+2}.
2. All CPUs in the system or hard partition must have the same core clock speed or speed range and the same cache size.
3. All Intel® QPI links must have the same data rate, except for Intel® QPI links which are disabled or in slow mode.

Additionally, for the Intel® Itanium® Processor 9300 Series:

4. If variable frequency mode (VFM) is enabled in one CPU it must be enabled in all CPUs. If VFM mode is disabled in one CPU it must be disabled in all CPUs.
5. Mixing an enabled VFM part with an fixed frequency mode (FFM) part within the same system or hard partition.

2.11 Supported Power-up Voltage Sequence

The supported order of voltage sequencing for the processor, detailed in Figure 2-17 and Figure 2-18 and Table 2-39, is VCC33_SM, VccArarat(12V), VCCA, VCCIO, VCCUNCORE and VCCCORE for the Intel® Itanium® Processor 9500 Series processor and followed by VCCCACHE for the Intel® Itanium® Processor 9300 Series processor. If customers need to apply VccArarat(12V) before VCC33_SM, the processor will not sustain damage. The application of VCC33_SM before VccArarat(12V) allows the PIROM to be read before the processor is powered.

Once started, the power up sequence must complete within 1000 ms, as defined by the time limit for PWRGOOD to be asserted. VCC33_SM is brought up first to allow platforms to read the socket Processor Information data and the PROCTYPE pin.

VccArarat (12V) is the input voltage to the Ararat regulator. The VCCA supply is used to power the processor's analog circuits. VCCIO is used to power the I/O circuits. Once VCCIO is up and stable the external environment can generate the SYSINT clock signals. Once the SYSINT clocks are valid, the external environment can assert the

VROUTPUT_ENABLE0 signal. After VROUTPUT_ENABLE0 is asserted the sequence of powering up the VCCUNCORE and VCCCORE supplies and the VCCCACHE (Intel® Itanium® Processor 9300 Series) begins.

For the Intel® Itanium® Processor 9300 Series, the VCCUNCORE, VCCCORE and VCCCACHE supplies power the sysint, cores and large cache arrays respectively.

For the Intel® Itanium® Processor 9500 Series, the VCCUNCORE and VCCCORE supplies power the sysint, the cores and the large cache arrays respectively.

When all supplies are up and stable, Ararat asserts VRPWRGD which signals the external environment that it can assert the PWRGOOD signal. PWRGOOD assertion initiates the processor internal cold reset sequence.

With reference to the power sequencing timing requirements imposed by the Ararat VR as shown in Figure 2-17 and Figure 2-18, timing specifications for the elapsed time taken for an Ararat regulator to bring up each of its output voltages can be found in the *Ararat 170 Watt Voltage Regulator Module Design Guide* for the Intel® Itanium® Processor 9300 Series and the *Ararat II Voltage Regulator Module Design Guide* for the Intel® Itanium® Processor 9500 Series.

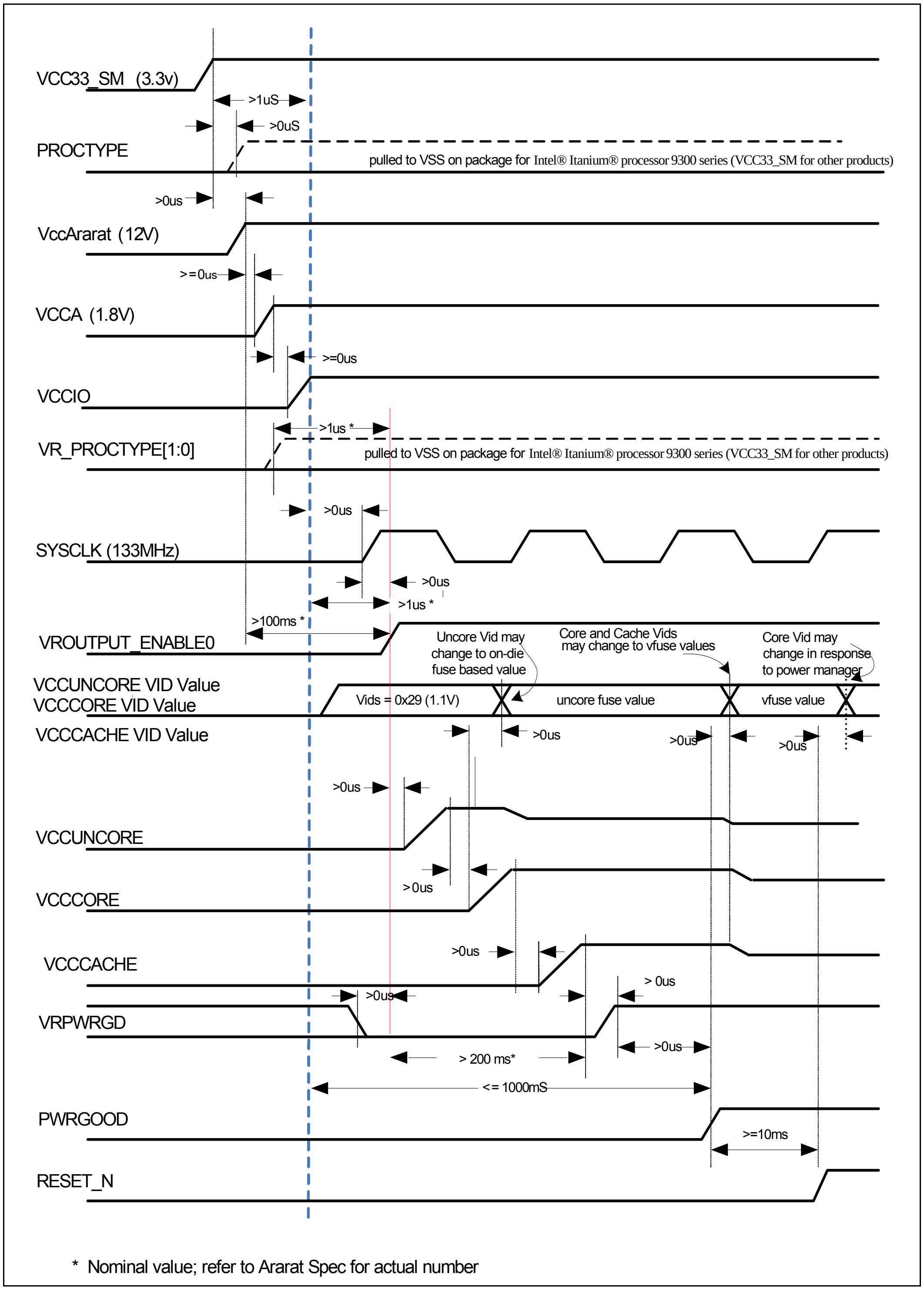
When the platform asserts PWRGOOD to the processor, the Intel® Itanium® Processor 9300 Series requires a minimum of 10 ms to complete its internal reset sequence before deasserting RESET_N, while the Intel® Itanium® Processor 9500 Series requires a minimum of 15 ms. For platforms that use both processors, a minimum of 15 ms is needed to meet the requirements of both processors.

During platform initialization, the RESET_N pin to any component in the platform can be removed ONLY after all other components have had sufficient time to sample their respective reset pins. This is needed to prevent unknown behavior that may result if any one system component comes out of reset before other components have received the reset signal.

With the exception of standby miscellaneous pins, all input pins, bi-directional pins, and terminated output pins must not be allowed to exceed the processor's actual VCCIO voltage prior to and during ramp up of the VCCIO supply.

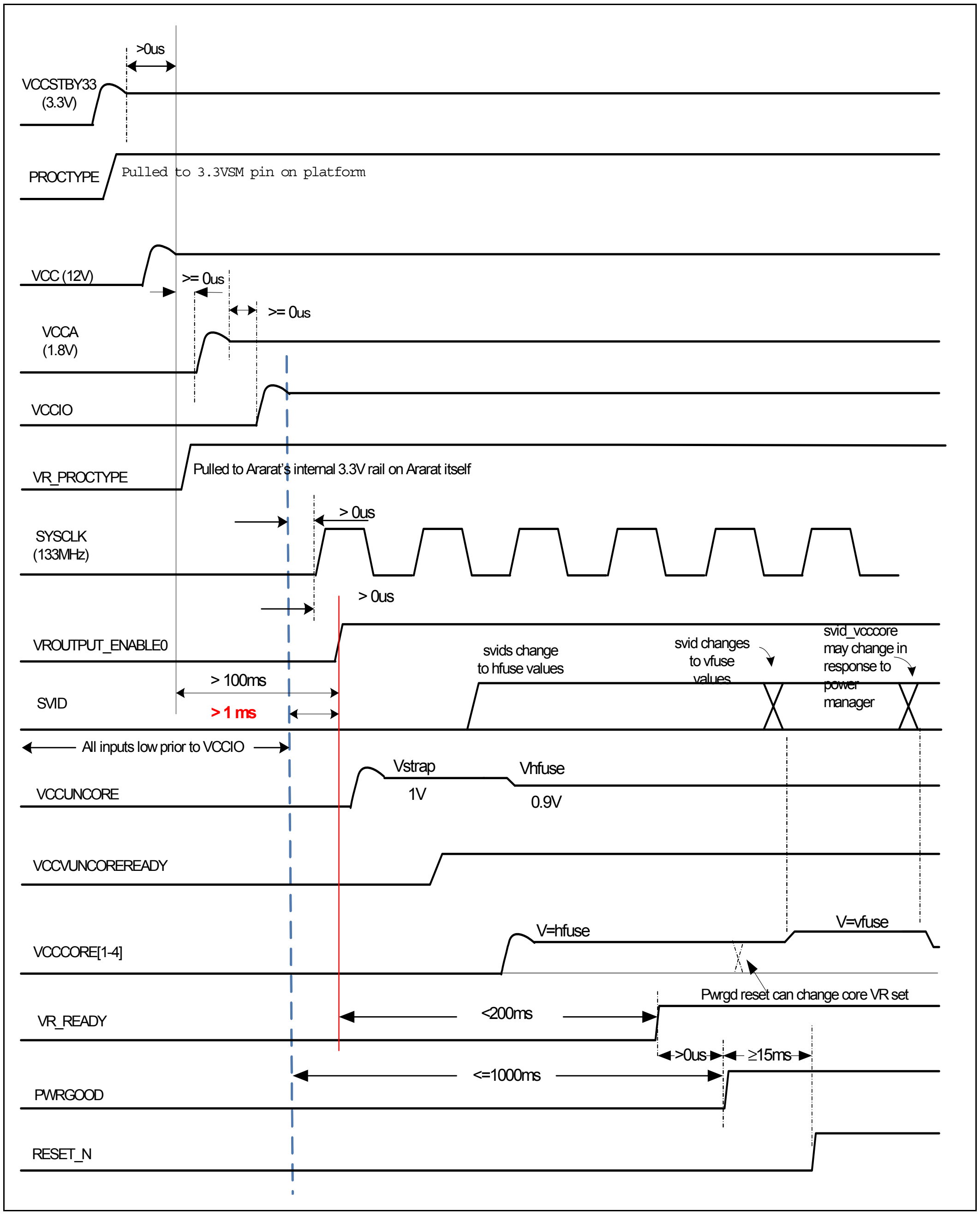
2.11.1 Supported Power-up Voltage Sequence for the Intel® Itanium® Processor 9300 Series

Figure 2-17. Supported Power-up Voltage Sequence Timing Requirements for the Intel® Itanium® Processor 9300 Series



2.11.2 Supported Power-up Voltage Sequence for the Intel® Itanium® Processor 9500 Series

Figure 2-18. Supported Power-up Sequence Timing Requirements for Intel® Itanium® Processor 9500 Series



2.11.3 Power-up Voltage Sequence Timing Requirements

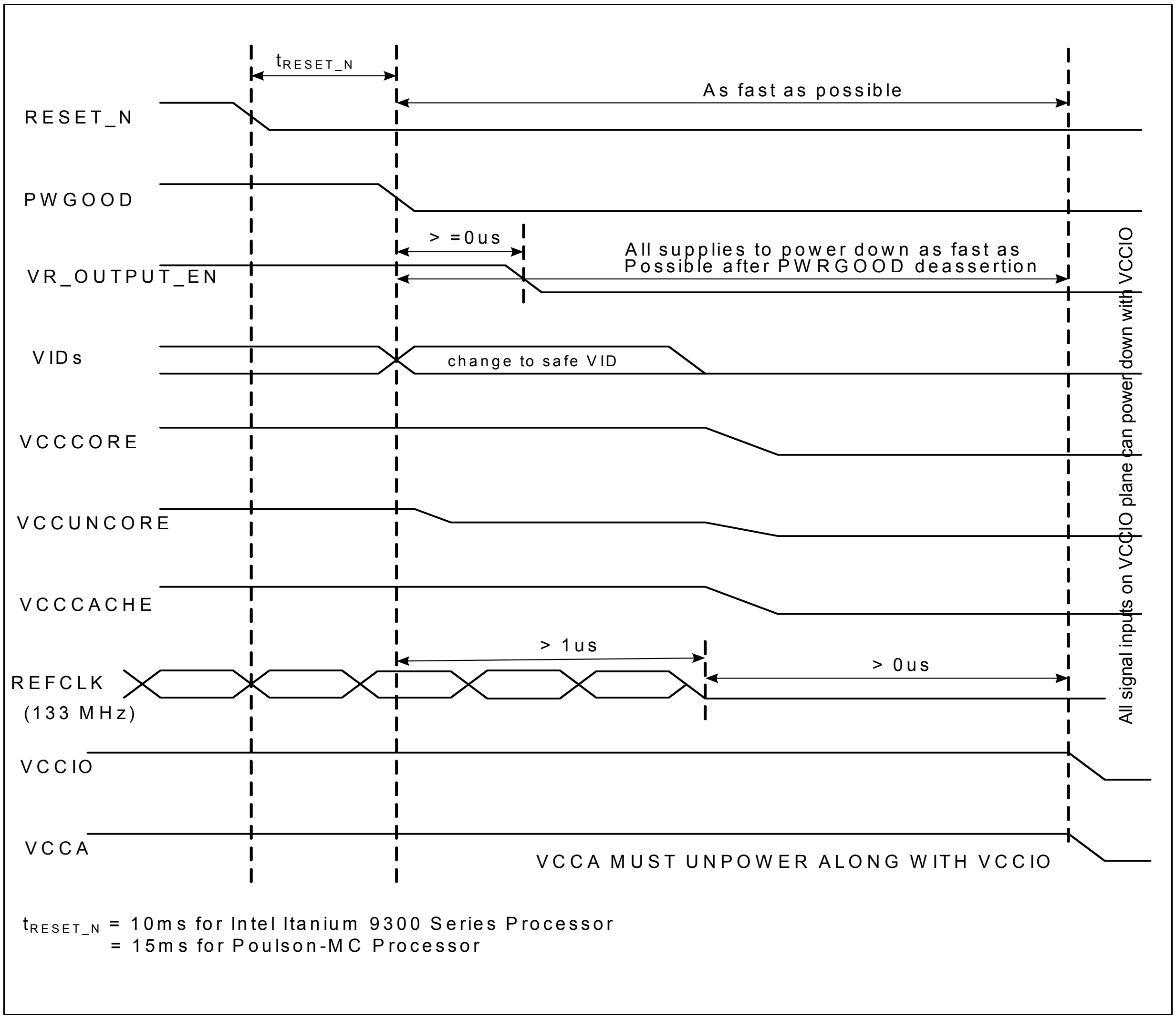
Table 2-39. Power-up Voltage Sequence Timing Requirements

Parameter	Min	Max	Unit
VCC33_SM stable high to VCCA delay	>0		
VCCA to VCCIO delay time	0		µs
VCCIO to PWRGOOD high delay time		1000	ms
VCCIO stable high to SYSCLK	>0		µs
SYSCLK valid before VROUTPUTENABLE0 high	>0		µs
VCCIO stable before VROUTPUT_ENABLE0 high for Intel® Itanium® Processor 9300 Series [1]	>1		µs
VCCIO stable before VROUTPUT_ENABLE0 high for Intel® Itanium® Processor 9500 Series [2]	>1		ms
VROUTPUT_ENABLE0 high to VRPWRGOOD high for Intel® Itanium® Processor 9300 Series [1]		200	ms
VROUTPUT_ENABLE0 high to VR_READY for Intel® Itanium® Processor 9500 Series [2]		200	ms
VCCUNCORE time to stabilize [1]	1	5	ms
Delay from VCCUNCORE at programmed VID value to VCCCORE [1]	0.05	8	ms
VCCCORE steady at safe VID value [1]	0.05	3	ms
VCCCORE transition time from safe VID to programmed VID [1]		2.5	
Delay from VCCCORE/VCCUNCORE/VCCCACHE at programmed values to VRPWRGOOD high for Intel® Itanium® Processor 9300 Series [1]	0.05	3	
VRPWRGD high to PWRGOOD high for Intel® Intel® Itanium® Processor 9300 Series	>0		ms
VR_READY high to PWRGOOD high for Intel® Itanium® Processor 9500 Series	>0		ms
PWRGOOD high to RESET_N high (t_{RESET_N}) Intel® Itanium® Processor 9300 Series	10		ms
PWRGOOD high to RESET_N high (t_{RESET_N}) Intel® Itanium® Processor 9500 Series	15		ms

2.12 Supported Power-down Voltage Sequence

The supported power down sequence of voltage for the processor is detailed in Figure 2-19. It should be noted that when the processor is required to be physically removed from its socket, power rails VCC33_SM and Vcc(12V) must also be powered down before removal of the processor.

Figure 2-19. Supported Power-down Voltage Sequence Timing Requirements



2.13 Timing Relationship Between RESET_N and SKTID

In the processor, the SKTID pins are time-shared:

SKTID[0] is interpreted as a NodeID bit during cold reset and pwrgood reset. It is interpreted as the error reset modifier during warm-logic reset if SKTID[0] is asserted.

SKTID[2] is interpreted as a NodeID bit during cold reset and pwrgood reset, and it is interpreted as an error input being signaled by the system at all other times (except during non-cold resets when it is ignored). Figure 2-20 and Table 2-40 show the timing relationship between RESET_N and SKTID pins for different reset cases.

The LRGSCLSYS pin is sampled only during the PWRGOOD and cold reset period.

The BOOTMODE[2:0] and FLASHROM_CFG[1:0] pins are sampled during the assertion of all resets except warm-logic resets.

Figure 2-20. RESET_N and SKITID Timing for Warm and Cold Resets

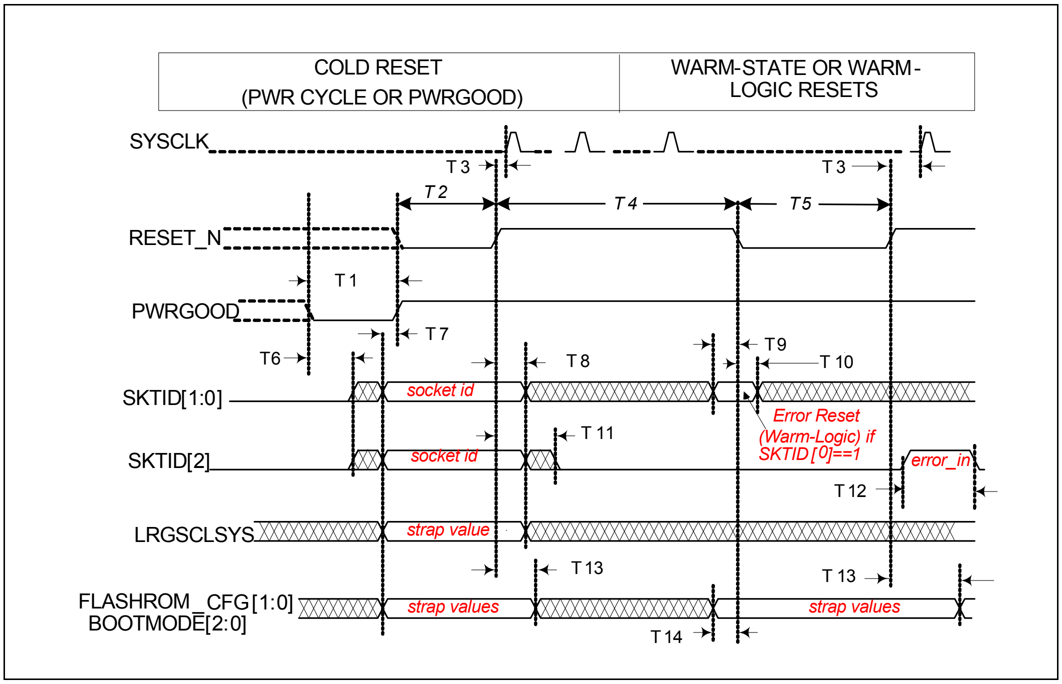


Table 2-40. RESET_N and SKTID Timing (Sheet 1 of 2)

Parameter	Description	MIN	MAX	UNIT
T1	PWRGOOD deasserted delay to RESET_N asserted	0	200	ns
T2	PWRGOOD asserted delay to RESET_N deasserted (Intel® Itanium® Processor 9300 Series)	10		ms
T2	PWRGOOD asserted delay to RESET_N deasserted (Intel® Itanium® Processor 9500 Series)	15		ms
T3	RESET_N setup and hold relative to SYSCLK asserted	500		ps
T4	RESET_N deasserted pulse width	8		SYSCLK cycles
T5	RESET_N asserted pulse width (Intel® Itanium® Processor 9300 Series)	10		ms
T5	RESET_N asserted pulse width (Intel® Itanium® Processor 9500 Series)	15		ms
T6	SKTID[2:0] (as rst modifier, error) hold after PWRGOOD deasserted	0		ns
T7	SKTID[2:0] (as socket id), LRGSCLSYS, BOOTMODE[2:0], FLASHROM_CFG[1:0] setup to PWRGOOD deasserted	0		ns
T8	SKTID[2:0] (as socket id), LRGSCLSYS hold after RESET_N deasserted	0		ns
T9	SKTID[1:0] (as rst modifier) setup to RESET_N asserted	200		ns
T10	SKTID[1:0] (as rst modifier) hold after RESET_N asserted	200		ns

Table 2-40. RESET_N and SKTID Timing (Sheet 2 of 2)

Parameter	Description	MIN	MAX	UNIT
T11	RESET_N deasserted delay to SKTID[2] deasserted (as error in)		100	ns
T12	SKTID[2] (as error in) asserted pulse width	3		SYSCLK cycles
T13	BOOTMODE[2:0], FLASHROM_CFG[1:0] hold after RESET_N deasserted	1		us
T14	BOOTMODE[2:)], FLASHROM_CFG[1:0] setup to RESET_N asserted	0		ns

2.14 Test Access Port (TAP) Connection

The recommended TAP connectivity is detailed in the *Intel® Itanium® Platform Debug Port Design Guide (DPDG)*.

§

3 Pin Listing

3.1 Processor Package *Bottom* Pin Assignments

This section provides a sorted package bottom pin list in Table 3-1 and Table 3-2. Table 3-1 is a listing of all processor package bottom side pins ordered alphabetically by pin name. Table 3-2 is a listing of all processor package bottom side pins ordered by pin number. All pins are defined for both Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series except where noted.

3.1.1 Package Bottom Pin Listing by Pin Name

Table 3-1. Pin List by Pin Name (Sheet 1 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
G10	BOOTMODE[0]		I
G9	BOOTMODE[1]		I
C3	CPU_PRES1_N		I/O
D37	CPU_PRES2_N		I/O
AT36	CPU_PRES3_N		I/O
AT3	CPU_PRES4_N		I/O
J37	CSI0RNCLK	Differential	I
B33	CSI0RNDAT[0]	Differential	I
D34	CSI0RNDAT[1]	Differential	I
B34	CSI0RNDAT[2]	Differential	I
D35	CSI0RNDAT[3]	Differential	I
C36	CSI0RNDAT[4]	Differential	I
E37	CSI0RNDAT[5]	Differential	I
F36	CSI0RNDAT[6]	Differential	I
G35	CSI0RNDAT[7]	Differential	I
H36	CSI0RNDAT[8]	Differential	I
J35	CSI0RNDAT[9]	Differential	I
L36	CSI0RNDAT[10]	Differential	I
L38	CSI0RNDAT[11]	Differential	I
N37	CSI0RNDAT[12]	Differential	I
P36	CSI0RNDAT[13]	Differential	I
R37	CSI0RNDAT[14]	Differential	I
T36	CSI0RNDAT[15]	Differential	I
T38	CSI0RNDAT[16]	Differential	I
U36	CSI0RNDAT[17]	Differential	I
V38	CSI0RNDAT[18]	Differential	I
W37	CSI0RNDAT[19]	Differential	I
K37	CSI0RPCLK	Differential	I

Table 3-1. Pin List by Pin Name (Sheet 2 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
A33	CSI0RPDAT[0]	Differential	I
C34	CSI0RPDAT[1]	Differential	I
B35	CSI0RPDAT[2]	Differential	I
E35	CSI0RPDAT[3]	Differential	I
D36	CSI0RPDAT[4]	Differential	I
E38	CSI0RPDAT[5]	Differential	I
F37	CSI0RPDAT[6]	Differential	I
G36	CSI0RPDAT[7]	Differential	I
H37	CSI0RPDAT[8]	Differential	I
J36	CSI0RPDAT[9]	Differential	I
L37	CSI0RPDAT[10]	Differential	I
M38	CSI0RPDAT[11]	Differential	I
N38	CSI0RPDAT[12]	Differential	I
P37	CSI0RPDAT[13]	Differential	I
R38	CSI0RPDAT[14]	Differential	I
T37	CSI0RPDAT[15]	Differential	I
U38	CSI0RPDAT[16]	Differential	I
V36	CSI0RPDAT[17]	Differential	I
V37	CSI0RPDAT[18]	Differential	I
W36	CSI0RPDAT[19]	Differential	I
K33	CSI0TNCLK	Differential	O
K30	CSI0TNDAT[0]	Differential	O
J31	CSI0TNDAT[1]	Differential	O
G31	CSI0TNDAT[2]	Differential	O
F30	CSI0TNDAT[3]	Differential	O
K32	CSI0TNDAT[4]	Differential	O
F31	CSI0TNDAT[5]	Differential	O
E32	CSI0TNDAT[6]	Differential	O

Table 3-1. Pin List by Pin Name (Sheet 3 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
F33	CSI0TNDAT[7]	Differential	O
H33	CSI0TNDAT[8]	Differential	O
L31	CSI0TNDAT[9]	Differential	O
L33	CSI0TNDAT[10]	Differential	O
M34	CSI0TNDAT[11]	Differential	O
N32	CSI0TNDAT[12]	Differential	O
N34	CSI0TNDAT[13]	Differential	O
R34	CSI0TNDAT[14]	Differential	O
R33	CSI0TNDAT[15]	Differential	O
U33	CSI0TNDAT[16]	Differential	O
V32	CSI0TNDAT[17]	Differential	O
V34	CSI0TNDAT[18]	Differential	O
W32	CSI0TNDAT[19]	Differential	O
K34	CSI0TPCLK	Differential	O
J30	CSI0TPDAT[0]	Differential	O
H31	CSI0TPDAT[1]	Differential	O
G30	CSI0TPDAT[2]	Differential	O
E30	CSI0TPDAT[3]	Differential	O
J32	CSI0TPDAT[4]	Differential	O
F32	CSI0TPDAT[5]	Differential	O
E33	CSI0TPDAT[6]	Differential	O
G33	CSI0TPDAT[7]	Differential	O
H34	CSI0TPDAT[8]	Differential	O
L32	CSI0TPDAT[9]	Differential	O
M33	CSI0TPDAT[10]	Differential	O
M35	CSI0TPDAT[11]	Differential	O
N33	CSI0TPDAT[12]	Differential	O
P34	CSI0TPDAT[13]	Differential	O
R35	CSI0TPDAT[14]	Differential	O
T33	CSI0TPDAT[15]	Differential	O
U34	CSI0TPDAT[16]	Differential	O
V33	CSI0TPDAT[17]	Differential	O
W34	CSI0TPDAT[18]	Differential	O
Y32	CSI0TPDAT[19]	Differential	O
AK38	CSI1RNCLK	Differential	I
AU33	CSI1RNDAT[0]	Differential	I
AV33	CSI1RNDAT[1]	Differential	I
AV34	CSI1RNDAT[2]	Differential	I
AR34	CSI1RNDAT[3]	Differential	I
AT35	CSI1RNDAT[4]	Differential	I

Table 3-1. Pin List by Pin Name (Sheet 4 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AP36	CSI1RNDAT[5]	Differential	I
AP37	CSI1RNDAT[6]	Differential	I
AN37	CSI1RNDAT[7]	Differential	I
AM36	CSI1RNDAT[8]	Differential	I
AL37	CSI1RNDAT[9]	Differential	I
AJ37	CSI1RNDAT[10]	Differential	I
AH38	CSI1RNDAT[11]	Differential	I
AG36	CSI1RNDAT[12]	Differential	I
AF38	CSI1RNDAT[13]	Differential	I
AF36	CSI1RNDAT[14]	Differential	I
AE37	CSI1RNDAT[15]	Differential	I
AD36	CSI1RNDAT[16]	Differential	I
AC37	CSI1RNDAT[17]	Differential	I
AA38	CSI1RNDAT[18]	Differential	I
Y38	CSI1RNDAT[19]	Differential	I
AK37	CSI1RPCLK	Differential	I
AT33	CSI1RPDAT[0]	Differential	I
AV32	CSI1RPDAT[1]	Differential	I
AU34	CSI1RPDAT[2]	Differential	I
AR33	CSI1RPDAT[3]	Differential	I
AU35	CSI1RPDAT[4]	Differential	I
AP35	CSI1RPDAT[5]	Differential	I
AR37	CSI1RPDAT[6]	Differential	I
AN36	CSI1RPDAT[7]	Differential	I
AM35	CSI1RPDAT[8]	Differential	I
AL36	CSI1RPDAT[9]	Differential	I
AJ36	CSI1RPDAT[10]	Differential	I
AH37	CSI1RPDAT[11]	Differential	I
AH36	CSI1RPDAT[12]	Differential	I
AG38	CSI1RPDAT[13]	Differential	I
AF37	CSI1RPDAT[14]	Differential	I
AE38	CSI1RPDAT[15]	Differential	I
AD37	CSI1RPDAT[16]	Differential	I
AC38	CSI1RPDAT[17]	Differential	I
AB38	CSI1RPDAT[18]	Differential	I
Y37	CSI1RPDAT[19]	Differential	I
AJ32	CSI1TNCLK	Differential	O
AL27	CSI1TNDAT[0]	Differential	O
AN28	CSI1TNDAT[1]	Differential	O
AL28	CSI1TNDAT[2]	Differential	O

Table 3-1. Pin List by Pin Name (Sheet 5 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AN29	CSI1TNDAT[3]	Differential	O
AP31	CSI1TNDAT[4]	Differential	O
AL30	CSI1TNDAT[5]	Differential	O
AN32	CSI1TNDAT[6]	Differential	O
AN34	CSI1TNDAT[7]	Differential	O
AM31	CSI1TNDAT[8]	Differential	O
AL33	CSI1TNDAT[9]	Differential	O
AK33	CSI1TNDAT[10]	Differential	O
AH34	CSI1TNDAT[11]	Differential	O
AH32	CSI1TNDAT[12]	Differential	O
AG33	CSI1TNDAT[13]	Differential	O
AE33	CSI1TNDAT[14]	Differential	O
AE34	CSI1TNDAT[15]	Differential	O
AC34	CSI1TNDAT[16]	Differential	O
AB34	CSI1TNDAT[17]	Differential	O
AA35	CSI1TNDAT[18]	Differential	O
Y34	CSI1TNDAT[19]	Differential	O
AK32	CSI1TPCLK	Differential	O
AL26	CSI1TPDAT[0]	Differential	O
AN27	CSI1TPDAT[1]	Differential	O
AM28	CSI1TPDAT[2]	Differential	O
AP29	CSI1TPDAT[3]	Differential	O
AP30	CSI1TPDAT[4]	Differential	O
AM30	CSI1TPDAT[5]	Differential	O
AP32	CSI1TPDAT[6]	Differential	O
AN33	CSI1TPDAT[7]	Differential	O
AN31	CSI1TPDAT[8]	Differential	O
AL32	CSI1TPDAT[9]	Differential	O
AK34	CSI1TPDAT[10]	Differential	O
AJ34	CSI1TPDAT[11]	Differential	O
AH33	CSI1TPDAT[12]	Differential	O
AG34	CSI1TPDAT[13]	Differential	O
AF33	CSI1TPDAT[14]	Differential	O
AE35	CSI1TPDAT[15]	Differential	O
AD34	CSI1TPDAT[16]	Differential	O
AB35	CSI1TPDAT[17]	Differential	O
AA36	CSI1TPDAT[18]	Differential	O
Y35	CSI1TPDAT[19]	Differential	O
A21	CSI2RNCLK	Differential	I
J22	CSI2RNDAT[0]	Differential	I

Table 3-1. Pin List by Pin Name (Sheet 6 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
H21	CSI2RNDAT[1]	Differential	I
G20	CSI2RNDAT[2]	Differential	I
F21	CSI2RNDAT[3]	Differential	I
E23	CSI2RNDAT[4]	Differential	I
E20	CSI2RNDAT[5]	Differential	I
D21	CSI2RNDAT[6]	Differential	I
C21	CSI2RNDAT[7]	Differential	I
B20	CSI2RNDAT[8]	Differential	I
C22	CSI2RNDAT[9]	Differential	I
B23	CSI2RNDAT[10]	Differential	I
B25	CSI2RNDAT[11]	Differential	I
C26	CSI2RNDAT[12]	Differential	I
A25	CSI2RNDAT[13]	Differential	I
D26	CSI2RNDAT[14]	Differential	I
C27	CSI2RNDAT[15]	Differential	I
B28	CSI2RNDAT[16]	Differential	I
B30	CSI2RNDAT[17]	Differential	I
C31	CSI2RNDAT[18]	Differential	I
C33	CSI2RNDAT[19]	Differential	I
A22	CSI2RPCLK	Differential	I
J21	CSI2RPDAT[0]	Differential	I
G21	CSI2RPDAT[1]	Differential	I
G19	CSI2RPDAT[2]	Differential	I
F20	CSI2RPDAT[3]	Differential	I
E22	CSI2RPDAT[4]	Differential	I
D20	CSI2RPDAT[5]	Differential	I
D22	CSI2RPDAT[6]	Differential	I
B21	CSI2RPDAT[7]	Differential	I
A20	CSI2RPDAT[8]	Differential	I
C23	CSI2RPDAT[9]	Differential	I
A23	CSI2RPDAT[10]	Differential	I
B24	CSI2RPDAT[11]	Differential	I
B26	CSI2RPDAT[12]	Differential	I
A26	CSI2RPDAT[13]	Differential	I
D27	CSI2RPDAT[14]	Differential	I
C28	CSI2RPDAT[15]	Differential	I
B29	CSI2RPDAT[16]	Differential	I
A30	CSI2RPDAT[17]	Differential	I
B31	CSI2RPDAT[18]	Differential	I
C32	CSI2RPDAT[19]	Differential	I

Table 3-1. Pin List by Pin Name (Sheet 7 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
H29	CSI2TNCLK	Differential	O
H23	CSI2TNDAT[0]	Differential	O
G24	CSI2TNDAT[1]	Differential	O
F25	CSI2TNDAT[2]	Differential	O
D24	CSI2TNDAT[3]	Differential	O
H26	CSI2TNDAT[4]	Differential	O
F26	CSI2TNDAT[5]	Differential	O
E29	CSI2TNDAT[6]	Differential	O
J26	CSI2TNDAT[7]	Differential	O
F28	CSI2TNDAT[8]	Differential	O
H27	CSI2TNDAT[9]	Differential	O
K28	CSI2TNDAT[10]	Differential	O
M29	CSI2TNDAT[11]	Differential	O
P30	CSI2TNDAT[12]	Differential	O
M31	CSI2TNDAT[13]	Differential	O
R30	CSI2TNDAT[14]	Differential	O
P32	CSI2TNDAT[15]	Differential	O
T31	CSI2TNDAT[16]	Differential	O
U29	CSI2TNDAT[17]	Differential	O
U31	CSI2TNDAT[18]	Differential	O
W30	CSI2TNDAT[19]	Differential	O
J29	CSI2TPCLK	Differential	O
G23	CSI2TPDAT[0]	Differential	O
G25	CSI2TPDAT[1]	Differential	O
E25	CSI2TPDAT[2]	Differential	O
E24	CSI2TPDAT[3]	Differential	O
G26	CSI2TPDAT[4]	Differential	O
F27	CSI2TPDAT[5]	Differential	O
D29	CSI2TPDAT[6]	Differential	O
J27	CSI2TPDAT[7]	Differential	O
G28	CSI2TPDAT[8]	Differential	O
H28	CSI2TPDAT[9]	Differential	O
K29	CSI2TPDAT[10]	Differential	O
M30	CSI2TPDAT[11]	Differential	O
P31	CSI2TPDAT[12]	Differential	O
N31	CSI2TPDAT[13]	Differential	O
T30	CSI2TPDAT[14]	Differential	O
R32	CSI2TPDAT[15]	Differential	O
T32	CSI2TPDAT[16]	Differential	O
U30	CSI2TPDAT[17]	Differential	O

Table 3-1. Pin List by Pin Name (Sheet 8 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
V31	CSI2TPDAT[18]	Differential	O
W31	CSI2TPDAT[19]	Differential	O
AU21	CSI3RNCLK	Differential	I
AN18	CSI3RNDAT[0]	Differential	I
AL17	CSI3RNDAT[1]	Differential	I
AM16	CSI3RNDAT[2]	Differential	I
AN17	CSI3RNDAT[3]	Differential	I
AP19	CSI3RNDAT[4]	Differential	I
AR19	CSI3RNDAT[5]	Differential	I
AV17	CSI3RNDAT[6]	Differential	I
AU18	CSI3RNDAT[7]	Differential	I
AV19	CSI3RNDAT[8]	Differential	I
AT20	CSI3RNDAT[9]	Differential	I
AT22	CSI3RNDAT[10]	Differential	I
AU23	CSI3RNDAT[11]	Differential	I
AV24	CSI3RNDAT[12]	Differential	I
AU25	CSI3RNDAT[13]	Differential	I
AU26	CSI3RNDAT[14]	Differential	I
AT27	CSI3RNDAT[15]	Differential	I
AU28	CSI3RNDAT[16]	Differential	I
AV29	CSI3RNDAT[17]	Differential	I
AU30	CSI3RNDAT[18]	Differential	I
AV31	CSI3RNDAT[19]	Differential	I
AT21	CSI3RPCLK	Differential	I
AM18	CSI3RPDAT[0]	Differential	I
AL16	CSI3RPDAT[1]	Differential	I
AM15	CSI3RPDAT[2]	Differential	I
AN16	CSI3RPDAT[3]	Differential	I
AN19	CSI3RPDAT[4]	Differential	I
AR18	CSI3RPDAT[5]	Differential	I
AV16	CSI3RPDAT[6]	Differential	I
AT18	CSI3RPDAT[7]	Differential	I
AU19	CSI3RPDAT[8]	Differential	I
AR20	CSI3RPDAT[9]	Differential	I
AR22	CSI3RPDAT[10]	Differential	I
AT23	CSI3RPDAT[11]	Differential	I
AV23	CSI3RPDAT[12]	Differential	I
AU24	CSI3RPDAT[13]	Differential	I
AT26	CSI3RPDAT[14]	Differential	I
AR27	CSI3RPDAT[15]	Differential	I

Table 3-1. Pin List by Pin Name (Sheet 9 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AT28	CSI3RPDAT[16]	Differential	I
AV28	CSI3RPDAT[17]	Differential	I
AU29	CSI3RPDAT[18]	Differential	I
AU31	CSI3RPDAT[19]	Differential	I
AK29	CSI3TNCLK	Differential	O
AL20	CSI3TNDAT[0]	Differential	O
AM20	CSI3TNDAT[1]	Differential	O
AM23	CSI3TNDAT[2]	Differential	O
AN21	CSI3TNDAT[3]	Differential	O
AN23	CSI3TNDAT[4]	Differential	O
AM24	CSI3TNDAT[5]	Differential	O
AP25	CSI3TNDAT[6]	Differential	O
AN26	CSI3TNDAT[7]	Differential	O
AM26	CSI3TNDAT[8]	Differential	O
AJ27	CSI3TNDAT[9]	Differential	O
AH29	CSI3TNDAT[10]	Differential	O
AJ30	CSI3TNDAT[11]	Differential	O
AG31	CSI3TNDAT[12]	Differential	O
AF30	CSI3TNDAT[13]	Differential	O
AF31	CSI3TNDAT[14]	Differential	O
AD32	CSI3TNDAT[15]	Differential	O
AC31	CSI3TNDAT[16]	Differential	O
AB33	CSI3TNDAT[17]	Differential	O
AA31	CSI3TNDAT[18]	Differential	O
AA32	CSI3TNDAT[19]	Differential	O
AK28	CSI3TPCLK	Differential	O
AK20	CSI3TPDAT[0]	Differential	O
AM21	CSI3TPDAT[1]	Differential	O
AL23	CSI3TPDAT[2]	Differential	O
AP21	CSI3TPDAT[3]	Differential	O
AN22	CSI3TPDAT[4]	Differential	O
AN24	CSI3TPDAT[5]	Differential	O
AR25	CSI3TPDAT[6]	Differential	O
AP26	CSI3TPDAT[7]	Differential	O
AM25	CSI3TPDAT[8]	Differential	O
AK27	CSI3TPDAT[9]	Differential	O
AJ29	CSI3TPDAT[10]	Differential	O
AJ31	CSI3TPDAT[11]	Differential	O
AH31	CSI3TPDAT[12]	Differential	O
AG30	CSI3TPDAT[13]	Differential	O

Table 3-1. Pin List by Pin Name (Sheet 10 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AF32	CSI3TPDAT[14]	Differential	O
AE32	CSI3TPDAT[15]	Differential	O
AC32	CSI3TPDAT[16]	Differential	O
AC33	CSI3TPDAT[17]	Differential	O
AB31	CSI3TPDAT[18]	Differential	O
AA33	CSI3TPDAT[19]	Differential	O
H18	CSI4RNCLK	Differential	I
B15	CSI4RNDAT[0]	Differential	I
D15	CSI4RNDAT[1]	Differential	I
C16	CSI4RNDAT[2]	Differential	I
A17	CSI4RNDAT[3]	Differential	I
B18	CSI4RNDAT[4]	Differential	I
C17	CSI4RNDAT[5]	Differential	I
D19	CSI4RNDAT[6]	Differential	I
E17	CSI4RNDAT[7]	Differential	I
E18	CSI4RNDAT[8]	Differential	I
F17	CSI4RNDAT[9]	Differential	I
G18	CSI4RPCLK	Differential	I
A15	CSI4RPDAT[0]	Differential	I
D16	CSI4RPDAT[1]	Differential	I
B16	CSI4RPDAT[2]	Differential	I
A18	CSI4RPDAT[3]	Differential	I
B19	CSI4RPDAT[4]	Differential	I
C18	CSI4RPDAT[5]	Differential	I
C19	CSI4RPDAT[6]	Differential	I
D17	CSI4RPDAT[7]	Differential	I
E19	CSI4RPDAT[8]	Differential	I
F18	CSI4RPDAT[9]	Differential	I
L21	CSI4TNCLK	Differential	O
M14	CSI4TNDAT[0]	Differential	O
K13	CSI4TNDAT[1]	Differential	O
K15	CSI4TNDAT[2]	Differential	O
J14	CSI4TNDAT[3]	Differential	O
G15	CSI4TNDAT[4]	Differential	O
J16	CSI4TNDAT[5]	Differential	O
K17	CSI4TNDAT[6]	Differential	O
L18	CSI4TNDAT[7]	Differential	O
K19	CSI4TNDAT[8]	Differential	O
L20	CSI4TNDAT[9]	Differential	O
L22	CSI4TPCLK	Differential	O

Table 3-1. Pin List by Pin Name (Sheet 11 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
M15	CSI4TPDAT[0]	Differential	O
K14	CSI4TPDAT[1]	Differential	O
J15	CSI4TPDAT[2]	Differential	O
H14	CSI4TPDAT[3]	Differential	O
G16	CSI4TPDAT[4]	Differential	O
H16	CSI4TPDAT[5]	Differential	O
J17	CSI4TPDAT[6]	Differential	O
K18	CSI4TPDAT[7]	Differential	O
J19	CSI4TPDAT[8]	Differential	O
K20	CSI4TPDAT[9]	Differential	O
AP17	CSI5RNCLK	Differential	I
AL12	CSI5RNDAT[0]	Differential	I
AM13	CSI5RNDAT[1]	Differential	I
AN14	CSI5RNDAT[2]	Differential	I
AP15	CSI5RNDAT[3]	Differential	I
AR13	CSI5RNDAT[4]	Differential	I
AT13	CSI5RNDAT[5]	Differential	I
AU14	CSI5RNDAT[6]	Differential	I
AR15	CSI5RNDAT[7]	Differential	I
AU15	CSI5RNDAT[8]	Differential	I
AT16	CSI5RNDAT[9]	Differential	I
AR17	CSI5RPCLK	Differential	I
AL13	CSI5RPDAT[0]	Differential	I
AN13	CSI5RPDAT[1]	Differential	I
AP14	CSI5RPDAT[2]	Differential	I
AP16	CSI5RPDAT[3]	Differential	I
AR14	CSI5RPDAT[4]	Differential	I
AU13	CSI5RPDAT[5]	Differential	I
AV14	CSI5RPDAT[6]	Differential	I
AT15	CSI5RPDAT[7]	Differential	I
AU16	CSI5RPDAT[8]	Differential	I
AT17	CSI5RPDAT[9]	Differential	I
AJ22	CSI5TNCLK	Differential	O
AG13	CSI5TNDAT[0]	Differential	O
AH14	CSI5TNDAT[1]	Differential	O
AJ15	CSI5TNDAT[2]	Differential	O
AG16	CSI5TNDAT[3]	Differential	O
AH17	CSI5TNDAT[4]	Differential	O
AH19	CSI5TNDAT[5]	Differential	O
AK18	CSI5TNDAT[6]	Differential	O

Table 3-1. Pin List by Pin Name (Sheet 12 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AG19	CSI5TNDAT[7]	Differential	O
AJ20	CSI5TNDAT[8]	Differential	O
AL21	CSI5TNDAT[9]	Differential	O
AK22	CSI5TPCLK	Differential	O
AH13	CSI5TPDAT[0]	Differential	O
AJ14	CSI5TPDAT[1]	Differential	O
AK15	CSI5TPDAT[2]	Differential	O
AH16	CSI5TPDAT[3]	Differential	O
AJ17	CSI5TPDAT[4]	Differential	O
AJ19	CSI5TPDAT[5]	Differential	O
AK19	CSI5TPDAT[6]	Differential	O
AG20	CSI5TPDAT[7]	Differential	O
AJ21	CSI5TPDAT[8]	Differential	O
AL22	CSI5TPDAT[9]	Differential	O
H12	ERROR[0]_N		O
J12	ERROR[1]_N		O
AT11	FBD0NBIAN[0]	Differential	I
AU9	FBD0NBIAN[1]	Differential	I
AV8	FBD0NBIAN[2]	Differential	I
AR10	FBD0NBIAN[3]	Differential	I
AT8	FBD0NBIAN[4]	Differential	I
AT6	FBD0NBIAN[5]	Differential	I
AP4	FBD0NBIAN[6]	Differential	I
AN2	FBD0NBIAN[7]	Differential	I
AN3	FBD0NBIAN[8]	Differential	I
AL3	FBD0NBIAN[9]	Differential	I
AL1	FBD0NBIAN[10]	Differential	I
AK2	FBD0NBIAN[11]	Differential	I
AR2	FBD0NBIAN[12]	Differential	I
AU4	FBD0NBIAN[13]	Differential	I
AV11	FBD0NBIAN[14]	Differential	I
AU11	FBD0NBIAP[0]	Differential	I
AU10	FBD0NBIAP[1]	Differential	I
AV9	FBD0NBIAP[2]	Differential	I
AT10	FBD0NBIAP[3]	Differential	I
AU8	FBD0NBIAP[4]	Differential	I
AU6	FBD0NBIAP[5]	Differential	I
AR4	FBD0NBIAP[6]	Differential	I
AP2	FBD0NBIAP[7]	Differential	I
AN4	FBD0NBIAP[8]	Differential	I

Table 3-1. Pin List by Pin Name (Sheet 13 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AM3	FBD0NBIAP[9]	Differential	I
AL2	FBD0NBIAP[10]	Differential	I
AK3	FBD0NBIAP[11]	Differential	I
AR3	FBD0NBIAP[12]	Differential	I
AU5	FBD0NBIAP[13]	Differential	I
AV12	FBD0NBIAP[14]	Differential	I
AN9	FBD0NBIBN[0]	Differential	I
AM9	FBD0NBIBN[1]	Differential	I
AP7	FBD0NBIBN[2]	Differential	I
AP6	FBD0NBIBN[3]	Differential	I
AM5	FBD0NBIBN[4]	Differential	I
AK5	FBD0NBIBN[5]	Differential	I
AG1	FBD0NBIBN[6]	Differential	I
AF3	FBD0NBIBN[7]	Differential	I
AF2	FBD0NBIBN[8]	Differential	I
AE3	FBD0NBIBN[9]	Differential	I
AD1	FBD0NBIBN[10]	Differential	I
AB1	FBD0NBIBN[11]	Differential	I
AH2	FBD0NBIBN[12]	Differential	I
AJ4	FBD0NBIBN[13]	Differential	I
AM10	FBD0NBIBN[14]	Differential	I
AP9	FBD0NBIBP[0]	Differential	I
AM8	FBD0NBIBP[1]	Differential	I
AR7	FBD0NBIBP[2]	Differential	I
AN6	FBD0NBIBP[3]	Differential	I
AM6	FBD0NBIBP[4]	Differential	I
AL5	FBD0NBIBP[5]	Differential	I
AH1	FBD0NBIBP[6]	Differential	I
AG3	FBD0NBIBP[7]	Differential	I
AF1	FBD0NBIBP[8]	Differential	I
AE2	FBD0NBIBP[9]	Differential	I
AD2	FBD0NBIBP[10]	Differential	I
AC1	FBD0NBIBP[11]	Differential	I
AJ2	FBD0NBIBP[12]	Differential	I
AK4	FBD0NBIBP[13]	Differential	I
AL10	FBD0NBIBP[14]	Differential	I
AR5	FBD0NBICLKAN0	Differential	I
AT5	FBD0NBICLKAP0	Differential	I
AH3	FBD0NBICLKBN0	Differential	I
AH4	FBD0NBICLKBP0	Differential	I

Table 3-1. Pin List by Pin Name (Sheet 14 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AL6	FBD0REFSYSCLKN	Differential	I
AL7	FBD0REFSYSCLKP	Differential	I
V4	FBD0SBOAN[0]	Differential	O
W1	FBD0SBOAN[1]	Differential	O
V2	FBD0SBOAN[2]	Differential	O
U1	FBD0SBOAN[3]	Differential	O
T1	FBD0SBOAN[4]	Differential	O
N3	FBD0SBOAN[5]	Differential	O
M1	FBD0SBOAN[6]	Differential	O
L3	FBD0SBOAN[7]	Differential	O
L1	FBD0SBOAN[8]	Differential	O
P1	FBD0SBOAN[9]	Differential	O
J2	FBD0SBOAN[10]	Differential	O
W4	FBD0SBOAP[0]	Differential	O
W2	FBD0SBOAP[1]	Differential	O
V3	FBD0SBOAP[2]	Differential	O
V1	FBD0SBOAP[3]	Differential	O
T2	FBD0SBOAP[4]	Differential	O
N2	FBD0SBOAP[5]	Differential	O
N1	FBD0SBOAP[6]	Differential	O
M3	FBD0SBOAP[7]	Differential	O
L2	FBD0SBOAP[8]	Differential	O
P2	FBD0SBOAP[9]	Differential	O
K2	FBD0SBOAP[10]	Differential	O
AK8	FBD0SBOBN[0]	Differential	O
AJ7	FBD0SBOBN[1]	Differential	O
AH6	FBD0SBOBN[2]	Differential	O
AF7	FBD0SBOBN[3]	Differential	O
AF6	FBD0SBOBN[4]	Differential	O
AC4	FBD0SBOBN[5]	Differential	O
AB3	FBD0SBOBN[6]	Differential	O
AD6	FBD0SBOBN[7]	Differential	O
AA2	FBD0SBOBN[8]	Differential	O
AD7	FBD0SBOBN[9]	Differential	O
Y3	FBD0SBOBN[10]	Differential	O
AK9	FBD0SBOBP[0]	Differential	O
AK7	FBD0SBOBP[1]	Differential	O
AH7	FBD0SBOBP[2]	Differential	O
AF8	FBD0SBOBP[3]	Differential	O
AG6	FBD0SBOBP[4]	Differential	O

Table 3-1. Pin List by Pin Name (Sheet 15 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AD4	FBD0SBOBP[5]	Differential	O
AC3	FBD0SBOBP[6]	Differential	O
AD5	FBD0SBOBP[7]	Differential	O
AA3	FBD0SBOBP[8]	Differential	O
AE7	FBD0SBOBP[9]	Differential	O
Y4	FBD0SBOBP[10]	Differential	O
R2	FBD0SBOCLKAN0	Differential	O
R3	FBD0SBOCLKAP0	Differential	O
AE5	FBD0SBOCLKBN0	Differential	O
AF5	FBD0SBOCLKBP0	Differential	O
L8	FBD1NBICLKCN0	Differential	I
M8	FBD1NBICLKCP0	Differential	I
R7	FBD1NBICLKDN0	Differential	I
P7	FBD1NBICLKDP0	Differential	I
V9	FBD1NBICN[0]	Differential	I
V7	FBD1NBICN[1]	Differential	I
T8	FBD1NBICN[2]	Differential	I
U10	FBD1NBICN[3]	Differential	I
R9	FBD1NBICN[4]	Differential	I
P9	FBD1NBICN[5]	Differential	I
K9	FBD1NBICN[6]	Differential	I
J11	FBD1NBICN[7]	Differential	I
G11	FBD1NBICN[8]	Differential	I
G8	FBD1NBICN[9]	Differential	I
H9	FBD1NBICN[10]	Differential	I
F11	FBD1NBICN[11]	Differential	I
L12	FBD1NBICN[12]	Differential	I
M9	FBD1NBICN[13]	Differential	I
Y8	FBD1NBICN[14]	Differential	I
W9	FBD1NBICP[0]	Differential	I
V8	FBD1NBICP[1]	Differential	I
U8	FBD1NBICP[2]	Differential	I
U9	FBD1NBICP[3]	Differential	I
R8	FBD1NBICP[4]	Differential	I
N9	FBD1NBICP[5]	Differential	I
K8	FBD1NBICP[6]	Differential	I
J10	FBD1NBICP[7]	Differential	I
H11	FBD1NBICP[8]	Differential	I
H8	FBD1NBICP[9]	Differential	I
J9	FBD1NBICP[10]	Differential	I

Table 3-1. Pin List by Pin Name (Sheet 16 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
F10	FBD1NBICP[11]	Differential	I
L11	FBD1NBICP[12]	Differential	I
M10	FBD1NBICP[13]	Differential	I
Y9	FBD1NBICP[14]	Differential	I
AB6	FBD1NBIDN[0]	Differential	I
AA6	FBD1NBIDN[1]	Differential	I
W7	FBD1NBIDN[2]	Differential	I
W6	FBD1NBIDN[3]	Differential	I
U5	FBD1NBIDN[4]	Differential	I
T7	FBD1NBIDN[5]	Differential	I
M6	FBD1NBIDN[6]	Differential	I
M5	FBD1NBIDN[7]	Differential	I
N8	FBD1NBIDN[8]	Differential	I
K4	FBD1NBIDN[9]	Differential	I
L7	FBD1NBIDN[10]	Differential	I
J7	FBD1NBIDN[11]	Differential	I
P5	FBD1NBIDN[12]	Differential	I
R5	FBD1NBIDN[13]	Differential	I
AC8	FBD1NBIDN[14]	Differential	I
AB5	FBD1NBIDP[0]	Differential	I
AA7	FBD1NBIDP[1]	Differential	I
Y7	FBD1NBIDP[2]	Differential	I
V6	FBD1NBIDP[3]	Differential	I
U6	FBD1NBIDP[4]	Differential	I
T6	FBD1NBIDP[5]	Differential	I
N6	FBD1NBIDP[6]	Differential	I
L5	FBD1NBIDP[7]	Differential	I
N7	FBD1NBIDP[8]	Differential	I
K5	FBD1NBIDP[9]	Differential	I
L6	FBD1NBIDP[10]	Differential	I
K7	FBD1NBIDP[11]	Differential	I
P6	FBD1NBIDP[12]	Differential	I
T5	FBD1NBIDP[13]	Differential	I
AB8	FBD1NBIDP[14]	Differential	I
AD9	FBD1REFSYSCLKN	Differential	I
AC9	FBD1REFSYSCLKP	Differential	I
A8	FBD1SBOCLKCN0	Differential	O
A7	FBD1SBOCLKCP0	Differential	O
E4	FBD1SBOCLKDN0	Differential	O
E3	FBD1SBOCLKDP0	Differential	O

Table 3-1. Pin List by Pin Name (Sheet 17 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
D12	FBD1SBOCN[0]	Differential	O
E8	FBD1SBOCN[1]	Differential	O
E7	FBD1SBOCN[2]	Differential	O
C9	FBD1SBOCN[3]	Differential	O
C8	FBD1SBOCN[4]	Differential	O
B10	FBD1SBOCN[5]	Differential	O
C11	FBD1SBOCN[6]	Differential	O
A12	FBD1SBOCN[7]	Differential	O
C13	FBD1SBOCN[8]	Differential	O
B9	FBD1SBOCN[9]	Differential	O
B13	FBD1SBOCN[10]	Differential	O
D11	FBD1SBOCP[0]	Differential	O
E9	FBD1SBOCP[1]	Differential	O
D7	FBD1SBOCP[2]	Differential	O
D9	FBD1SBOCP[3]	Differential	O
C7	FBD1SBOCP[4]	Differential	O
A10	FBD1SBOCP[5]	Differential	O
B11	FBD1SBOCP[6]	Differential	O
A11	FBD1SBOCP[7]	Differential	O
C12	FBD1SBOCP[8]	Differential	O
B8	FBD1SBOCP[9]	Differential	O
A13	FBD1SBOCP[10]	Differential	O
H1	FBD1SBODN[0]	Differential	O
G3	FBD1SBODN[1]	Differential	O
G4	FBD1SBODN[2]	Differential	O
F2	FBD1SBODN[3]	Differential	O
D2	FBD1SBODN[4]	Differential	O
C4	FBD1SBODN[5]	Differential	O
B6	FBD1SBODN[6]	Differential	O
D5	FBD1SBODN[7]	Differential	O
F7	FBD1SBODN[8]	Differential	O
B4	FBD1SBODN[9]	Differential	O
G6	FBD1SBODN[10]	Differential	O
H2	FBD1SBODP[0]	Differential	O
H3	FBD1SBODP[1]	Differential	O
G5	FBD1SBODP[2]	Differential	O
F3	FBD1SBODP[3]	Differential	O
E2	FBD1SBODP[4]	Differential	O
D4	FBD1SBODP[5]	Differential	O
C6	FBD1SBODP[6]	Differential	O

Table 3-1. Pin List by Pin Name (Sheet 18 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
D6	FBD1SBODP[7]	Differential	O
F6	FBD1SBODP[8]	Differential	O
B5	FBD1SBODP[9]	Differential	O
H6	FBD1SBODP[10]	Differential	O
N28	FLASHROM_CFG[0]		I
M28	FLASHROM_CFG[1]		I
L28	FLASHROM_CFG[2]		I
N27	FLASHROM_CLK		O
L30	FLASHROM_CS[0]_N		O
P29	FLASHROM_CS[1]_N		O
R29	FLASHROM_CS[2]_N		O
N29	FLASHROM_CS[3]_N		O
T28	FLASHROM_DATI		I
R28	FLASHROM_DATO		O
L27	FLASHROM_WP_N		I
K10	FORCEPR_N		I
M11	LRGSCLSYS		I
K12	MEM_THROTTLE_L		I
AJ25	PIR_A0	Power/Other	I
AJ24	PIR_A1	Power/Other	I
AG24	PIR_SCL	Power/Other	I
AH24	PIR_SDA	Power/Other	I/O
AF11	PRBMODE_RDY_N		O
AF12	PRBMODE_REQST_N		I
L10	PROCHOT_N		O
AP1	PROCTYPE		I
AR9	PWRGOOD		I
V12	RESET_N	Power/Other	I
AD12	RSVD		I
A1	RSVD		
A2	RSVD		
A35	RSVD		
A37	RSVD		
A38	RSVD		
A4	RSVD		
AA11	RSVD		
AA27	RSVD		
AC12	RSVD		
AC27	RSVD		
AC28	RSVD		

Table 3-1. Pin List by Pin Name (Sheet 19 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AC29	RSVD		
AD27	RSVD		
AD29	RSVD		
AD30	RSVD		
AE12	RSVD		
AE27	RSVD		
AE30	RSVD		
AG21	RSVD		
AH21	RSVD		
AK12	RSVD		
AL31	RSVD		
AL8	RSVD		
AM11	RSVD		
AM38	RSVD		
AN11	RSVD		
AN38	RSVD		
AP27	RSVD		
AR1	RSVD		
AR38	RSVD		
AT2	RSVD		
AT37	RSVD		
AT38	RSVD		
AU1	RSVD		
AU2	RSVD		
AU3	RSVD		
AU36	RSVD		
AU37	RSVD		
AV1	RSVD		
AV2	RSVD		
AV35	RSVD		
AV37	RSVD		
AV38	RSVD		
AV4	RSVD		
B2	RSVD		
B3	RSVD		
B36	RSVD		
B37	RSVD		
B38	RSVD		
C1	RSVD		
C2	RSVD		

Table 3-1. Pin List by Pin Name (Sheet 20 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
C37	RSVD		
D1	RSVD		
D38	RSVD		
F1	RSVD		
F38	RSVD		
G1	RSVD		
G38	RSVD		
H13	RSVD		
J20	RSVD		
L13	RSVD		
M13	RSVD		
M20	RSVD		
M21	RSVD		
M36	RSVD		
M4	RSVD		
P10	RSVD (Intel® Itanium® Processor 9300 Series) SVID_CLK2 (Intel® Itanium® Processor 9500 Series)		
P27	RSVD		
R10	RSVD (Intel® Itanium® Processor 9300 Series) SVID_DATIO (Intel® Itanium® Processor 9500 Series)		
R27	RSVD		
T11	RSVD (Intel® Itanium® Processor 9300 Series) SVID_ALERT_N2 (Intel® Itanium® Processor 9500 Series)		
U4	RSVD		
V27	RSVD		
V29	RSVD		
W10	RSVD		
W12	RSVD		
W27	RSVD		
Y10	RSVD		
AG29	SKTID[0]		I
AH28	SKTID[1]		I
AG28	SKTID[2]		I
AE28	SM_WP		I
AT32	SMBCLK	SMBus	I/O
AR32	SMBDAT	SMBus	I/O

Table 3-1. Pin List by Pin Name (Sheet 21 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AT30	SPDCLK		I/O
AT31	SPDDAT		I/O
Y12	SYSCLK	Differential	I
AA12	SYSCLK_N	Differential	I
V11	SYSUTST_REFCLK	Differential	I
U11	SYSUTST_REFCLK_N	Differential	I
P11	TCK		I
P12	TDI		I
N12	TDO		O
Y28	TESTHI[1]		I
W29	TESTHI[2]		I
V28	TESTHI[4]		I
A5	THERMALERT_N		O
A6	THERMTRIP_N		O
R12	TMS		I
AL11	TRIGGER[0]_N		I/O
AP11	TRIGGER[1]_N		I/O
N11	TRST_N		I
AV6	VCC33_SM	Power/Other	
AV7	VCC33_SM	Power/Other	
A27	VCCA	Power/Other	
A28	VCCA	Power/Other	
A31	VCCA	Power/Other	
A32	VCCA	Power/Other	
AV21	VCCA	Power/Other	
AV22	VCCA	Power/Other	
AV26	VCCA	Power/Other	
AV27	VCCA	Power/Other	
AA37	VCCIO	Power/Other	
AB28	VCCIO	Power/Other	
AB30	VCCIO	Power/Other	
AB36	VCCIO	Power/Other	
AD11	VCCIO	Power/Other	
AD31	VCCIO	Power/Other	
AE29	VCCIO	Power/Other	
AF10	VCCIO	Power/Other	
AF27	VCCIO	Power/Other	
AG14	VCCIO	Power/Other	
AG18	VCCIO	Power/Other	
AG25	VCCIO	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 22 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AG35	VCCIO	Power/Other	
AH12	VCCIO	Power/Other	
AH22	VCCIO	Power/Other	
AH27	VCCIO	Power/Other	
AK13	VCCIO	Power/Other	
AK17	VCCIO	Power/Other	
AK23	VCCIO	Power/Other	
AL15	VCCIO	Power/Other	
AL25	VCCIO	Power/Other	
AL35	VCCIO	Power/Other	
AM14	VCCIO	Power/Other	
AM19	VCCIO	Power/Other	
AM29	VCCIO	Power/Other	
AM33	VCCIO	Power/Other	
AN12	VCCIO	Power/Other	
AP20	VCCIO	Power/Other	
AP24	VCCIO	Power/Other	
AP34	VCCIO	Power/Other	
AR12	VCCIO	Power/Other	
AR23	VCCIO	Power/Other	
AR28	VCCIO	Power/Other	
AR30	VCCIO	Power/Other	
AR35	VCCIO	Power/Other	
AT25	VCCIO	Power/Other	
AU20	VCCIO	Power/Other	
C14	VCCIO	Power/Other	
C24	VCCIO	Power/Other	
C29	VCCIO	Power/Other	
D32	VCCIO	Power/Other	
E14	VCCIO	Power/Other	
E27	VCCIO	Power/Other	
E34	VCCIO	Power/Other	
F16	VCCIO	Power/Other	
F23	VCCIO	Power/Other	
F35	VCCIO	Power/Other	
G13	VCCIO	Power/Other	
G29	VCCIO	Power/Other	
G34	VCCIO	Power/Other	
H17	VCCIO	Power/Other	
H19	VCCIO	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 23 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
H22	VCCIO	Power/Other	
H24	VCCIO	Power/Other	
H32	VCCIO	Power/Other	
J34	VCCIO	Power/Other	
K24	VCCIO	Power/Other	
K27	VCCIO	Power/Other	
K35	VCCIO	Power/Other	
L15	VCCIO	Power/Other	
M18	VCCIO	Power/Other	
M23	VCCIO	Power/Other	
M26	VCCIO	Power/Other	
N36	VCCIO	Power/Other	
T27	VCCIO	Power/Other	
T35	VCCIO	Power/Other	
U28	VCCIO	Power/Other	
W35	VCCIO	Power/Other	
Y27	VCCIO	Power/Other	
Y30	VCCIO	Power/Other	
Y33	VCCIO	Power/Other	
AA1	VCCIO_FBD	Power/Other	
AA8	VCCIO_FBD	Power/Other	
AB4	VCCIO_FBD	Power/Other	
AB9	VCCIO_FBD	Power/Other	
AC2	VCCIO_FBD	Power/Other	
AC6	VCCIO_FBD	Power/Other	
AE4	VCCIO_FBD	Power/Other	
AE8	VCCIO_FBD	Power/Other	
AG4	VCCIO_FBD	Power/Other	
AJ1	VCCIO_FBD	Power/Other	
AJ5	VCCIO_FBD	Power/Other	
AM4	VCCIO_FBD	Power/Other	
AN7	VCCIO_FBD	Power/Other	
AP10	VCCIO_FBD	Power/Other	
AP5	VCCIO_FBD	Power/Other	
AR8	VCCIO_FBD	Power/Other	
AT7	VCCIO_FBD	Power/Other	
E10	VCCIO_FBD	Power/Other	
E12	VCCIO_FBD	Power/Other	
E5	VCCIO_FBD	Power/Other	
F8	VCCIO_FBD	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 24 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
H7	VCCIO_FBD	Power/Other	
J1	VCCIO_FBD	Power/Other	
J4	VCCIO_FBD	Power/Other	
N4	VCCIO_FBD	Power/Other	
T10	VCCIO_FBD	Power/Other	
T3	VCCIO_FBD	Power/Other	
W5	VCCIO_FBD	Power/Other	
Y2	VCCIO_FBD	Power/Other	
T12	VFUSERM		I
AN1	VR_FAN_N		O
K38	VR_THERMALERT_N		O
H38	VR_THERMTRIP_N		O
AL38	VROUTPUT_ENABLE0		I
AM1	VRPWRGD (Intel® Itanium® Processor 9300 Series) VR_READY2 (Intel® Itanium® Processor 9500 Series)		O
A14	VSS	Power/Other	
A16	VSS	Power/Other	
A19	VSS	Power/Other	
A24	VSS	Power/Other	
A29	VSS	Power/Other	
A3	VSS	Power/Other	
A34	VSS	Power/Other	
A36	VSS	Power/Other	
A9	VSS	Power/Other	
AA10	VSS	Power/Other	
AA28	VSS	Power/Other	
AA29	VSS	Power/Other	
AA30	VSS	Power/Other	
AA34	VSS	Power/Other	
AA4	VSS	Power/Other	
AA5	VSS	Power/Other	
AA9	VSS	Power/Other	
AB10	VSS	Power/Other	
AB11	VSS	Power/Other	
AB12	VSS	Power/Other	
AB2	VSS	Power/Other	
AB27	VSS	Power/Other	
AB29	VSS	Power/Other	
AB32	VSS	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 25 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AB37	VSS	Power/Other	
AB7	VSS	Power/Other	
AC10	VSS	Power/Other	
AC11	VSS	Power/Other	
AC30	VSS	Power/Other	
AC35	VSS	Power/Other	
AC36	VSS	Power/Other	
AC5	VSS	Power/Other	
AC7	VSS	Power/Other	
AD10	VSS	Power/Other	
AD28	VSS	Power/Other	
AD3	VSS	Power/Other	
AD33	VSS	Power/Other	
AD35	VSS	Power/Other	
AD38	VSS	Power/Other	
AD8	VSS	Power/Other	
AE1	VSS	Power/Other	
AE10	VSS	Power/Other	
AE11	VSS	Power/Other	
AE31	VSS	Power/Other	
AE36	VSS	Power/Other	
AE6	VSS	Power/Other	
AE9	VSS	Power/Other	
AF28	VSS	Power/Other	
AF29	VSS	Power/Other	
AF34	VSS	Power/Other	
AF35	VSS	Power/Other	
AF4	VSS	Power/Other	
AF9	VSS	Power/Other	
AG12	VSS	Power/Other	
AG15	VSS	Power/Other	
AG17	VSS	Power/Other	
AG2	VSS	Power/Other	
AG22	VSS	Power/Other	
AG23	VSS	Power/Other	
AG26	VSS	Power/Other	
AG27	VSS	Power/Other	
AG32	VSS	Power/Other	
AG37	VSS	Power/Other	
AG5	VSS	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 26 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AG7	VSS	Power/Other	
AH10	VSS	Power/Other	
AH15	VSS	Power/Other	
AH18	VSS	Power/Other	
AH20	VSS	Power/Other	
AH23	VSS	Power/Other	
AH25	VSS	Power/Other	
AH26	VSS	Power/Other	
AH30	VSS	Power/Other	
AH35	VSS	Power/Other	
AH5	VSS	Power/Other	
AJ12	VSS	Power/Other	
AJ13	VSS	Power/Other	
AJ16	VSS	Power/Other	
AJ18	VSS	Power/Other	
AJ23	VSS	Power/Other	
AJ26	VSS	Power/Other	
AJ28	VSS	Power/Other	
AJ3	VSS	Power/Other	
AJ33	VSS	Power/Other	
AJ35	VSS	Power/Other	
AJ38	VSS	Power/Other	
AJ6	VSS	Power/Other	
AJ8	VSS	Power/Other	
AK1	VSS	Power/Other	
AK11	VSS	Power/Other	
AK14	VSS	Power/Other	
AK16	VSS	Power/Other	
AK21	VSS	Power/Other	
AK24	VSS	Power/Other	
AK25	VSS	Power/Other	
AK26	VSS	Power/Other	
AK30	VSS	Power/Other	
AK31	VSS	Power/Other	
AK35	VSS	Power/Other	
AK36	VSS	Power/Other	
AK6	VSS	Power/Other	
AL14	VSS	Power/Other	
AL18	VSS	Power/Other	
AL19	VSS	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 27 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AL24	VSS	Power/Other	
AL29	VSS	Power/Other	
AL34	VSS	Power/Other	
AL4	VSS	Power/Other	
AL9	VSS	Power/Other	
AM12	VSS	Power/Other	
AM17	VSS	Power/Other	
AM2	VSS	Power/Other	
AM22	VSS	Power/Other	
AM27	VSS	Power/Other	
AM32	VSS	Power/Other	
AM34	VSS	Power/Other	
AM37	VSS	Power/Other	
AM7	VSS	Power/Other	
AN10	VSS	Power/Other	
AN15	VSS	Power/Other	
AN20	VSS	Power/Other	
AN25	VSS	Power/Other	
AN30	VSS	Power/Other	
AN35	VSS	Power/Other	
AN5	VSS	Power/Other	
AN8	VSS	Power/Other	
AP12	VSS	Power/Other	
AP13	VSS	Power/Other	
AP18	VSS	Power/Other	
AP22	VSS	Power/Other	
AP23	VSS	Power/Other	
AP28	VSS	Power/Other	
AP3	VSS	Power/Other	
AP33	VSS	Power/Other	
AP38	VSS	Power/Other	
AP8	VSS	Power/Other	
AR11	VSS	Power/Other	
AR16	VSS	Power/Other	
AR21	VSS	Power/Other	
AR24	VSS	Power/Other	
AR26	VSS	Power/Other	
AR29	VSS	Power/Other	
AR31	VSS	Power/Other	
AR36	VSS	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 28 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AR6	VSS	Power/Other	
AT1	VSS	Power/Other	
AT12	VSS	Power/Other	
AT14	VSS	Power/Other	
AT19	VSS	Power/Other	
AT24	VSS	Power/Other	
AT29	VSS	Power/Other	
AT34	VSS	Power/Other	
AT4	VSS	Power/Other	
AT9	VSS	Power/Other	
AU12	VSS	Power/Other	
AU17	VSS	Power/Other	
AU22	VSS	Power/Other	
AU27	VSS	Power/Other	
AU32	VSS	Power/Other	
AU38	VSS	Power/Other	
AU7	VSS	Power/Other	
AV10	VSS	Power/Other	
AV13	VSS	Power/Other	
AV15	VSS	Power/Other	
AV18	VSS	Power/Other	
AV20	VSS	Power/Other	
AV25	VSS	Power/Other	
AV3	VSS	Power/Other	
AV30	VSS	Power/Other	
AV36	VSS	Power/Other	
AV5	VSS	Power/Other	
B1	VSS	Power/Other	
B12	VSS	Power/Other	
B14	VSS	Power/Other	
B17	VSS	Power/Other	
B22	VSS	Power/Other	
B27	VSS	Power/Other	
B32	VSS	Power/Other	
B7	VSS	Power/Other	
C10	VSS	Power/Other	
C15	VSS	Power/Other	
C20	VSS	Power/Other	
C25	VSS	Power/Other	
C30	VSS	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 29 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
C35	VSS	Power/Other	
C38	VSS	Power/Other	
C5	VSS	Power/Other	
D10	VSS	Power/Other	
D13	VSS	Power/Other	
D14	VSS	Power/Other	
D18	VSS	Power/Other	
D23	VSS	Power/Other	
D25	VSS	Power/Other	
D28	VSS	Power/Other	
D3	VSS	Power/Other	
D30	VSS	Power/Other	
D31	VSS	Power/Other	
D33	VSS	Power/Other	
D8	VSS	Power/Other	
E1	VSS	Power/Other	
E11	VSS	Power/Other	
E13	VSS	Power/Other	
E15	VSS	Power/Other	
E16	VSS	Power/Other	
E21	VSS	Power/Other	
E26	VSS	Power/Other	
E28	VSS	Power/Other	
E31	VSS	Power/Other	
E36	VSS	Power/Other	
E6	VSS	Power/Other	
F12	VSS	Power/Other	
F13	VSS	Power/Other	
F14	VSS	Power/Other	
F15	VSS	Power/Other	
F19	VSS	Power/Other	
F22	VSS	Power/Other	
F24	VSS	Power/Other	
F29	VSS	Power/Other	
F34	VSS	Power/Other	
F4	VSS	Power/Other	
F5	VSS	Power/Other	
F9	VSS	Power/Other	
G12	VSS	Power/Other	
G14	VSS	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 30 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
G17	VSS	Power/Other	
G2	VSS	Power/Other	
G22	VSS	Power/Other	
G27	VSS	Power/Other	
G32	VSS	Power/Other	
G37	VSS	Power/Other	
G7	VSS	Power/Other	
H10	VSS	Power/Other	
H15	VSS	Power/Other	
H20	VSS	Power/Other	
H25	VSS	Power/Other	
H30	VSS	Power/Other	
H35	VSS	Power/Other	
H4	VSS	Power/Other	
H5	VSS	Power/Other	
J13	VSS	Power/Other	
J18	VSS	Power/Other	
J23	VSS	Power/Other	
J24	VSS	Power/Other	
J25	VSS	Power/Other	
J28	VSS	Power/Other	
J3	VSS	Power/Other	
J33	VSS	Power/Other	
J38	VSS	Power/Other	
J5	VSS	Power/Other	
J6	VSS	Power/Other	
J8	VSS	Power/Other	
K1	VSS	Power/Other	
K11	VSS	Power/Other	
K16	VSS	Power/Other	
K21	VSS	Power/Other	
K22	VSS	Power/Other	
K23	VSS	Power/Other	
K25	VSS	Power/Other	
K26	VSS	Power/Other	
K3	VSS	Power/Other	
K31	VSS	Power/Other	
K36	VSS	Power/Other	
K6	VSS	Power/Other	
L14	VSS	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 31 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
L16	VSS	Power/Other	
L17	VSS	Power/Other	
L19	VSS	Power/Other	
L23	VSS	Power/Other	
L24	VSS	Power/Other	
L25	VSS	Power/Other	
L26	VSS	Power/Other	
L29	VSS	Power/Other	
L34	VSS	Power/Other	
L35	VSS	Power/Other	
L4	VSS	Power/Other	
L9	VSS	Power/Other	
M12	VSS	Power/Other	
M16	VSS	Power/Other	
M17	VSS	Power/Other	
M19	VSS	Power/Other	
M2	VSS	Power/Other	
M22	VSS	Power/Other	
M24	VSS	Power/Other	
M25	VSS	Power/Other	
M27	VSS	Power/Other	
M32	VSS	Power/Other	
M37	VSS	Power/Other	
M7	VSS	Power/Other	
N10	VSS	Power/Other	
N30	VSS	Power/Other	
N35	VSS	Power/Other	
N5	VSS	Power/Other	
P28	VSS	Power/Other	
P3	VSS	Power/Other	
P33	VSS	Power/Other	
P35	VSS	Power/Other	
P38	VSS	Power/Other	
P4	VSS	Power/Other	
P8	VSS	Power/Other	
R1	VSS	Power/Other	
R11	VSS	Power/Other	
R31	VSS	Power/Other	
R36	VSS	Power/Other	
R4	VSS	Power/Other	

Table 3-1. Pin List by Pin Name (Sheet 32 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
R6	VSS	Power/Other	
T29	VSS	Power/Other	
T34	VSS	Power/Other	
T4	VSS	Power/Other	
T9	VSS	Power/Other	
U12	VSS	Power/Other	
U2	VSS	Power/Other	
U27	VSS	Power/Other	
U3	VSS	Power/Other	
U32	VSS	Power/Other	
U35	VSS	Power/Other	
U37	VSS	Power/Other	
U7	VSS	Power/Other	
V10	VSS	Power/Other	
V30	VSS	Power/Other	
V35	VSS	Power/Other	
V5	VSS	Power/Other	
W11	VSS	Power/Other	
W28	VSS	Power/Other	
W3	VSS	Power/Other	
W33	VSS	Power/Other	
W38	VSS	Power/Other	
W8	VSS	Power/Other	
Y1	VSS	Power/Other	
Y11	VSS	Power/Other	
Y29	VSS	Power/Other	
Y31	VSS	Power/Other	
Y36	VSS	Power/Other	
Y5	VSS	Power/Other	
Y6	VSS	Power/Other	
AJ11	XDPOCP_STRB_IN_N		I
AH11	XDPOCP_STRB_OUT_N		O
AH8	XDPOCPD[0]_N		I/O
AG8	XDPOCPD[1]_N		I/O
AJ9	XDPOCPD[2]_N		I/O
AG9	XDPOCPD[3]_N		I/O
AH9	XDPOCPD[4]_N		I/O
AG10	XDPOCPD[5]_N		I/O
AJ10	XDPOCPD[6]_N		I/O
AK10	XDPOCPD[7]_N		I/O

Table 3-1. Pin List by Pin Name (Sheet 33 of 33)

Pin Number	Pin Name	Signal Buffer Type	Direction
AG11	XDPOCPFRAME_N		I/O

3.1.2 Pin Listing by Pin Number

Table 3-2. Pin List by Pin Number (Sheet 1 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
A1	RSVD		
A2	RSVD		
A3	VSS	Power/Other	
A4	RSVD		
A5	THERMALERT_N		O
A6	THERMTRIP_N		O
A7	FBD1SBOCLKCP0	Differential	O
A8	FBD1SBOCLKCN0	Differential	O
A9	VSS	Power/Other	
A10	FBD1SBOCP[5]	Differential	O
A11	FBD1SBOCP[7]	Differential	O
A12	FBD1SBOCN[7]	Differential	O
A13	FBD1SBOCP[10]	Differential	O
A14	VSS	Power/Other	
A15	CSI4RPDAT[0]	Differential	I
A16	VSS	Power/Other	
A17	CSI4RNDAT[3]	Differential	I
A18	CSI4RPDAT[3]	Differential	I
A19	VSS	Power/Other	
A20	CSI2RPDAT[8]	Differential	I
A21	CSI2RNCLK	Differential	I
A22	CSI2RPCLK	Differential	I
A23	CSI2RPDAT[10]	Differential	I
A24	VSS	Power/Other	
A25	CSI2RNDAT[13]	Differential	I
A26	CSI2RPDAT[13]	Differential	I
A27	VCCA	Power/Other	
A28	VCCA	Power/Other	
A29	VSS	Power/Other	
A30	CSI2RPDAT[17]	Differential	I
A31	VCCA	Power/Other	
A32	VCCA	Power/Other	
A33	CSI0RPDAT[0]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 2 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
A34	VSS	Power/Other	
A35	RSVD		
A36	VSS	Power/Other	
A37	RSVD		
A38	RSVD		
AA1	VCCIO_FBD	Power/Other	
AA2	FBD0SBOBN[8]	Differential	O
AA3	FBD0SBOBP[8]	Differential	O
AA4	VSS	Power/Other	
AA5	VSS	Power/Other	
AA6	FBD1NBIDN[1]	Differential	I
AA7	FBD1NBIDP[1]	Differential	I
AA8	VCCIO_FBD	Power/Other	
AA9	VSS	Power/Other	
AA10	VSS	Power/Other	
AA11	RSVD		
AA12	SYSCLK_N	Differential	I
AA27	RSVD		
AA28	VSS	Power/Other	
AA29	VSS	Power/Other	
AA30	VSS	Power/Other	
AA31	CSI3TNDAT[18]	Differential	O
AA32	CSI3TNDAT[19]	Differential	O
AA33	CSI3TPDAT[19]	Differential	O
AA34	VSS	Power/Other	
AA35	CSI1TNDAT[18]	Differential	O
AA36	CSI1TPDAT[18]	Differential	O
AA37	VCCIO	Power/Other	
AA38	CSI1RNDAT[18]	Differential	I
AB1	FBD0NBIBN[11]	Differential	I
AB2	VSS	Power/Other	
AB3	FBD0SBOBN[6]	Differential	O
AB4	VCCIO_FBD	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 3 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AB5	FBD1NBIDP[0]	Differential	I
AB6	FBD1NBIDN[0]	Differential	I
AB7	VSS	Power/Other	
AB8	FBD1NBIDP[14]	Differential	I
AB9	VCCIO_FBD	Power/Other	
AB10	VSS	Power/Other	
AB11	VSS	Power/Other	
AB12	VSS	Power/Other	
AB27	VSS	Power/Other	
AB28	VCCIO	Power/Other	
AB29	VSS	Power/Other	
AB30	VCCIO	Power/Other	
AB31	CSI3TPDAT[18]	Differential	O
AB32	VSS	Power/Other	
AB33	CSI3TNDAT[17]	Differential	O
AB34	CSI1TNDAT[17]	Differential	O
AB35	CSI1TPDAT[17]	Differential	O
AB36	VCCIO	Power/Other	
AB37	VSS	Power/Other	
AB38	CSI1RPDAT[18]	Differential	I
AC1	FBD0NBIBP[11]	Differential	I
AC2	VCCIO_FBD	Power/Other	
AC3	FBD0SBOBP[6]	Differential	O
AC4	FBD0SBOBN[5]	Differential	O
AC5	VSS	Power/Other	
AC6	VCCIO_FBD	Power/Other	
AC7	VSS	Power/Other	
AC8	FBD1NBIDN[14]	Differential	I
AC9	FBD1REFSYSCLKP	Differential	I
AC10	VSS	Power/Other	
AC11	VSS	Power/Other	
AC12	RSVD		
AC27	RSVD		
AC28	RSVD		
AC29	RSVD		
AC30	VSS	Power/Other	
AC31	CSI3TNDAT[16]	Differential	O
AC32	CSI3TPDAT[16]	Differential	O
AC33	CSI3TPDAT[17]	Differential	O
AC34	CSI1TNDAT[16]	Differential	O

Table 3-2. Pin List by Pin Number (Sheet 4 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AC35	VSS	Power/Other	
AC36	VSS	Power/Other	
AC37	CSI1RNDAT[17]	Differential	I
AC38	CSI1RPDAT[17]	Differential	I
AD1	FBD0NBIBN[10]	Differential	I
AD2	FBD0NBIBP[10]	Differential	I
AD3	VSS	Power/Other	
AD4	FBD0SBOBP[5]	Differential	O
AD5	FBD0SBOBP[7]	Differential	O
AD6	FBD0SBOBN[7]	Differential	O
AD7	FBD0SBOBN[9]	Differential	O
AD8	VSS	Power/Other	
AD9	FBD1REFSYSCLKN	Differential	I
AD10	VSS	Power/Other	
AD11	VCCIO	Power/Other	
AD12	RSVD		
AD27	RSVD		
AD28	VSS	Power/Other	
AD29	RSVD		
AD30	RSVD		
AD31	VCCIO	Power/Other	
AD32	CSI3TNDAT[15]	Differential	O
AD33	VSS	Power/Other	
AD34	CSI1TPDAT[16]	Differential	O
AD35	VSS	Power/Other	
AD36	CSI1RNDAT[16]	Differential	I
AD37	CSI1RPDAT[16]	Differential	I
AD38	VSS	Power/Other	
AE1	VSS	Power/Other	
AE2	FBD0NBIBP[9]	Differential	I
AE3	FBD0NBIBN[9]	Differential	I
AE4	VCCIO_FBD	Power/Other	
AE5	FBD0SBOCLKBN0	Differential	O
AE6	VSS	Power/Other	
AE7	FBD0SBOBP[9]	Differential	O
AE8	VCCIO_FBD	Power/Other	
AE9	VSS	Power/Other	
AE10	VSS	Power/Other	
AE11	VSS	Power/Other	
AE12	RSVD		

Table 3-2. Pin List by Pin Number (Sheet 5 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AE27	RSVD		
AE28	SM_WP		I
AE29	VCCIO	Power/Other	
AE30	RSVD		
AE31	VSS	Power/Other	
AE32	CSI3TPDAT[15]	Differential	O
AE33	CSI1TNDAT[14]	Differential	O
AE34	CSI1TNDAT[15]	Differential	O
AE35	CSI1TPDAT[15]	Differential	O
AE36	VSS	Power/Other	
AE37	CSI1RNDAT[15]	Differential	I
AE38	CSI1RPDAT[15]	Differential	I
AF1	FBD0NBIBP[8]	Differential	I
AF2	FBD0NBIBN[8]	Differential	I
AF3	FBD0NBIBN[7]	Differential	I
AF4	VSS	Power/Other	
AF5	FBD0SBOCLKBP0	Differential	O
AF6	FBD0SBOBN[4]	Differential	O
AF7	FBD0SBOBN[3]	Differential	O
AF8	FBD0SBOBP[3]	Differential	O
AF9	VSS	Power/Other	
AF10	VCCIO	Power/Other	
AF11	PRBMODE_RDY_N		O
AF12	PRBMODE_REQST_N		I
AF27	VCCIO	Power/Other	
AF28	VSS	Power/Other	
AF29	VSS	Power/Other	
AF30	CSI3TNDAT[13]	Differential	O
AF31	CSI3TNDAT[14]	Differential	O
AF32	CSI3TPDAT[14]	Differential	O
AF33	CSI1TPDAT[14]	Differential	O
AF34	VSS	Power/Other	
AF35	VSS	Power/Other	
AF36	CSI1RNDAT[14]	Differential	I
AF37	CSI1RPDAT[14]	Differential	I
AF38	CSI1RNDAT[13]	Differential	I
AG1	FBD0NBIBN[6]	Differential	I
AG2	VSS	Power/Other	
AG3	FBD0NBIBP[7]	Differential	I
AG4	VCCIO_FBD	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 6 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AG5	VSS	Power/Other	
AG6	FBD0SBOBP[4]	Differential	O
AG7	VSS	Power/Other	
AG8	XDPOCPD[1]_N		I/O
AG9	XDPOCPD[3]_N		I/O
AG10	XDPOCPD[5]_N		I/O
AG11	XDPOCPFRAME_N		I/O
AG12	VSS	Power/Other	
AG13	CSI5TNDAT[0]	Differential	O
AG14	VCCIO	Power/Other	
AG15	VSS	Power/Other	
AG16	CSI5TNDAT[3]	Differential	O
AG17	VSS	Power/Other	
AG18	VCCIO	Power/Other	
AG19	CSI5TNDAT[7]	Differential	O
AG20	CSI5TPDAT[7]	Differential	O
AG21	RSVD		
AG22	VSS	Power/Other	
AG23	VSS	Power/Other	
AG24	PIR_SCL	Power/Other	I
AG25	VCCIO	Power/Other	
AG26	VSS	Power/Other	
AG27	VSS	Power/Other	
AG28	SKTID[2]		I
AG29	SKTID[0]		I
AG30	CSI3TPDAT[13]	Differential	O
AG31	CSI3TNDAT[12]	Differential	O
AG32	VSS	Power/Other	
AG33	CSI1TNDAT[13]	Differential	O
AG34	CSI1TPDAT[13]	Differential	O
AG35	VCCIO	Power/Other	
AG36	CSI1RNDAT[12]	Differential	I
AG37	VSS	Power/Other	
AG38	CSI1RPDAT[13]	Differential	I
AH1	FBD0NBIBP[6]	Differential	I
AH2	FBD0NBIBN[12]	Differential	I
AH3	FBD0NBICLKBN0	Differential	I
AH4	FBD0NBICLKBP0	Differential	I
AH5	VSS	Power/Other	
AH6	FBD0SBOBN[2]	Differential	O

Table 3-2. Pin List by Pin Number (Sheet 7 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AH7	FBD0SBOBP[2]	Differential	O
AH8	XDPOCPD[0]_N		I/O
AH9	XDPOCPD[4]_N		I/O
AH10	VSS	Power/Other	
AH11	XDPOCP_STRB_OUT_N		O
AH12	VCCIO	Power/Other	
AH13	CSI5TPDAT[0]	Differential	O
AH14	CSI5TNDAT[1]	Differential	O
AH15	VSS	Power/Other	
AH16	CSI5TPDAT[3]	Differential	O
AH17	CSI5TNDAT[4]	Differential	O
AH18	VSS	Power/Other	
AH19	CSI5TNDAT[5]	Differential	O
AH20	VSS	Power/Other	
AH21	RSVD		
AH22	VCCIO	Power/Other	
AH23	VSS	Power/Other	
AH24	PIR_SDA	Power/Other	I/O
AH25	VSS	Power/Other	
AH26	VSS	Power/Other	
AH27	VCCIO	Power/Other	
AH28	SKTID[1]		I
AH29	CSI3TNDAT[10]	Differential	O
AH30	VSS	Power/Other	
AH31	CSI3TPDAT[12]	Differential	O
AH32	CSI1TNDAT[12]	Differential	O
AH33	CSI1TPDAT[12]	Differential	O
AH34	CSI1TNDAT[11]	Differential	O
AH35	VSS	Power/Other	
AH36	CSI1RPDAT[12]	Differential	I
AH37	CSI1RPDAT[11]	Differential	I
AH38	CSI1RNDAT[11]	Differential	I
AJ1	VCCIO_FBD	Power/Other	
AJ2	FBD0NBIBP[12]	Differential	I
AJ3	VSS	Power/Other	
AJ4	FBD0NBIBN[13]	Differential	I
AJ5	VCCIO_FBD	Power/Other	
AJ6	VSS	Power/Other	
AJ7	FBD0SBOBN[1]	Differential	O
AJ8	VSS	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 8 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AJ9	XDPOCPD[2]_N		I/O
AJ10	XDPOCPD[6]_N		I/O
AJ11	XDPOCP_STRB_IN_N		I
AJ12	VSS	Power/Other	
AJ13	VSS	Power/Other	
AJ14	CSI5TPDAT[1]	Differential	O
AJ15	CSI5TNDAT[2]	Differential	O
AJ16	VSS	Power/Other	
AJ17	CSI5TPDAT[4]	Differential	O
AJ18	VSS	Power/Other	
AJ19	CSI5TPDAT[5]	Differential	O
AJ20	CSI5TNDAT[8]	Differential	O
AJ21	CSI5TPDAT[8]	Differential	O
AJ22	CSI5TNCLK	Differential	O
AJ23	VSS	Power/Other	
AJ24	PIR_A1	Power/Other	I
AJ25	PIR_A0	Power/Other	I
AJ26	VSS	Power/Other	
AJ27	CSI3TNDAT[9]	Differential	O
AJ28	VSS	Power/Other	
AJ29	CSI3TPDAT[10]	Differential	O
AJ30	CSI3TNDAT[11]	Differential	O
AJ31	CSI3TPDAT[11]	Differential	O
AJ32	CSI1TNCLK	Differential	O
AJ33	VSS	Power/Other	
AJ34	CSI1TPDAT[11]	Differential	O
AJ35	VSS	Power/Other	
AJ36	CSI1RPDAT[10]	Differential	I
AJ37	CSI1RNDAT[10]	Differential	I
AJ38	VSS	Power/Other	
AK1	VSS	Power/Other	
AK2	FBD0NBIAN[11]	Differential	I
AK3	FBD0NBIAP[11]	Differential	I
AK4	FBD0NBIBP[13]	Differential	I
AK5	FBD0NBIBN[5]	Differential	I
AK6	VSS	Power/Other	
AK7	FBD0SBOBP[1]	Differential	O
AK8	FBD0SBOBN[0]	Differential	O
AK9	FBD0SBOBP[0]	Differential	O
AK10	XDPOCPD[7]_N		I/O

Table 3-2. Pin List by Pin Number (Sheet 9 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AK11	VSS	Power/Other	
AK12	RSVD		
AK13	VCCIO	Power/Other	
AK14	VSS	Power/Other	
AK15	CSI5TPDAT[2]	Differential	O
AK16	VSS	Power/Other	
AK17	VCCIO	Power/Other	
AK18	CSI5TNDAT[6]	Differential	O
AK19	CSI5TPDAT[6]	Differential	O
AK20	CSI3TPDAT[0]	Differential	O
AK21	VSS	Power/Other	
AK22	CSI5TPCLK	Differential	O
AK23	VCCIO	Power/Other	
AK24	VSS	Power/Other	
AK25	VSS	Power/Other	
AK26	VSS	Power/Other	
AK27	CSI3TPDAT[9]	Differential	O
AK28	CSI3TPCLK	Differential	O
AK29	CSI3TNCLK	Differential	O
AK30	VSS	Power/Other	
AK31	VSS	Power/Other	
AK32	CSI1TPCLK	Differential	O
AK33	CSI1TNDAT[10]	Differential	O
AK34	CSI1TPDAT[10]	Differential	O
AK35	VSS	Power/Other	
AK36	VSS	Power/Other	
AK37	CSI1RPCLK	Differential	I
AK38	CSI1RNCLK		I
AL1	FBD0NBIAN[10]	Differential	I
AL2	FBD0NBIAP[10]	Differential	I
AL3	FBD0NBIAN[9]	Differential	I
AL4	VSS	Power/Other	
AL5	FBD0NBIBP[5]	Differential	I
AL6	FBD0REFSYSCLKN	Differential	I
AL7	FBD0REFSYSCLKP	Differential	I
AL8	RSVD		
AL9	VSS	Power/Other	
AL10	FBD0NBIBP[14]	Differential	I
AL11	TRIGGER[0]_N		I/O
AL12	CSI5RNDAT[0]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 10 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AL13	CSI5RPDAT[0]	Differential	I
AL14	VSS	Power/Other	
AL15	VCCIO	Power/Other	
AL16	CSI3RPDAT[1]	Differential	I
AL17	CSI3RNDAT[1]	Differential	I
AL18	VSS	Power/Other	
AL19	VSS	Power/Other	
AL20	CSI3TNDAT[0]	Differential	O
AL21	CSI5TNDAT[9]	Differential	O
AL22	CSI5TPDAT[9]	Differential	O
AL23	CSI3TPDAT[2]	Differential	O
AL24	VSS	Power/Other	
AL25	VCCIO	Power/Other	
AL26	CSI1TPDAT[0]	Differential	O
AL27	CSI1TNDAT[0]	Differential	O
AL28	CSI1TNDAT[2]	Differential	O
AL29	VSS	Power/Other	
AL30	CSI1TNDAT[5]	Differential	O
AL31	RSVD		
AL32	CSI1TPDAT[9]	Differential	O
AL33	CSI1TNDAT[9]	Differential	O
AL34	VSS	Power/Other	
AL35	VCCIO	Power/Other	
AL36	CSI1RPDAT[9]	Differential	I
AL37	CSI1RNDAT[9]	Differential	I
AL38	VROUTPUT_ENABLE0		I
AM1	VRPWRGD (Intel® Itanium® Processor 9300 Series) VR_READY (Intel® Itanium® Processor 9500 Series)		O
AM2	VSS	Power/Other	
AM3	FBD0NBIAP[9]	Differential	I
AM4	VCCIO_FBD	Power/Other	
AM5	FBD0NBIBN[4]	Differential	I
AM6	FBD0NBIBP[4]	Differential	I
AM7	VSS	Power/Other	
AM8	FBD0NBIBP[1]	Differential	I
AM9	FBD0NBIBN[1]	Differential	I
AM10	FBD0NBIBN[14]	Differential	I
AM11	RSVD		
AM12	VSS	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 11 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AM13	CSI5RNDAT[1]	Differential	I
AM14	VCCIO	Power/Other	
AM15	CSI3RPDAT[2]	Differential	I
AM16	CSI3RNDAT[2]	Differential	I
AM17	VSS	Power/Other	
AM18	CSI3RPDAT[0]	Differential	I
AM19	VCCIO	Power/Other	
AM20	CSI3TNDAT[1]	Differential	O
AM21	CSI3TPDAT[1]	Differential	O
AM22	VSS	Power/Other	
AM23	CSI3TNDAT[2]	Differential	O
AM24	CSI3TNDAT[5]	Differential	O
AM25	CSI3TPDAT[8]	Differential	O
AM26	CSI3TNDAT[8]	Differential	O
AM27	VSS	Power/Other	
AM28	CSI1TPDAT[2]	Differential	O
AM29	VCCIO	Power/Other	
AM30	CSI1TPDAT[5]	Differential	O
AM31	CSI1TNDAT[8]	Differential	O
AM32	VSS	Power/Other	
AM33	VCCIO	Power/Other	
AM34	VSS	Power/Other	
AM35	CSI1RPDAT[8]	Differential	I
AM36	CSI1RNDAT[8]	Differential	I
AM37	VSS	Power/Other	
AM38	RSVD		
AN1	VR_FAN_N		O
AN2	FBD0NBIAN[7]	Differential	I
AN3	FBD0NBIAN[8]	Differential	I
AN4	FBD0NBIAP[8]	Differential	I
AN5	VSS	Power/Other	
AN6	FBD0NBIBP[3]	Differential	I
AN7	VCCIO_FBD	Power/Other	
AN8	VSS	Power/Other	
AN9	FBD0NBIBN[0]	Differential	I
AN10	VSS	Power/Other	
AN11	RSVD		
AN12	VCCIO	Power/Other	
AN13	CSI5RPDAT[1]	Differential	I
AN14	CSI5RNDAT[2]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 12 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AN15	VSS	Power/Other	
AN16	CSI3RPDAT[3]	Differential	I
AN17	CSI3RNDAT[3]	Differential	I
AN18	CSI3RNDAT[0]	Differential	I
AN19	CSI3RPDAT[4]	Differential	I
AN20	VSS	Power/Other	
AN21	CSI3TNDAT[3]	Differential	O
AN22	CSI3TPDAT[4]	Differential	O
AN23	CSI3TNDAT[4]	Differential	O
AN24	CSI3TPDAT[5]	Differential	O
AN25	VSS	Power/Other	
AN26	CSI3TNDAT[7]	Differential	O
AN27	CSI1TPDAT[1]	Differential	O
AN28	CSI1TNDAT[1]	Differential	O
AN29	CSI1TNDAT[3]	Differential	O
AN30	VSS	Power/Other	
AN31	CSI1TPDAT[8]	Differential	O
AN32	CSI1TNDAT[6]	Differential	O
AN33	CSI1TPDAT[7]	Differential	O
AN34	CSI1TNDAT[7]	Differential	O
AN35	VSS	Power/Other	
AN36	CSI1RPDAT[7]	Differential	I
AN37	CSI1RNDAT[7]	Differential	I
AN38	RSVD		
AP1	PROCTYPE		I
AP2	FBD0NBIAP[7]	Differential	I
AP3	VSS	Power/Other	
AP4	FBD0NBIAN[6]	Differential	I
AP5	VCCIO_FBD	Power/Other	
AP6	FBD0NBIBN[3]	Differential	I
AP7	FBD0NBIBN[2]	Differential	I
AP8	VSS	Power/Other	
AP9	FBD0NBIBP[0]	Differential	I
AP10	VCCIO_FBD	Power/Other	
AP11	TRIGGER[1]_N		I/O
AP12	VSS	Power/Other	
AP13	VSS	Power/Other	
AP14	CSI5RPDAT[2]	Differential	I
AP15	CSI5RNDAT[3]	Differential	I
AP16	CSI5RPDAT[3]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 13 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AP17	CSI5RNCLK	Differential	I
AP18	VSS	Power/Other	
AP19	CSI3RNDAT[4]	Differential	I
AP20	VCCIO	Power/Other	
AP21	CSI3TPDAT[3]	Differential	O
AP22	VSS	Power/Other	
AP23	VSS	Power/Other	
AP24	VCCIO	Power/Other	
AP25	CSI3TNDAT[6]	Differential	O
AP26	CSI3TPDAT[7]	Differential	O
AP27	RSVD		
AP28	VSS	Power/Other	
AP29	CSI1TPDAT[3]	Differential	O
AP30	CSI1TPDAT[4]	Differential	O
AP31	CSI1TNDAT[4]	Differential	O
AP32	CSI1TPDAT[6]	Differential	O
AP33	VSS	Power/Other	
AP34	VCCIO	Power/Other	
AP35	CSI1RPDAT[5]	Differential	I
AP36	CSI1RNDAT[5]	Differential	I
AP37	CSI1RNDAT[6]	Differential	I
AP38	VSS	Power/Other	
AR1	RSVD		
AR2	FBD0NBIAN[12]	Differential	I
AR3	FBD0NBIAP[12]	Differential	I
AR4	FBD0NBIAP[6]	Differential	I
AR5	FBD0NBICLKAN0	Differential	I
AR6	VSS	Power/Other	
AR7	FBD0NBIBP[2]	Differential	I
AR8	VCCIO_FBD	Power/Other	
AR9	PWRGOOD		I
AR10	FBD0NBIAN[3]	Differential	I
AR11	VSS	Power/Other	
AR12	VCCIO	Power/Other	
AR13	CSI5RNDAT[4]	Differential	I
AR14	CSI5RPDAT[4]	Differential	I
AR15	CSI5RNDAT[7]	Differential	I
AR16	VSS	Power/Other	
AR17	CSI5RPCLK	Differential	I
AR18	CSI3RPDAT[5]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 14 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AR19	CSI3RNDAT[5]	Differential	I
AR20	CSI3RPDAT[9]	Differential	I
AR21	VSS	Power/Other	
AR22	CSI3RPDAT[10]	Differential	I
AR23	VCCIO	Power/Other	
AR24	VSS	Power/Other	
AR25	CSI3TPDAT[6]	Differential	O
AR26	VSS	Power/Other	
AR27	CSI3RPDAT[15]	Differential	I
AR28	VCCIO	Power/Other	
AR29	VSS	Power/Other	
AR30	VCCIO	Power/Other	
AR31	VSS	Power/Other	
AR32	SMBDAT	SMBus	I/O
AR33	CSI1RPDAT[3]	Differential	I
AR34	CSI1RNDAT[3]	Differential	I
AR35	VCCIO	Power/Other	
AR36	VSS	Power/Other	
AR37	CSI1RPDAT[6]	Differential	I
AR38	RSVD		
AT1	VSS	Power/Other	
AT2	RSVD		
AT3	CPU_PRES4_N		I/O
AT4	VSS	Power/Other	
AT5	FBD0NBICLKAP0	Differential	I
AT6	FBD0NBIAN[5]	Differential	I
AT7	VCCIO_FBD	Power/Other	
AT8	FBD0NBIAN[4]	Differential	I
AT9	VSS	Power/Other	
AT10	FBD0NBIAP[3]	Differential	I
AT11	FBD0NBIAN[0]	Differential	I
AT12	VSS	Power/Other	
AT13	CSI5RNDAT[5]	Differential	I
AT14	VSS	Power/Other	
AT15	CSI5RPDAT[7]	Differential	I
AT16	CSI5RNDAT[9]	Differential	I
AT17	CSI5RPDAT[9]	Differential	I
AT18	CSI3RPDAT[7]	Differential	I
AT19	VSS	Power/Other	
AT20	CSI3RNDAT[9]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 15 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AT21	CSI3RPCLK	Differential	I
AT22	CSI3RNDAT[10]	Differential	I
AT23	CSI3RPDAT[11]	Differential	I
AT24	VSS	Power/Other	
AT25	VCCIO	Power/Other	
AT26	CSI3RPDAT[14]	Differential	I
AT27	CSI3RNDAT[15]	Differential	I
AT28	CSI3RPDAT[16]	Differential	I
AT29	VSS	Power/Other	
AT30	SPDCLK		I/O
AT31	SPDDAT		I/O
AT32	SMBCLK	SMBus	I/O
AT33	CSI1RPDAT[0]	Differential	I
AT34	VSS	Power/Other	
AT35	CSI1RNDAT[4]	Differential	I
AT36	CPU_PRES3_N		I/O
AT37	RSVD		
AT38	RSVD		
AU1	RSVD		
AU2	RSVD		
AU3	RSVD		
AU4	FBD0NBIAN[13]	Differential	I
AU5	FBD0NBIAP[13]	Differential	I
AU6	FBD0NBIAP[5]	Differential	I
AU7	VSS	Power/Other	
AU8	FBD0NBIAP[4]	Differential	I
AU9	FBD0NBIAN[1]	Differential	I
AU10	FBD0NBIAP[1]	Differential	I
AU11	FBD0NBIAP[0]	Differential	I
AU12	VSS	Power/Other	
AU13	CSI5RPDAT[5]	Differential	I
AU14	CSI5RNDAT[6]	Differential	I
AU15	CSI5RNDAT[8]	Differential	I
AU16	CSI5RPDAT[8]	Differential	I
AU17	VSS	Power/Other	
AU18	CSI3RNDAT[7]	Differential	I
AU19	CSI3RPDAT[8]	Differential	I
AU20	VCCIO	Power/Other	
AU21	CSI3RNCLK	Differential	I
AU22	VSS	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 16 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AU23	CSI3RNDAT[11]	Differential	I
AU24	CSI3RPDAT[13]	Differential	I
AU25	CSI3RNDAT[13]	Differential	I
AU26	CSI3RNDAT[14]	Differential	I
AU27	VSS	Power/Other	
AU28	CSI3RNDAT[16]	Differential	I
AU29	CSI3RPDAT[18]	Differential	I
AU30	CSI3RNDAT[18]	Differential	I
AU31	CSI3RPDAT[19]	Differential	I
AU32	VSS	Power/Other	
AU33	CSI1RNDAT[0]	Differential	I
AU34	CSI1RPDAT[2]	Differential	I
AU35	CSI1RPDAT[4]	Differential	I
AU36	RSVD		
AU37	RSVD		
AU38	VSS	Power/Other	
AV1	RSVD		
AV2	RSVD		
AV3	VSS	Power/Other	
AV4	RSVD		
AV5	VSS	Power/Other	
AV6	VCC33_SM	Power/Other	
AV7	VCC33_SM	Power/Other	
AV8	FBD0NBIAN[2]	Differential	I
AV9	FBD0NBIAP[2]	Differential	I
AV10	VSS	Power/Other	
AV11	FBD0NBIAN[14]	Differential	I
AV12	FBD0NBIAP[14]	Differential	I
AV13	VSS	Power/Other	
AV14	CSI5RPDAT[6]	Differential	I
AV15	VSS	Power/Other	
AV16	CSI3RPDAT[6]	Differential	I
AV17	CSI3RNDAT[6]	Differential	I
AV18	VSS	Power/Other	
AV19	CSI3RNDAT[8]	Differential	I
AV20	VSS	Power/Other	
AV21	VCCA	Power/Other	
AV22	VCCA	Power/Other	
AV23	CSI3RPDAT[12]	Differential	I
AV24	CSI3RNDAT[12]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 17 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
AV25	VSS	Power/Other	
AV26	VCCA	Power/Other	
AV27	VCCA	Power/Other	
AV28	CSI3RPDAT[17]	Differential	I
AV29	CSI3RNDAT[17]	Differential	I
AV30	VSS	Power/Other	
AV31	CSI3RNDAT[19]	Differential	I
AV32	CSI1RPDAT[1]	Differential	I
AV33	CSI1RNDAT[1]	Differential	I
AV34	CSI1RNDAT[2]	Differential	I
AV35	RSVD		
AV36	VSS	Power/Other	
AV37	RSVD		
AV38	RSVD		
B1	VSS	Power/Other	
B2	RSVD		
B3	RSVD		
B4	FBD1SBODN[9]	Differential	O
B5	FBD1SBODP[9]	Differential	O
B6	FBD1SBODN[6]	Differential	O
B7	VSS	Power/Other	
B8	FBD1SBOCP[9]	Differential	O
B9	FBD1SBOCN[9]	Differential	O
B10	FBD1SBOCN[5]	Differential	O
B11	FBD1SBOCP[6]	Differential	O
B12	VSS	Power/Other	
B13	FBD1SBOCN[10]	Differential	O
B14	VSS	Power/Other	
B15	CSI4RNDAT[0]	Differential	I
B16	CSI4RPDAT[2]	Differential	I
B17	VSS	Power/Other	
B18	CSI4RNDAT[4]	Differential	I
B19	CSI4RPDAT[4]	Differential	I
B20	CSI2RNDAT[8]	Differential	I
B21	CSI2RPDAT[7]	Differential	I
B22	VSS	Power/Other	
B23	CSI2RNDAT[10]	Differential	I
B24	CSI2RPDAT[11]	Differential	I
B25	CSI2RNDAT[11]	Differential	I
B26	CSI2RPDAT[12]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 18 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
B27	VSS	Power/Other	
B28	CSI2RNDAT[16]	Differential	I
B29	CSI2RPDAT[16]	Differential	I
B30	CSI2RNDAT[17]	Differential	I
B31	CSI2RPDAT[18]	Differential	I
B32	VSS	Power/Other	
B33	CSI0RNDAT[0]	Differential	I
B34	CSI0RNDAT[2]	Differential	I
B35	CSI0RPDAT[2]	Differential	I
B36	RSVD		
B37	RSVD		
B38	RSVD		
C1	RSVD		
C2	RSVD		
C3	CPU_PRES1_N		I/O
C4	FBD1SBODN[5]	Differential	O
C5	VSS	Power/Other	
C6	FBD1SBODP[6]	Differential	O
C7	FBD1SBOCP[4]	Differential	O
C8	FBD1SBOCN[4]	Differential	O
C9	FBD1SBOCN[3]	Differential	O
C10	VSS	Power/Other	
C11	FBD1SBOCN[6]	Differential	O
C12	FBD1SBOCP[8]	Differential	O
C13	FBD1SBOCN[8]	Differential	O
C14	VCCIO	Power/Other	
C15	VSS	Power/Other	
C16	CSI4RNDAT[2]	Differential	I
C17	CSI4RNDAT[5]	Differential	I
C18	CSI4RPDAT[5]	Differential	I
C19	CSI4RPDAT[6]	Differential	I
C20	VSS	Power/Other	
C21	CSI2RNDAT[7]	Differential	I
C22	CSI2RNDAT[9]	Differential	I
C23	CSI2RPDAT[9]	Differential	I
C24	VCCIO	Power/Other	
C25	VSS	Power/Other	
C26	CSI2RNDAT[12]	Differential	I
C27	CSI2RNDAT[15]	Differential	I
C28	CSI2RPDAT[15]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 19 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
C29	VCCIO	Power/Other	
C30	VSS	Power/Other	
C31	CSI2RNDAT[18]	Differential	I
C32	CSI2RPDAT[19]	Differential	I
C33	CSI2RNDAT[19]	Differential	I
C34	CSI0RPDAT[1]	Differential	I
C35	VSS	Power/Other	
C36	CSI0RNDAT[4]	Differential	I
C37	RSVD		
C38	VSS	Power/Other	
D1	RSVD		
D2	FBD1SBODN[4]	Differential	O
D3	VSS	Power/Other	
D4	FBD1SBODP[5]	Differential	O
D5	FBD1SBODN[7]	Differential	O
D6	FBD1SBODP[7]	Differential	O
D7	FBD1SBOCP[2]	Differential	O
D8	VSS	Power/Other	
D9	FBD1SBOCP[3]	Differential	O
D10	VSS	Power/Other	
D11	FBD1SBOCP[0]	Differential	O
D12	FBD1SBOCN[0]	Differential	O
D13	VSS	Power/Other	
D14	VSS	Power/Other	
D15	CSI4RNDAT[1]	Differential	I
D16	CSI4RPDAT[1]	Differential	I
D17	CSI4RPDAT[7]	Differential	I
D18	VSS	Power/Other	
D19	CSI4RNDAT[6]	Differential	I
D20	CSI2RPDAT[5]	Differential	I
D21	CSI2RNDAT[6]	Differential	I
D22	CSI2RPDAT[6]	Differential	I
D23	VSS	Power/Other	
D24	CSI2TNDAT[3]	Differential	O
D25	VSS	Power/Other	
D26	CSI2RNDAT[14]	Differential	I
D27	CSI2RPDAT[14]	Differential	I
D28	VSS	Power/Other	
D29	CSI2TPDAT[6]	Differential	O
D30	VSS	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 20 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
D31	VSS	Power/Other	
D32	VCCIO	Power/Other	
D33	VSS	Power/Other	
D34	CSI0RNDAT[1]	Differential	I
D35	CSI0RNDAT[3]	Differential	I
D36	CSI0RPDAT[4]	Differential	I
D37	CPU_PRES2_N		I/O
D38	RSVD		
E1	VSS	Power/Other	
E2	FBD1SBODP[4]	Differential	O
E3	FBD1SBOCLKDP0	Differential	O
E4	FBD1SBOCLKDN0	Differential	O
E5	VCCIO_FBD	Power/Other	
E6	VSS	Power/Other	
E7	FBD1SBOCN[2]	Differential	O
E8	FBD1SBOCN[1]	Differential	O
E10	VCCIO_FBD	Power/Other	
E11	VSS	Power/Other	
E12	VCCIO_FBD	Power/Other	
E13	VSS	Power/Other	
E14	VCCIO	Power/Other	
E15	VSS	Power/Other	
E16	VSS	Power/Other	
E17	CSI4RNDAT[7]	Differential	I
E18	CSI4RNDAT[8]	Differential	I
E19	CSI4RPDAT[8]	Differential	I
E20	CSI2RNDAT[5]	Differential	I
E21	VSS	Power/Other	
E22	CSI2RPDAT[4]	Differential	I
E23	CSI2RNDAT[4]	Differential	I
E24	CSI2TPDAT[3]	Differential	O
E25	CSI2TPDAT[2]	Differential	O
E26	VSS	Power/Other	
E27	VCCIO	Power/Other	
E28	VSS	Power/Other	
E29	CSI2TNDAT[6]	Differential	O
E30	CSI0TPDAT[3]	Differential	O
E31	VSS	Power/Other	
E32	CSI0TNDAT[6]	Differential	O
E33	CSI0TPDAT[6]	Differential	O

Table 3-2. Pin List by Pin Number (Sheet 21 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
E34	VCCIO	Power/Other	
E35	CSI0RPDAT[3]	Differential	I
E36	VSS	Power/Other	
E37	CSI0RNDAT[5]	Differential	I
E38	CSI0RPDAT[5]	Differential	I
E9	FBD1SBOCP[1]	Differential	O
F1	RSVD		
F2	FBD1SBODN[3]	Differential	O
F3	FBD1SBODP[3]	Differential	O
F4	VSS	Power/Other	
F5	VSS	Power/Other	
F6	FBD1SBODP[8]	Differential	O
F7	FBD1SBODN[8]	Differential	O
F8	VCCIO_FBD	Power/Other	
F9	VSS	Power/Other	
F10	FBD1NBICP[11]	Differential	I
F11	FBD1NBICN[11]	Differential	I
F12	VSS	Power/Other	
F13	VSS	Power/Other	
F14	VSS	Power/Other	
F15	VSS	Power/Other	
F16	VCCIO	Power/Other	
F17	CSI4RNDAT[9]	Differential	I
F18	CSI4RPDAT[9]	Differential	I
F19	VSS	Power/Other	
F20	CSI2RPDAT[3]	Differential	I
F21	CSI2RNDAT[3]	Differential	I
F22	VSS	Power/Other	
F23	VCCIO	Power/Other	
F24	VSS	Power/Other	
F25	CSI2TNDAT[2]	Differential	O
F26	CSI2TNDAT[5]	Differential	O
F27	CSI2TPDAT[5]	Differential	O
F28	CSI2TNDAT[8]	Differential	O
F29	VSS	Power/Other	
F30	CSI0TNDAT[3]	Differential	O
F31	CSI0TNDAT[5]	Differential	O
F32	CSI0TPDAT[5]	Differential	O
F33	CSI0TNDAT[7]	Differential	O
F34	VSS	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 22 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
F35	VCCIO	Power/Other	
F36	CSI0RNDAT[6]	Differential	I
F37	CSI0RPDAT[6]	Differential	I
F38	RSVD		
G1	RSVD		
G2	VSS	Power/Other	
G3	FBD1SBODN[1]	Differential	O
G4	FBD1SBODN[2]	Differential	O
G5	FBD1SBODP[2]	Differential	O
G6	FBD1SBODN[10]	Differential	O
G7	VSS	Power/Other	
G8	FBD1NBICN[9]	Differential	I
G9	BOOTMODE[1]		I
G10	BOOTMODE[0]		I
G11	FBD1NBICN[8]	Differential	I
G12	VSS	Power/Other	
G13	VCCIO	Power/Other	
G14	VSS	Power/Other	
G15	CSI4TNDAT[4]	Differential	O
G16	CSI4TPDAT[4]	Differential	O
G17	VSS	Power/Other	
G18	CSI4RPCLK	Differential	I
G19	CSI2RPDAT[2]	Differential	I
G20	CSI2RNDAT[2]	Differential	I
G21	CSI2RPDAT[1]	Differential	I
G22	VSS	Power/Other	
G23	CSI2TPDAT[0]	Differential	O
G24	CSI2TNDAT[1]	Differential	O
G25	CSI2TPDAT[1]	Differential	O
G26	CSI2TPDAT[4]	Differential	O
G27	VSS	Power/Other	
G28	CSI2TPDAT[8]	Differential	O
G29	VCCIO	Power/Other	
G30	CSI0TPDAT[2]	Differential	O
G31	CSI0TNDAT[2]	Differential	O
G32	VSS	Power/Other	
G33	CSI0TPDAT[7]	Differential	O
G34	VCCIO	Power/Other	
G35	CSI0RNDAT[7]	Differential	I
G36	CSI0RPDAT[7]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 23 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
G37	VSS	Power/Other	
G38	RSVD		
H1	FBD1SBODN[0]	Differential	O
H2	FBD1SBODP[0]	Differential	O
H3	FBD1SBODP[1]	Differential	O
H4	VSS	Power/Other	
H5	VSS	Power/Other	
H6	FBD1SBODP[10]	Differential	O
H7	VCCIO_FBD	Power/Other	
H8	FBD1NBICP[9]	Differential	I
H9	FBD1NBICN[10]	Differential	I
H10	VSS	Power/Other	
H11	FBD1NBICP[8]	Differential	I
H12	ERROR[0]_N		O
H13	RSVD		
H14	CSI4TPDAT[3]	Differential	O
H15	VSS	Power/Other	
H16	CSI4TPDAT[5]	Differential	O
H17	VCCIO	Power/Other	
H18	CSI4RNCLK	Differential	I
H19	VCCIO	Power/Other	
H20	VSS	Power/Other	
H21	CSI2RNDAT[1]	Differential	I
H22	VCCIO	Power/Other	
H23	CSI2TNDAT[0]	Differential	O
H24	VCCIO	Power/Other	
H25	VSS	Power/Other	
H26	CSI2TNDAT[4]	Differential	O
H27	CSI2TNDAT[9]	Differential	O
H28	CSI2TPDAT[9]	Differential	O
H29	CSI2TNCLK	Differential	O
H30	VSS	Power/Other	
H31	CSI0TPDAT[1]	Differential	O
H32	VCCIO	Power/Other	
H33	CSI0TNDAT[8]	Differential	O
H34	CSI0TPDAT[8]	Differential	O
H35	VSS	Power/Other	
H36	CSI0RNDAT[8]	Differential	I
H37	CSI0RPDAT[8]	Differential	I
H38	VR_THERMTRIP_N		O

Table 3-2. Pin List by Pin Number (Sheet 24 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
J1	VCCIO_FBD	Power/Other	
J2	FBD0SBOAN[10]	Differential	O
J3	VSS	Power/Other	
J4	VCCIO_FBD	Power/Other	
J5	VSS	Power/Other	
J6	VSS	Power/Other	
J7	FBD1NBIDN[11]	Differential	I
J8	VSS	Power/Other	
J9	FBD1NBICP[10]	Differential	I
J10	FBD1NBICP[7]	Differential	I
J11	FBD1NBICN[7]	Differential	I
J12	ERROR[1]_N		O
J13	VSS	Power/Other	
J14	CSI4TNDAT[3]	Differential	O
J15	CSI4TPDAT[2]	Differential	O
J16	CSI4TNDAT[5]	Differential	O
J17	CSI4TPDAT[6]	Differential	O
J18	VSS	Power/Other	
J19	CSI4TPDAT[8]	Differential	O
J20	RSVD		
J21	CSI2RPDAT[0]	Differential	I
J22	CSI2RNDAT[0]	Differential	I
J23	VSS	Power/Other	
J24	VSS	Power/Other	
J25	VSS	Power/Other	
J26	CSI2TNDAT[7]	Differential	O
J27	CSI2TPDAT[7]	Differential	O
J28	VSS	Power/Other	
J29	CSI2TPCLK	Differential	O
J30	CSI0TPDAT[0]	Differential	O
J31	CSI0TNDAT[1]	Differential	O
J32	CSI0TPDAT[4]	Differential	O
J33	VSS	Power/Other	
J34	VCCIO	Power/Other	
J35	CSI0RNDAT[9]	Differential	I
J36	CSI0RPDAT[9]	Differential	I
J37	CSI0RNCLK	Differential	I
J38	VSS	Power/Other	
K1	VSS	Power/Other	
K2	FBD0SBOAP[10]	Differential	O

Table 3-2. Pin List by Pin Number (Sheet 25 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
K3	VSS	Power/Other	
K4	FBD1NBIDN[9]	Differential	I
K5	FBD1NBIDP[9]	Differential	I
K6	VSS	Power/Other	
K7	FBD1NBIDP[11]	Differential	I
K8	FBD1NBICP[6]	Differential	I
K9	FBD1NBICN[6]	Differential	I
K10	FORCEPR_N		I
K11	VSS	Power/Other	
K12	MEM_THROTTLE_L		I
K13	CSI4TNDAT[1]	Differential	O
K14	CSI4TPDAT[1]	Differential	O
K15	CSI4TNDAT[2]	Differential	O
K16	VSS	Power/Other	
K17	CSI4TNDAT[6]	Differential	O
K18	CSI4TPDAT[7]	Differential	O
K19	CSI4TNDAT[8]	Differential	O
K20	CSI4TPDAT[9]	Differential	O
K21	VSS	Power/Other	
K22	VSS	Power/Other	
K23	VSS	Power/Other	
K24	VCCIO	Power/Other	
K25	VSS	Power/Other	
K26	VSS	Power/Other	
K27	VCCIO	Power/Other	
K28	CSI2TNDAT[10]	Differential	O
K29	CSI2TPDAT[10]	Differential	O
K30	CSI0TNDAT[0]	Differential	O
K31	VSS	Power/Other	
K32	CSI0TNDAT[4]	Differential	O
K33	CSI0TNCLK	Differential	O
K34	CSI0TPCLK	Differential	O
K35	VCCIO	Power/Other	
K36	VSS	Power/Other	
K37	CSI0RPCLK	Differential	I
K38	VR_THERMALERT_N		O
L1	FBD0SBOAN[8]	Differential	O
L2	FBD0SBOAP[8]	Differential	O
L3	FBD0SBOAN[7]	Differential	O
L4	VSS	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 26 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
L5	FBD1NBIDP[7]	Differential	I
L6	FBD1NBIDP[10]	Differential	I
L7	FBD1NBIDN[10]	Differential	I
L8	FBD1NBICLKCN0	Differential	I
L9	VSS	Power/Other	
L10	PROCHOT_N		O
L11	FBD1NBICP[12]	Differential	I
L12	FBD1NBICN[12]	Differential	I
L13	RSVD		
L14	VSS	Power/Other	
L15	VCCIO	Power/Other	
L16	VSS	Power/Other	
L17	VSS	Power/Other	
L18	CSI4TNDAT[7]	Differential	O
L19	VSS	Power/Other	
L20	CSI4TNDAT[9]	Differential	O
L21	CSI4TNCLK	Differential	O
L22	CSI4TPCLK	Differential	O
L23	VSS	Power/Other	
L24	VSS	Power/Other	
L25	VSS	Power/Other	
L26	VSS	Power/Other	
L27	FLASHROM_WP_N		I
L28	FLASHROM_CFG[2]		I
L29	VSS	Power/Other	
L30	FLASHROM_CS[0]_N		O
L31	CSI0TNDAT[9]	Differential	O
L32	CSI0TPDAT[9]	Differential	O
L33	CSI0TNDAT[10]	Differential	O
L34	VSS	Power/Other	
L35	VSS	Power/Other	
L36	CSI0RNDAT[10]	Differential	I
L37	CSI0RPDAT[10]	Differential	I
L38	CSI0RNDAT[11]	Differential	I
M1	FBD0SBOAN[6]	Differential	O
M2	VSS	Power/Other	
M3	FBD0SBOAP[7]	Differential	O
M4	RSVD		
M5	FBD1NBIDN[7]	Differential	I
M6	FBD1NBIDN[6]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 27 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
M7	VSS	Power/Other	
M8	FBD1NBICLKCP0	Differential	I
M9	FBD1NBICN[13]	Differential	I
M10	FBD1NBICP[13]	Differential	I
M11	LRGSCLSYS		I
M12	VSS	Power/Other	
M13	RSVD		
M14	CSI4TNDAT[0]	Differential	O
M15	CSI4TPDAT[0]	Differential	O
M16	VSS	Power/Other	
M17	VSS	Power/Other	
M18	VCCIO	Power/Other	
M19	VSS	Power/Other	
M20	RSVD		
M21	RSVD		
M22	VSS	Power/Other	
M23	VCCIO	Power/Other	
M24	VSS	Power/Other	
M25	VSS	Power/Other	
M26	VCCIO	Power/Other	
M27	VSS	Power/Other	
M28	FLASHROM_CFG[1]		I
M29	CSI2TNDAT[11]	Differential	O
M30	CSI2TPDAT[11]	Differential	O
M31	CSI2TNDAT[13]	Differential	O
M32	VSS	Power/Other	
M33	CSI0TPDAT[10]	Differential	O
M34	CSI0TNDAT[11]	Differential	O
M35	CSI0TPDAT[11]	Differential	O
M36	RSVD		
M37	VSS	Power/Other	
M38	CSI0RPDAT[11]	Differential	I
N1	FBD0SBOAP[6]	Differential	O
N2	FBD0SBOAP[5]	Differential	O
N3	FBD0SBOAN[5]	Differential	O
N4	VCCIO_FBD	Power/Other	
N5	VSS	Power/Other	
N6	FBD1NBIDP[6]	Differential	I
N7	FBD1NBIDP[8]	Differential	I
N8	FBD1NBIDN[8]	Differential	I

Table 3-2. Pin List by Pin Number (Sheet 28 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
N9	FBD1NBICP[5]	Differential	I
N10	VSS	Power/Other	
N11	TRST_N		I
N12	TDO		O
N27	FLASHROM_CLK		O
N28	FLASHROM_CFG[0]		I
N29	FLASHROM_CS[3]_N		O
N30	VSS	Power/Other	
N31	CSI2TPDAT[13]	Differential	O
N32	CSI0TNDAT[12]	Differential	O
N33	CSI0TPDAT[12]	Differential	O
N34	CSI0TNDAT[13]	Differential	O
N35	VSS	Power/Other	
N36	VCCIO	Power/Other	
N37	CSI0RNDAT[12]	Differential	I
N38	CSI0RPDAT[12]	Differential	I
P1	FBD0SBOAN[9]	Differential	O
P2	FBD0SBOAP[9]	Differential	O
P3	VSS	Power/Other	
P4	VSS	Power/Other	
P5	FBD1NBIDN[12]	Differential	I
P6	FBD1NBIDP[12]	Differential	I
P7	FBD1NBICLKDP0	Differential	I
P8	VSS	Power/Other	
P9	FBD1NBICN[5]	Differential	I
P10	RSVD[1] (Intel® Itanium® Processor 9300 Series) SVID_CLK2[2] (Intel® Itanium® Processor 9500 Series)		
P11	TCK		I
P12	TDI		I
P27	RSVD		
P28	VSS	Power/Other	
P29	FLASHROM_CS[1]_N		O
P30	CSI2TNDAT[12]	Differential	O
P31	CSI2TPDAT[12]	Differential	O
P32	CSI2TNDAT[15]	Differential	O
P33	VSS	Power/Other	
P34	CSI0TPDAT[13]	Differential	O
P35	VSS	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 29 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
P36	CSI0RNDAT[13]	Differential	I
P37	CSI0RPDAT[13]	Differential	I
P38	VSS	Power/Other	
R1	VSS	Power/Other	
R2	FBD0SBOCLKAN0	Differential	O
R3	FBD0SBOCLKAP0	Differential	O
R4	VSS	Power/Other	
R5	FBD1NBIDN[13]	Differential	I
R6	VSS	Power/Other	
R7	FBD1NBICLKDN0	Differential	I
R8	FBD1NBICP[4]	Differential	I
R9	FBD1NBICN[4]	Differential	I
R10	RSVD[1] (Intel® Itanium® Processor 9300 Series) SVID_DATIO[2] (Intel® Itanium® Processor 9500 Series)		
R11	VSS	Power/Other	
R12	TMS		I
R27	RSVD		
R28	FLASHROM_DATO		O
R29	FLASHROM_CS[2]_N		O
R30	CSI2TNDAT[14]	Differential	O
R31	VSS	Power/Other	
R32	CSI2TPDAT[15]	Differential	O
R33	CSI0TNDAT[15]	Differential	O
R34	CSI0TNDAT[14]	Differential	O
R35	CSI0TPDAT[14]	Differential	O
R36	VSS	Power/Other	
R37	CSI0RNDAT[14]	Differential	I
R38	CSI0RPDAT[14]	Differential	I
T1	FBD0SBOAN[4]	Differential	O
T2	FBD0SBOAP[4]	Differential	O
T3	VCCIO_FBD	Power/Other	
T4	VSS	Power/Other	
T5	FBD1NBIDP[13]	Differential	I
T6	FBD1NBIDP[5]	Differential	I
T7	FBD1NBIDN[5]	Differential	I
T8	FBD1NBICN[2]	Differential	I
T9	VSS	Power/Other	
T10	VCCIO_FBD	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 30 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
T11	RSVD[1] (Intel® Itanium® Processor 9300 Series) SVID_ALERT_N[2] (Intel® Itanium® Processor 9500 Series)		
T12	VFUSERM		I
T27	VCCIO	Power/Other	
T28	FLASHROM_DATI		I
T29	VSS	Power/Other	
T30	CSI2TPDAT[14]	Differential	O
T31	CSI2TNDAT[16]	Differential	O
T32	CSI2TPDAT[16]	Differential	O
T33	CSI0TPDAT[15]	Differential	O
T34	VSS	Power/Other	
T35	VCCIO	Power/Other	
T36	CSI0RNDAT[15]	Differential	I
T37	CSI0RPDAT[15]	Differential	I
T38	CSI0RNDAT[16]	Differential	I
U1	FBD0SBOAN[3]	Differential	O
U2	VSS	Power/Other	
U3	VSS	Power/Other	
U4	RSVD		
U5	FBD1NBIDN[4]	Differential	I
U6	FBD1NBIDP[4]	Differential	I
U7	VSS	Power/Other	
U8	FBD1NBICP[2]	Differential	I
U9	FBD1NBICP[3]	Differential	I
U10	FBD1NBICN[3]	Differential	I
U11	SYSUTST_REFCLK_N	Differential	I
U12	VSS	Power/Other	
U27	VSS	Power/Other	
U28	VCCIO	Power/Other	
U29	CSI2TNDAT[17]	Differential	O
U30	CSI2TPDAT[17]	Differential	O
U31	CSI2TNDAT[18]	Differential	O
U32	VSS	Power/Other	
U33	CSI0TNDAT[16]	Differential	O
U34	CSI0TPDAT[16]	Differential	O
U35	VSS	Power/Other	
U36	CSI0RNDAT[17]	Differential	I
U37	VSS	Power/Other	

Table 3-2. Pin List by Pin Number (Sheet 31 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
U38	CSI0RPDAT[16]	Differential	I
V1	FBD0SBOAP[3]	Differential	O
V2	FBD0SBOAN[2]	Differential	O
V3	FBD0SBOAP[2]	Differential	O
V4	FBD0SBOAN[0]	Differential	O
V5	VSS	Power/Other	
V6	FBD1NBIDP[3]	Differential	I
V7	FBD1NBICN[1]	Differential	I
V8	FBD1NBICP[1]	Differential	I
V9	FBD1NBICN[0]	Differential	I
V10	VSS	Power/Other	
V11	SYSUTST_REFCLK	Differential	I
V12	RESET_N	Power/Other	I
V27	RSVD		
V28	TESTHI[4]		I
V29	RSVD		
V30	VSS	Power/Other	
V31	CSI2TPDAT[18]	Differential	O
V32	CSI0TNDAT[17]	Differential	O
V33	CSI0TPDAT[17]	Differential	O
V34	CSI0TNDAT[18]	Differential	O
V35	VSS	Power/Other	
V36	CSI0RPDAT[17]	Differential	I
V37	CSI0RPDAT[18]	Differential	I
V38	CSI0RNDAT[18]	Differential	I
W1	FBD0SBOAN[1]	Differential	O
W2	FBD0SBOAP[1]	Differential	O
W3	VSS	Power/Other	
W4	FBD0SBOAP[0]	Differential	O
W5	VCCIO_FBD	Power/Other	
W6	FBD1NBIDN[3]	Differential	I
W7	FBD1NBIDN[2]	Differential	I
W8	VSS	Power/Other	
W9	FBD1NBICP[0]	Differential	I
W10	RSVD		
W11	VSS	Power/Other	
W12	RSVD		
W27	RSVD		
W28	VSS	Power/Other	
W29	TESTHI[2]		I

Table 3-2. Pin List by Pin Number (Sheet 32 of 32)

Pin Number	Pin Name	Signal Buffer Type	Direction
W30	CSI2TNDAT[19]	Differential	O
W31	CSI2TPDAT[19]	Differential	O
W32	CSI0TNDAT[19]	Differential	O
W33	VSS	Power/Other	
W34	CSI0TPDAT[18]	Differential	O
W35	VCCIO	Power/Other	
W36	CSI0RPDAT[19]	Differential	I
W37	CSI0RNDAT[19]	Differential	I
W38	VSS	Power/Other	
Y1	VSS	Power/Other	
Y2	VCCIO_FBD	Power/Other	
Y3	FBD0SBOBN[10]	Differential	O
Y4	FBD0SBOBP[10]	Differential	O
Y5	VSS	Power/Other	
Y6	VSS	Power/Other	
Y7	FBD1NBIDP[2]	Differential	I
Y8	FBD1NBICN[14]	Differential	I
Y9	FBD1NBICP[14]	Differential	I
Y10	RSVD		
Y11	VSS	Power/Other	
Y12	SYSCLK	Differential	I
Y27	VCCIO	Power/Other	
Y28	TESTHI[1]		I
Y29	VSS	Power/Other	
Y30	VCCIO	Power/Other	
Y31	VSS	Power/Other	
Y32	CSI0TPDAT[19]	Differential	O
Y33	VCCIO	Power/Other	
Y34	CSI1TNDAT[19]	Differential	O
Y35	CSI1TPDAT[19]	Differential	O
Y36	VSS	Power/Other	
Y37	CSI1RPDAT[19]	Differential	I
Y38	CSI1RNDAT[19]	Differential	I

3.2 Processor Package Top Pin Assignments

This section provides two-dimensional tables of the package top pin assignments. These pins connect to the Ararat Voltage Regulator Power Module and do not connect to the motherboard.

3.2.1 Top-Side J1 Connector Two-Dimensional Table

3.2.1.1 Top-Side J1 Connector Two-Dimensional Table for the Intel® Itanium® Processor 9300 Series

Table 3-3 is a two dimensional table of the Intel® Itanium® Processor 9300 Series package top-side J1 connector.

Table 3-3. Top-Side J1 Connector Two-Dimensional Table (Intel® Itanium® Processor 9300 Series) (Sheet 1 of 2)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>A</td><td>VID_VCCCORE[1]</td><td rowspan="3">NO CONNECT</td><td>VID_VCCCORE[2]</td><td rowspan="4">NO CONNECT</td><td>A</td></tr>
<tr><td>B</td><td>VID_VCCCORE[3]</td><td>VID_VCCCORE[4]</td><td>B</td></tr>
<tr><td>C</td><td>VID_VCCCORE[5]</td><td>VID_VCCCORE[6]</td><td>C</td></tr>
<tr><td>D</td><td colspan="3">VCCCORE</td><td>D</td></tr>
<tr><td>E</td><td colspan="4">VCCCORE</td><td>E</td></tr>
<tr><td>F</td><td colspan="4">VSS</td><td>F</td></tr>
<tr><td>G</td><td colspan="4">VSS</td><td>G</td></tr>
<tr><td>H</td><td colspan="4">VCCCORE</td><td>H</td></tr>
<tr><td>J</td><td colspan="4">VCCCORE</td><td>J</td></tr>
<tr><td>K</td><td colspan="4">VSS</td><td>K</td></tr>
<tr><td>L</td><td colspan="4">VSS</td><td>L</td></tr>
<tr><td>M</td><td colspan="4">VCCCORE</td><td>M</td></tr>
<tr><td>N</td><td colspan="4">VCCCORE</td><td>N</td></tr>
<tr><td>P</td><td colspan="4">VSS</td><td>P</td></tr>
<tr><td>R</td><td colspan="4">VSS</td><td>R</td></tr>
<tr><td>T</td><td colspan="4">VCCCACHE</td><td>T</td></tr>
<tr><td>U</td><td colspan="4">VCCCACHE</td><td>U</td></tr>
<tr><td>V</td><td colspan="4">VSS</td><td>V</td></tr>
<tr><td>W</td><td colspan="4">VSS</td><td>W</td></tr>
<tr><td>Y</td><td colspan="4">VCCCACHE</td><td>Y</td></tr>
<tr><td>AA</td><td colspan="4">VCCCACHE</td><td>AA</td></tr>
<tr><td>AB</td><td colspan="4">VCCCACHE</td><td>AB</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

Table 3-3. Top-Side J1 Connector Two-Dimensional Table (Intel® Itanium® Processor 9300 Series) (Sheet 2 of 2)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>AC</td><td colspan="4">VSS</td><td>AC</td></tr>
<tr><td>AD</td><td colspan="4">VSS</td><td>AD</td></tr>
<tr><td>AE</td><td colspan="4">VCCCACHE</td><td>AE</td></tr>
<tr><td>AF</td><td colspan="4">VCCCACHE</td><td>AF</td></tr>
<tr><td>AG</td><td colspan="4">VSS</td><td>AG</td></tr>
<tr><td>AH</td><td colspan="4">VSS</td><td>AH</td></tr>
<tr><td>AJ</td><td colspan="4">VCCCORE</td><td>AJ</td></tr>
<tr><td>AK</td><td colspan="4">VCCCORE</td><td>AK</td></tr>
<tr><td>AL</td><td colspan="4">VSS</td><td>AL</td></tr>
<tr><td>AM</td><td colspan="4">VSS</td><td>AM</td></tr>
<tr><td>AN</td><td colspan="4">VCCCORE</td><td>AN</td></tr>
<tr><td>AP</td><td colspan="4">VCCCORE</td><td>AP</td></tr>
<tr><td>AR</td><td colspan="4">VSS</td><td>AR</td></tr>
<tr><td>AT</td><td colspan="4">VSS</td><td>AT</td></tr>
<tr><td>AU</td><td>Reserved</td><td rowspan="4">NO CONNECT</td><td>Reserved</td><td rowspan="4">NO CONNECT</td><td>AU</td></tr>
<tr><td>AV</td><td>VSSCACHESENSE</td><td>VCCCACHESENSE</td><td>AV</td></tr>
<tr><td>AW</td><td>VROUTPUT_ENABLE0</td><td>CPU_PRESA_N</td><td>AW</td></tr>
<tr><td>AY</td><td>VR_PROCTYPE_0</td><td>VR_PROCTYPE_1</td><td>AY</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

3.2.1.2 Top-Side J1 Connector Two-Dimensional Table for the Intel® Itanium® Processor 9500 Series

Table 3-4 is a two-dimensional table of the Intel® Itanium® Processor 9500 Series package top-side J1 connector.

Table 3-4. Top-Side J1 Connector Two-Dimensional Table (Intel® Itanium® Processor 9500 Series) (Sheet 1 of 3)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>A</td><td rowspan="2">NO CONNECT</td><td rowspan="3">NO CONNECT</td><td rowspan="3">NO CONNECT</td><td rowspan="4">NO CONNECT</td><td>A</td></tr>
<tr><td>B</td><td>B</td></tr>
<tr><td>C</td><td>RESERVED</td><td>C</td></tr>
<tr><td>D</td><td colspan="3">VCCCORE</td><td>D</td></tr>
<tr><td>E</td><td colspan="4">VSS</td><td>E</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

Table 3-4. Top-Side J1 Connector Two-Dimensional Table (Intel® Itanium® Processor 9500 Series) (Sheet 2 of 3)

	1	2	3	4	
F	VSS				F
G	VCCCORE				G
H	VCCCORE				H
J	VCCCORE				J
K	VSS				K
L	VSS				L
M	VCCUNCORE				M
N	VCCUNCORE				N
P	VCCUNCORE				P
R	VCCUNCORE				R
T	VSS				T
U	VSS				U
V	VSS				V
W	VCCUNCORE				W
Y	VCCUNCORE				Y
AA	VCCUNCORE				AA
AB	VCCUNCORE				AB
AC	VSS				AC
AD	VSS				AD
AE	VSS				AE
AF	VCCUNCORE				AF
AG	VCCUNCORE				AG
AH	VCCUNCORE				AH
AJ	VCCUNCORE				AJ
AK	VSS				AK
AL	VSS				AL
AM	VCCCORE				AM
AN	VCCCORE				AN
AP	VCCCORE				AP
AR	VSS				AR
AT	VSS				AT
	1	2	3	4	

Table 3-4. Top-Side J1 Connector Two-Dimensional Table (Intel® Itanium® Processor 9500 Series) (Sheet 3 of 3)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>AU</td><td>VSS</td><td rowspan="4">NO CONNECT</td><td>VSS</td><td rowspan="4">NO CONNECT</td><td>AU</td></tr>
<tr><td>AV</td><td>CPU_PRESA_N</td><td>NO CONNECT</td><td>AV</td></tr>
<tr><td>AW</td><td>VROUTPUT_ENABLE0</td><td>VCCUNCORE</td><td>AW</td></tr>
<tr><td>AY</td><td>VR_PROCTYPE_0</td><td>VR_PROCTYPE_1</td><td>AY</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

3.2.2 Top-Side J2 Connector Two-Dimensional Table

3.2.2.1 Top-Side J2 Connector Two-Dimensional Table for the Intel® Itanium® Processor 9300 Series

Table 3-5 is a two-dimensional table of the Intel® Itanium® Processor 9300 Series Processor package top-side J2 connector.

Table 3-5. Top-Side J2 Connector Two-Dimensional Table (Intel® Itanium® Processor 9300 Series) (Sheet 1 of 2)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>A</td><td>VID_VCCUNCORE[1]</td><td rowspan="3">NO CONNECT</td><td>VID_VCCUNCORE[3]</td><td rowspan="4">NO CONNECT</td><td>A</td></tr>
<tr><td>B</td><td>VID_VCCUNCORE[2]</td><td>VID_VCCUNCORE[5]</td><td>B</td></tr>
<tr><td>C</td><td>VID_VCCUNCORE[4]</td><td>VID_VCCUNCORE[6]</td><td>C</td></tr>
<tr><td>D</td><td colspan="3">VCCCORE</td><td>D</td></tr>
<tr><td>E</td><td colspan="4">VCCCORE</td><td>E</td></tr>
<tr><td>F</td><td colspan="4">VSS</td><td>F</td></tr>
<tr><td>G</td><td colspan="4">VSS</td><td>G</td></tr>
<tr><td>H</td><td colspan="4">VCCCORE</td><td>H</td></tr>
<tr><td>J</td><td colspan="4">VCCCORE</td><td>J</td></tr>
<tr><td>K</td><td colspan="4">VSS</td><td>K</td></tr>
<tr><td>L</td><td colspan="4">VSS</td><td>L</td></tr>
<tr><td>M</td><td colspan="4">VCCCORE</td><td>M</td></tr>
<tr><td>N</td><td colspan="4">VCCCORE</td><td>N</td></tr>
<tr><td>P</td><td colspan="4">VSS</td><td>P</td></tr>
<tr><td>R</td><td colspan="4">VSS</td><td>R</td></tr>
<tr><td>T</td><td colspan="4">VCCUNCORE</td><td>T</td></tr>
<tr><td>U</td><td colspan="4">VCCUNCORE</td><td>U</td></tr>
<tr><td>V</td><td colspan="4">VSS</td><td>V</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

Table 3-5. Top-Side J2 Connector Two-Dimensional Table (Intel® Itanium® Processor 9300 Series) (Sheet 2 of 2)

	1	2	3	4	
W	VSS				W
Y	VCCUNCORE				Y
AA	VCCUNCORE				AA
AB	VCCUNCORE				AB
AC	VSS				AC
AD	VSS				AD
AE	VCCUNCORE				AE
AF	VCCUNCORE				AF
AG	VSS				AG
AH	VSS				AH
AJ	VCCCORE				AJ
AK	VCCCORE				AK
AL	VSS				AL
AM	VSS				AM
AN	VCCCORE				AN
AP	VCCCORE				AP
AR	VSS				AR
AT	VSS				AT
AU	Reserved	NO CONNECT	Reserved	NO CONNECT	AU
AV	VCCCORESENSE		VR_THERMTRIP_N		AV
AW	VSSCORESENSE		VR_THERMALERT_N		AW
AY	VID_VCCCORE[0]		CPU_PRESB_N		AY
	1	2	3	4	

3.2.2.2 Top-Side J2 Connector Two-Dimensional Table for the Intel® Itanium® Processor 9500 Series

Table 3-6 is a two-dimensional table of the Intel® Itanium® Processor 9500 Series package top-side J2 connector.

Table 3-6. Top-Side J2 Connector Two-Dimensional Table (Intel® Itanium® Processor 9500 Series) (Sheet 1 of 2)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>A</td><td>NO CONNECT</td><td rowspan="3">NO CONNECT</td><td>NO CONNECT</td><td rowspan="4">NO CONNECT</td><td>A</td></tr>
<tr><td>B</td><td>NO CONNECT</td><td>VR_READY</td><td>B</td></tr>
<tr><td>C</td><td>RESERVED</td><td>RESERVED</td><td>C</td></tr>
<tr><td>D</td><td colspan="3">VCCCORE</td><td>D</td></tr>
<tr><td>E</td><td colspan="4">VSS</td><td>E</td></tr>
<tr><td>F</td><td colspan="4">VSS</td><td>F</td></tr>
<tr><td>G</td><td colspan="4">VCCCORE</td><td>G</td></tr>
<tr><td>H</td><td colspan="4">VCCCORE</td><td>H</td></tr>
<tr><td>J</td><td colspan="4">VCCCORE</td><td>J</td></tr>
<tr><td>K</td><td colspan="4">VCCCORE</td><td>K</td></tr>
<tr><td>L</td><td colspan="4">VSS</td><td>L</td></tr>
<tr><td>M</td><td colspan="4">VSS</td><td>M</td></tr>
<tr><td>N</td><td colspan="4">VSS</td><td>N</td></tr>
<tr><td>P</td><td colspan="4">VSS</td><td>P</td></tr>
<tr><td>R</td><td colspan="4">VCCCORE</td><td>R</td></tr>
<tr><td>T</td><td colspan="4">VCCCORE</td><td>T</td></tr>
<tr><td>U</td><td colspan="4">VCCCORE</td><td>U</td></tr>
<tr><td>V</td><td colspan="4">VCCCORE</td><td>V</td></tr>
<tr><td>W</td><td colspan="4">VSS</td><td>W</td></tr>
<tr><td>Y</td><td colspan="4">VSS</td><td>Y</td></tr>
<tr><td>AA</td><td colspan="4">VSS</td><td>AA</td></tr>
<tr><td>AB</td><td colspan="4">VSS</td><td>AB</td></tr>
<tr><td>AC</td><td colspan="4">VCCCORE</td><td>AC</td></tr>
<tr><td>AD</td><td colspan="4">VCCCORE</td><td>AD</td></tr>
<tr><td>AE</td><td colspan="4">VCCCORE</td><td>AE</td></tr>
<tr><td>AF</td><td colspan="4">VCCCORE</td><td>AF</td></tr>
<tr><td>AG</td><td colspan="4">VSS</td><td>AG</td></tr>
<tr><td>AH</td><td colspan="4">VSS</td><td>AH</td></tr>
<tr><td>AJ</td><td colspan="4">VSS</td><td>AJ</td></tr>
<tr><td>AK</td><td colspan="4">VSS</td><td>AK</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

Table 3-6. Top-Side J2 Connector Two-Dimensional Table (Intel® Itanium® Processor 9500 Series) (Sheet 2 of 2)

	1	2	3	4	
AL	VCCCOCRE				AL
AM	VCCCORE				AM
AN	VCCCORE				AN
AP	VCCCORE				AP
AR	VSS				AR
AT	VSS				AT
AU	VSS	NO CONNECT	VSS	NO CONNECT	AU
AV	CPU_PRESB_N		VR_THERMTRIP_N		AV
AW	NO CONNECT		VR_THERMALERT_N		AW
AY	NO CONNECT		NO CONNECT		AY
	1	2	3	4	

3.2.3 Top-Side J3 Connector Two-Dimensional Table

3.2.3.1 Top-Side J3 Connector Two-Dimensional Table for the Intel® Itanium® Processor 9300 Series

Table 3-7 is a two-dimensional table of the Intel® Itanium® Processor 9300 Series package top-side J3 connector.

Table 3-7. Top-Side J3 Connector Two-Dimensional Table (Intel® Itanium® Processor 9300 Series) (Sheet 1 of 2)

	1	2	3	4	
A	Reserved	NO CONNECT	Reserved	NO CONNECT	A
B	VR_FAN_N		Reserved		B
C	Reserved		VRPWRGD		C
D	VCCCORE				D
E	VCCCORE				E
F	VSS				F
G	VSS				G
H	VCCCORE				H
J	VCCCORE				J
K	VSS				K
L	VSS				L
M	VCCCORE				M
	1	2	3	4	

Table 3-7. Top-Side J3 Connector Two-Dimensional Table (Intel® Itanium® Processor 9300 Series) (Sheet 2 of 2)

	1	2	3	4	
N	VCCCORE				N
P	VSS				P
R	VSS				R
T	VCCCACHE				T
U	VCCCACHE				U
V	VSS				V
W	VSS				W
Y	VCCCACHE				Y
AA	VCCCACHE				AA
AB	VCCCACHE				AB
AC	VSS				AC
AD	VSS				AD
AE	VCCCACHE				AE
AF	VCCCACHE				AF
AG	VSS				AG
AH	VSS				AH
AJ	VCCCORE				AJ
AK	VCCCORE				AK
AL	VSS				AL
AM	VSSVSS				AM
AN	VCCCORE				AN
AP	VCCCORE				AP
AR	VSS				AR
AT	VSS				AT
AU	Reserved	NO CONNECT	Reserved	NO CONNECT	AU
AV	CPU_PRESB_N		VSSUNCORESENSE		AV
AW	VID_VCCUNCORE[0]		VCCUNCORESENSE		AW
AY	Reserved		Reserved		AY
	1	2	3	4	

3.2.3.2 Top-Side J3 Connector Two-Dimensional Table for the Intel® Itanium® Processor 9500 Series

Table 3-8 is a two-dimensional table of the Intel® Itanium® Processor 9500 Series package top-side J3 connector.

Table 3-8. Top-Side J3 Connector Two-Dimensional Table (Intel® Itanium® Processor 9500 Series) (Sheet 1 of 2)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>A</td><td>NO CONNECT</td><td rowspan="3">NO CONNECT</td><td>NO CONNECT</td><td rowspan="4">NO CONNECT</td><td>A</td></tr>
<tr><td>B</td><td>VR_FAN_N</td><td>NO CONNECT</td><td>B</td></tr>
<tr><td>C</td><td>NO CONNECT</td><td>NO CONNECT</td><td>C</td></tr>
<tr><td>D</td><td colspan="3">VCCCORE</td><td>D</td></tr>
<tr><td>E</td><td colspan="4">VSS</td><td>E</td></tr>
<tr><td>F</td><td colspan="4">VSS</td><td>F</td></tr>
<tr><td>G</td><td colspan="4">VCCCORE</td><td>G</td></tr>
<tr><td>H</td><td colspan="4">VCCCORE</td><td>H</td></tr>
<tr><td>J</td><td colspan="4">VCCCORE</td><td>J</td></tr>
<tr><td>K</td><td colspan="4">VSS</td><td>K</td></tr>
<tr><td>L</td><td colspan="4">VSS</td><td>L</td></tr>
<tr><td>M</td><td colspan="4">VCCCORE</td><td>M</td></tr>
<tr><td>N</td><td colspan="4">VCCCORE</td><td>N</td></tr>
<tr><td>P</td><td colspan="4">VCCCORE</td><td>P</td></tr>
<tr><td>R</td><td colspan="4">VCCCORE</td><td>R</td></tr>
<tr><td>T</td><td colspan="4">VSS</td><td>T</td></tr>
<tr><td>U</td><td colspan="4">VSS</td><td>U</td></tr>
<tr><td>V</td><td colspan="4">VSS</td><td>V</td></tr>
<tr><td>W</td><td colspan="4">VCCUNCORE</td><td>W</td></tr>
<tr><td>Y</td><td colspan="4">VCCUNCORE</td><td>Y</td></tr>
<tr><td>AA</td><td colspan="4">VCCUNCORE</td><td>AA</td></tr>
<tr><td>AB</td><td colspan="4">VCCUNCORE</td><td>AB</td></tr>
<tr><td>AC</td><td colspan="4">VSS</td><td>AC</td></tr>
<tr><td>AD</td><td colspan="4">VSS</td><td>AD</td></tr>
<tr><td>AE</td><td colspan="4">VSS</td><td>AE</td></tr>
<tr><td>AF</td><td colspan="4">VCCUNCORE</td><td>AF</td></tr>
<tr><td>AG</td><td colspan="4">VCCUNCORE</td><td>AG</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

Table 3-8. Top-Side J3 Connector Two-Dimensional Table (Intel® Itanium® Processor 9500 Series) (Sheet 2 of 2)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>AH</td><td colspan="4">VCCUNCORE</td><td>AH</td></tr>
<tr><td>AJ</td><td colspan="4">VCCUNCORE</td><td>AJ</td></tr>
<tr><td>AK</td><td colspan="4">VSS</td><td>AK</td></tr>
<tr><td>AL</td><td colspan="4">VSS</td><td>AL</td></tr>
<tr><td>AM</td><td colspan="4">VCCCORE</td><td>AM</td></tr>
<tr><td>AN</td><td colspan="4">VCCCORE</td><td>AN</td></tr>
<tr><td>AP</td><td colspan="4">VCCCORE</td><td>AP</td></tr>
<tr><td>AR</td><td colspan="4">VSS</td><td>AR</td></tr>
<tr><td>AT</td><td colspan="4">VSS</td><td>AT</td></tr>
<tr><td>AU</td><td>SVID_DATA</td><td rowspan="4">NO CONNECT</td><td>SVID_CLK</td><td rowspan="4">NO CONNECT</td><td>AU</td></tr>
<tr><td>AV</td><td>VSS</td><td>VSS</td><td>AV</td></tr>
<tr><td>AW</td><td>SVID_ALERT_N</td><td>CPU_PRESB_N</td><td>AW</td></tr>
<tr><td>AY</td><td>NO CONNECT</td><td>Reserved</td><td>AY</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

3.2.4 Top-Side J4 Connector Two-Dimensional Table

3.2.4.1 Top-Side J4 Connector Two-Dimensional Table for the Intel® Itanium® Processor 9300 Series

Table 3-9 is a two-dimensional table of the Intel® Itanium® Processor 9300 Series package top-side J4 connector.

Table 3-9. Top-Side J4 Connector Two-Dimensional Table (Intel® Itanium® Processor 9300 Series) (Sheet 1 of 2)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>A</td><td>VID_VCCCACHE[0]</td><td rowspan="3">NO CONNECT</td><td>VID_VCCCACHE[1]</td><td rowspan="4">NO CONNECT</td><td>A</td></tr>
<tr><td>B</td><td>VID_VCCCACHE[5]</td><td>VID_VCCCACHE[2]</td><td>B</td></tr>
<tr><td>C</td><td>VID_VCCCACHE[4]</td><td>VID_VCCCACHE[3]</td><td>C</td></tr>
<tr><td>D</td><td colspan="3">VCCCORE</td><td>D</td></tr>
<tr><td>E</td><td colspan="4">VCCCORE</td><td>E</td></tr>
<tr><td>F</td><td colspan="4">VSS</td><td>F</td></tr>
<tr><td>G</td><td colspan="4">VSS</td><td>G</td></tr>
<tr><td>H</td><td colspan="4">VCCCORE</td><td>H</td></tr>
<tr><td>J</td><td colspan="4">VCCCORE</td><td>J</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

Table 3-9. Top-Side J4 Connector Two-Dimensional Table (Intel® Itanium® Processor 9300 Series) (Sheet 2 of 2)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>K</td><td colspan="4">VSS</td><td>K</td></tr>
<tr><td>L</td><td colspan="4">VSS</td><td>L</td></tr>
<tr><td>M</td><td colspan="4">VCCCORE</td><td>M</td></tr>
<tr><td>N</td><td colspan="4">VCCCORE</td><td>N</td></tr>
<tr><td>P</td><td colspan="4">VSS</td><td>P</td></tr>
<tr><td>R</td><td colspan="4">VSS</td><td>R</td></tr>
<tr><td>T</td><td colspan="4">VCCUNCORE</td><td>T</td></tr>
<tr><td>U</td><td colspan="4">VCCUNCORE</td><td>U</td></tr>
<tr><td>V</td><td colspan="4">VSS</td><td>V</td></tr>
<tr><td>W</td><td colspan="4">VSS</td><td>W</td></tr>
<tr><td>Y</td><td colspan="4">VCCUNCORE</td><td>Y</td></tr>
<tr><td>AA</td><td colspan="4">VCCUNCORE</td><td>AA</td></tr>
<tr><td>AB</td><td colspan="4">VCCUNCORE</td><td>AB</td></tr>
<tr><td>AC</td><td colspan="4">VSS</td><td>AC</td></tr>
<tr><td>AD</td><td colspan="4">VSS</td><td>AD</td></tr>
<tr><td>AE</td><td colspan="4">VCCUNCORE</td><td>AE</td></tr>
<tr><td>AF</td><td colspan="4">VCCUNCORE</td><td>AF</td></tr>
<tr><td>AG</td><td colspan="4">VSS</td><td>AG</td></tr>
<tr><td>AH</td><td colspan="4">VSS</td><td>AH</td></tr>
<tr><td>AJ</td><td colspan="4">VCCCORE</td><td>AJ</td></tr>
<tr><td>AK</td><td colspan="4">VCCCORE</td><td>AK</td></tr>
<tr><td>AL</td><td colspan="4">VSS</td><td>AL</td></tr>
<tr><td>AM</td><td colspan="4">VSS</td><td>AM</td></tr>
<tr><td>AN</td><td colspan="4">VCCCORE</td><td>AN</td></tr>
<tr><td>AP</td><td colspan="4">VCCCORE</td><td>AP</td></tr>
<tr><td>AR</td><td colspan="4">VSS</td><td>AR</td></tr>
<tr><td>AT</td><td colspan="4">VSS</td><td>AT</td></tr>
<tr><td>AU</td><td>VCCIO</td><td rowspan="4">NO CONNECT</td><td>Reserved</td><td rowspan="4">NO CONNECT</td><td>AU</td></tr>
<tr><td>AV</td><td>Reserved</td><td>Reserved</td><td>AV</td></tr>
<tr><td>AW</td><td>Reserved</td><td>CPU_PRESA_N</td><td>AW</td></tr>
<tr><td>AY</td><td>Reserved</td><td>Reserved</td><td>AY</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

3.2.4.2 Top-Side J4 Connector Two-Dimensional Table for the Intel® Itanium® Processor 9500 Series

Table 3-10 is a two-dimensional table of the Intel® Itanium® Processor 9500 Series package top-side J4 connector.

Table 3-10. Top-Side J4 Connector Two-Dimensional Table (Intel® Itanium® Processor 9500 Series) (Sheet 1 of 2)

	1	2	3	4	
A	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	A
B	RESERVED		RESERVED		B
C	RESERVED		RESERVED		C
D	VCCCORE				D
E	VSS				E
F	VSS				F
G	VCCCORE				G
H	VCCCORE				H
J	VCCCORE				J
K	VCCCORE				K
L	VSS				L
M	VSS				M
N	VSS				N
P	VSS				P
R	VCCCORE				R
T	VCCCORE				T
U	VCCCORE				U
V	VCCCORE				V
W	VSS				W
Y	VSS				Y
AA	VSS				AA
AB	VSS				AB
AC	VCCCORE				AC
AD	VCCCORE				AD
AE	VCCCORE				AE
AF	VCCCORE				AF
AG	VSS				AG
	1	2	3	4	

Table 3-10. Top-Side J4 Connector Two-Dimensional Table (Intel® Itanium® Processor 9500 Series) (Sheet 2 of 2)

<table>
<tr><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th></th></tr>
<tr><td>AH</td><td colspan="4">VSS</td><td>AH</td></tr>
<tr><td>AJ</td><td colspan="4">VSS</td><td>AJ</td></tr>
<tr><td>AK</td><td colspan="4">VSS</td><td>AK</td></tr>
<tr><td>AL</td><td colspan="4">VCCCORE</td><td>AL</td></tr>
<tr><td>AM</td><td colspan="4">VCCCORE</td><td>AM</td></tr>
<tr><td>AN</td><td colspan="4">VCCCORE</td><td>AN</td></tr>
<tr><td>AP</td><td colspan="4">VCCCORE</td><td>AP</td></tr>
<tr><td>AR</td><td colspan="4">VSS</td><td>AR</td></tr>
<tr><td>AT</td><td colspan="4">VSS</td><td>AT</td></tr>
<tr><td>AU</td><td>VCCIO</td><td rowspan="4">NO CONNECT</td><td>VSS</td><td rowspan="4">NO CONNECT</td><td>AU</td></tr>
<tr><td>AV</td><td>Reserved</td><td>RESERVED</td><td>AV</td></tr>
<tr><td>AW</td><td>CPU_PRESA_N</td><td>NO CONNECT</td><td>AW</td></tr>
<tr><td>AY</td><td>NO CONNECT</td><td>NO CONNECT</td><td>AY</td></tr>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td></td></tr>
</table>

§

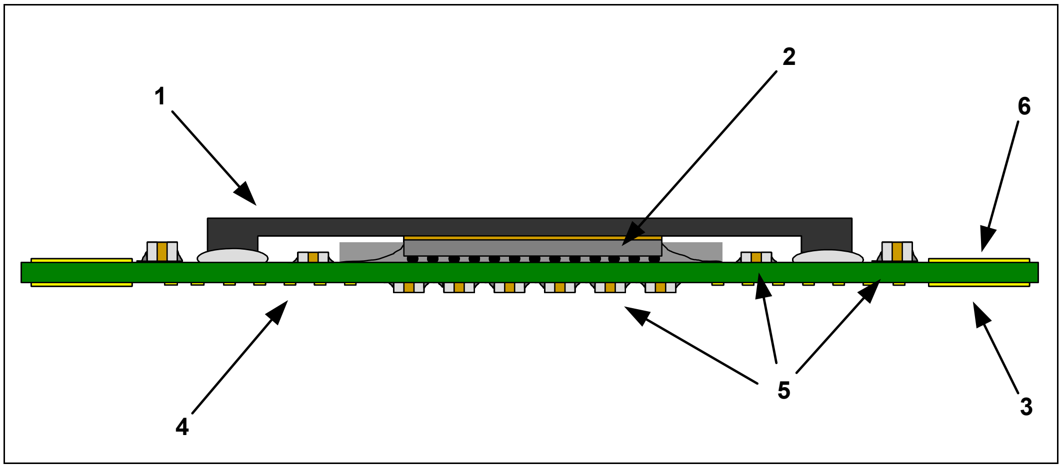
4 Mechanical Specifications

The Intel® Itanium® Processor 9300 Series and 9500 Series are packaged in a FC-LGA package that interfaces with the motherboard via an LGA1248 socket. The package top side consists of lands that interface with a LGA connector for direct power delivery to the core, cache and system interface. The package also consists of an integrated heatsink spreader (IHS), which is attached to the package substrate and die and serves as the mating surface for the processor component thermal solutions, such as a heatsink. The bottom side of the package has 1248 lands, a 38 x 38 mm pad array which interfaces with the LGA1248 socket. Figure 4-1 shows a sketch of the processor package components and how they are assembled together.

The package components shown in Figure 4-1 include the following:

1. Integrated Heat Spreader (IHS).
2. Processor die.
3. Internal test pads for power delivery.
4. LGA lands for I/O.
5. Decoupling and server management components.
6. LGA lands for power delivery.

Figure 4-1. Processor Package Assembly Sketch



Note: This drawing is not to scale and is for reference only. Processor power delivery and thermal solutions, and the socket are not shown.

4.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 4-2, Figure 4-3, Figure 4-4 and Figure 4-5. The package mechanical drawings for the Intel® Itanium® Processor 9500 Series processor are shown in Figure 4-6, Figure 4-7, Figure 4-8 and Figure 4-9. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions will include:

1. Package reference with tolerances (total height, length, width, and so on).
2. IHS parallelism and tilt.
3. Land dimensions.
4. Top-side and back-side component keepout dimensions.
5. Reference datums.

All drawing dimensions are in mm.

4.2 Intel® Itanium® Processor 9300 Series

Figure 4-2. Intel® Itanium® Processor 9300 Series Package Drawing (Sheet 1 of 4)

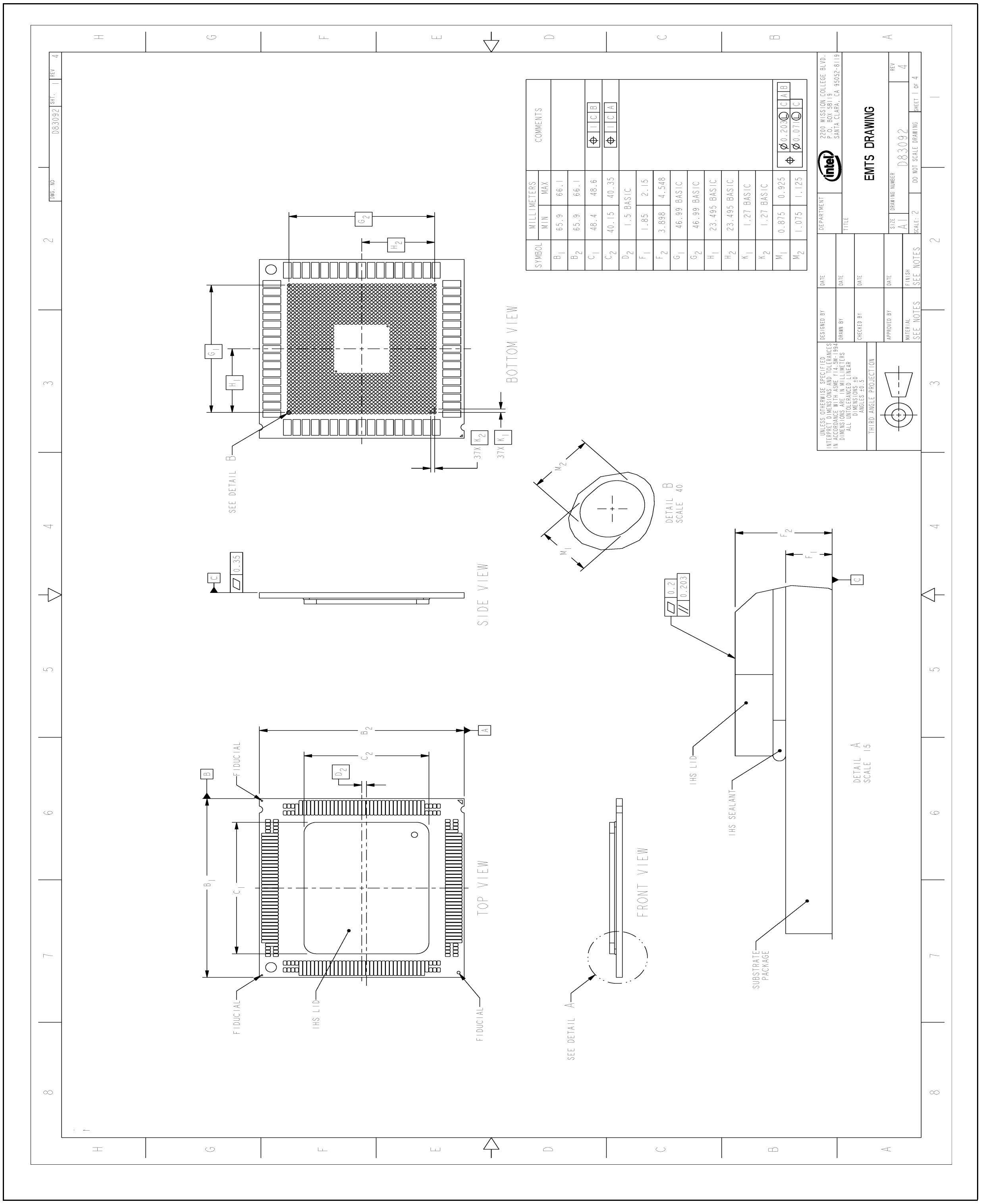
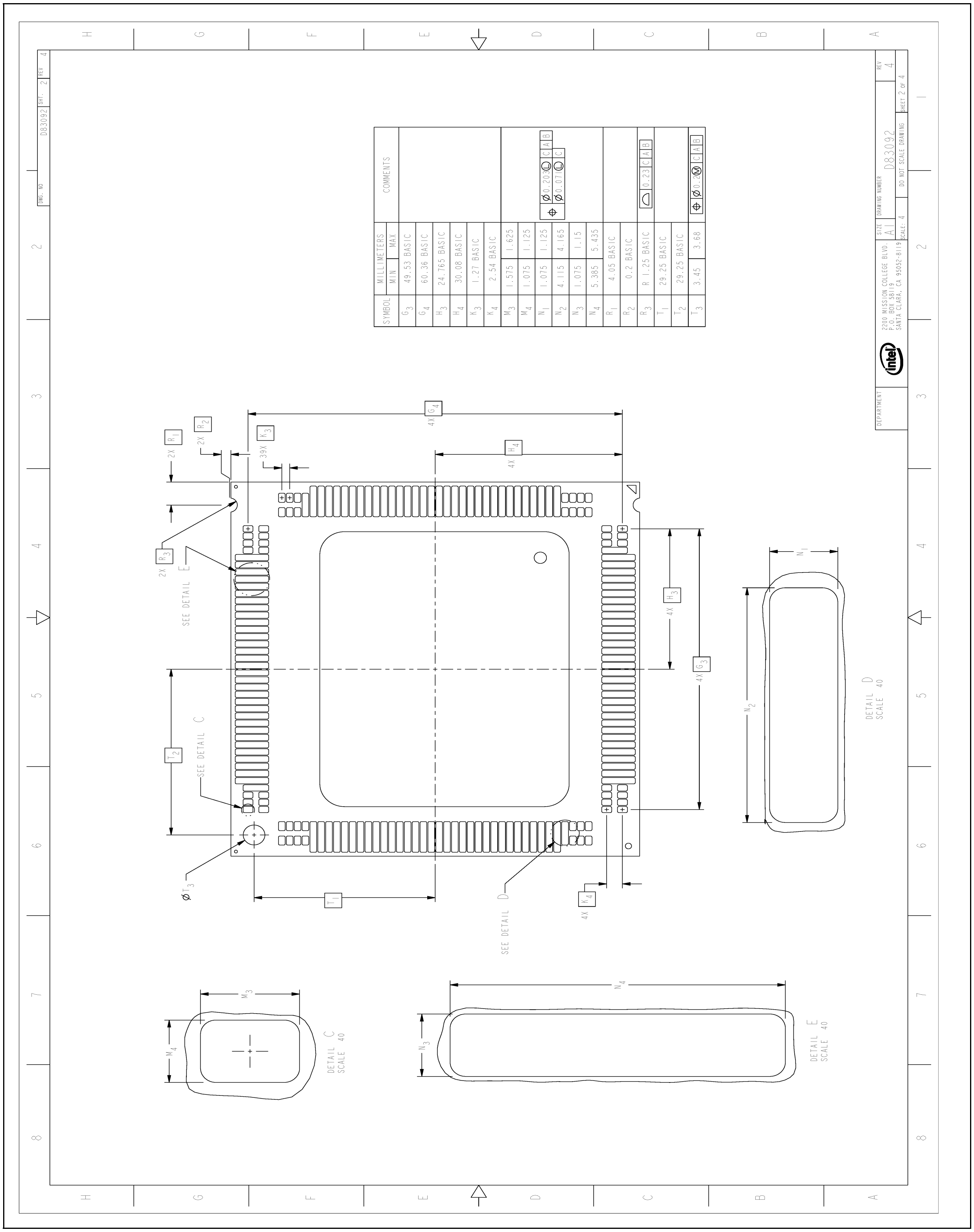


Figure 4-3. Intel® Itanium® Processor 9300 Series Processor Package Drawing (Sheet 2 of 4)



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	COMMENTS
G_3	49.53 BASIC		
G_4	60.36 BASIC		
H_3	24.765 BASIC		
H_4	30.08 BASIC		
K_3	1.27 BASIC		
K_4	2.54 BASIC		
M_3	1.575	1.625	⌖ Ø0.203 Ⓛ C A B / Ø0.071 Ⓛ C
M_4	1.075	1.125	
N_1	1.075	1.125	
N_2	4.115	4.165	
N_3	1.075	1.15	
N_4	5.385	5.435	
R_1	4.05 BASIC		
R_2	0.2 BASIC		
R_3	R 1.25 BASIC		⌓ 0.23 C A B
T_1	29.25 BASIC		
T_2	29.25 BASIC		
T_3	3.45	3.68	⌖ Ø0.2 Ⓜ C A B

Figure 4-4. Intel® Itanium® Processor 9300 Series Package Drawing (Sheet 3 of 4)

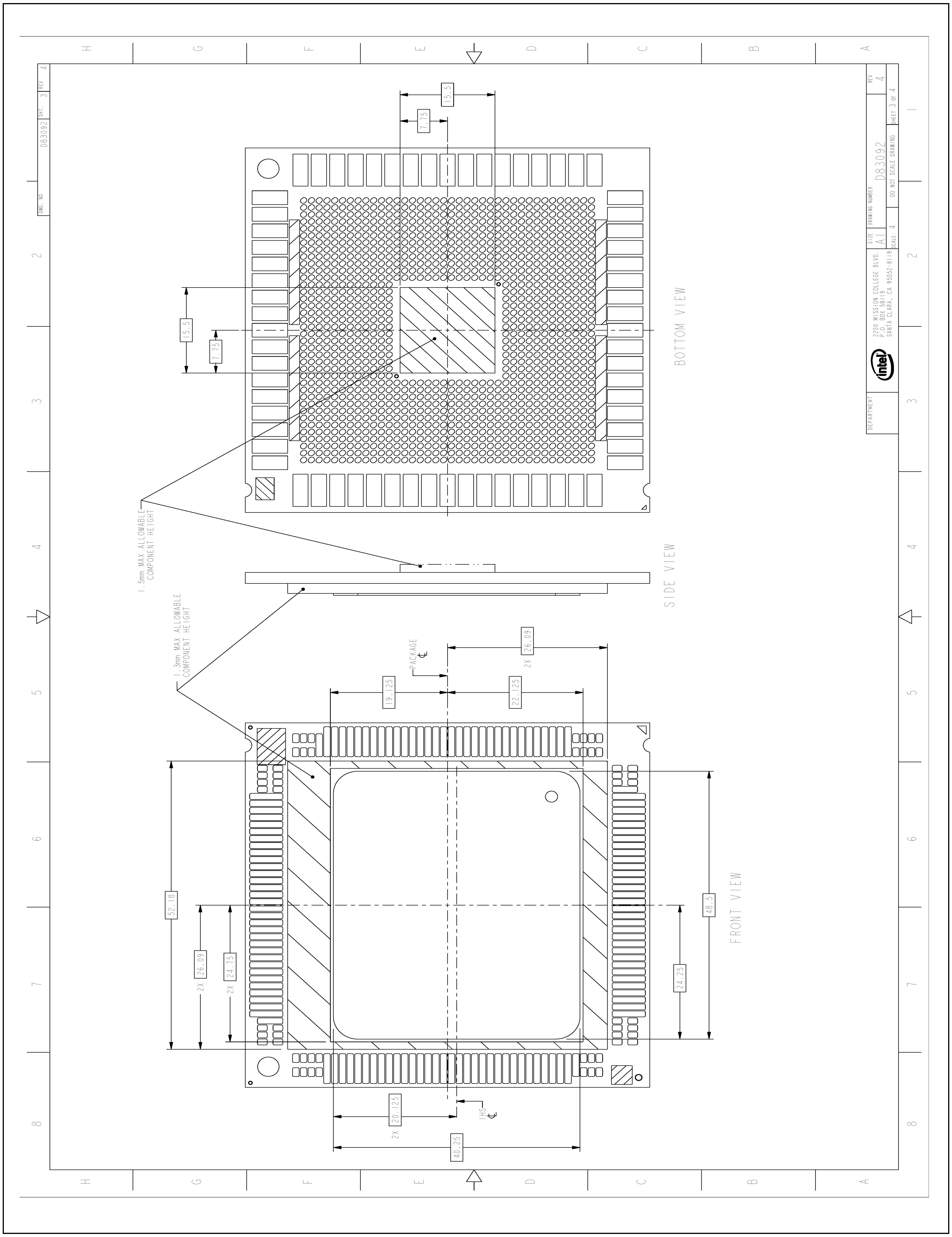


Figure 4-5. Intel® Itanium® Processor 9300 Series Package Drawing (Sheet 4 of 4)

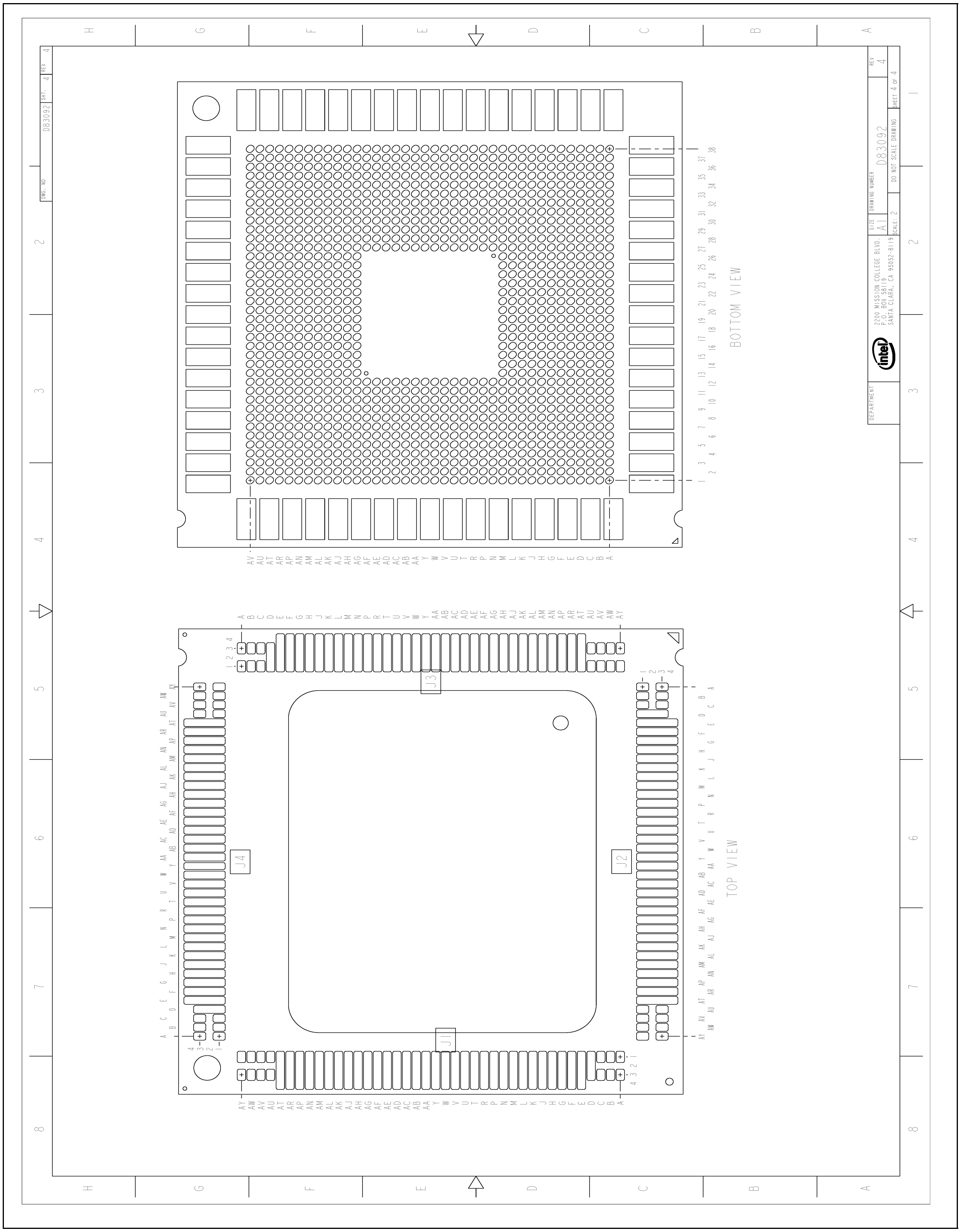


Figure 4-6. Intel® Itanium® Processor 9500 Series Package Drawing (Sheet 1 of 4)

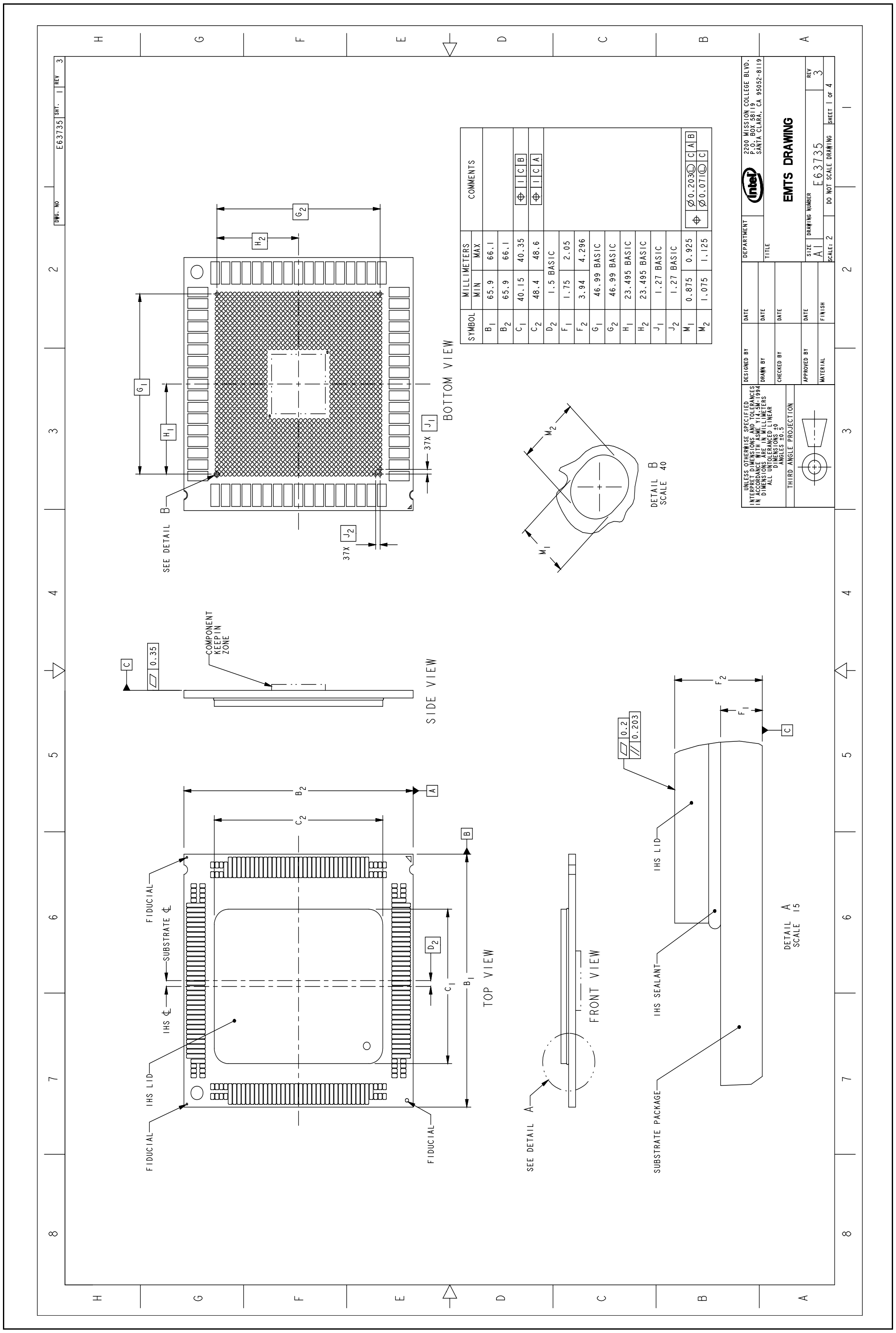


Figure 4-7. Intel® Itanium® Processor 9500 Series Package Drawing (Sheet 2 of 4)

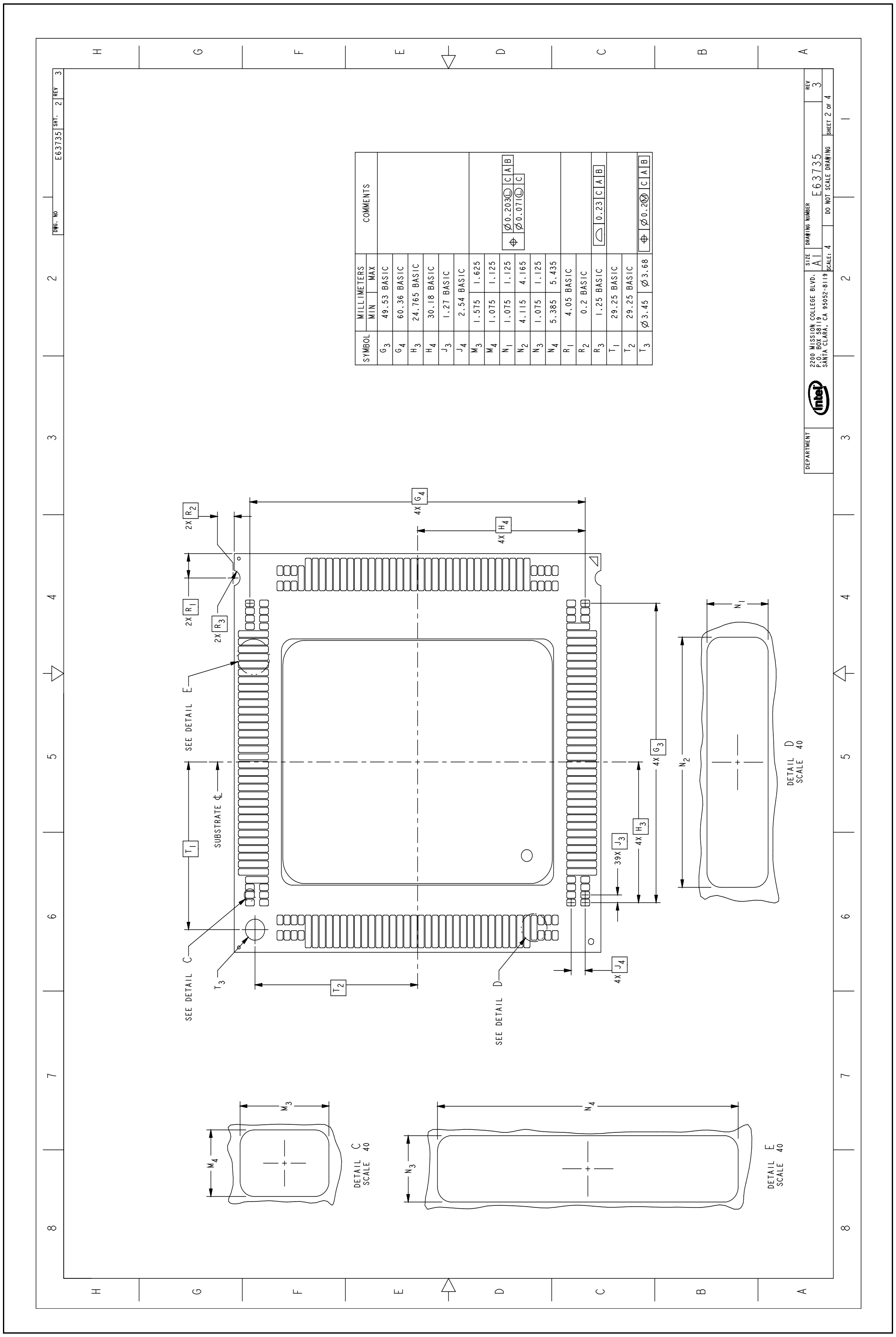


Figure 4-8. Intel® Itanium® Processor 9500 Series Package Drawing (Sheet 3 of 4)

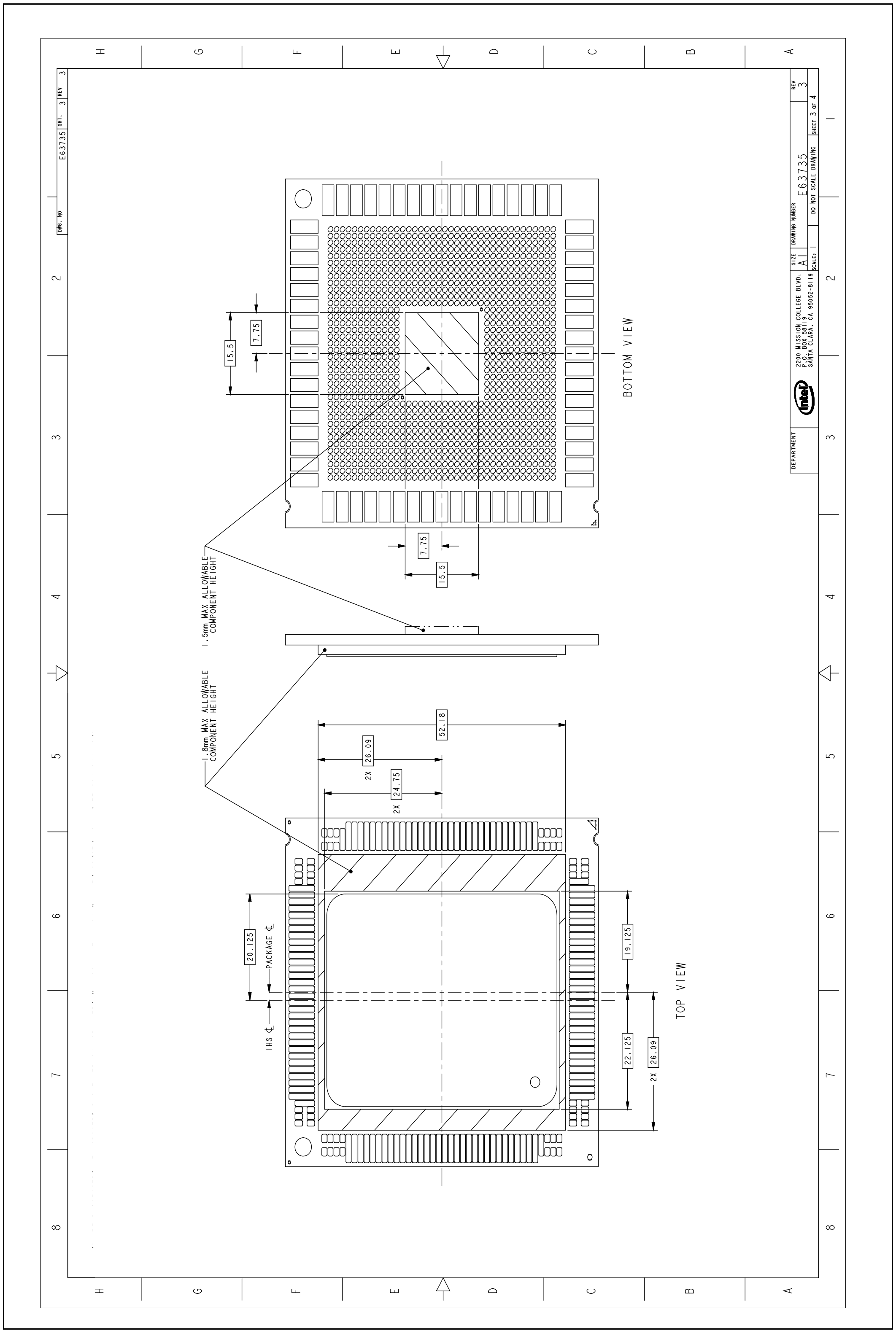
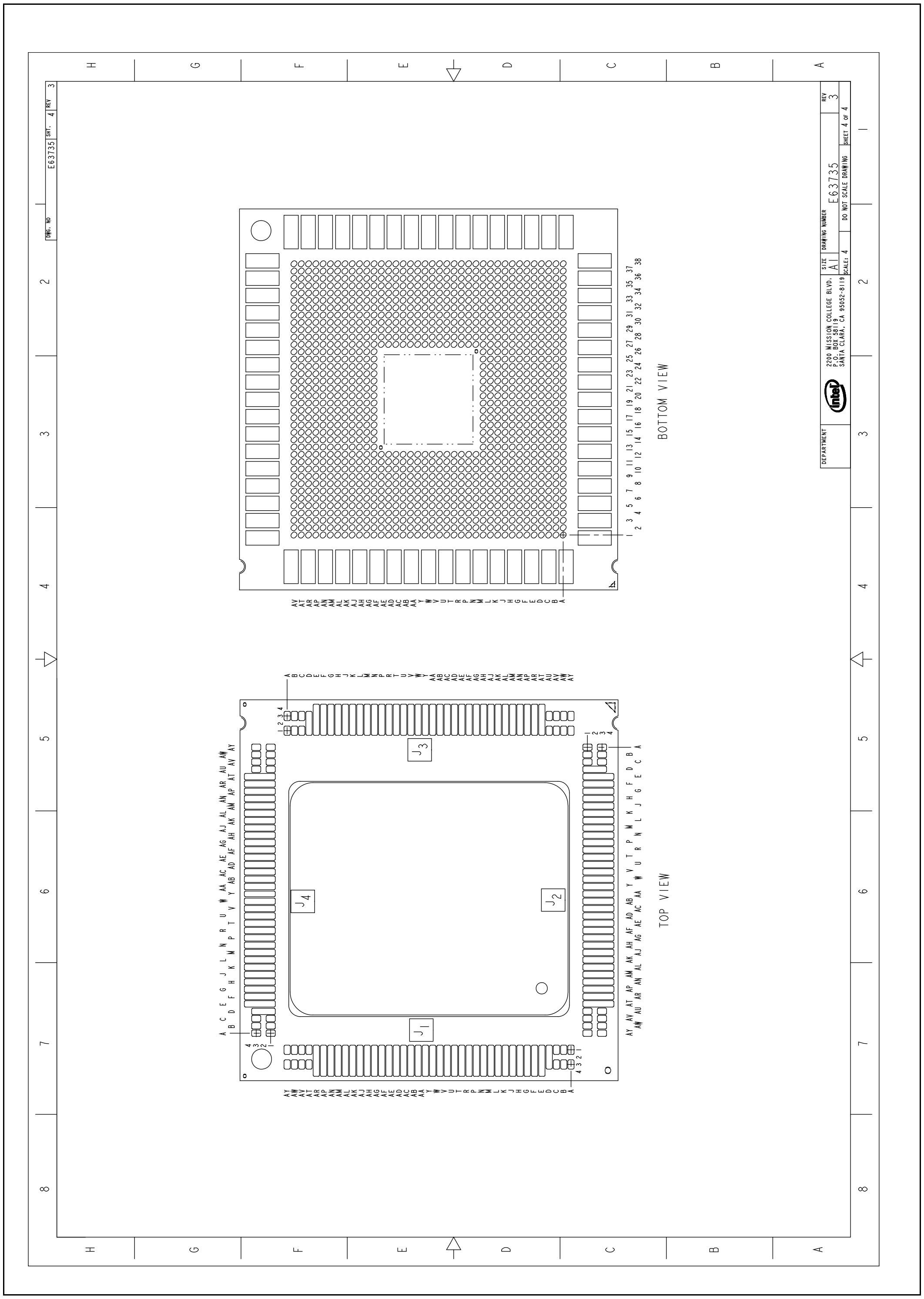


Figure 4-9. Intel® Itanium® Processor 9500 Series Package Drawing (Sheet 4 of 4)



4.3 Processor Component Keepout Zones

The processor may contain components on the substrate that define component keepout zone requirements. A thermal and mechanical solution design must not intrude into the required keepout zones. Decoupling capacitors are typically mounted to both the top-side and bottom-side of the package substrate. See Figure 4-4 for Intel® Itanium® 9300 Series Processor keepout zones and Figure 4-8 for Intel® Itanium® 9500 Series Processor keepout zones.

4.4 Package Loading Specifications

Table 4-1 provides dynamic and static load specifications for the processor package. These mechanical load limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Also, any mechanical system or component testing should not exceed the maximum limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solutions.

Table 4-1. Processor Loading Specifications

Parameter	Maximum	Unit	Notes
Static Compressive Load	1000	N	1, 2, 3
Dynamic Compressive Load t < 30 ms	1793	N	1, 3
Transient t < 1 s	1090	N	1, 3

Notes:
1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the allowable static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. These parameters are based on limited testing for design characterization. Loading limits are for the package only and do not include the limits of the processor socket.

4.5 Package Handling Guidelines

Table 4-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 4-2. Package Handling Guidelines

Parameter	Maximum Recommended	Unit	Notes
Shear	356	N	1, 4
Tensile	156	N	2, 4
Torque	8	N-m	3, 4

Note:
1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. A tensile load is defined as a pulling load applied to the IHS in the direction normal to the IHS surface.
3. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.
4. These guidelines are based on limited testing for design characterization.

The Intel® Itanium® Processor 9300 Series can be inserted into and removed from a LGA1248 socket and engaged and disengaged with the Ararat voltage regulator up to a maximum limit as specified in Table 4-3.

Table 4-3. Processor Package Insertion Specification

Package	Durability Limit
1248-Land FCLGA	15

4.6 Processor Mass Specifications

The typical mass of the Intel® Itanium® Processor 9300 Series and 9500 Series is 55 g. This mass [weight] includes all the components that are included in the package.

4.7 Processor Materials

Table 4-4 lists some of the package components and associated materials.

Lead and other materials banned in Restriction on Hazardous Substances (RoHS) Directive are either (1) below all applicable substrate thresholds as proposed by the EU or (2) an approved/pending exemption applies.

Note: RoHS implementation details are not fully defined and may change.

Table 4-4. Package Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plating over Copper
Substrate	Fiber-Reinforced Resin
Package Lands	Gold Plating over Nickel

4.8 Package Markings

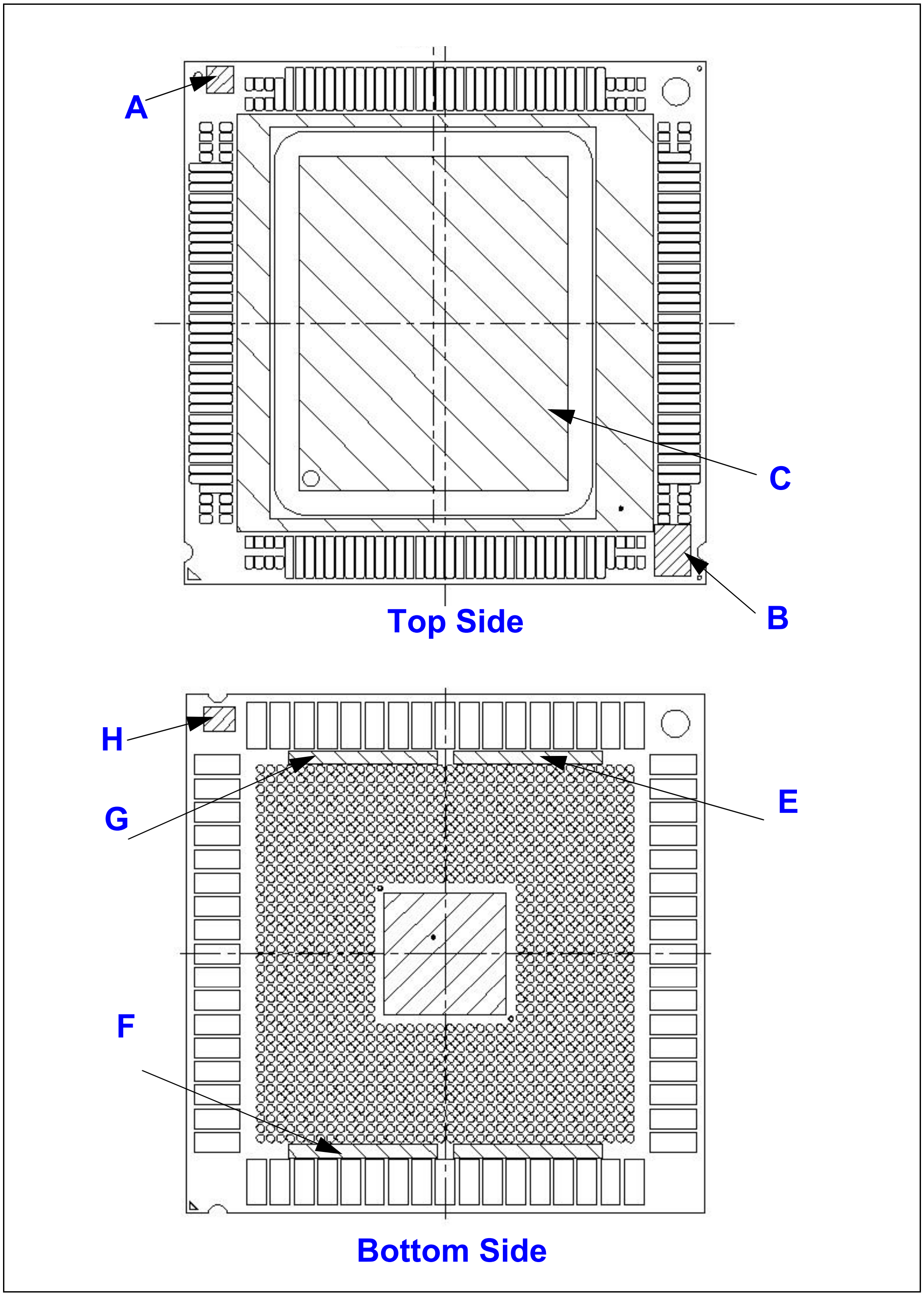
Bottom side marks on the package substrate provide the necessary processor identification and tracking information. This information is captured in Table 4-5 and their locations are illustrated in Figure 4-10.

Table 4-5. 1248 FCLGA Package Marking Zones

Zone	Engineering Samples	Production Units
Zone A	2D Matrix Mark: VID	
Zone B	Visual Identification (VID) Mark	
Zone C	Line 1: INTEL CONFIDENTIAL Line 2: Mask and Copy Right Date Codes	Line 1: Product Name Line 2: Mask and Copy Right Date Codes, Lead Free product designator
Zone E	Intel	
Zone F	Finish Process Order (FPO) and Serial #	
Zone G	Processor ID	
Zone H	2D Matrix Mark: Finish Process Order (FPO) and Serial #	

Notes:
1. VID (Visual Identification): Is a unique number which can be used for the purpose of tracking the processor. It is used by Intel to retrieve processor related information.
2. FPO (Finish Process Order): Is a unique number. It can be used for tracking purposes. It is used by Intel to retrieve processor and shipping order information.

Figure 4-10. Processor Marking Zones



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5 Thermal Specifications

This chapter provides the thermal specifications of the Intel® Itanium® Processor 9300 Series and the Intel® Itanium® Processor 9500 Series processors.

The Intel® Itanium® Processor 9300 Series and the Intel® Itanium® Processor 9500 Series processors' power and thermal management is built from four subsystems or components. These are power measurement components, the temperature measurement components, the frequency control components and the voltage control components that work in concert allowing the management system to maximize performance within a given power and thermal envelope. This results in higher average core frequency performance compared to a worst-case fixed frequency. It boosts performance based on application activity. The power and thermal management system is fully integrated within the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series.

The power and thermal management system is designed for repeatable performance under the same operating conditions. It provides several hooks to the OS and system management to monitor and change the processor performance and thermal status. With the power and thermal management system on the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series, typical applications see a higher core frequency, resulting in higher performance.

For the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series, base frequency is based on an activity factor determined by the highest known activity factor in benchmark suites. Boost frequency is available when the processor is not power limited.

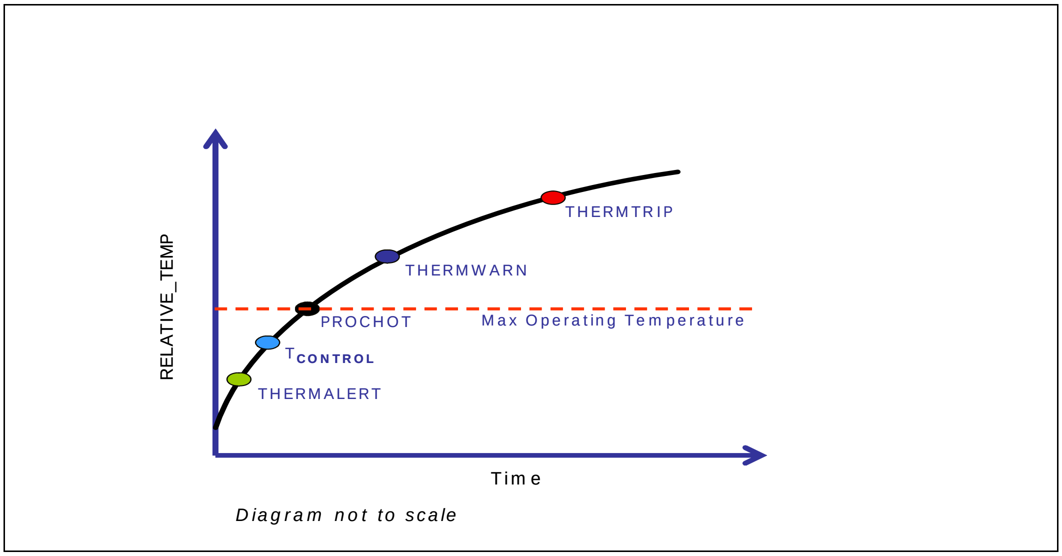
The Intel® Itanium® Processor 9500 Series enables Intel® Turbo Boost Technology featuring sustained boost. Processor performance is optimized for a given power envelope and is integrated into the processor core. Power management optimizes the processor performance for a given TDP “Thermal Design Power”. The core activity levels are monitored in real time, and each core enforces its own AFT “Activity Factor Throttling” to keep the processor at TDP for high activity applications. Instruction dispersal is lowered in a core to keep the activity of the core within TDP when an over TDP condition is detected. AFT is transparent to software running on the processor.

5.1 Thermal Features

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series have internal thermal sensors which sense when a certain temperature is reached on the processor core. These sensors are used to control various thermal states. Figure 5-1 shows an approximate relationship between temperature, time, and the THERMALERT, TCONTROL, PROCHOT, THERMWARN, and THERMTRIP points.

Note: Figure 5-1 is not intended to show an exact relationship in time or temperature as a processor's thermal state advances from one state to the next state. Cooling solution performance degradation and processor workload variations will affect the processor thermal state.

Figure 5-1. Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series' Thermal States



5.1.1 Digital Thermometer

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series uses a thermal sensing device called Digital Thermometer (DT) to read the values from the thermal sensors available on the processor die. The DT also compares these values to a thermal trip point that is hard-wired. Calibration information is used to translate the DT output to processor temperature in degrees Celsius relative to the PROCHOT setpoint. DT readout is available in CSR or via SMBus. When it is below the PROCHOT setpoint the DT readout will have a positive value. The DT has a limited range. It will report out the value of its upper or lower limits when it has reached the limits and set QR_CSR_IPF_THERM_STATUS.valid = 1'b0.

5.1.1.1 Thermal Sensor Accuracy Distribution for the Intel® Itanium® Processor 9300 Series

Table 5-1 shows the processor thermal sensor accuracy with respect to the DT readout for the an Intel® Itanium® Processor 9300 Series. The margin of error is relative to PROCHOT and represents the typical ±3-sigma range. This data is for a large sample of parts. It should be noted that a particular part should be consistent across the entire operating range.

Table 5-1. Thermal Sensor Accuracy Distribution for the Intel® Itanium® Processor 9300 Series (Sheet 1 of 2)

DT Readout	Expected Margin of Error Relative to PROCHOT
0x83 - 0x80, 0x00 - 0x07	±1°C
0x08 - 0x0E	±2°C
0x0F - 0x14	±3°C
0x15 - 0x1B	±4°C
0x1C - 0x22	±5°C
0x23 - 0x29	±6°C

Table 5-1. Thermal Sensor Accuracy Distribution for the Intel® Itanium® Processor 9300 Series (Sheet 2 of 2)

DT Readout	Expected Margin of Error Relative to PROCHOT
0x2A - 0x30	±7°C
0x31 - 0x37	±8°C
0x38- 0x3E	±9°C
0x3F - 0x45	±10°C

5.1.1.2 Thermal Sensor Accuracy Distribution for the Intel® Itanium® Processor 9500 Series

Table 5-2 shows the processor thermal sensor accuracy with respect to the DT readout for the Intel® Itanium® Processor 9500 Series . The margin of error is relative to PROCHOT and represents the typical ±3-sigma range. For the Intel® Itanium® Processor 9500 Series, it is based on presilicon simulation data. It should be noted that a particular part should be consistent across the entire operating range.

Table 5-2. Thermal Sensor Accuracy Distribution for the Intel® Itanium® Processor 9500 Series

DT Readout	Expected Margin of Error Relative to PROCHOT
0x83 - 0x80, 0x00 - 0x03	± 1°C
0x04 - 0x32	± 3°C
0x33 - 0x49	± 5°C

5.1.2 Thermal Management

5.1.2.1 Overview

The Thermal Management controller on the processor will measure the die temperature using thermal sensors placed in several key locations on the die. Each sensor is fed into a central thermometer logic block. For the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series, the central thermometer logic block will report the highest temperature of all sensors. Referring to Figure 5-1, the sequence of steps taken by the processor thermal management system are presented in steps (a) to (d).

a. If $T>=T_{PROCHOT}$ and the Intel® Itanium® Processor 9300 Series is operating at boost frequency, then the thermal management system will instruct the processor to go to base voltage and frequency.

   After a delay, if the processor temperature is below the $T_{PROCHOT}$ threshold, normal operation will resume including the Intel® Itanium® Processor 9300 Series being allowed to operate at boost frequency if appropriate.

   If $T>=T_{PROCHOT}$, the Intel® Itanium® Processor 9500 Series thermal management system will reduce the activity factor maximum limit. After a delay, if the processor temperature is below $T_{PROCHOT}$ threshold, normal operation will resume and the previous Intel® Itanium® Processor 9500 Series activity factor maximum limit will be restored.

b. If $T>=T_{PROCHOT}$ and the Intel® Itanium® Processor 9300 Series is already at or below base voltage and frequency, then the thermal management system will assert PROCHOT_N and the processor will enter Single Issue Mode (SIM) and transition to the voltage and frequency of the lowest supported P-state.

A Corrected Machine Check Interrupt (CMCI) is issued when processor enters and exits SIM.

If T>= $T_{PROCHOT}$ the Intel® Itanium® Processor 9500 Series and the activity factor maximum limit is already reduced, then the thermal management system will assert PROCHOT_N and the processor will enter Single Issue Mode (SIM) and transition to the lowest P-state.

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series will remain in this low power mode until the temperature decreases and drops below (TPROCHOT - THYSTERESIS). The processor will be in this low power mode for a minimum of 1 second and after 1 second will resume normal operation as soon as the temperature has decreased sufficiently.

c. If T>=$T_{THERMWARN}$, then the processor will issue a fatal MCA *and PROCHOT_N will remain asserted; the thermal management controller becomes non-functional.* The processor cannot recover except via cold reset. The processor will continue to throttle if T>=$T_{PROCHOT}$ when it comes out of reset.

Data integrity is not guaranteed beyond $T_{THERMWARN}$.

d. If T>= $T_{THERMTRIP}$, then the thermal management system will assert THERMTRIP_N and halt processor clocks.

$T_{THERMTRIP}$ *is enforced* to prevent physical damage to the processor.

Cold reset is required to recover.

5.1.2.2 Implementation

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series thermal management features are designed to operate independently of software, including the operating system. The thermal sensors are on the die of the processor and the frequency and voltage control resides completely on the processor. In order to reduce the processor power while throttling, some execution units on the processor are shut down, limiting the processor to executing only one instruction per cycle.

When the PROCHOT threshold is crossed and the processor enters low power mode, a CMCI is sent to the OS and to the System Abstraction Layer (SAL). This interrupt is sent out when entering throttling (CMCI entry) and also when the processor is exiting the SIM phase (CMCI exit) to inform the system of the performance status. Note that the temperature could cool below the throttle trip point but exiting SIM is still subject to the minimum time of 1 second. Information on the CMCI interrupt can be found in the *Intel® Itanium® Processor Family Interrupt Architecture Guide.*

There is a mechanism to bypass the PROCHOT setpoint. When it is bypassed, both the THERMALERT_N and THERMTRIP_N signals, as well as THERMWARN threshold, still operate as normal. There is also a mode that emulates PROCHOT setpoint for testing. The processor can be placed in this mode by a Processor Abstraction Layer (PAL) call. Another PAL call will return the processor to normal operation. These special modes are intended for debug purposes only.

5.1.3 Thermal Alert

THERMALERT_N is a programmable thermal alert signal which is part of the Intel Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series' thermal management system. THERMALERT_N is asserted when the measured temperature from the processor's digital thermometer (DT) is equal to or exceeds QR_CSR_IPF_THERM_CONFIG.thermalert_assert_hot_thresh below PROCHOT. THERMALERT_N will deassert after the DT readout is below PROCHOT by the sum of the values in QR_CSR_IPF_THERM_CONFIG.thermalert_assert_hot_thresh and

QR_CSR_IPF_THERM_CONFIG.thermalert_deassert_thresh. Intel recommends using the values listed in the PIROM when programming QR_CSR_IPF_THERM_CONFIG.thermalert_assert_hot_thresh and QR_CSR_IPF_THERM_CONFIG.thermalert_deassert_thresh. The default values for QR_CSR_IPF_THERM_CONFIG.thermalert_assert_hot_thresh and QR_CSR_IPF_THERM_CONFIG.thermalert_deassert_thresh are 10°C and 4°C respectively for the Intel® Itanium® Processor 9300 Series. For the Intel® Itanium® Processor 9500 Series, the default values are 0°C.

This signal can be used by the platform to implement thermal regulation features such as generating an external interrupt to tell the operating system that the processor core die temperature is increasing.

5.1.4 $T_{CONTROL}$

$T_{CONTROL}$ is a thermal monitoring setpoint which is specified as a relative temperature in degrees Celsius below the PROCHOT_N threshold. The minimum value of the $T_{CONTROL}$ threshold is specified in Table 5-3 for the Intel® Itanium® Processor 9300 Series and Table 5-4 for the Intel® Itanium® Processor 9500 Series, and the default value is available in the PIROM. $T_{CONTROL}$ value applies to the full range of the processor operating power and is independent of the processor core configuration or executed applications. A server thermal management controller can monitor the processor temperature via the Digital Thermal Sensor (DTS) readout, and use the $T_{CONTROL}$ value as the threshold at which active system thermal management must be engaged. This will ensure reliable processor operation over its expected life. Note that no internal response is generated by the processor at $T_{CONTROL}$. Customers can utilize THERMALERT_N as an interrupt to program an alternative temperature monitoring threshold value to provide margin in their cooling solution design. See *Intel® Itanium® Processor 9300 Series Thermal Mechanical Design Guide* for additional guidance on implementing a compliant processor thermal solution.

5.1.5 Thermal Warning

THERMWARN is the temperature beyond which data integrity is not guaranteed and PROCHOT_N remains asserted.

5.1.6 Thermal Trip

The Intel® Itanium® Processor 9300 Series nd Intel® Itanium® Processor 9500 Series protects itself from catastrophic overheating by use of an internal thermal sensor. The sensor trip point is set well above the maximum operating temperature to ensure that there are no false trips. The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series will issue THERMTRIP_N and stop all execution when the junction temperature exceeds a safe operating level. At this point THERMTRIP_N is asserted. If THERMTRIP_N is asserted, processor voltages (VCCCORE, VCCUNCORE, AND VCCCACHE) must be removed within the timeframe defined in Table 2-36.

Data will be lost or corrupt, and transaction time outs will occur if the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series go into thermal trip. The part that shuts down may still have pending snoops or memory reads that the other sockets in the partition may have requested.

Once THERMTRIP_N is asserted, the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series remain stopped until RESET_N is asserted. If the die temperature has dropped below the trip level, a RESET_N pulse can be used to reset the processor. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP_N and remain stopped. It is recommended to allow the processor case temperature to drop below the specified design target before issuing a reset to the processor. Please see Section 5.2 and Table 5-3 for details on the case temperature.

Note: In a partitioned system, sockets in the same partition are in the same coherency domain, so they cannot continue to operate if even one of the processors asserts THERMTRIP_N and shuts down. Moreover, a cold reset is required to get the part back up after a THERMTRIP event. Because cold reset will reset all the sockets in the partition, the other sockets cannot continue running without a reset event.

5.1.7 PROCHOT

The temperature at PROCHOT represents the maximum normal operating temperature of the processor. PROCHOT_N is asserted when the processor temperature is greater than or equal to $T_{PROCHOT}$.

PROCHOT_N is a signal from the processor to the platform indicating that the processor has detected an over-temperature condition and it is taking corrective measures. This pin is not asserted when FORCEPR_N or VR_THERMALERT_N is asserted unless the thermal system has detected a PROCHOT condition independent of those input signals. The condition may occur due to any of the following conditions:

- The thermal environment is outside of the limits defined for full performance operation.
- The processor power consumption is unbalanced due to very high activity factors in some cores coupled with very low activity factors in others.

5.1.8 FORCEPR_N Signal Pin

FORCEPR_N is an input pin that will force the processor into one of two modes. The default mode is the same state as PROCHOT_N. The processor will go into Single Issue Mode (SIM) and also transition to the voltage and frequency of the lowest supported P-state. Time limits and CMCI generation are the same as PROCHOT_N. The second mode, selectable via QR_CSR_IPF_THERM_CONFIG.forcepr_mode, disables SIM and timer functions while maintaining core frequency and voltage throttling. Both modes can be disabled via QR_CSR_IPF_THERM_CONFIG.forcepr_disable.

5.1.9 Ararat Voltage Regulator Thermal Signals

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series package allows the Ararat Voltage Regulator to signal to the platform when it approaches its own thermal limits. The specific signals for this purpose are VR_FAN_N, VR_THERMALERT_N, and VR_THERMTRIP_N.

The processor does not monitor or respond to the VR_FAN_N and VR_THERMTRIP_N pins. The response to VR_THERMALERT_N is to force the processor into the same state as PROCHOT_N. The processor will go into SIM and also transition to the voltage and frequency of the lowest supported P-state. Time limits and CMCI generation are active. This response may be disabled via R_CSR_IPF_THERM_CONFIG.vr_thermalert_disable.

5.2 Package Thermal Specifications and Considerations

This section lists the thermal parameters of the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series package. See Table 5-3 and Table 5-4 for the T_{CASE} design target at Thermal Design Power (TDP) and the minimum Tcontrol specification for the Intel® Itanium® Processor 9300 Series and the Intel® Itanium® Processor 9500 Series, respectively. The case temperature is defined as the temperature measured at the center of the processor substrate on the top surface of the IHS.

Table 5-3. Thermal Specification for the Intel® Itanium® Processor 9300 Series

TDP - Thermal Design Power (W)	Max Operating Temperature (DT Readout)	T_{CASE} (°C) Min	T_{CASE} (°C) @ TDP	Minimum $T_{CONTROL}$ (DT Readout)	Notes
185	0	5	88	5	1, 2, 3, 4, 5
155	0	5	88	5	1, 2, 3, 4, 5
130	0	5	88	5	1, 2, 3, 4, 5

Notes:
1. The processor maximum temperature is reached at $T_{PROCHOT}$. That is when DT readout is equal to zero.
2. Intel recommends that the thermal solution designs target the processor Thermal Design Power (TDP), instead of its spontaneous maximum power consumption.
3. Processor TDP is determined at the T_{CASE} equal to T_{CASE}@TDP
4. Tcase is provided for the purpose of designing a processor compatible thermal solution.
5. The THERMALERT and TCONTROL values are temperature offsets below $T_{PROCHOT}$.

T_{CASE} cannot be used as proxy for power dissipation due to the variation in work load imbalances between cores.

TDPmax is 185 W or 155 W or 130 W depending on the SKU.

The combined max short-term (<250 ms) power for the Ararat supplies (VCC_CORE, VCC_UNCORE and VCC_CACHE) is limited to 230 W, and the total of all supplies is limited to 250 W for the 185 W SKUs.

Table 5-4. Thermal Specification for the Intel® Itanium® Processor 9500 Series Processor

TDP - Thermal Design Power (W)	Max Operating Temperature (DT Readout)	T_{CASE} (°C) Min	T_{CASE} (°C) @ TDP	Minimum $T_{CONTROL}$ (DT Readout)	Notes
170	0	5	78	3	1
130	0	5	78	3	1,2,3,4,5

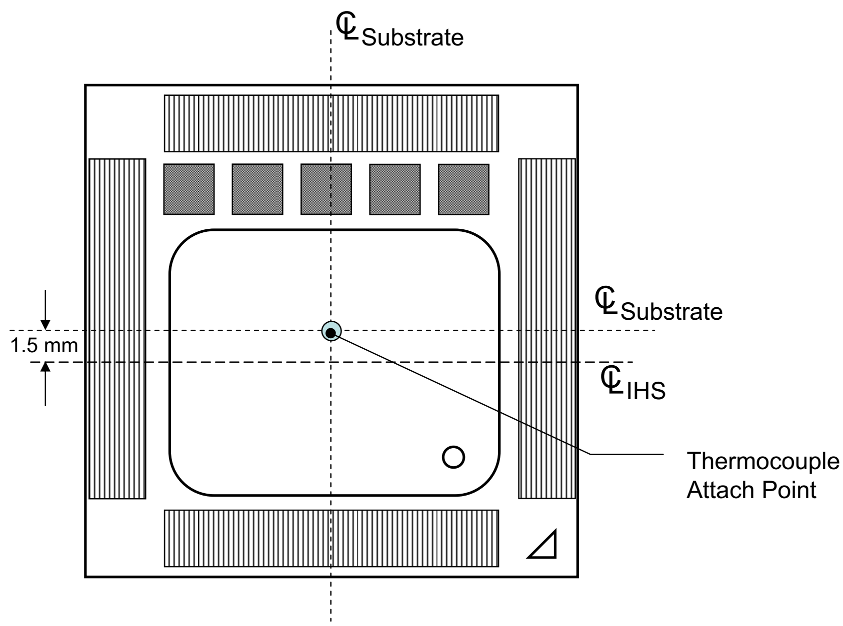
Notes:
1. The processor maximum temperature is reached at $T_{PROCHOT}$. That is when DT readout is equal to zero.

T_{CASE} cannot be used as proxy for power dissipation due to the variation in work load imbalances between cores.

TDPmax is 170W or 130W depending on the SKU.

Figure 5-2 contains dimensions for the thermocouple location on the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series. This location must be used for the placement of a thermocouple for case temperature measurement.

Figure 5-2. Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series Package Thermocouple Location



Not to scale.

Note: Refer to the Package Mechanical Drawings in Chapter 4.

5.3 Storage Conditions Specifications

Environmental Storage Condition limits define the temperature and relative humidity limits to which the device is exposed to while being stored. The specified storage conditions are for component level prior to installation onto board.

Non operating storage condition limits for the component once installed onto the application board are not specified. Intel does not conduct component level certification assessments post subsequent applications such as components sub-assembly (FRU: Field Replaceable Unit), or installation onto a board given the multitude of attach methods, and board types used by customers. Provided as general guidance only, Intel® board products are specified and certified to meet the following temperature and humidity limits (Non-Operating Temperature Limit: -40°C to 70°C and Humidity: 50% to 90%, non condensing with a maximum wet bulb of 28°C).

Table specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality and reliability may be affected.

Table 5-5. Storage Condition Ratings

Symbol	Parameter	Min	Max	Notes
$T_{abs\ storage}$	The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-55°C	125°C	1, 2, 3, 4
$T_{sustained\ storage}$	The minimum/maximum device storage temperature for a sustained period of time.	-5°C	40°C	1, 2, 3, 4
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	-	60% @ 24°C	1, 2, 3, 4
$T_{imesustained\ storage}$	A prolonged or extended period of time; typically associated with sustained storage conditions.	0 months	12 months	1, 2, 3, 4

Notes:
1. Storage conditions are applicable to storage environments only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
2. These ratings apply to the Intel component and do not include the tray or packaging.
3. Failure to adhere to this specification can affect the long-term reliability of the processor.
4. Device storage temperature qualification methods follow JESD22-A119 (low temp) and JESD22-A103 (high temp) standards.

§

6 System Management Bus Interface

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series package includes a system management bus (SMBus) interface. This chapter describes the features of the SMBus and its components.

6.1 Introduction

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series package includes an SMBus interface which allows access to a memory component subdivided into two sections (referred to as the PIROM and the Scratch EEPROM), and sideband access to the processor's control & status registers (CSRs). This chapter is devoted to the PIROM field definitions of the memory component. For details of SMBus transactions used to access processor Control and Status Registers (CSRs), refer to the *RS - Intel® Itanium® 9300 Processor External Design Specification* or the *RS - Intel® Itanium® Processor 9500 Series External Design Specification*.

The PIROM consists of the following sections:

- General
- Processor
- Processor Core
- Processor Uncore
- Cache
- Package
- Part Number
- Thermal Reference
- Feature
- Other

Details on each of these sections are described in Section 6.4.

The processor SMBus implementation uses the clock and data signals of the System Management Bus (SMBus) Specification. Layout and routing guidelines are available in the *Intel® Itanium® 9300 Series and Intel® Itanium® 9500 Series Platform Design Guide.*

6.2 SMBus Memory Component

6.2.1 Processor Information ROM (PIROM)

Table 6-1 maps the PIROM offsets to the field definitions, which are described in Section 6.4.

Table 6-1. Processor Information ROM Data (Sheet 1 of 6)

Sec #	Offset	Field Name	Data Type	Description	Example
General					
0	00h	Data Format Revision	Hex	Incremented with PIROM Table revisions	Rev 1.6 = 0x10
1	01h	EEPROM Size	Hex	Size in Bytes	128 bytes = 0080h; that is, 02h[7:0] = 0x00 01h[7:0] = 0x80
2	02h				
3	03h	Processor Data Address	Hex Byte pointer	Pointer to the section of PIROM containing Processor Production Data	0x0F; 0x00 if not present
4	04h	Processor Core Address	Hex Byte pointer	Pointer to the section of PIROM containing Processor Core Data	0x22; 0x00 if not present
5	05h	Processor Uncore Address	Hex Byte pointer	Pointer to the section of PIROM containing Processor Uncore Data	0x2E; 0x00 if not present
6	06h	Processor Cache Address	Hex Byte pointer	Pointer to the section of PIROM containing Processor Cache Data	0x46; 0x00 if not present
7	07h	Package Data Address	Hex Byte pointer	Pointer to the section of PIROM containing Processor Package Data	0x4F; 0x00 if not present
8	08h	Part Number Data Address	Hex Byte pointer	Pointer to the section of PIROM containing Processor Part Number Data	0x56; 0x00 if not present
9	09h	Thermal Reference Data Address	Hex Byte pointer	Pointer to the section of PIROM containing Processor Thermal Reference Data	0x6B; 0x00 if not present
10	0Ah	Feature Data Address	Hex Byte pointer	Pointer to the section of PIROM containing Processor Features Data	0x72; 0x00 if not present
11	0Bh	Other Data Address	Hex Byte pointer	Pointer to the section of PIROM containing Processor “Other” Data	0x7D; 0x00 if not present
12	0Ch	RESERVED	Hex	Reserved for future use	0Ch = 0x00
13	0Dh				0Dh = 0x00
14	0Eh	Checksum	Hex	Add up by byte and take 2's complement	
Processor					
21	15h	Sample/Production	Hex	Identifies sample parts separately from production parts	0x01 = Production 0x00 = Sample
22	16h	Voltage Regulator Type Required	Hex	Identifies Ararat type required	0x00 for Intel® Itanium® Processor 9300 Series, 0x01 for Intel® Itanium® Processor 9500 Series
23	17h	VCCA	4 binary coded decimal (bcd) digits	Processor Analog Voltage Supply in four 4-bit Hex digits (in mV)	1.800V = 1800 17h = 00 18h = 18
24	18h				

Table 6-1. Processor Information ROM Data (Sheet 2 of 6)

Sec #	Offset	Field Name	Data Type	Description	Example
25	19h	VCCA Voltage Tolerance High	2 Hex digits	Total tolerance (DC+AC) in mV	61mV = 3Dh
26	1Ah	VCCA Voltage Tolerance Low	2 Hex digits	Total tolerance (DC+AC) in mV	61mV = 3Dh
27	1Bh	VCCIO Voltage	6 bcd digits	Voltage in six 4-bit Hex digits in mV^-2	1.11250V = 001125 1Bh = 25 1Ch = 11 1Dh = 00
28	1Ch				
29	1Dh				
30	1Eh	VCCIO Voltage Tolerance High	2 Hex digits	Total tolerance (DC+AC) in mV	28 mV = 0x1C
31	1Fh	VCCIO Voltage Tolerance Low	2 Hex digits	Total tolerance (DC+AC) in mV	28 mV = 0x1C
32	20h	RESERVED	Hex	Reserved for future use	0x00
33	21h	Checksum	Hex	Add up by byte and take 2's complement	
Core					
34	22h	Architecture Revision	2 Hex Digits	From CPUID	Taken from CPUID[3].archrev
35	23h	Processor Core Family	2 Hex Digits	From CPUID	Taken from CPUID[3].family
36	24h	Processor Core Model	2 Hex Digits	From CPUID	Taken from CPUID[3].model
37	25h	Processor Core Stepping	2 Hex Digits	From CPUID	Taken from CPUID[3].revision
38	26h	Boost Core Frequency (Intel® Itanium® Processor 9300 Series) Core Count (0x26) RESERVED (0x27) (Intel® Itanium® Processor 9500 Series)	4 bcd digits (Intel® Itanium® Processor 9300 Series) 2 bcd digits (0x26) 2 Hex digits (0x27) (Intel® Itanium® Processor 9500 Series)	Maximum Specified operating frequency of this part in MHz (Intel® Itanium® Processor 9300 Series) Number of available cores in the processor (0x26) (Intel® Itanium® Processor 9500 Series)	1733 MHz = 1733 26h = 33 27h = 17 (Intel® Itanium® Processor 9300 Series) 26h = 08 27h = 0x00 (Intel® Itanium® Processor 9500 Series)
39	27h				
40	28h	Core Voltage ID	4 bcd digits	Voltage in four 4-bit Hex digits (in mV)	1200 mV = 1200h 28h = 00 29h = 12
41	29h				
42	2Ah	Core Voltage Tolerance, High	2 Hex digits	Edge finger tolerance in mV, +	20 mV = 0x14
43	2Bh	Core Voltage Tolerance, Low	2 Hex digits	Edge finger tolerance in mV, -	20 mV = 0x14
44	2Ch	RESERVED	Hex	Reserved for future use	0x00
45	2Dh	Checksum	Hex	Add up by byte and take 2's complement	
Uncore					
46	2Eh	Maximum Intel® QuickPath Interconnect Link Transfer Rate	6 bcd digits	Maximum Intel® QuickPath Interconnect Link Transfer rate for this part in MT/s	4.8 GT/s = 004800 2Eh = 00 2Fh = 48 30h = 00
47	2Fh				
48	30h				

Table 6-1. Processor Information ROM Data (Sheet 3 of 6)

Sec #	Offset	Field Name	Data Type	Description	Example
49	31h	Minimum Intel® QuickPath Interconnect Link Transfer Rate	6 bcd digits	Minimum Intel® QuickPath Interconnect Link Transfer rate for this part in MT/s	4.8 GT/s = 004800 31h = 00 32h = 48 33h = 00
50	32h				
51	33h				
52	34h	Intel® QuickPath Interconnect version Number	4 8-bit ASCII Hex characters	Intel® QuickPath Interconnect version number supported by processor	01.0 = 34h = 0x30 35h = 0x2E 36h = 0x31 37h = 0x30
53	35h				
54	36h				
55	37h				
56	38h	Memory Support flags	Hex	Bit[0] FBD1 Support (LSB) Bit[1] MB1 Support Bit[2] MB2 Support Bits[7:3] (MSBs) reserved 1 = supported, 0 = not supported	0x01 = FB-DIMM 1 only 0x02 = MB1 only 0x03 = FB-DIMM 1 and MB1 supported 0x04 = MB2 only 0x06=MB2 and MB1 support (Intel® Itanium® Processor 9500 Series)
57	39h	Maximum Memory Transfer Rate	6 bcd digits	Maximum Memory Transfer rate for this part in GT/s	800 MT/s = 000800 GT/s 39h = 00 3Ah = 08 3Bh = 00
58	3Ah				
59	3Bh				
60	3Ch	Minimum Memory Transfer Rate	6 bcd digits	Minimum Memory Transfer rate for this part in MT/s	800 MT/s = 000800 GT/s 3Ch = 00 3Dh = 08 3Eh = 00
61	3Dh				
62	3Eh				
63	3Fh	Uncore Voltage ID	4 bcd digits	Voltage in four 4-bit Hex digits (in mV)	1200 mV = 1200 3Fh = 00 40h = 12
64	40h				
65	41h	Uncore Voltage Tolerance, High	2 Hex digits	Edge finger tolerance in mV, +	20 mV = 0x14
66	42h	Uncore Voltage Tolerance, Low	2 Hex digits	Edge finger tolerance in mV, -	20 mV = 0x14
67	43h	RESERVED	Hex	Reserved for future use	42h = 0x00 43h = 0x00
68	44h				
69	45h	Checksum	Hex	Add up by byte and take 2's complement	
Cache					
70	46h	L3 (LLC) Cache Size	4 bcd digits	Size of the Cache, in MB.	24MB = 0024 46h = 24 47h = 00
71	47h				
72	48h	Cache Voltage ID (Intel® Itanium® Processor 9300 Series) RESERVED (Intel® Itanium® Processor 9500 Series	4 bcd digits (Intel® Itanium® Processor 9300 Series) 2 Hex digits (Intel® Itanium® Processor 9500 Series)	Voltage in four 4-bit bcd digits (in mV) (Intel® Itanium® Processor 9300 Series) Reserved for future use (Intel® Itanium® Processor 9500 Series)	1163 mV = 1163 48h = 63 49 = 11 (Intel® Itanium® Processor 9300 Series) 48h = 0x00 49h = 0x00 (Intel® Itanium® Processor 9500 Series)
73	49h				

Table 6-1. Processor Information ROM Data (Sheet 4 of 6)

Sec #	Offset	Field Name	Data Type	Description	Example
74	4Ah	Cache Voltage Tolerance, High (Intel® Itanium® Processor 9300 Series) RESERVED (Intel® Itanium® Processor 9500 Series)	2 Hex digits	Edge finger tolerance in mV, + (Intel® Itanium® Processor 9300 Series) Reserved for future use (Intel® Itanium® Processor 9500 Series)	20 mV = 0x14 (Intel® Itanium® Processor 9300 Series) 4Ah = 0x00 (Intel® Itanium® Processor 9500 Series)
75	4Bh	Cache Voltage Tolerance, Low (Intel® Itanium® Processor 9300 Series) RESERVED (Intel® Itanium® Processor 9500 Series)	2 Hex digits	Edge finger tolerance in mV, - (Intel® Itanium® Processor 9300 Series) Reserved for future use (Intel® Itanium® Processor 9500 Series)	20 mV = 0x14 (Intel® Itanium® Processor 9300 Series) 4Bh = 0x00 (Intel® Itanium® Processor 9500 Series)
76	4Ch	RESERVED	Hex	Reserved for future use	4Ch = 0x00 4Dh = 0x00
77	4Dh				
78	4Eh	Checksum	Hex	Add up by byte and take 2's complement	
Package					
79	4Fh	Package Revision	Five 8-bit ASCII Hex characters	Package Revision Tracking Number	Revision = 0INT3 4Fh = 0x30 50h = 0x49 51h = 0x4E 52h = 0x54 53h = 0x33
80	50h				
81	51h				
82	52h				
83	53h				
84	54h	Substrate Revision Software ID (Intel® Itanium® Processor 9300 Series) RESERVED (Intel® Itanium® Processor 9500 Series)	Hex	2-bit substrate revision number: 2 Bits (MSB) 6 Bits reserved (LSB) (Intel® Itanium® Processor 9300 Series) Reserved for future use for Intel® Itanium® Processor 9500 Series	00b MSB 000000b Reserved (Intel® Itanium® Processor 9300 Series) 0x00 (Intel® Itanium® Processor 9500 Series)
85	55h	Checksum	Hex	Add up by byte and take 2's complement	
Part Numbers					
86	56h	Processor Part Number	Seven 8-bit ASCII Hex Characters	Processor Part Number	PPN = 80603LW 56h = 0x57 = "W" 57h = 0x4C = "L" 58h = 0x33 = "3" 59h = 0x30 = "0" 5Ah = 0x36 = "6" 5Bh = 0x30 = "0" 5Ch = 0x38 = "8"
87	57h				
88	58h				
89	59h				
90	5Ah				
91	5Bh				
92	5Ch				

Table 6-1. Processor Information ROM Data (Sheet 5 of 6)

Sec #	Offset	Field Name	Data Type	Description	Example
93	5Dh	Processor Electronic Signature	16 Digit Hex Number	64 - bit identification number; may have padded zeros.	
94	5Eh				
95	5Fh				
96	60h				
97	61h				
98	62h				
99	63h				
100	64h				
101	65h	Base Core Freq	4 bcd digits	Base Core Frequency for this part	f = 1600 Mhz 65h = 00 66h = 16
102	66h				
103	67h	RESERVED (Intel® Itanium® Processor 9300 Series) Uncore Frequency (Intel® Itanium® Processor 9500 Series)	4 bcd digits	Reserved for future use (Intel® Itanium® processor 9300 series) Nominal operating uncore frequency in MHz (Intel® Itanium® Processor 9500 Series)	67h = 0x00 68h = 0x00 (Intel® Itanium® Processor 9300 Series) 2.4 GHz = 67h=0x00 68h=0x24 (Intel® Itanium® Processor 9500 Series)
104	68h				
105	69h	RESERVED	Hex	Reserved for future use	69h = 0x00
106	6Ah	Checksum	Hex	Add up by byte and take 2's complement	
Thermal Reference					
107	6Bh	THERMALERT_N hot assertion	2 Hex digits	Recommended THERMALERT_N assertion threshold value	10C below PROCHOT_N = 0x0A
108	6Ch	THERMALERT_N hot deassertion hysteresis	2 Hex digits	Recommended THERMALERT_N deassertion threshold value	2C deassert = 0x02 This indicates a THERMALERT_N deassert of 10C + 2C =12C below PROCHOT_N
109	6Dh	Maximum TDP	2 Hex digits	Thermal Design Power Max	185 W = 0xB9
110	6Eh	TCONTROL	2 Hex digits	Default processor thermal monitoring setpoint in C	5C below PROCHOT_N = 0x5
111	6Fh	RESERVED	Hex	Reserved for future use	6Fh = 0x00 70h = 0x00
112	70h				
113	71h	Checksum	Hex	Add up by byte and take 2's complement	

Table 6-1. Processor Information ROM Data (Sheet 6 of 6)

Sec #	Offset	Field Name	Data Type	Description	Example
Features					
114	72h	Processor Core Feature Flags	8 digit Hex number	From CPUID	Flag = 0x4387FBFF 72h = 0xFF 73h = 0xFB 74h = 0x87 75h = 0x43 (Intel® Itanium® Processor 9300 Series)
115	73h	RESERVED (Intel® Itanium® Processor 9500 Series)		Reserved for future use (Intel® Itanium® Processor 9500 Series)	72h = 0x00 73h = 0x00 74h = 0x00 75h = 0x00 (Intel® Itanium® Processor 9500 Series)
116	74h				
117	75h				
118	76h	RESERVED	Hex	Reserved for future use	76h = 0x00 77h = 0x00
119	77h				
120	78h	Package Feature Flags	Hex	Bit[7:4] reserved Bit[3] = THERMALERT_N threshold values present Bit[2] = SCRATCH EEPROM present Bit[1] = Core VID present Bit[0] reserved where a 1 indicates valid data	Flag = 0x000E 78h = 0x0E 79h = 0x00
121	79h				
122	7Ah	RESERVED	Hex	Reserved for future use	7Ah = 0x00
123	7Bh	Number of Devices in TAP Chain	Hex	Bits [7:4] Number Devices in processor TAP chain Bits [3:0] Reserved	5 devices for Intel® Itanium® Processor 9300 Series = 0x50 9 devices for Intel® Itanium® Processor 9500 Series = 0x90
124	7Ch	Checksum	Hex	Add up by byte and take 2's complement	
Other					
125	7Dh	RESERVED	Hex	Reserved for future use	7Dh = 0x00 7Eh = 0x00 7Fh = 0x00
126	7Eh				
127	7Fh				

6.2.2 Scratch EEPROM

Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series support a Scratch EEPROM section, which may be used for other data at the system vendor's discretion. The data in this EEPROM, once programmed, can be write-protected by asserting the active-high SM_WP signal. This signal has a weak pull-down (10 kΩ) to allow the EEPROM to be programmed in systems with no implementation of this signal. The Scratch EEPROM resides in the upper half of the memory component (addresses 80 - FFh). The lower half comprises the Processor Information ROM (addresses 00 - 7Fh), which is permanently write-protected.

6.2.3 PIROM and Scratch EEPROM Supported SMBus Transactions

The PIROM responds to two SMBus packet types: Read Byte and Write Byte. However, since the PIROM is write-protected, it will acknowledge a Write Byte command but ignores the data. The Scratch EEPROM responds to Read Byte and Write Byte commands. Table 6-2 illustrates the Read Byte command. Table 6-3 illustrates the Write Byte command.

In the tables, ‘S’ represents the SMBus start bit, ‘P’ represents a stop bit, ‘A’ represents an acknowledge (ACK), and ‘///’ represents a negative acknowledge (NACK). The shaded bits are transmitted by the PIROM or Scratch EEPROM, and the bits that aren’t shaded are transmitted by the SMBus host controller. In the tables, the data addresses indicate 8 bits.

The SMBus host controller should transmit 8 bits with the most significant bit indicating which section of the EEPROM is to be addressed: the PIROM (MSB = 0) or the Scratch EEPROM (MSB = 1).

Table 6-2.Read Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	S	Slave Address	Read	A	Data	///	P
1	7-bits	1	1	8-bits	1	1	7-bits	1	1	8-bits	1	1

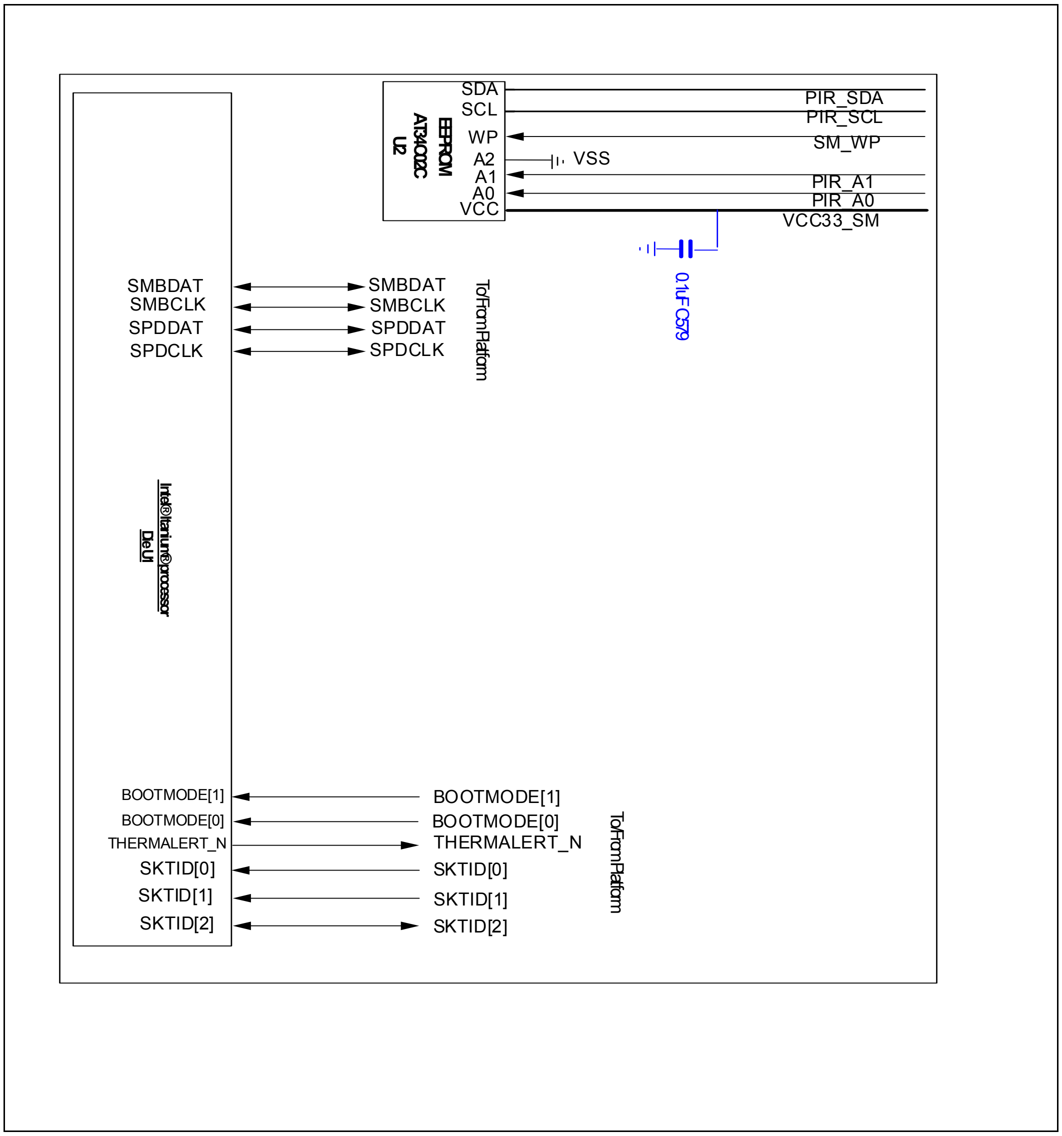
Table 6-3.Write Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	Data	A	P
1	7-bits	1	1	8-bits	1	8-bits	1	1

6.3 Memory Component Addressing

The Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series PIR_A[1:0] pins are used as the memory address selection signals. The processor does not specify the value on these pins. It is left to the system architect to set the SMBus memory map. If the processor is the only device on the bus, these pins may be tied to VSS. PIR_A[2] is tied to VSS internal to the processor. Figure 6-1 shows the address connections within the processor package.

Figure 6-1. Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series Package



6.4 PIROM Field Definitions

PIROM data is divided into sections containing similar data. Each section contains specific fields defined in the following sections.

6.4.1 General

To maintain backward compatibility, the General section defines the starting address for each subsequent section of the PIROM. Software should check for the offset before reading data from a particular section of the ROM.

The General section begins with offset 00h which contains Data Format Revision information, followed by the EEPROM size, both formatted in Hex bytes. The data format revision is used whenever fields within the PIROM are updated with new values. Normally the revision would begin at a value of 1. If a field, or bit assignment within a field, is changed such that software needs to discern between the old and new definition, then the data format revision field should be incremented.

6.4.2 Processor Data

This section contains following pieces of data:

- Sample or Production field to identify a pre-production sample or a production unit.
- Required voltage regulator field
- VCCA and VCCIO voltage specs.

The sample or production field is a two-bit, LSB-aligned value. 0x00 indicates unlocked PIROM section. This is the case in most samples. 0x01 indicates a locked PIROM section. Some samples and all production parts will be locked.

The required voltage regulator field for the Intel® Itanium® Processor 9300 Series is 0x00. The required voltage regulator field for the Intel® Itanium® Processor 9500 Series is 0x01.

6.4.3 Processor Core Data

This section contains silicon-related data relevant to the processor cores.

6.4.3.1 CPUID

Offset 22h-25h contains a copy of the results in EAX[31:0] from Function 1 of the CPUID instruction.

6.4.3.2 Boost Core Frequency

Offset 26h-27h provides the boost core frequency for the processor. The frequency should equate to the markings on the processor even if the parts are not limited or locked to the intended speed. Format of this field is in MHz, rounded to a whole number, and encoded as four 4 bit-bcd digits. Offset 26h contains the core count for the Intel® Itanium® Processor 9500 Series, while offset 27h is RESERVED for the Intel® Itanium® Processor 9500 Series.

Example: For the Intel® Itanium® processor 9300 series, the 1733 GHz processor will have a value of 1733. For the Intel® Itanium® Processor 9500 Series eight core SKU, 0x26 will have a value of 8.

6.4.3.3 Core Voltage

Offset 28h-29h is the nominal core voltage for this part, rounded to the next thousandth, is in mV and is reflected in bcd.

Example: 1500 mV is represented as 1500.

6.4.3.4 Core Voltage Tolerance

Offsets 2Ah and 2Bh contain the core voltage tolerances, high and low respectively. These use a decimal to Hexadecimal conversion.

Example: 19 mV tolerance would be saved as 13h.

6.4.4 Processor Uncore Data

This section contains silicon-related data relevant to the processor Uncore.

6.4.4.1 Maximum Intel® QuickPath Interconnect Link Transfer Rate

Offset 2Eh-30h provides maximum operating link transfer rate for the Intel® QuickPath Interconnect. A link rate of 4.8 GT/s is expressed as 6 bcd digits in MT/s.

Example: 4.8 GT/s = 004800.

6.4.4.2 Minimum Operating Intel® QuickPath Interconnect Link Transfer Rate

Offset 31h-33h provides minimum “operating” link transfer rate for the Intel® QuickPath Interconnect. Systems may need to read this offset to decide if all installed processors support the same link transfer rate. This does not relate to the “link power up” transfer rate of 1/4th Ref Clk. This value is represented by 6 bcd digits.

6.4.4.3 Intel® QuickPath Interconnect Version Number

Offset 34h-37h provides the Intel® QuickPath Interconnect Version Number as four 8-bit ASCII characters.

Example: The Intel® Itanium® Processor 9300 Series processor supports Intel® QuickPath Interconnect Version Number 1.0. Therefore, offset 34h-37h has an ASCII value “01.0”, in reverse order.

34h: 30h, 35h: 2E, 36h: 31h, 37h: 30h.

6.4.4.4 Memory Type Support

Offset 38h signifies the type of memory support for this processor and platform.

A 01h signifies FBD1 support only (for Intel® Itanium® Processor 9300 Series), 02h is Intel® 7500 Scalable Memory Buffer support only, and 04h represents support for Intel® 7510/7520 Scalable Memory Buffers (Intel® Itanium® Processor 9500 Series) only. A 06h represents support for both Intel® 7500 Scalable Memory Buffer and Intel® 7510/7520 Scalable Memory Buffers.

6.4.4.5 Maximum Memory Transfer Rate

Offset 39h-3Bh provides maximum memory transfer rate on the Intel® Scalable Memory Interconnect (Intel® SMI). Systems may need to read this offset to decide if processors and Intel® 75xx Scalable Memory Buffers support the same Intel® SMI transfer rate. Six 4-bit BCD digits are used to provide the maximum transfer rate in MT/s.

Example: A speed of 4.8 GT/s is shown as 004800h.

6.4.4.6 Minimum Memory Transfer Rate

Offset 3Ch-3Eh provides minimum “operating” memory transfer rate on the Intel® Scalable Memory Interconnect. Six 4-bit BCD digits are used to provide the minimum transfer rate in MT/s.

6.4.4.7 Uncore Voltage

Offset 3Fh-40h is the nominal processor Uncore voltage for this part, rounded to the next thousandthin mV and reflected in BCD.

Example: 1200 mV is stored as 3Fh: 00h, 40h: 12h.

6.4.4.8 Uncore Voltage Tolerance

Offset 41h and 42h contain the Uncore voltage tolerances, high and low respectively. These use a decimal to Hexadecimal conversion. Example: 20 mV tolerance would be saved as 14h.

6.4.5 Cache Data

This section contains cache related data.

6.4.5.1 L3 Cache Size

Offset 46h-47h is the L3 cache size field. The field reflects the size of the level three cache in MBytes in bcd format.

Example: The Intel® Itanium® Processor 9300 Series has a 24 MB L3 cache. Thus, offsets 46h & 47h will contain 24 & 00 respectively.

6.4.5.2 Cache Voltage

Offset 48h-49h is the nominal processor cache voltage for the Intel® Itanium® Processor 9300 Series processor, rounded to the next thousandth, in mV and is reflected in bcd.

These fields are RESERVED for the Intel® Itanium® Processor 9500 Series.

6.4.5.3 Cache Voltage Tolerance

Offset 4Ah and 4Bh contain the cache voltage tolerances, high and low respectively. These use a decimal to Hexadecimal conversion.

Example: 20 mV tolerance would be saved as 14h.

These fields are RESERVED for the Intel® Itanium® Processor 9500 Series.

6.4.6 Package Data

6.4.6.1 Package Revision

This section describes the package revision location at offset 4Fh-53h used to capture package technology. This field tracks the highest level revision. It is provided in ASCII Hex format of five characters.

This field is at offset 4Fh through 53h for the substrate layout design.

6.4.6.2 Substrate Revision Software ID

This field is at offset 54h for the substrate layout design for the Intel® Itanium® Processor 9300 Series.

The field at offset 54h is reserved for the Intel® Itanium® Processor 9500 Series.

6.4.7 Part Number Data

This section between 56h and 6Ah provides part tracing ability. It also includes the processor's base frequency at 65h-66h.

6.4.7.1 Processor Part Number

Offset 56h-5Ch contains seven ASCII characters reflecting the Intel part number for the processor. This information is typically marked on the outside of the processor. If the part number is less than 7 characters, a leading space is inserted into the value.

Example: A processor with a part number of 80546KF will have data as 46h, 4bh, 36h, 34h, 35h, 30h, 38h starting at offset 56h.

6.4.7.2 Processor Electronic Signature

Offset 5Dh-64h contains a unique 64-bit identification number.

6.4.7.3 Base Frequency (Core)

Offset 65h-66h contain a bcd representation of core base frequency.

Example: A processor with a core base frequency of 1600 MHz will have data as 00, 16 starting at offset 65h.

6.4.7.4 Base Frequency (Uncore)

Offset 67h-68h contain the uncore frequency for the Intel® Itanium® Processor 9500 Series.

Example: a processor with an uncore frequency of 2.4 GHz will have data as 00, 24 starting at offset 67h.

6.4.8 Thermal Reference Data

6.4.8.1 Recommended Thermalert Hot Assertion Byte

Offset 6Bh contains the thermalert threshold expressed as the number of degrees C below the PROCHOT_N (thermal throttling) temperature in Hex format.

6.4.8.2 Recommended Thermalert Hot De-assertion Hysteresis

The de-assertion threshold is expressed as the number of degrees C below the thermalert hot threshold value in Hex format.

Example: reading offset 6Bh=00001010 and 6Ch=0000010, then programming the CSRs with these values means THERMALERT_N will be asserted when junction temperature rises to 10C below the PROCHOT_N (thermal throttle) threshold and will remain asserted until the junction temperature drops to 12°C below the PROCHOT_N threshold.

6.4.8.3 Thermal Design Power

Offset 6Dh is programmed with 2 Hex digits representing the max TDP of the part.

Example: 6Dh = 0xB9 indicates a 185 W part.

6.4.8.4 TControl

Offset 6Eh contains the recommended TControl spec in degrees C below PROCHOT_N temperature in Hex format.

6.4.9 Feature Data

This section provides information on key features that the platform may need to understand without powering on the processor.

6.4.9.1 Processor Core Feature Flags

For the Intel® Itanium® Processor 9300 Series, offset 72h-75h contains a copy of results in EDX[31:0] from Function 1 of the CPUID instruction. These details provide instruction and feature support by product family. These fields are RESERVED for the Intel® Itanium® Processor 9500 Series processor.

6.4.9.2 Package Feature Flags

Offset 78h-79h provides additional feature information from the processor. This field is defined as follows:

Table 6-4. Offset 78h/79h Definitions

Bit	Definition
4-32	Reserved
3	Thermal calibration offset byte present
2	Scratch (OEM) EEPROM present (set if there is a scratch ROM at offset 80 - FFh)
1	Core VID present (set if there is a VID provided by the processor)
0	Reserved

6.4.9.3 Number of Devices in TAP Chain

At offset 7Bh, a 4-bit Hex digit is used to tell how many devices are in the TAP Chain. The four bits are the most significant bits at this offset.

Since Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series processors have one TAP per core plus a sysint TAP, this field would be set to 50h for the Intel® Itanium® Processor 9300 Series processor and 90 for the Intel®

Itanium® Processor 9500 Series. Note that even reduced core count Itanium products (for example, 2-core Intel® Itanium® Processor 9300 Series) will still have all devices on the TAP chain.

6.4.10 Other Data

Addresses 7Dh-7Fh are listed as reserved.

6.4.11 Checksums

The Processor Information section of the ROM includes multiple checksums. Table 6-5 includes the checksum values for each section defined in the 128 byte PIROM section, except the Other Data section.

Table 6-5. 128 Byte PIROM Checksum Values

Section	Checksum Address
General	0Eh
Processor Data	21h
Processor Core Data	2Dh
Processor Uncore Data	45h
Cache Data	4Eh
Package Data	55h
Part Number Data	6Ah
Thermal Reference Data	71h
Feature Data	7Ch
Other Data	None Defined

Checksums are automatically calculated and programmed. The first step in calculating the checksum is to add each byte from the field to the next subsequent byte. The second step is to take the 2's complement of the first step. This value is the checksum.

Example: For a byte string of AA445Ch, the resulting checksum will be B6h.

AA = 10101010 44 = 01000100 5C = 0101100

First step: add the bytes.

AA + 44 + 5C = 01001010

Second step: take 2's complement.

10110101 +1 = 10110110

Checksum is 0xB6.

§

7 Signal Definitions

This Chapter provides an alphabetical listing of all Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series signals. The tables list the signal directions (Input, Output, I/O) and signal descriptions.

For a complete pinout listing including processor specific pins, please refer to Chapter 3, “Pin Listing”.

Table 7-1. Signal Definitions for the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series (Sheet 1 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BOOTMODE[1:0]</td><td>I</td><td>The BOOTMODE[1:0] inputs specify which way the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series will boot. For details on the modes, refer to the Intel® Itanium® Processor 9300 Series External Design Specification or the Intel® Itanium® Processor 9500 Series External Design Specification. To pull any of these inputs high, they should be strapped to VCCIO through a pull-up resistor, and to pull these low, they should be strapped to GND. These pins are sampled during all resets except warm-logic reset.</td></tr>
<tr><td>CPU_PRES[A|B]_N</td><td>I/O</td><td>CPU Present pads. These pins at the top of the package are part of a daisy chain that indicates to the platform that the processor and Ararat are properly installed into the socket.</td></tr>
<tr><td>CPU_PRES[1:4]_N</td><td>I/O</td><td>CPU Present Pads. These pads at the bottom of the package are part of a daisy chain that indicates to the platform that the processor and Ararat are properly installed into the socket. Motherboard routing guidelines for these pins are documented in the Intel® Itanium® 9300 Series Processor and Intel® Itanium® Processor 9500 Series Platform Design Guide.</td></tr>
<tr><td>CSI[5:0]R[P/N]CLK</td><td>I</td><td>The receive clock signals are inputs to the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series and are required to be the same frequency at both ends but may differ by a fixed phase. An Intel® QuickPath Interconnect local receiver port receives a forwarded clock from the transmitter side of the remote port and vice-versa, to maintain timing reference at either end of the link.
<table>
<tr><th>Intel® QuickPath Interconnect</th><th>5:0</th><th>R</th><th>P/N</th><th>CLK0</th></tr>
<tr><td>Interface Name</td><td>Port Number</td><td>Receiver</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Clock0</td></tr>
</table>
Example: CSI4RPCLK represents port 5 clock receive signal and positive bit of the differential pair.</td></tr>
<tr><td>CSI[5:0]T[P/N]CLK</td><td>O</td><td>These transmit clock signals are driven by the processor and are required to be the same frequency at both ends but may differ by a fixed phase. An Intel® QuickPath Interconnect local port transmit side sends a forwarded clock to the receive side of the remote port and vice-versa, to maintain timing reference at either end of the link.
<table>
<tr><th>Intel® QuickPath Interconnect</th><th>5:0</th><th>T</th><th>P/N</th><th>CLK0</th></tr>
<tr><td>Interface Name</td><td>Port Number</td><td>Transmitter</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Clock0</td></tr>
</table>
Example: CSI4TPCLK represents port 5 clock transmit signal and positive bit of the differential pair.</td></tr>
</table>

Table 7-1. Signal Definitions for the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series (Sheet 2 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>CSI[3:0]R[P/N]Dat[19:0],
CSI[5:4]R[P/N]Dat[9:0]</td><td>I</td><td>These input data signals provide means of communication between two ports via one uni-directional transfer link (In). The RX links, are terminally ground referenced. The ports [3:0] with [19:0] bit lanes can be configured as a full width link with all 20 active lanes, a half width link with 10 active lanes or as a quarter width link with five active lanes.
<table>
<tr><th>Intel® QuickPath Interconnect</th><th>5:0</th><th>R</th><th>P/N</th><th>DAT[19:0]</th></tr>
<tr><td>Interface Name</td><td>Port Number</td><td>Receiver</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr>
</table>
Example: CSI4RPDAT[0] represents port 5 Data, lane 0, receive signal and positive bit of the differential pair.</td></tr>
<tr><td>CSI[3:0]T[P/N]Dat[19:0],
CSI[5:4]T[P/N]Dat[9:0]</td><td>O</td><td>These output data signals provide means of communication between two ports via one uni-directional transfer link (Out).The links, Tx, are terminally ground referenced. The ports [3:0] with [19:0] bit lanes can be configured as a full width link with 20 active lanes, a half width link with 10 active lanes or as a quarter width link with five active lanes.
<table>
<tr><th>Intel® QuickPath Interconnect</th><th>5:0</th><th>T</th><th>P/N</th><th>DAT[19:0]</th></tr>
<tr><td>Interface Name</td><td>Port Number</td><td>Transmitter</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr>
</table>
Example: CSI4TPDAT[0] represents port 5 Data, lane 0, transmit signal and positive bit of the differential pair.</td></tr>
<tr><td>ERROR[0]_N</td><td>O</td><td>Side band signaling for system management.
Refer to the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series Platform Design Guide for pin considerations.</td></tr>
<tr><td>ERROR[1]_N</td><td>O</td><td>Side band signaling for system management. Assertion on this pin indicates that an error reset response is required from the platform.
Refer to the Intel® Itanium® Processor 9300 Series and Intel® Itanium® Processor 9500 Series Platform Design Guide for pin considerations.</td></tr>
<tr><td>FBD0NBICLK[A/B][P/N]0</td><td>I</td><td>These differential pair clock signals generated from the branch zero, channel A and B of FB-DIMMs are input to the processor.
<table>
<tr><th>FB-DIMM</th><th>0</th><th>NB</th><th>I</th><th>CLK</th><th>A/B</th><th>P/N</th></tr>
<tr><td>Interface Name</td><td>Branch Number</td><td>North Bound</td><td>Input</td><td>Clock</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td></tr>
</table>
Example: FBD0NBICLKAP0 represents FB-DIMM branch 0, northbound clock input signal of channel A and positive bit of the differential pair.</td></tr>
</table>

Table 7-1. Signal Definitions for the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series (Sheet 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>FBD1NBICLK[C/D][P/N]0</td><td>I</td><td>These differential pair clock signals generated from the branch one, channel C and D of FB-DIMMs are input to the processor.
<table>
<tr><th>FB-DIMM</th><th>1</th><th>NB</th><th>I</th><th>CLK</th><th>C/D</th><th>P/N</th></tr>
<tr><td>Interface Name</td><td>Branch Number</td><td>North Bound</td><td>Input</td><td>Clock</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td></tr>
</table>
Example: FBD1NBICLKDP0 represent FB-DIMM branch 1, northbound clock input signal of channel D and positive bit of the differential pair.</td></tr>
<tr><td>FBD0SBOCLK[A/B][P/N]0</td><td>O</td><td>These differential pair output clock signals generated from the processor are inputs to the branch zero, channel A and B of FB-DIMMs.
<table>
<tr><th>FB-DIMM</th><th>0</th><th>SB</th><th>O</th><th>CLK</th><th>A/B</th><th>P/N</th></tr>
<tr><td>Interface Name</td><td>Branch Number</td><td>South Bound</td><td>Output</td><td>Clock</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td></tr>
</table>
Example: FBD0SBICLKAP0 represent FB-DIMM branch 0, southbound clock output signal of channel A and positive bit of the differential pair.</td></tr>
<tr><td>FBD1SBOCLK[C/D][P/N]0</td><td>O</td><td>These differential pair output clock signals generated from the processor are inputs to the branch one, channel C and D of FB-DIMMs.
<table>
<tr><th>FB-DIMM</th><th>1</th><th>SB</th><th>O</th><th>CLK</th><th>C/D</th><th>P/N</th></tr>
<tr><td>Interface Name</td><td>Branch Number</td><td>South Bound</td><td>Output</td><td>Clock</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td></tr>
</table>
Example: FBD1SBICLKDP0 represents FB-DIMM branch 1, southbound clock output signal of channel D and positive bit of the differential pair.</td></tr>
<tr><td>FBD[0/1]REFSYSCLK[P/N]</td><td>I</td><td>These signals are no longer used by the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series.</td></tr>
<tr><td>FBD0NBI[A/B][P/N][12:0]</td><td>I</td><td>These differential pair data signals generated from the branch zero, channel A and B of FB-DIMMs are input to the processor.
<table>
<tr><th>FB-DIMM</th><th>0</th><th>NB</th><th>I</th><th>A/B</th><th>P/N</th><th>[12:0]</th></tr>
<tr><td>Interface Name</td><td>Branch Number</td><td>North Bound</td><td>Input</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr>
</table>
Example: FBD0NBIAP[0] represent FB-DIMM branch 0, northbound data input lane 0 signal of channel A and positive bit of the differential pair.</td></tr>
<tr><td>FBD0NBI[A/B][P/N][13]</td><td>I</td><td>These signals are spare lanes, and are intended for Reliability, Availability, and Serviceability (RAS) coverage on the Intel® Itanium® 9500 Processor Series. These signals are not used by Intel® Itanium® 9300 Processor Series.</td></tr>
</table>

Table 7-1. Signal Definitions for the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series (Sheet 4 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>FBD1NBI[C/D][P/N][12:0]</td><td>I</td><td>These differential pair data signals generated from the branch one, channel C and D of FB-DIMMs are input to the processor.
<table>
<tr><th>FB-DIMM</th><th>1</th><th>NB</th><th>I</th><th>C/D</th><th>P/N</th><th>[12:0]</th></tr>
<tr><td>Interface Name</td><td>Branch Number</td><td>North Bound</td><td>Input</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr>
</table>
Example: FBD1NBICP[0] represents FB-DIMM branch 1, northbound data input lane 0 signal of channel C and positive bit of the differential pair.</td></tr>
<tr><td>FBD1NBI[C/D][P/N][13]</td><td>I</td><td>These signals are spare lanes, and are intended for Reliability, Availability, and Serviceability (RAS) coverage on the Intel® Itanium® 9500 Processor Series. These signals are not used by Intel® Itanium® 9300 Processor Series.</td></tr>
<tr><td>FBD0SBO[A/B][P/N][9:0]</td><td>O</td><td>These differential pair output data signals generated from the processor to the branch zero, channel A and B of FB-DIMMs.
<table>
<tr><th>FB-DIMM</th><th>0</th><th>SB</th><th>O</th><th>A/B</th><th>P/N</th><th>[9:0]</th></tr>
<tr><td>Interface Name</td><td>Branch Number</td><td>South Bound</td><td>Output</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr>
</table>
Example: FBD0SBOAP[0] represents FB-DIMM branch 1, southbound data output lane 0 signal of channel A and positive bit of the differential pair.</td></tr>
<tr><td>FBD0SBO[A/B][P/N][10]</td><td>O</td><td>These signals are spare lanes, and are intended for Reliability, Availability, and Serviceability (RAS) coverage on the Intel® Itanium® 9500 Processor Series. These signals are not used by Intel® Itanium® 9300 Processor Series.</td></tr>
<tr><td>FBD1SBO[C/D][P/N][9:0]</td><td>O</td><td>These differential pair output data signals generated from the processor to the branch one, channel C and D of FB-DIMMs.
<table>
<tr><th>FB-DIMM</th><th>1</th><th>NB</th><th>O</th><th>C/D</th><th>P/N</th><th>[9:0]</th></tr>
<tr><td>Interface Name</td><td>Branch Number</td><td>North Bound</td><td>Output</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr>
</table>
Example: FBD1SBOCP[0] represents FB-DIMM branch 1, southbound data output lane 0 signal of channel C and positive bit of the differential pair.</td></tr>
<tr><td>FBD1SBO[C/D][P/N][10]</td><td>O</td><td>These signals are spare lanes, and are intended for Reliability, Availability, and Serviceability (RAS) coverage on the Intel® Itanium® 9500 Processor Series. These signals are not used by Intel® Itanium® 9300 Processor Series.</td></tr>
<tr><td>FLASHROM_CFG[2:0]</td><td>I</td><td>These are input signals to the processor that would initialize and map the Flash ROM upon reset. After reset is deasserted this input would be ignored by the processor logic. These pins are sampled during all resets except warm-logic reset.</td></tr>
<tr><td>FLASHROM_CLK</td><td>O</td><td>The Flash ROM clock.</td></tr>
<tr><td>FLASHROM_CS[3:0]_N</td><td>O</td><td>Flash ROM chip selects. Up to four separate flash ROM parts may be used.</td></tr>
<tr><td>FLASHROM_DATI</td><td>I</td><td>Serial Data Input (from ROM(s) to processor).</td></tr>
<tr><td>FLASHROM_DATO</td><td>O</td><td>Serial Data Output (from processor to ROM(s))</td></tr>
<tr><td>FLASHROM_WP_N</td><td>O</td><td>Flash ROM write-protect.</td></tr>
</table>

Table 7-1. Signal Definitions for the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series (Sheet 5 of 8)

Name	Type	Description
FORCEPR_N	I	When logic 0, forces processor power reduction. Refer to the *Intel® Itanium® 9300 Series Processor and Intel® Itanium® Processor 9500 Series Platform Design Guide* for a detailed signal description.
LRGSCLSYS	I	The header mode is selected by the LRGSCLSYS strapping pin value sampled only during COLD reset. LRGSCLSYS, when tied to VCCIO using a 50 ohm resistor, puts the processor in extended header mode, and LRGSCLSYS, when tied to GND, puts the processor in standard header mode.
MEM_THROTTLE_L	I	When this pin is asserted on the Intel® Itanium® Processor 9300 Series, the internal memory controllers throttle the memory command issue rate to a configurable fraction of the nominal command rate settings. This pin is not used on the Intel® Itanium® 9500 Processor Series.
PIR_SCL	I	(Processor Information ROM Serial Clock): The PIR_SCL input clock is used to clock data into and out of the on package PIROM device. This signal applies to the EEPROM, which is composed of the PIROM and the OEM Scratch PAD.
PIR_SDA	I/O	(Processor Information ROM Serial Data): The PIR_SDA pin is a bidirectional signal for serial data transfer. This signal applies to the EEPROM, which is composed of the PIROM and the OEM Scratch PAD.
PIR_A0, PIR_A1	I	(Processor Information ROM Address[0:1]): The PIR_A[0:1] pins are used as the PIROM memory address selection signals. This bus applies to the EEPROM, which is composed of the PIROM and the OEM Scratch PAD.
SM_WP	I	WP (Write Protect) can be used to write protect the Scratch EEPROM. The Scratch EEPROM is write-protected when this input is pulled high to VCC33_SM.
PRBMODE_REQ_N	I	Input from Extended Debug Port (XDP) to make a probe mode request.
PRBMODE_RDY_N	O	Output to XDP to acknowledge probe mode request.
PROCHOT_N	O	The assertion of PROCHOT_N (processor hot) indicates that the processor die temperature has reached its thermal limit.
PROCTYPE	O	PROCTYPE output informs the platform the processor type. PROCTYPE is tied to VSS internally to indicate the Intel® Itanium® 9300 Processor Series and VCC33_SM internally to indicate the Intel® Itanium® 9500 Processor Series. This pin does not require a platform pull-up or pull-down.
PWRGOOD	I	The processor requires this signal to be a clean indication that all the processor clocks and power supplies are stable and within their specifications. “Clean” implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor. This signal is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET_N	I	Asserting the RESET_N signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. BOOTMODE[0:1] signals are sampled during all RESET_N assertions for selecting appropriate BOOTMODE.
RSVD		These pins are reserved and must be left unconnected.
SKTID[2:0]	I	Socket ID strapping pins. To pull any of these inputs high, they should be strapped to VCCIO, and to pull them low, they should be strapped to VSS. SKTID[2:0] partially determine the node address.
SMBCLK	I	The SMBus Clock (SMBCLK) signal is an input clock to the system management logic which is required for operation of the system management features of the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series processors. This clock is driven by the SMBus controller and is asynchronous to other clocks in the processor. This is an open drain signal. Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series are Slave only.
SMBDAT	I/O	The SMBus Data (SMBDAT) signal is the data signal for the SMBus. This signal provides the single-bit mechanism for transferring data between SMBus devices. This is an open drain signal. Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series are Slave only.

Table 7-1. Signal Definitions for the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series (Sheet 6 of 8)

Name	Type	Description
SPDCLK	I/O	This is a bi-directional clock signal between the processor, DRAM SPD registers and external components on the board. This is an open drain signal. The Intel® Itanium® Processor 9300 Series and 9500 Series Processors are Master only; refer to the *Intel® Itanium® Processor 9300 Series External Design Specification* or *Intel® Itanium® Processor 9500 Series External Design Specification* for limitations.
SPDDAT	I/O	This is a bi-directional data signal between the processor, DRAM SPD registers and external components on the board. This is an open drain signal. Intel® Itanium® Processor 9300 Series and 9500 Series Processors are Master only; refer to the *Intel®* Itanium® Processor 9300 Series External Design Specification or *Intel®* Itanium® Processor 9500 Series External Design Specification for limitations.
SVID_CLK	O	This a source-synchronous clock used by the processor to transmit voltage ID data to the Ararat II voltage regulator. This is an open drain signal. See *Ararat II Voltage Regulator Module Design Guide* for termination requirements for the Intel® Itanium® 9500 Processor Series.
SVID_DATIO	I/0	This is a bi-directional data signal between the Intel® Itanium® 9500 Processor Series and the Ararat II voltage regulator. This is an open drain signal. See *Ararat II Voltage Regulator Module Design Guide* for termination requirements for the Intel® Itanium® 9500 Processor Series.
SVID_ALERT_N	I	This is an asynchronous signal driven by the Ararat II voltage regulator to indicate the need to read the status register. See *Ararat II Voltage Regulator Design Guide* for termination requirements for the Intel® Itanium® 9500 Processor Series.
SYSCLK/SYSCLK_N	I	The differential clock pair SYSCLK/SYSCLK_N provides the fundamental clock source for the processor. All processor link agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of SYSCLK crossing the falling edge of SYSCLK_N. This differential clock pair should not be asserted until VCCA, VCCIO, VCC33_SM, and VCC (12 V Ararat) are stabilized.
SYSUTST_REFCLK/ SYSUTST_REFCLK_N	I	These serve as reference clocks for the processor socket logic analyzer interposer device during debug. It is not used by the processor, and is not connected internally to the die. Electrical specifications on these clocks are identical to SYSCLK/ SYSCLK_N.
TCK	I	Test Clock (TCK) provides the clock input for the processor TAP.
TDI	I	Test Data In (TDI) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	Test Data Out (TDO) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[1]	I	This pin must be tied to VCCIO using a 50 ohm resistor.
TESTHI[2]	I	This pin must be tied to VCCIO using a 50 ohm resistor.
TESTHI[4]	I	This pin must be tied to VCCIO using a 5k ohm resistor.
THERMALERT_N	O	Thermal Alert (THERMALERT_N) is an output signal and is asserted when the on-die thermal sensors readings exceed a pre-programmed threshold.
THERMTRIP_N	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. Thermal Trip will activate at a temperature that is significantly above the maximum case temperature (TCASE) to ensure that there are no false trips. Once activated, the processor will stop all execution and the signal remains latched until RESET_N goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET_N pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP_N and remain stopped.
TMS	I	Test Mode Select (TMS) is a JTAG specification support signal used by debug tools.
TRIGGER[1:0]	I	TRIGGER[1:0] pins are needed for XDP connectivity.
TRST_N	I	Test Reset (TRST_N) resets the TAP logic. TRST_N must be driven electrically low during power on Reset.
VCC33_SM	I	VCC33_SM is a 3.3 V supply to the processor package, required for the PIROM interface on the processor package and also Flash device. This pin must be routed to a 3.3 V supply.

Table 7-1. Signal Definitions for the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series (Sheet 7 of 8)

Name	Type	Description
VCCA	I	VCCA provides a +1.8 V isolated power supply to the analog portion of the internal PLL's. Refer to the Intel® Itanium® Processor 9300 Series and Intel® *Itanium® Processor 9500 Series Platform Design Guide* for routing/decoupling recommendations for VCCA.
VCCCACHE	I	This provides power to the Cache on the Intel® Itanium® 9300 Processor Series. This is on the top of the package and is driven by the Ararat Voltage Regulator. Actual value of the voltage is determined by the settings of VID_VCCCACHE[5:0].
VCCCACHESENSE/ VSSCACHESENSE		Remote sense lines used by the Ararat Voltage Regulator to sense VCCCACHE die voltage. The Voltage Regulator should not draw more than 0.1mA from these pads.
VCCCORE	I	This provides power to the Cores on the processor. This is on the top of the package and is driven by the Ararat Voltage Regulator. Actual value of the voltage is determined by the settings of VID_VCCCORE[6:0].
VCCCORESENSE/ VSSCORESENSE		Remote sense lines used by the Ararat Voltage Regulator to sense VCCCORE die voltage. The Voltage Regulator should not draw more than 0.1mA from these pads.
VCCUNCORE	I	This provides power to the Uncore on the processor. This is on the top of the package and is driven by the Ararat Voltage Regulator. Actual value of the voltage is determined by the settings of VID_VCCUNCORE[6:0].
VCCUNCORESENSE/ VSSUNCORESENSE		Remote sense lines used by the Ararat Voltage Regulator to sense VCCUNCORE die voltage. The Voltage Regulator should not draw more than 0.1mA from these pads.
VCCUNCOREREADY	I	This signal is sent to the processor from the Ararat. When high, the VCCUNCORE rail has completed its startup sequence and is at a nominal operating voltage.
VCCIO	I	VCCIO provides power to the input/output interface on the processor die.
VCCIO_FBD	I	VCCIO_FBD provides power to the FBD_DIMM input/output interface on the processor die.
VFUSERM	I	This pin must be tied to VCCIO or connected to VCCIO via 0 ohm resistor.
VID_VCCCORE[6:0] VID_VCCUNCORE[6:0] VID_VCCCACHE[5:0]	O	VCCCORE_VID, VCCUNCORE_VID and VID_VCCCACHE (Voltage ID) pads are used to support automatic selection of VCCCORE, VCCUNCORE and VCCCACHE by the Intel® Itanium® 9300 Processor Series. The VCCCORE, VCCUNCORE and VCCCACHE Voltage Regulator (Ararat) outputs must be disabled prior to these pins becoming invalid. The VID pins are needed to support processor voltage specification variations. The VCCCORE, VCCUNCORE and VCCCACHE Voltage Regulator (Ararat) outputs must supply the voltage that is requested by these pins, or disable itself.
VR_FAN_N	I/O	This signal is open drain/collector driven by Ararat Voltage Regulator into a pad at the top of the processor package and out through a pin at the bottom of the processor package. When asserted, it indicates that the temperature on the Ararat solution is approximately 10% below the VR_THERMTRIP_N limit. *The Processor cores do not monitor or respond to this signal.* The Platform could monitor this pin to implement thermal management, such as controlling fan speed (airflow). See *Ararat 170W Voltage Regulator Module Design Guide* and /or *Ararat II Voltage Regulator Module Design Guide*for platform-specific requirements.
VR_PROCTYPE[1:0]	O	VR_PROCTYPE output informs the Ararat Voltage Regulator the processor type. These pins are '00 on Intel® Itanium® 9300 Processor Series, and '01 for the Intel® Itanium® 9500 Processor Series. These pads are located at the top of the package. Future processors may use different bit configurations for this bus.
VR_THERMALERT_N	I /O	This signal is open drain/collector driven by Ararat Voltage Regulator into a pad at the top of the processor package and out through a pin at the bottom of the processor package. When asserted, it indicates that the temperature on the Ararat solution is about to exceed the VR_THERMTRIP_N limit. *When enabled in the processor, this signal causes the processor to enter a throttling state to reduce the power consumption level.* The Platform could monitor this pin to implement thermal management. See *Ararat 170W Voltage Regulator Module Design Guide* and/or *Ararat II Voltage Regulator Module Design Guide* for platform requirements on driving this signal.

Table 7-1. Signal Definitions for the Intel® Itanium® Processor 9300 Series and Intel® Itanium® 9500 Series (Sheet 8 of 8)

Name	Type	Description
VR_THERMTRIP_N	I/O	This signal is open drain/collector driven by Ararat Voltage Regulator into a pad at the top of the processor package and out through a pin at the bottom of the processor package. When asserted, it indicates that the temperature on the Ararat solution has exceeded a critical threshold and it is required to shut down the Ararat solution immediately. *The Processor cores do not monitor or respond to this signal.* The Platform should immediately de-assert VROUTPUT_ENABLE0. If the Platform does not respond to this signal, the Ararat Voltage Regulator is permitted to shutdown, but should latch VR_THERMTRIP_N low, which can be reset by a power cycle or de-assertion of VROUTPUT_ENABLE0. VR_THERMTRIP_N trip point is determined by the Ararat Voltage Regulator Module Design and it should be set such that VR_THERMTRIP_N is asserted prior to permanent damage to the Ararat voltage regulator. See *Ararat 170W Voltage Regulator Module Design Guide* and/or *Ararat II Voltage Regulator Module Design Guide* for platform requirements on driving this signal.
VROUTPUT_ENABLE0	I/O	This signal is an input to the processor package (bottom), and drives into the Ararat voltage regulator from the top of the package. When this signal is asserted, the VIDs become active and the voltage regulator's startup sequence begins. When this signal is pulled down, the Ararat Voltage regulator should shut down VCCCORE, VCCUNCORE and VCCCACHE (Intel® Itanium® 9300 Processor Series only). See *Ararat 170W Voltage Regulator Module Design Guide* and/or *Ararat II Voltage Regulator Module Design Guide* for platform requirements on driving this signal.
VRPWRGD (Ararat) /VR_READY (Ararat II)	I /O	This signal is open drain/collector driven by Ararat Voltage Regulator into a pad at the top of the processor package and out through a pin at the bottom of the processor package. When pulled up (active high state), it indicates that the supply voltages to VCCCORE, VCCUNCORE, and VCCCACHE are stable within their voltage specification, and indicates that the Ararat VR start up sequence is completed. This signal will transition to a logic low for power off sequencing and/or any Ararat VR fault condition. See *Ararat 170W Voltage Regulator Module Design Guide* and/or *Ararat II Voltage Regulator Module Design Guide* for platform requirements on pull-up resistors and filtering.
VSS	I	VSS is the ground plane for the processor.
XDPOCPD[7:0]	I/O	Bidirectional XDP data.
XDPOCP_STRB_IN_N	I	Input clock center-aligned with XDPOCP_FRAME_N and XDPOCPD[7:0].
XDPOCP_STRB_OUT_N	O	Output clock edge-aligned with XDPOCP_FRAME_N and XDPOCPD[7:0].
XDPOCP_FRAME_N	I/O	Bidirectional signal indicating valid data on XDPOCPD[7:0].

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