PLL620-28/-29

Low Phase Noise VCXO (for 100-200MHz Fund Xtal)

FEATURES

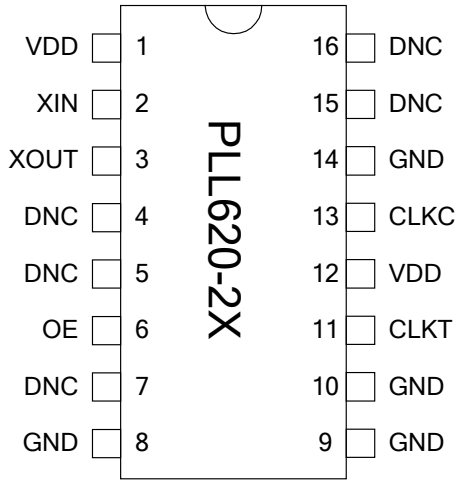
- 100MHz to 200MHz Fundamental Mode Crystal.
- Output range: 100 – 200MHz (no PLL).
- Low Injection Power for crystal 50uW.
- Sub 0.5pS RMS phase jitter (12kHz to 20MHz).
- PECL (PLL620-28) or LVDS output (PLL620-29).
- Supports 2.5V or 3.3V-Power Supply.
- Available in 16-Pin TSSOP.

DESCRIPTION

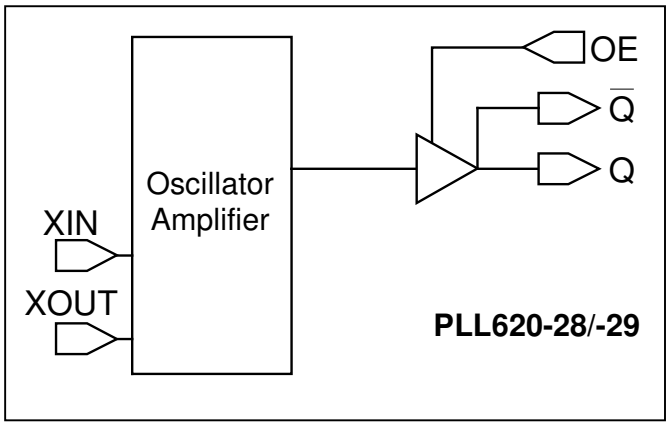
The PLL620-28/-29 family of XO ICs is specifically designed to work with high frequency fundamental and third overtone crystals. They achieve very low current into the crystal, resulting in better stability. Their very low jitter makes them ideal for the most demanding timing requirements.

PIN CONFIGURATION

(Top View)



BLOCK DIAGRAM



OUTPUT ENABLE LOGICAL LEVELS

Part #	OE	State
PLL620-28	0 (Default)	Output enabled
	1	Tri-state
PLL620-29	0	Tri-state
	1 (Default)	Output enabled

OE input: Logical states defined by PECL levels for PLL620-28
Logical states defined by CMOS levels for PLL620-29

PIN DESCRIPTIONS

Name	Pin number	Type	Description
XIN	2	I	Crystal input. See Crystal Specifications on page 2.
XOUT	3	I	Crystal output. See Crystal Specifications on page 2.
OE	6	I	Output enable pin. See Output Enable Logic Levels on page 1.
GND	8, 9, 10, 14	P	Ground.
CLKT	11	O	True output PECL (PLL620-28) or LVDS (PLL620-29)
CLKC	13	O	Complementary output PECL (PLL620-28) or LVDS (PLL620-29).
DNC	4, 5, 7, 15, 16	-	DO Not connect.
VDD	1, 12	P	Power supply.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Built-in Load Capacitance	C_L	IC only, no PCB capacitance included.		4		pF
Shunt Capacitance	C_0				2	pF
Oscillation Frequency	OF	Fund. Or 3rd Overtone	100		200	MHz
Recommended ESR	R_E				30	Ω

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I_{DD}	PECL/LVDS			100/80	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS) @ V_{DD} – 1.3V (PECL)	45 45	50 50	55 55	%
Short Circuit Current				±50		mA

4. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND.		2.5		ps
Period jitter peak-to-peak			18.5		
Accumulated jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles.		2.5		ps
Accumulated jitter peak-to-peak			24		
Integrated jitter RMS at 155MHz	Integrated 12 kHz to 20 MHz		0.3		ps

5. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	155.52MHz	-80	-110	-125	-143	-145	dBc/Hz

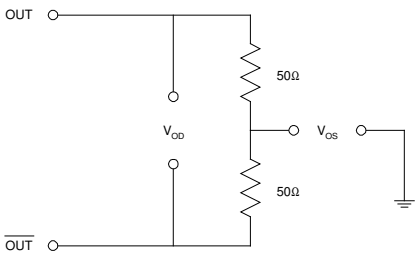
6. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

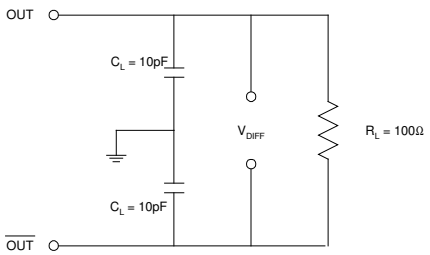
7. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

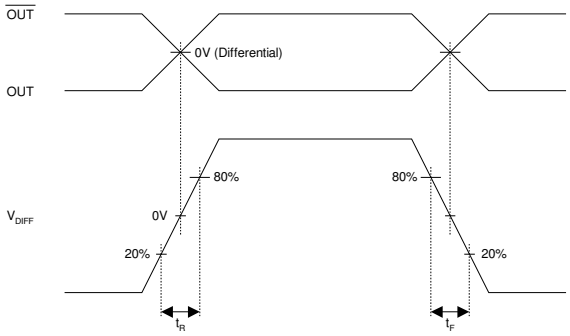
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



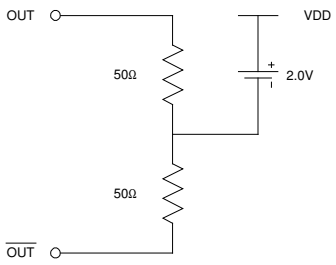
8. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

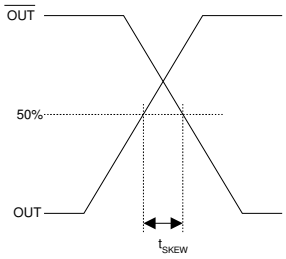
9. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

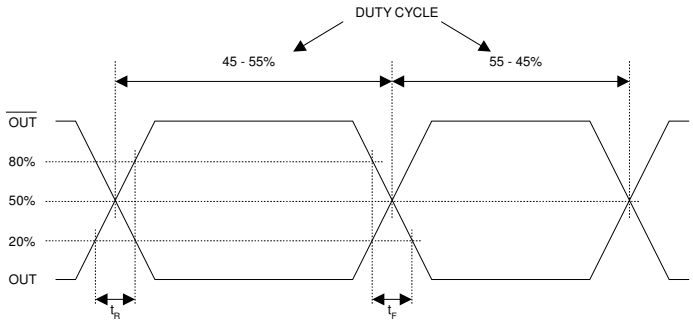
PECL Levels Test Circuit



PECL Output Skew



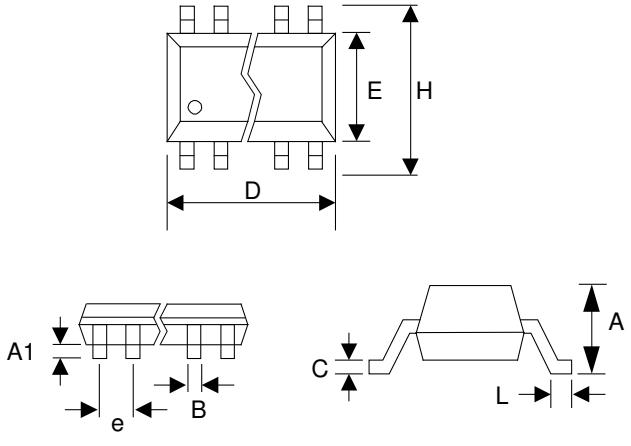
PECL Transistion Time Waveform



Low Phase Noise VCXO (for 100-200MHz Fund Xtal)

PACKAGE INFORMATION

16 PIN TSSOP (mm)		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL620-2X X C L R

PART NUMBER

PACKAGE TYPE
O=TSSOP

NONE= TUBE
R=TAPE AND REEL

NONE=NORMAL PACKAGE
L=GREEN PACKAGE

TEMPERATURE
C=COMMERCIAL,
I=INDUSTRIAL

Part / Order Number	Marking	Package Option	Temperature
PLL620-2XOC-R	P620-2XOC	TSSOP -Tape and Reel	0 to +70□C
PLL620-2XOC	P620-2XOC	TSSOP–Tubes	0 to +70□C
PLL620-2XOCL-R	P620-2XOCL	TSSOP-Tape and ReeL (GREEN)	0 to +70□C
PLL620-2XOC	P620-2XOCL	TSSOP–Tubes (GREEN)	0 to +70□C

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