

μHVIC™

SOT-23 Single Low-Side Driver IC

Features

- Wide VCC range (5V to 20V)
- CMOS Schmitt-triggered inputs
- Under voltage lockout
- 3.3V logic compatible
- Additional OUT pin
- Output in phase with inputs
- Leadfree, RoHS compliant

Typical Applications

- General purpose gate driver
- Industrial applications
- Switched-mode power supplies

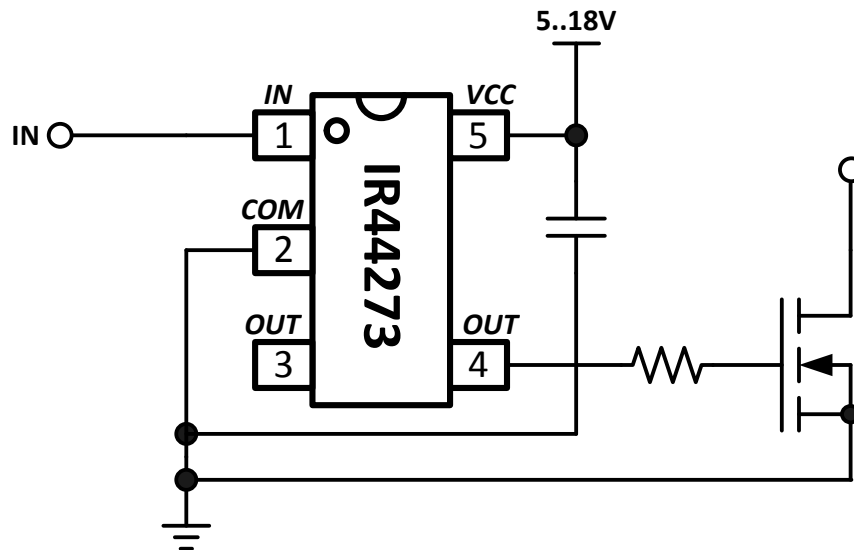
Product Summary

Topology	General Driver
IO+/- (typical)	1.5A

Package Options



Typical Connection Diagram



Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR44273LPBF	SOT23-5	Tape and Reel	3000	IR44273LTRPBF

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Description

The IR44273L is a low-voltage, wide VCC range, power MOSFET and IGBT non-inverting gate driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output driver features a current buffer stage. The design also includes an additional gate drive OUT pin for flexible PCB layout.

Qualification Information[†]

Qualification Level		Industrial ^{††}
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL1 ^{†††} 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)
IC Latch-Up Test		Class 1 Level A (per JESD78)
RoHS Compliant		Yes

- † Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
- †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. The device may not function or not be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_{CC}	Fixed supply voltage	-0.3	20	V
V_O	Output voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage	-0.3	$V_{CC} + 0.3$	
R_{thJA}	Thermal resistance, junction to ambient	—	151	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table.

Symbol	Definition	Min	Max	Units
V_{CC}	Fixed supply voltage	5.0	18	V
V_O	Output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN and EN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Static Electrical Characteristics

$V_{CC} = 15V$, $T_A = 25^\circ C$ unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to input leads: IN. The V_O and I_O parameters are referenced to COM and are applicable to the output leads: OUT.

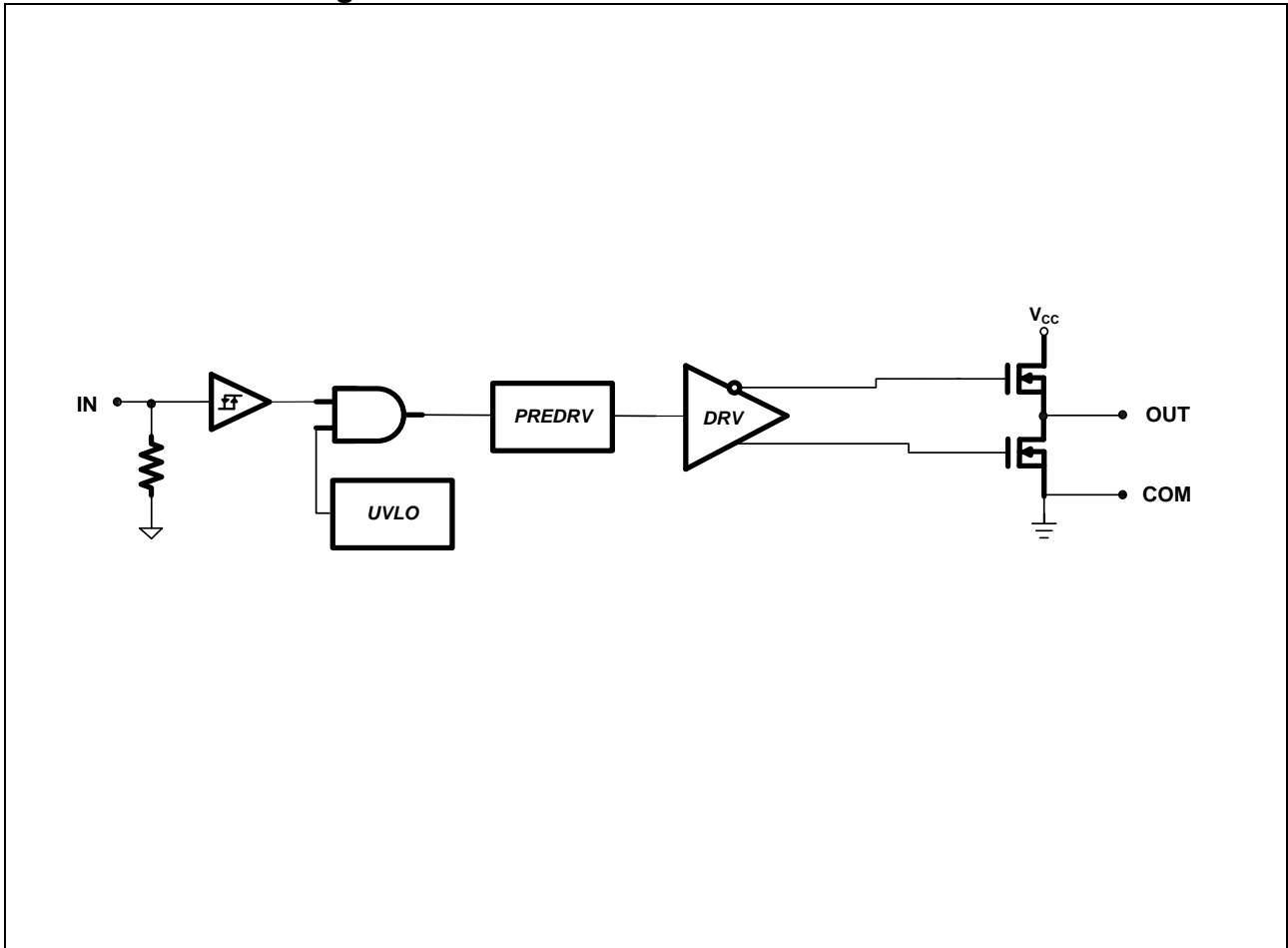
Symbol	Definition	Min	Typ	Max	Units	Test Conditions		
V_{CCUV+}	Vcc supply UVLO positive going threshold	—	—	5.0	V			
V_{CCUV-}	Vcc supply UVLO negative going threshold	4.15	—	—				
V_{CCUVH}	Vcc supply UVLO hysteresis	—	0.3	—				
V_{CLAMP}	Vcc Zener clamp voltage	—	21.4	—			$I_{CC}=5mA$	
V_{IL}	Logic "0" input voltage (OUT = LO)	—	—	0.6			A	
V_{IH}	Logic "1" input voltage (OUT = HI)	2.7	—	—				
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	2.0				
V_{OL}	Low level output voltage, V_O	—	—	0.12	$I_O = 20mA$			
I_{IN+}	Logic "1" input bias current	—	5	15	$V_{IN} = 5V$			
I_{IN-}	Logic "0" input bias current	-30	-10	—	$V_{IN} = 0V$			
I_{OCC}	Quiescent V_{CC} supply current	—	—	400	$V_{IN} = 0V$ or $5V$			
I_{O+}	Output high short circuit pulsed current	—	1.7	—	A	$V_O = 0V, V_{IN} = 5V$		
I_{O-}	Output low short circuit pulsed current	—	1.5	—		$V_O = 15V, V_{IN} = 0V$		

Dynamic Electrical Characteristics

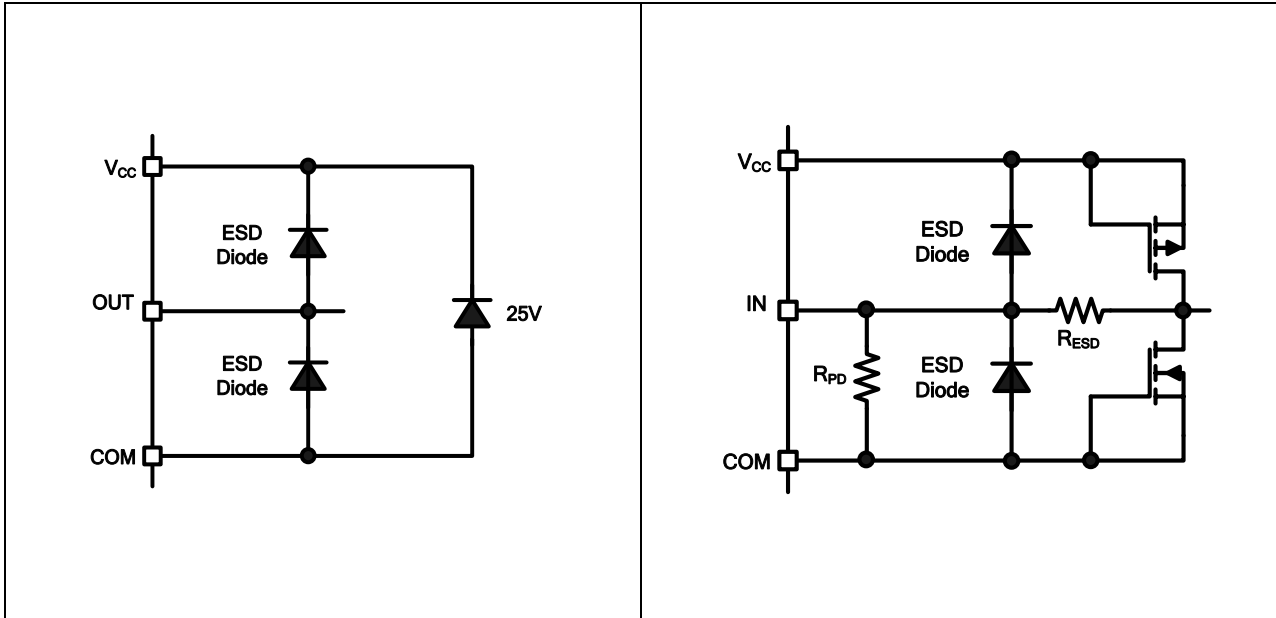
$V_{CC} = 15V$, $T_A = 25^\circ C$, and $C_L = 1000pF$ unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	50	—	ns	Figure 2
t_{off}	Turn-off propagation delay	—	50	—		
t_r	Turn-on rise time	—	10	—		
t_f	Turn-off fall time	—	10	—		

Functional Block Diagram



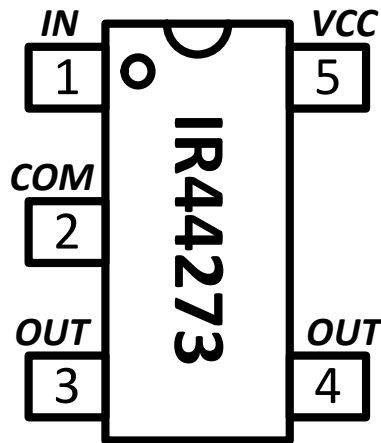
Input/Output Pin Equivalent Circuit Diagrams



Lead Definitions

PIN	Symbol	Description
1	IN	Logic input for gate driver output (OUT), in phase
2	COM	Ground
3	OUT	Gate drive output
4	OUT	Gate drive output
5	VCC	Supply Voltage

Lead Assignments



Timing Diagrams

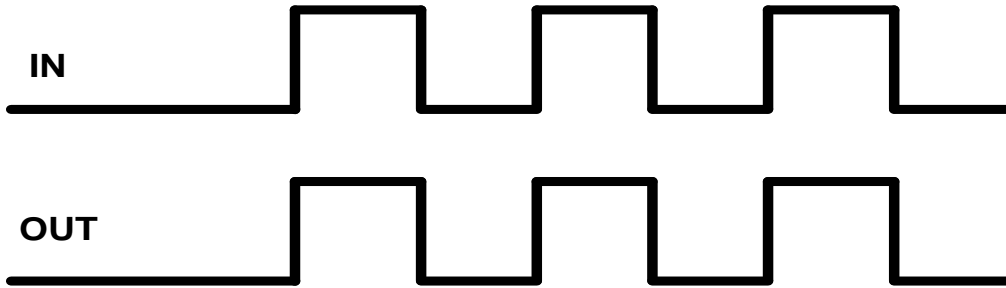


Figure 1: Input/output Timing Diagram

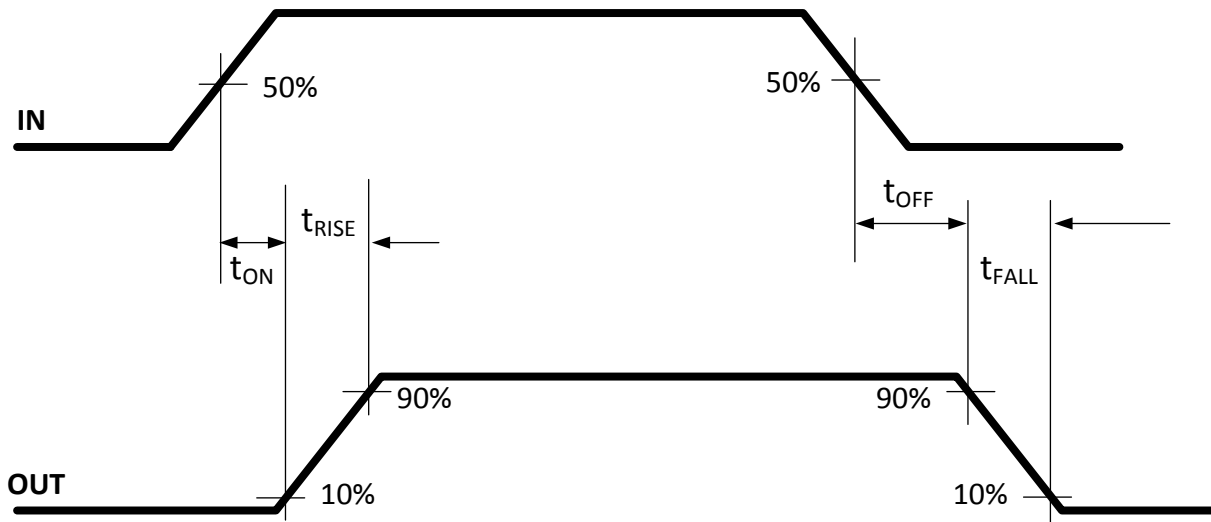
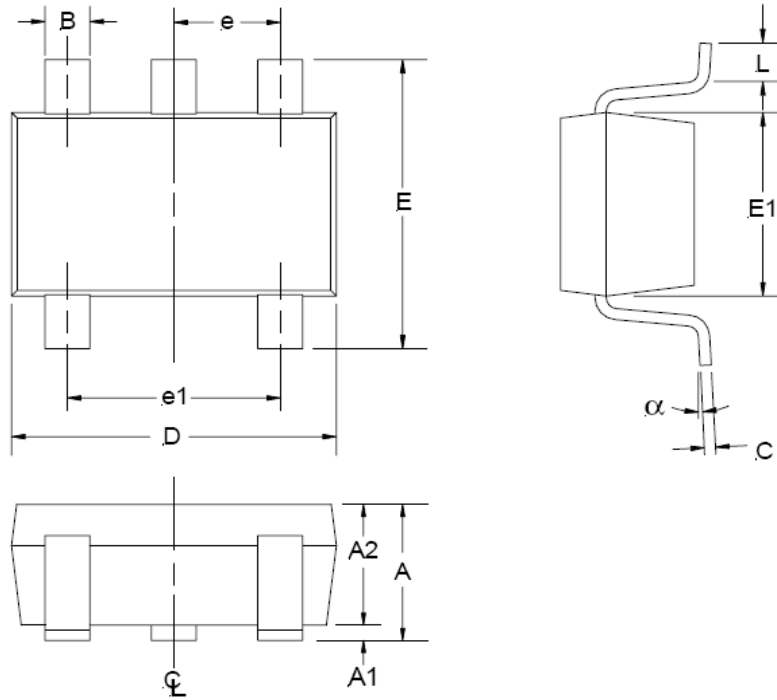


Figure 2: Switching Time Waveform Definitions

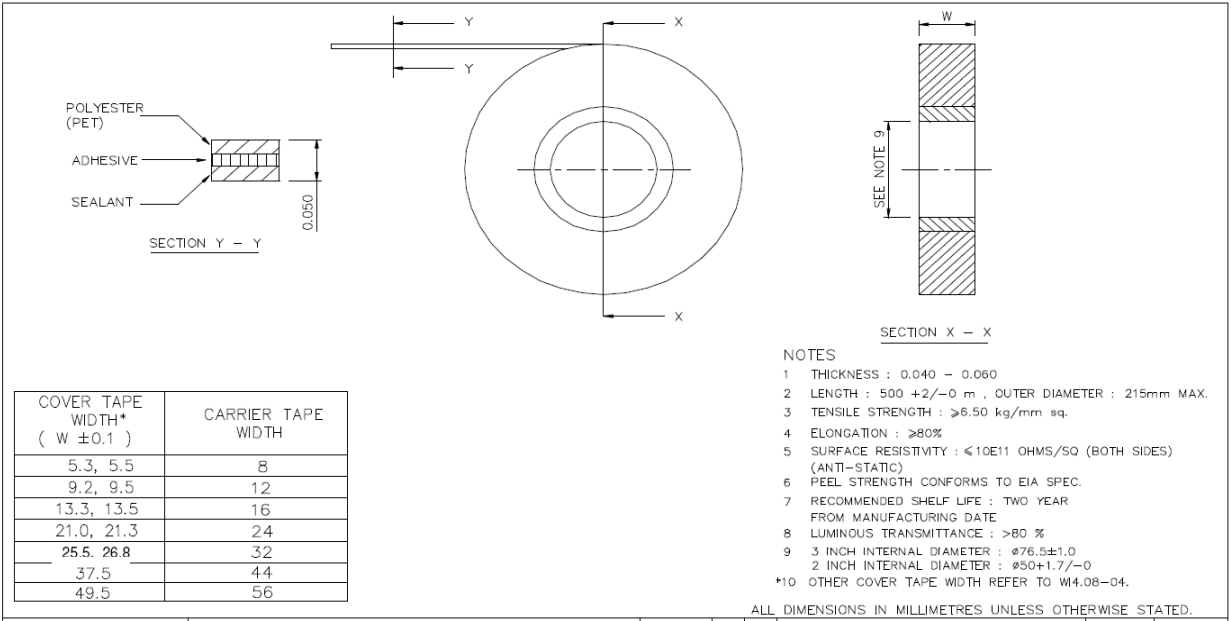
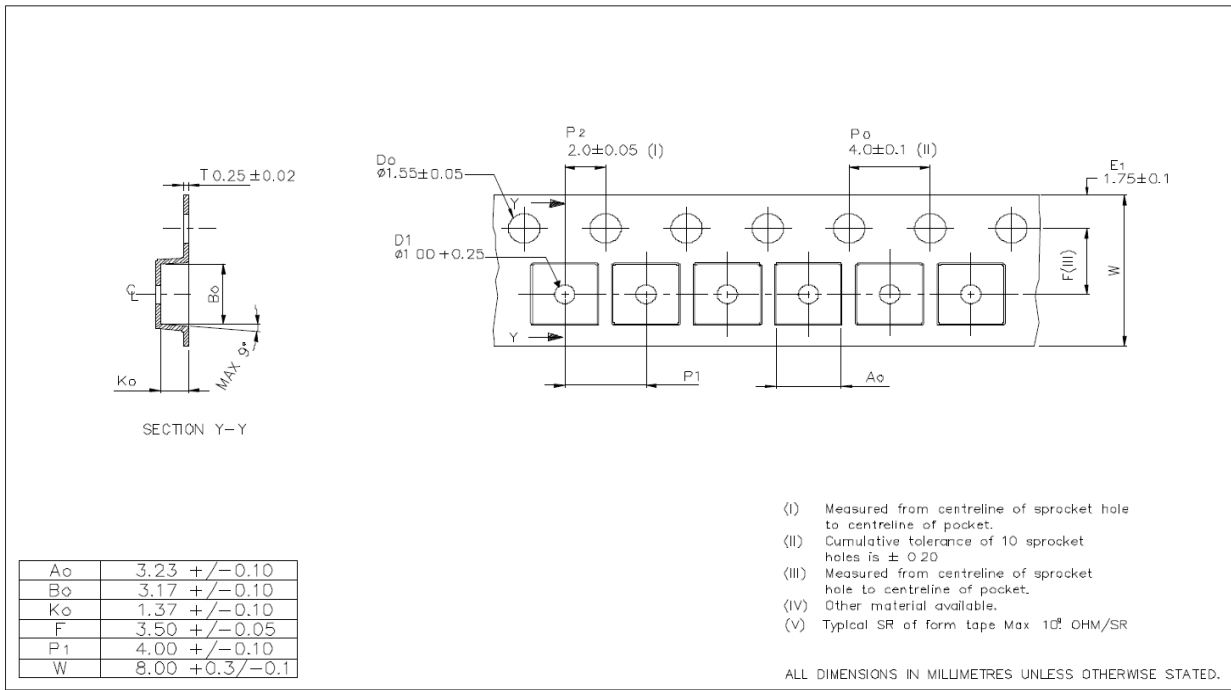
Package Details, SOT23-5



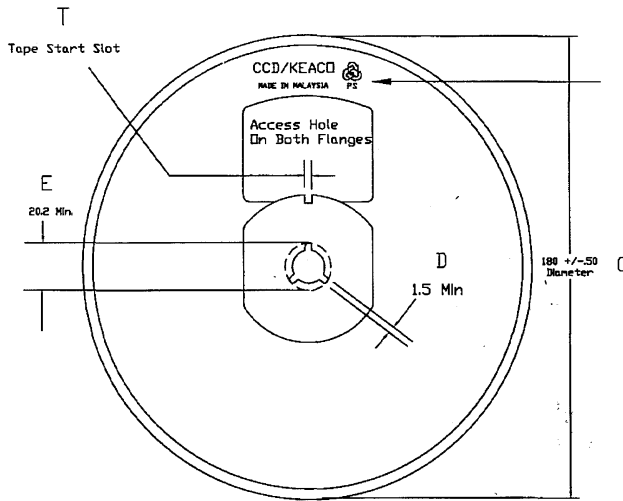
SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.25	0.50
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95 REF	
e1	1.90 REF	
L	0.35	0.55
α	0°	10°

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

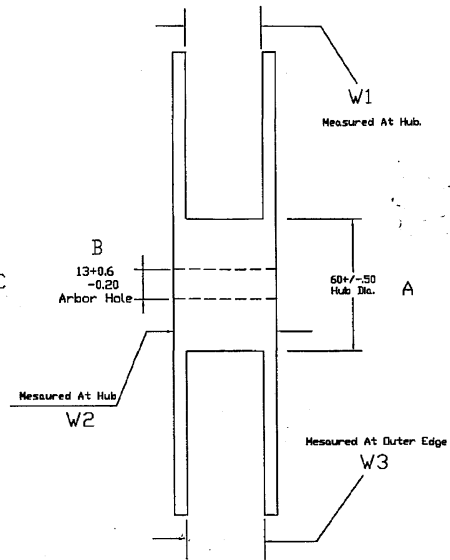
Package details: SOT23-5, Tape and Reel



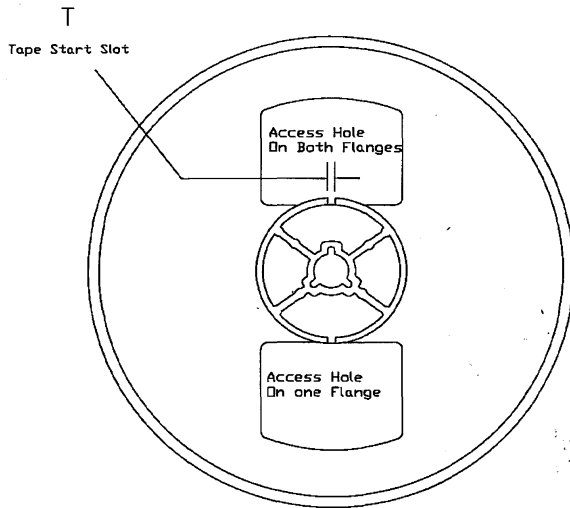
Package details: SOT23-5, Tape and Reel



FRONT VIEW



SIDE VIEW

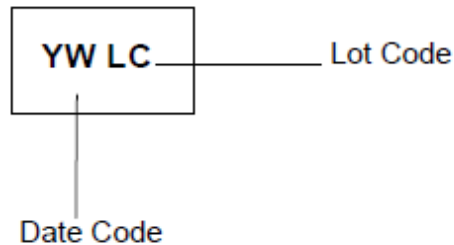


BACK VIEW

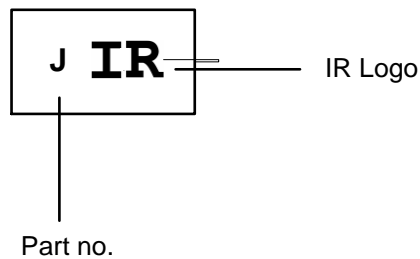
- NOTE:
1. MATERIAL : POLYSTYRENE
 2. SURFACE RESISTIVITY : $\leq 10E11$ OHMS/SQ (EXTERNAL DR DIPPED)
 3. STATIC DECAY : < 2 SEC. AT 50%RH

Part Marking Information

Top Marking



Bottom Marking



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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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