Texas Instruments

User's Guide
SLVU298–March 2009

TPS54040EVM-456 0.5-A, SWIFT™ Regulator Evaluation Module

This user's guide contains background information for the TPS54040 as well as support documentation for the TPS54040EVM-456 evaluation module (HPA456). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54040EVM-456.

Contents

List of Figures

List of Tables

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1 Introduction

This user's guide contains background information for the TPS54040 as well as support documentation for the TPS54040EVM-456 evaluation module (HPA456). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54040EVM-456.

1.1 Background

The TPS54040 dc/dc converter is designed to provide up to a 0.5-A output from an input voltage source of 3.5 V to 42 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPS54040 regulator. The switching frequency is internally set at a nominal 700 kHz. The high-side MOSFET is incorporated inside the TPS54040 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS54040 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54040 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 42 V for the TPS54040EVM-456.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54040EVM-456	VIN = 12 V to 42 V	0 A to 0.5 A

1.2 Performance Specification Summary

A summary of the TPS54040EVM-456 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 34 V and an output voltage of 5 V, unless otherwise specified. The TPS54040EVM-456 is designed and tested for V_{IN} = 12 V to 42 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54040EVM-456 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			12	34	42	V
Output voltage set point				5.0		V
Output current range	V_{IN} = 12 V to 42 V		0		0.5	A
Line regulation	I_O = 0.2 A, V_{IN} = 12 V to 42 V			±0.06%		
Load regulation	V_{IN} = 24 V, I_O = 0.001 A to 0.5 A			±0.07%		
Load transient response	I_O = 0.125 A to 0.375 A	Voltage change		–35		mV
		Recovery time		2		ms
	I_O = 0.375 A to 0.125 A	Voltage change		35		mV
		Recovery time		2		ms
Loop bandwidth	V_{IN} = 24 V, I_O = 0.5 A			15		kHz
Phase margin	V_{IN} = 24 V , I_O = 0.5 A			74		°
Input ripple voltage	I_O = 0.5 A			80		mVpp
Output ripple voltage	I_O = 0.5 A			5		mVpp
Output rise time				4		ms
Operating frequency				700		kHz
Maximum efficiency	TPS54040EVM-456, V_{IN} = 12 V, I_O = 0.3 A			92%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54040. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R_6. Changing the value of R_6 can change the output voltage above 0.8 V. The value of R_6 for a specific output voltage can be calculated using Equation 1.

$$R_6 = 10\ k\Omega \times \frac{(V_{OUT} - 0.8\ V)}{0.8\ V} \quad (1)$$

Table 3 lists the R_6 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 130 ns, and the maximum duty cycle is less than 91%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R_6 Value (kΩ)
1.8	12.4
2.5	21.5
3.3	31.6
5	52.3

Be aware that changing the output voltage can affect the loop response. It may be necessary to modify the compensation components. See the data sheet for details.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54040EVM-456 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54040EVM-456 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 0.5 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J2 through a pair of 20 AWG wires. The maximum load current capability must be 0.5 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP10 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range)
J2	V_{OUT}, 3.3 V at 0.5 A maximum
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	EN test point. Connect EN to ground to disable, open to enable.
TP4	Slow start monitor test point
TP5	PWRGD test point
TP6	PH test point
TP7	Output voltage test point at voltage divider. Used for loop response measurements.
TP8	Test point between voltage divider network and output. Used for loop response measurements.
TP9	Output voltage test point at OUT connector
TP10	GND test point at OUT connector

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.3 A with V_{IN} = 12 V, and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS54040EVM-456 at an ambient temperature of 25°C.

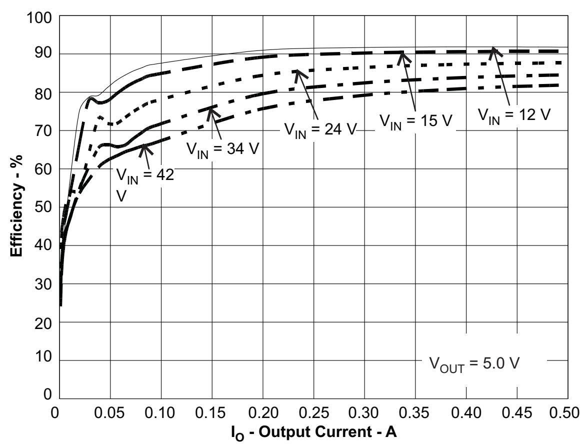

Figure 1. TPS54040EVM-456 Efficiency

Figure 2 shows the efficiency for the TPS54040EVM-456 at lower output currents between 0.001 A and 0.1 A at an ambient temperature of 25°C.

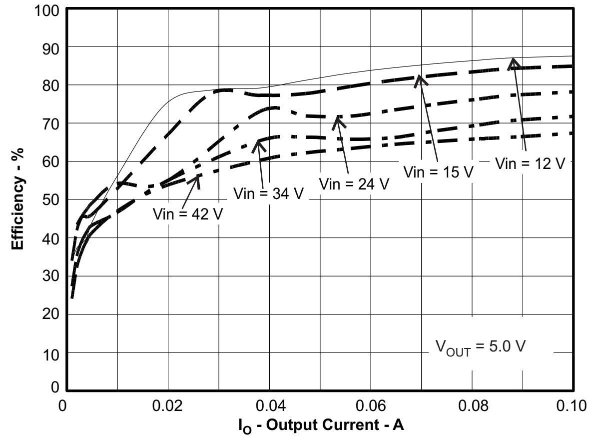

Figure 2. TPS54040EVM-456 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

The load regulation for the TPS54040EVM-456 is shown in Figure 3.

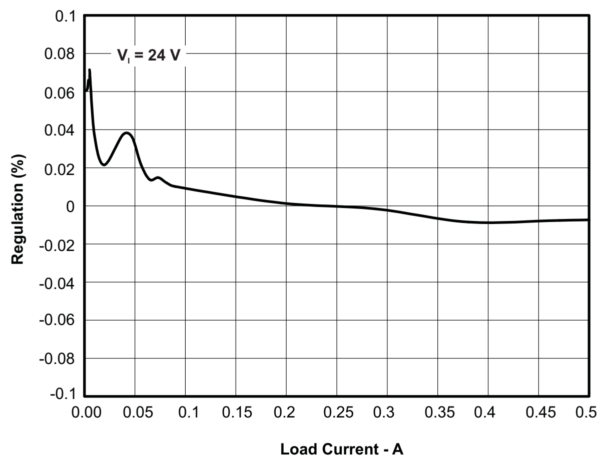

Figure 3. TPS54040EVM-456 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

The line regulation for the TPS54040EVM-456 is shown in Figure 4.

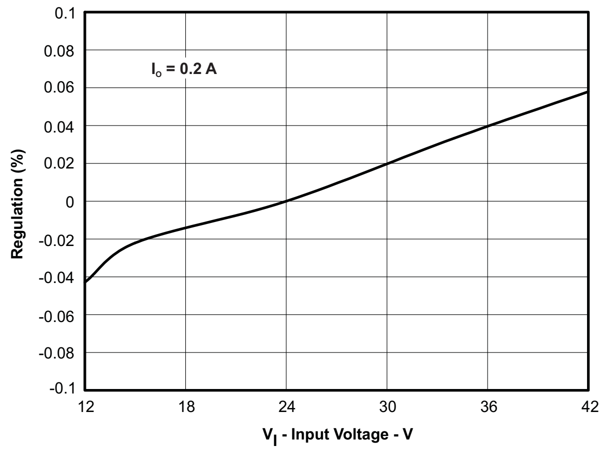

Figure 4. TPS54040EVM-456 Line Regulation

2.5 Load Transients

The TPS54040EVM-456 response to load transients is shown in Figure 5. The current step is from 25% to 75% of maximum rated load at a 24-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

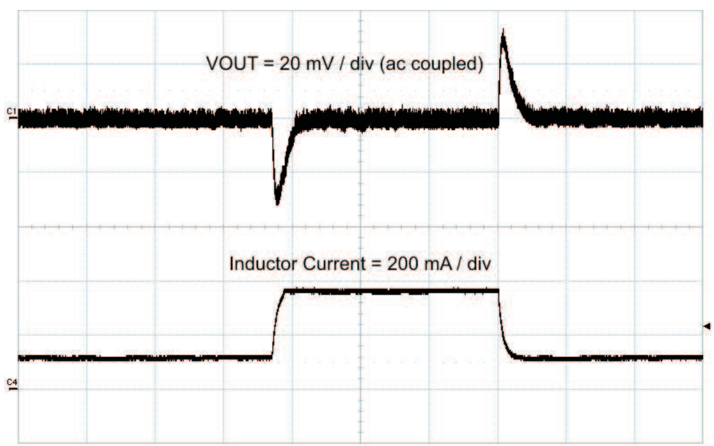

Figure 5. TPS54040EVM-456 Transient Response

2.6 Loop Characteristics

The TPS54040EVM-456 loop-response characteristics are shown in Figure 6 . Gain and phase plots are shown for V_{IN} voltage of 24 V. Load current for the measurement is 0.5 A.

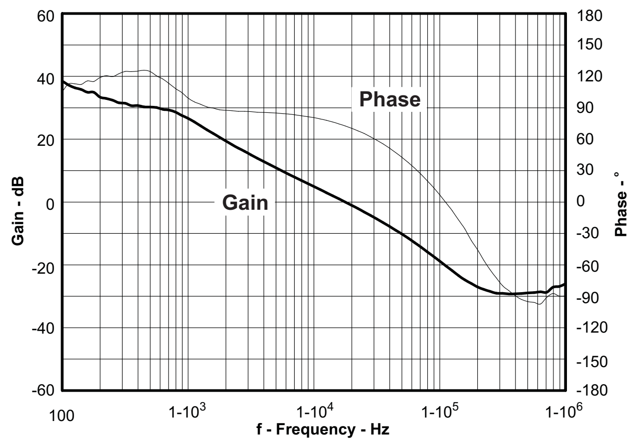

Figure 6. TPS54040EVM-456 Loop Response

2.7 Output Voltage Ripple

The TPS54040EVM-456 output voltage ripple is shown in Figure 7 . The output current is the rated full load of 0.5 A and V_{IN} = 34 V. The ripple voltage is measured directly across the output capacitors.

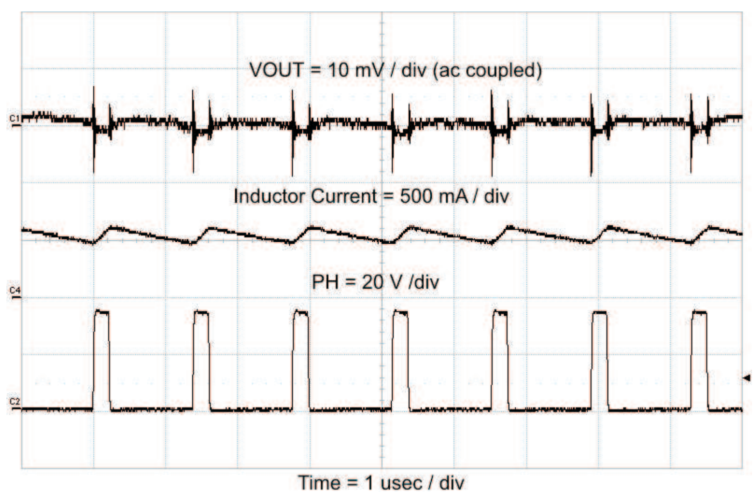

Figure 7. TPS54040EVM-456 Output Ripple

2.8 Input Voltage Ripple

The TPS54040EVM-456 input voltage ripple is shown in Figure 8 . The output current is the rated full load of 0.5 A and V_{IN} = 34 V. The ripple voltage is measured directly across the input capacitors.

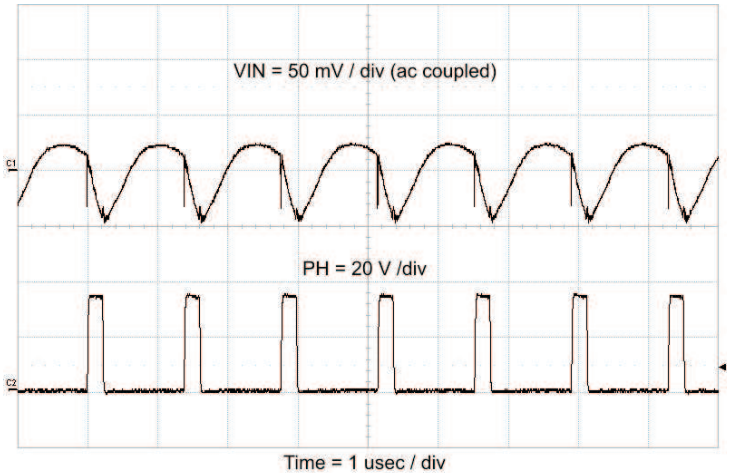

Figure 8. TPS54040EVM-456 Input Ripple

2.9 Powering Up

The start-up waveforms are shown in Figure 9. In Figure 9, the top trace shows V_{OUT} , and the bottom trace shows V_{IN}. The input voltage is initially applied, and when the input reaches the undervoltage lockout threshold, the start-up sequence begins and the output ramps up at the externally set slow start rate toward the set value of 5 V. The input voltage for these waveforms is 34 V.

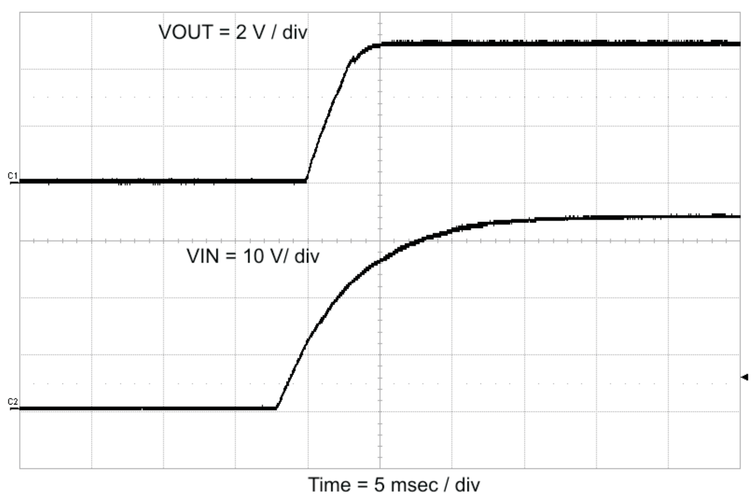

Figure 9. TPS54040EVM-456 Start-Up Relative to V_{IN}

2.10 Eco-mode™ Operation

At light load currents, the TPS54040 is designed to operate in pulse-skipping Eco-mode™ operation. When the COMP pin voltage lowers to 500 mA typical, the device enters Eco-mode™ operation.

Figure 10 shows Eco-mode operation; channel 1(C1) shows the output voltage, whereas channel 2(C2) shows the switching node (PH), and channel 4 (C4) shows the inductor current.

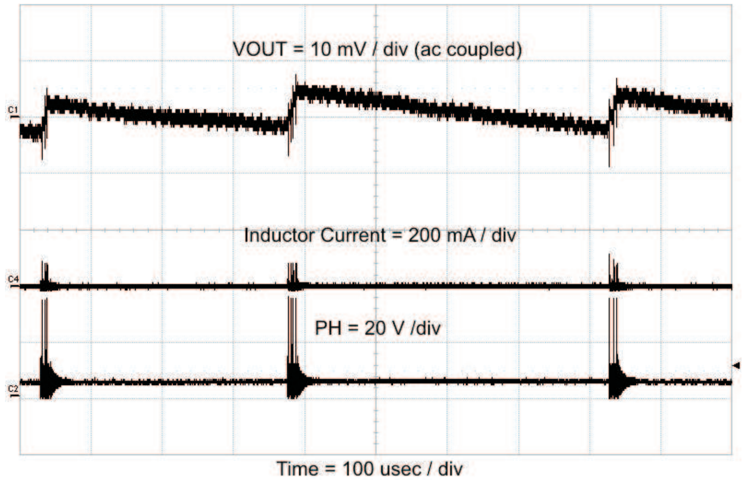

Figure 10. TPS54040EVM–456 Eco–mode™ Operation

3 Board Layout

This section provides a description of the TPS54040EVM-456, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54040EVM-456 is shown in Figure 11 through Figure 13. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and PH. Also on the top layer are connections for the remaining pins of the TPS54040 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including ten vias directly under the TPS54040 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C2 and C3) and bootstrap capacitor (C6) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace past the output capacitor (C5). For the TPS54040, an additional input bulk capacitor may be required (C1), depending on the EVM connection to the input supply.

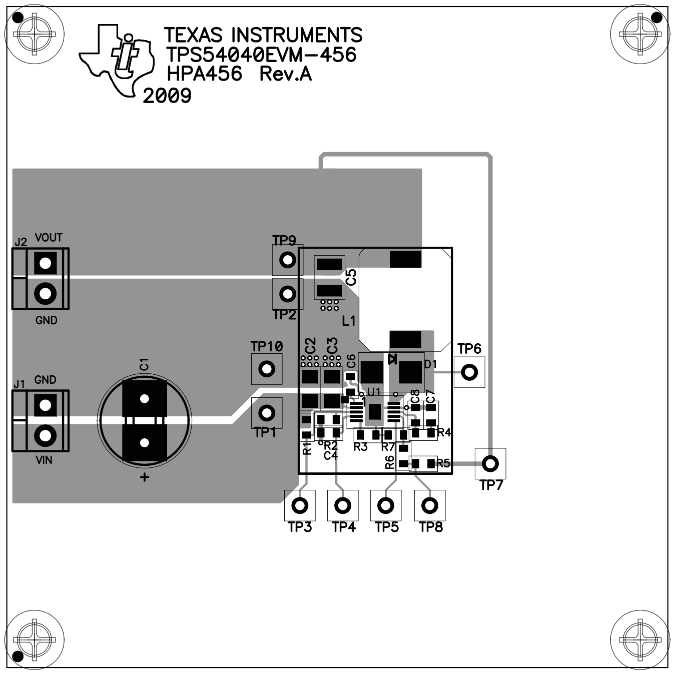

Figure 11. TPS54040EVM-456 Top-Side Layout

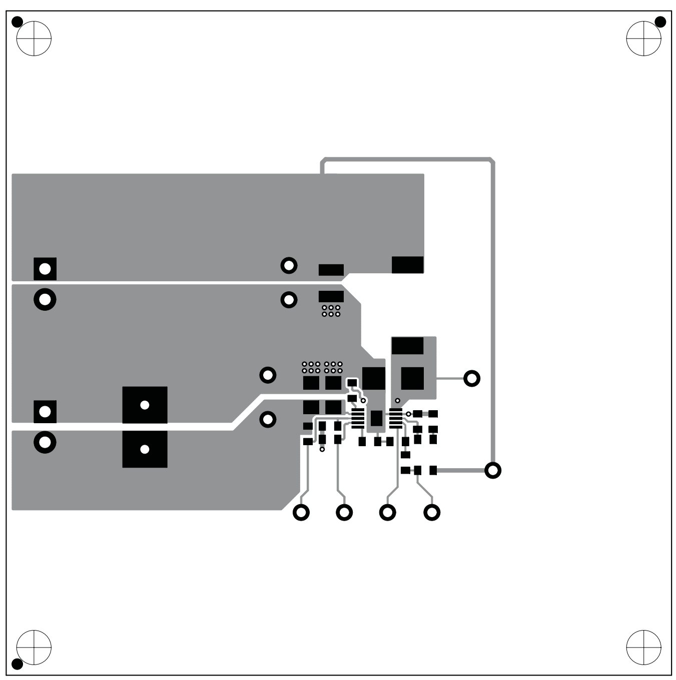

Figure 12. TPS54040EVM-456 Bottom-Side Layout

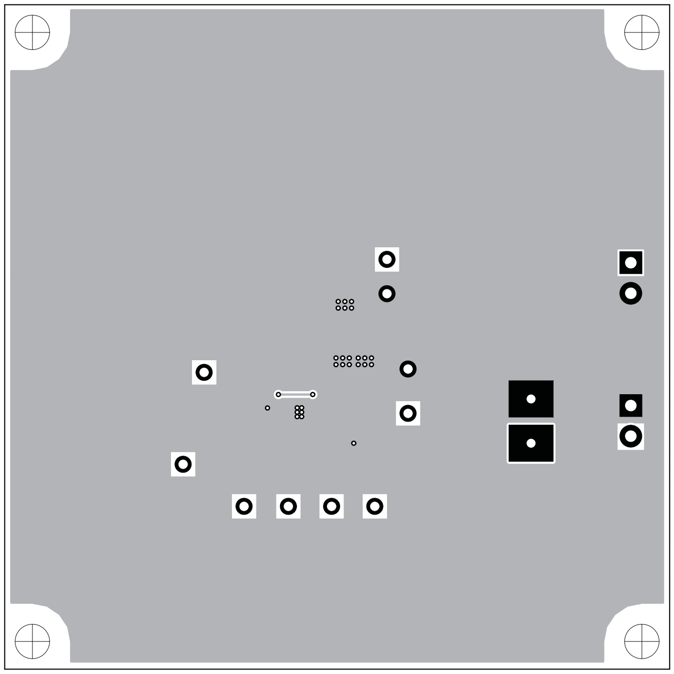

Figure 13. TPS54040EVM-456 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed-circuit board area for the components used in this design is 0.55 in^2. This area does not include test point or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54040EVM-456 schematic and bill of materials.

4.1 Schematic

Figure 14 is the schematic for the TPS54040EVM-456.

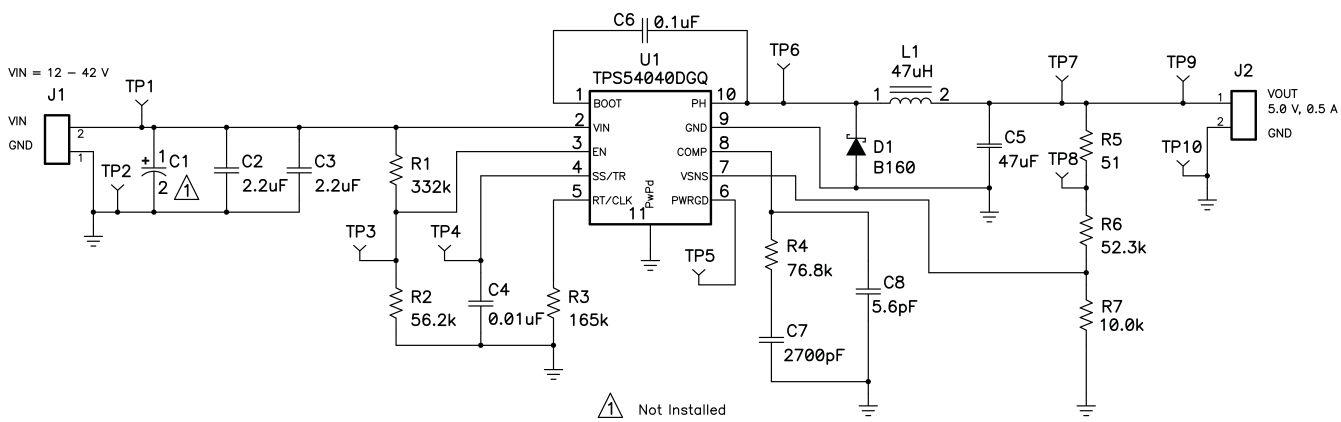

Figure 14. TPS54040EVM-456 Schematic

4.2 Bill of Materials

Table 5 presents the bill of materials for the TPS54040EVM-456.

Table 5. TPS54040EVM-456 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	Open	Capacitor, multi pattern, SM 1210 to E case + F THole	Multi sizes	Engineering Only	Std
2	C2, C3	2.2µF	Capacitor, Ceramic, 50V, X7R	1206	GRM31CR71H225KA 88L	Murata
1	C4	0.01µF	Capacitor, Ceramic, 25V, X5R, 20%	0603	Std	Std
1	C5	47µF	Capacitor, Ceramic, 10V, X5R	1210	Std	Std
1	C6	0.1µF	0.1µF Capacitor, Ceramic, 10V, X5R	0603	Std	Std
1	C7	2700pF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
1	C8	5.6pF	Capacitor, Ceramic, 25V, NPO, 5%	0603	Std	Std
1	D1	B160	Diode, Schottky,1A, 60V	SMB	B160B-13-F	Diodes Inc
2	J1, J2	ED1514	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 × 0.25 inch	ED1514	OST
1	L1	47µH	Inductor, SMT, 1.44A, 130milliohm	0.402 x 0.394 inch	MSS1048-473MLB	Coilcraft
1	R1	332kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	56.2kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	165kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	76.8kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	51kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	52.3kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R7	10kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
7	TP1, TP3, TP4, TP6, TP7, TP8, TP9	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
3	TP2, TP5, TP10	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keystone
1	U1	TPS54040DGQ	IC, DC-DC Converter, 42V, 0.5A	MSOP-10	TPS54040DGQ	TI
1	—		PCB, 3 inch × 3 inch × 0.062 inch		HPA456	Any

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range and the output voltage range of Table 1.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Тел: +7 (812) 336 43 04 (многоканальный)
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